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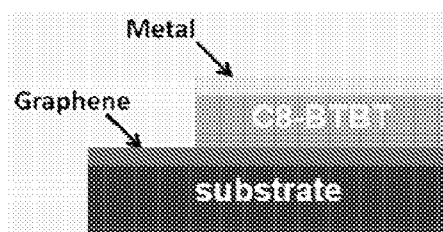
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(54) **Title:** METHOD FOR EPITAXIALLY GROWING ULTRATHIN ORGANIC CRYSTALLINE LAYERS ON SURFACE AND ITS APPLICATIONS

**Figure 7**

(57) **Abstract:** Disclosed is a method for depositing ultrathin layers of an organic semiconductor material on a support, and its applications in fabrication of electronic devices like OEFT and diodes. In the method, a source of an organic semiconductor material and a support are spaced from each other in a vacuum chamber and subjected to a temperature gradient, and the epitaxy initiates due to a van der Waals interaction between the organic molecules and the support. The ultrathin crystalline layers of the organic semiconductor material can be only a-few-molecule thick and even one-molecule thick in total. Further disclosed is a layered structure produced by said method and use of the layered structure in fabrication of logic gates.



METHOD FOR EPITAXIALLY GROWING ULTRATHIN ORGANIC CRYSTALLINE LAYERS ON SURFACE AND ITS APPLICATIONS

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Technical field

The present invention relates to a method for producing two-dimensional (2D) layered
10 heterostructures, and in particular, to a method for epitaxially growing ultrathin
crystalline layers of an organic semiconductor on a crystalline surface of a support
such as graphene and hexagonal boron nitride (hBN), as well as its applications in
fabrication of electronic devices like organic field-effect transistors (OEFTs).

15

Background art

Two-dimensional layered organic crystal represents a promising material for
electronic and photonic applications. Compared to bulk materials, crystalline
20 monolayers can effectively eliminate interlayer screening, thereby offering an ideal
system to directly investigate the effects of disorders and interfaces on charge
transport. Furthermore, both carrier injection and modulation would become more
efficient, so as to greatly improve the performance of OFETs.

25 OFETs are an important class of devices for flexible, low-cost, and lightweight
electronic applications such as drive circuits for LED displays, plastic RFID, and
sensors ^[1]. Nowadays a common structure of OFET is a planar device with
source/drain and gate electrodes, like a conventional CMOS. Due to the charge
hopping between the molecules, OFETs in general have a low carrier mobility of less
30 than $\sim 20 \text{ cm}^2/(\text{V}\cdot\text{s})$, much smaller than that of crystalline silicon ^[1,2]. As a result, the
application of OFETs is limited to those that do not demand high performance. In
addition, in order to consume less material in OFETs, it is highly desirable to use an
ultrathin layer down to molecular thickness as the channel. However, conventional
planar OFETs with an ultrathin channel (not more than 3 monolayers) generally have
35 very small mobility values of less than $0.1 \text{ cm}^2/(\text{V}\cdot\text{s})$ ^[3]. Therefore, extensive studies
have been carried out to address this issue.

Graphene is composed of one or more one-atom-thick layers of hexagonal carbon; it
is a pure two-dimensionally layered material with many appealing properties.
40 Graphene is a semimetal with zero bandgap. At the charge neutrality point, the density
of state (DOS) is zero, so the Fermi energy is highly tunable by the carrier density.

This is a distinctive feature compared to conventional metals. Graphene is transparent, absorbing $\sim 2.3\%$ of the visible light. It is also very flexible and is one of the strongest materials. These properties make graphene highly suitable for flexible and transparent device applications ^[4].

5

The use of graphene in transistors has been widely investigated because its carrier mobility can be as high as $\sim 2 \times 10^5 \text{ cm}^2/(\text{V}\cdot\text{s})$, much higher than that of silicon. However, the absence of bandgap inhibits the on/off ratio in graphene-based transistors. Although one can open up a bandgap by creating one-dimensional
10 graphene nanoribbons below 10 nm wide, the mobility is significantly degraded by edge roughness ^[5, 6]. To solve this issue, layered heterostructures formed by graphene and other semiconductors have been developed to impart a high on/off ratio to graphene-based transistors ^[7-9]. For these heterostructures, it is always desirable to invent processes and device structures that can be scaled up at low cost, and can
15 deliver transparent transistors with high performance (a high current and a high on/off ratio).

One approach to fabrication of graphene-based transistors is to combine graphene and other two-dimensional layers such as BN and MoS₂. These devices are usually
20 fabricated by tedious layer-by-layer transfer of these layered materials ^[7, 9]. First, graphene is exfoliated and transferred onto a Si/SiO₂ substrate to serve as the bottom electrode. Then, BN or MoS₂ is exfoliated on a separate substrate, followed by manually transferring it to the top of the graphene electrode under a microscope, so as to complete the heterostructure. Because the exfoliated sheets are different each time,
25 during the fabrication of such devices, multiple electron beam lithography steps are needed. Although such a structure can overcome the on/off-ratio problem in graphene-based devices, it cannot be scaled up for large-scale applications.

Another approach is to evaporate a thick organic material such as pentacene to allow
30 it to grow on graphene, as demonstrated by two groups ^[12, 13]. However, several drawbacks exist in this approach. First, the growth of the organic material is not well controlled and the quality of the layer formed is low; this process leads to a lot of grain boundaries in the organic film. Second, the thickness of the organic material crystal formed is very large (normally hundreds of nanometers), resulting in a device
35 that is not transparent and not suitable for applications such as LED displays.

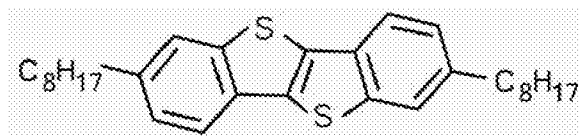
To integrate graphene with organic materials having a conjugated system, Samsung Electronics disclosed a scalable method based on coating or vapor-depositing an organic material such as phthalocyanine, pentacene, oligothiophene, polythiophene,
40 and polyphenylene onto the basal (0001) plane of graphene to reduce the interfacial resistance ^[10]. This method requires a solvent to assist the deposition of the organic

materials and may suffer from low electron mobility often seen in solution-assisted deposition. An electrical device comprising a layered structure formed by this method is also disclosed^[10]. In this layered structure, a basal plane of the graphene is a (0001) plane, and a layer comprising an organic material having a conjugated system is disposed on graphene via a π - π interaction. However, a detailed configuration of an electrical device employing such a structure is not specified.

Hexagonal boron nitride (hBN) is the most stable crystalline form of boron nitride, which has a layered structure similar to graphite but is basically an electrical insulator with a wide bandgap of ~ 5.2 eV. Due to its excellent dielectric and thermal properties, hBN is also useful in electronics e.g. as a substrate for semiconductors. Like graphene, BN is also an ideal support since it is atomically flat without dangling bonds. However, similar to the case of graphene, simple and scalable methods for forming hBN-supported ultrathin monolayers of organic semiconductor for electronic applications are still unavailable at low cost.

Therefore, there is still a need for a simple, scalable method for forming ultrathin crystalline layers of an organic semiconductor on the crystalline surface of a support such as graphene and hBN, so as to afford transparent heterostructures useful for electronic devices like OFETs.

With regard to organic semiconductors useful for the channel in OFETs, dioctylbenzothienobenzothiophene (C₈-BTBT, its formula is shown below) is one of the highest mobility organic molecules, which is co-invented by NIPPON KAYAKU co., Ltd^[2, 11].



It is therefore envisaged that C₈-BTBT, when used as a channel material, can provide high device mobility, a low threshold voltage, and high electrical stability for organic transistors. However, successful integration of ultrathin C₈-BTBT crystalline layers with two-dimensional supports like graphene or hBN to form a heterostructure useful for fabrication of planar OFETs has not been reported in the art yet.

Summary of invention

The present inventors have conducted extensive studies and developed a scalable method for epitaxially growing one or more two-dimensional layers of crystal of an organic semiconductor material on a support, such as graphene and hexagonal boron

nitride (hBN), at a temperature much lower than traditional vapor deposition methods. In this method, a source of an organic semiconductor material and a support are spaced from each other in a vacuum chamber and subjected to a temperature gradient, and the epitaxy initiates due to van der Waals (vdW) interaction between the organic molecules and the support. The method avoids use of any carrier gas or solvent, and thus simplifies the operation and saves cost.

One aspect of the present invention relates to a method for epitaxially growing two-dimensional layers of crystal of an organic semiconductor material on a crystalline surface of a support, and the method comprises the steps of

- 1) placing a support and a source of an organic semiconductor material in a vacuum chamber, in which the source and the support are spaced from each other,
- 2) applying a temperature gradient between the source and the support, wherein the temperature of the source is set such that the organic semiconductor material begins to evaporate or sublime, and the source temperature is higher than that of the support,
- 3) allowing the molecules of the organic semiconductor material to evaporate or sublime at the source temperature and grown on the crystalline surface of the support, and
- 4) controlling the time, pressure, and/or temperature of deposition such that a crystalline layer of desired thickness and morphology can be deposited on the support.

The inventors have surprisingly found that the method realizes epitaxial growth of 2D organic crystalline layers on the crystalline surface of graphene or hBN in which the organic molecules pack into a-few-nanometer thick monolayers stacked upon one another on the support and are unusually held by van der Waals forces. The molecular arrangement of these monolayers will be described in details below.

The method in accordance with the present invention is suitable for large-scale fabrication of a heterostructure in which one or more monolayers of an organic semiconductor material is epitaxially crystallized on the crystalline surface of a support. The heterostructure is transparent and exhibits a high on/off ratio without compromising mobility, thereby suitable for the fabrication of transparent logic transistors and diodes for possible applications in display drive circuits, LEDs, solar cells, and other complementary circuitry. Compared to other approaches, our method for the first time realizes scalable epitaxial growth of ultrathin crystalline layers of organic semiconductor materials on graphene or hBN, and the crystal formed has much higher quality.

Another aspect of the present invention relates to a layered structure, which comprising a support having a crystalline surface; and one or more two-dimensional layers of crystal of an organic semiconductor material epitaxially grown on the

crystalline surface of the support; wherein the total thickness of the one or more two-dimensional layers is 100 nm or less. The layered structure of this aspect can be obtained by the method described above. The present invention also relates to use of the layered structure in the fabrication of electronic devices like OFETs or diodes. The present invention further relates to an electronic device, such as OFETs or diodes, comprising the layered structure.

Yet another aspect of the present invention relates to logic gates, such as an AND gate or an OR gate, employing the layered structure of the present invention.

Description of the drawings

Hereinafter the preferred embodiments of the present invention will be described in detail with reference to the drawings. However, it is to be understood that the drawings are only illustrative and are not intended to limit the scope of the present invention to any extent. In the drawings,

Figure 1 shows a schematic configuration of the apparatus and the conditions for implementing the method in accordance with an embodiment of the present invention;

Figure 2 shows (a-n) sequential AFM images and (o) thickness of crystalline C₈-BTBT monolayers grown on a graphene support at different stages, in which the scale bars are 2 μm; (a) is the graphene sample before the growth of C₈-BTBT, wherein the graphene is on a SiO₂ substrate; (b)-(n) are sequential AFM snapshots for the same graphene sample after C₈-BTBT has grown thereon for 15 min to 95 min, tracking the growing process of different crystalline single-layers of C₈-BTBT; IL means Interfacial Layer (the first monolayer of C₈-BTBT in direct contact with graphene), 1L means the First Layer (the second C₈-BTBT monolayer on IL), and 2L, 3L and 4L mean the 2nd, 3rd and 4th layers, respectively (further C₈-BTBT monolayers above 1L);

Figure 3 shows (a) the AFM image of a single piece of uniform C₈-BTBT crystal grown on a graphene sample, and (b) its Raman mapping and (c-e) cross-polarized optical micrographs; the scale bars are 3 μm;

Figure 4 shows the spatial configuration of C₈-BTBT molecules in the crystalline layers on graphene; (a) is the scanning tunneling microscopy (STM) image of IL on graphene; (b) is the top view (top panel) and side view (bottom panels) of the most stable IL structure generated by density functional theory (DFT) calculations; (c) is the high-resolution AFM image of 2L, wherein the unit cell is marked with the a-b

coordinate system, and the insert is the Fast Fourier Transform of the AFM image with the lattice indices circled; (d) is the top view (left panel) and side view (right panel) of the 2L structure generated according to the AFM image in (c); (e) is a cartoon perspective view of the layered structure of 1L, 1L and 2L of C₈-BTBT crystal packed on graphene;

Figure 5 shows AFM images of C₈-BTBT crystal on hBN; (a) is the AFM image of C₈-BTBT grown on BN, wherein the 1L, 1L and 2L have the same meanings as in Figure 2, each followed by their thickness; (b) is the high-resolution AFM image of 1L C₈-BTBT on BN, wherein the unit cell is marked with the a-b coordinate system, and the inset is the Fast Fourier Transform of the AFM image; (c) is the high-resolution AFM image of 2L C₈-BTBT on BN; (d) is the high-resolution AFM image of bare hBN substrate, which shows the hexagonal lattice of hBN, in clear contrast to the C₈-BTBT crystal;

Figure 6 shows patterned growth of C₈-BTBT crystal on graphene, wherein the scale bars are 7 μm; (a) and (b) are optical microscopy images of a plasma-patterned graphene before and after C₈-BTBT growth, respectively; (c) and (d) are cross-polarized optical micrographs of the same area after C₈-BTBT growth;

Figure 7 shows a proposed device structure of a bottom-gate top-drain graphene/C₈-BTBT vertical OFET employing the layered heterostructure of the present invention; the thickness and width of each component are not drawn to scale; The peripheral wires connecting the electrodes are omitted;

Figure 8 shows characteristic of vertical OFETs featuring the graphene/C₈-BTBT layered structure of the present invention; (a) shows room-temperature J_{ds} - V_g characteristic curves of an OFET device having a ~15 nm (5-monolayer) thick C₈-BTBT crystal as the channel; V_{ds} =2V (upper curve) and 1V (lower curve), respectively; (b) shows room-temperature J_{ds} - V_{ds} characteristic curves of the same device as (a); V_g =-100 V, -90 V, -80 V, -70 V, and 0 V (from top to bottom), respectively; V_g refers to the gate voltage applied on the substrate; V_{ds} and J_{ds} refer to the applied bias voltage and measured current density between the graphene and the metal layer;

Figure 9 shows the room-temperature characteristics of a planar OFET device comprising a monolayer of C₈-BTBT crystal formed on hBN by the method of the present invention; (a) shows room-temperature double-sweep I_{ds} - V_g characteristic curves of the device (V_{ds} =-0.2V), with little hysteresis; the lower curve and the upper curve are drawn in linear and log scales, respectively; the inset depicts the extracted μ - V_g relationship, wherein the peak mobility is 4.3 cm²/(V·s); (b) shows

room-temperature I_{ds} - V_{ds} characteristic curves of the same device, wherein $V_g = -10$ V, -25 V, -30 V, -35 V and -40 V (from top to bottom), respectively; the inset is the optical microscopy image of the device; (c) shows I_{ds} - V_g characteristic curves ($V_{ds} = -0.2$ V) of the same device as (a), obtained at 300K, 290K, 270K, and 250K, respectively (from top to bottom); the inset depicts the μ -temperature relationship;

Figure 10 (a) shows room-temperature J_{ds} - V_{ds} characteristics of another device with a 19-layer thick C₈-BTBT crystal on graphene; $V_g = -100$ V, -90 V, -80 V, -70 V, -60 V, -50 V and -10 V (from top to bottom), respectively; (b) shows room-temperature J_{ds} - V_g characteristics of the device in (a); $V_{ds} = 24$ V, 9 V, 3 V and 1 V (from top to bottom), respectively; and

Figure 11 shows the schematic configuration and output values of (a) an OR gate and (b) an AND gate employing the graphene/C₈-BTBT layered structure of the present invention; the pull-up resistor for the AND gate and the pull-down resistor for the OR gate are both 5×10^9 Ohms; during the operation of both logic gates, $V_g = -100$ V, and $V_{dd} = 4$ V; the inserts schematically show the layered configuration of the gates.

Detailed description of the embodiments

Definitions

Unless otherwise indicated, the term “two-dimensional (2D) layer” or “monolayer” used herein means a one-atom-thick or one-molecule-thick crystalline layer of a substance, but its thickness may vary because of different packing configurations of the molecules constituting the crystalline layer. For example, a monolayer of C₈-BTBT is a one-molecule-thick layer of C₈-BTBT, the thickness of which may be approximately 0.6 to 3 nm depending on the packing configuration of C₈-BTBT molecules (see Figure 4e).

The term “graphene” used herein refers to a monolayer of hexagonal carbon or a multiple layers of hexagonal carbon stacked upon one another. Graphene in the context of this specification may have a thickness of 0.3 to 100 nm, but not limited thereto.

The term “hexagonal boron nitride” or “hBN” used herein refers to a monolayer of hexagonal boron nitride or a multiple layers of hexagonal boron nitride stack upon one another. hBN in the context of this specification may have a thickness of 0.3 to 100 nm, but not limited thereto.

The term “support” used herein refers to a physical base on which the organic

semiconductor crystal can epitaxially grow. It supports epitaxy of organic crystal by providing a substantially smooth crystalline surface and van der Waals interaction, but is not necessarily rigid. For example, when the support is ultrathin graphene or hBN, it may be flexible.

5

The term “substrate” used herein refers to a physical base routinely used for an element or unit structure in electronic devices, which may comprise a metal, a metalloid, a semiconductor, an insulator, or a combination thereof. Substrate can also be flexible and optically transparent plastics. In the present invention, the support is positioned on the substrate in the specific devices disclosed. However, in other applications, the support may be the same as the substrate.

15

The term “vacuum” used herein refers to an environment at a pressure below one atmosphere ($\sim 10^5$ P, or 760 Torr).

Method for epitaxial growth of crystalline monolayers

In one aspect, the present invention relates to a method for epitaxially growing two-dimensional layers of crystal of an organic semiconductor material on a crystalline surface of a support. The method comprises

20

1) placing a support and a source of an organic semiconductor material in a vacuum chamber, in which the source and the support are spaced from each other,

2) applying a temperature gradient between the source and the support, wherein the temperature of the source is set such that the organic semiconductor material begins to evaporate or sublime, and the source temperature is higher than that of the support,

25

3) allowing the molecules of the organic semiconductor material to evaporate or sublime at the source temperature and grown on the crystalline surface of the support, and

4) controlling the time, pressure, and/or temperature of deposition such that a crystalline layer of desired thickness and morphology can be deposited on the support.

30

In an embodiment of the method, the number of the 2D crystalline layers formed on the support may be 20 or less, preferably 10 or less, more preferably 5 or less. Each monolayer formed may appear as one whole piece or discrete pieces on the underlying layer or the graphene, and each piece may be a single crystal of pristine quality. The method of the present invention can achieve a large piece of monolayered single crystal of pristine quality having a size of tens of micrometers in width and/or length. In one embodiment of the method, there may be only one 2D crystalline layer grown on the support.

40

In an embodiment of the method, the organic semiconductor material to be deposited may be primarily composed of molecules having π -conjugate systems that allow

electrons and holes to move by hopping, tunneling, or other mechanisms. Typical examples of such molecules include aromatic polycyclic compounds (such as polyphenylene, pentacene, oligothiophene, and polythiophene), compounds comprising one or more porphyrin cores (such as porphyrin), and compounds comprising one or more phthalocyanine cores (such as phthalocyanine salts). Here “polycyclic compound” refers to a compound having two or more ring structures, in which each ring comprises carbon atoms and optional hetero atoms in the cyclic backbone, and these rings may be fused or not fused to one another. In one embodiment, the π -planes of the organic molecules in the grown semiconductor monolayer at the interface are substantially parallel to the crystalline surface of the support.

In a preferred embodiment, the organic semiconductor material is mainly composed of organic molecules having general formula (1) below:



wherein R^1 and R^2 are each independently hydrogen or a linear or branched alkyl group having 1 to 12 carbon atoms, preferably 1 to 10 carbon atoms, more preferably 1 to 8 atoms; Ar represents a monocyclic aromatic group or a fused polycyclic aromatic group, and may have hetero atoms in its cyclic backbone; n is an integer from 1 to 4, preferably 1 to 3, more preferably 1 or 2; R^1 and R^2 each may be bonded to any position on the core structure $[Ar]_n$, but if both are present, they are preferably at symmetric positions with respect to the center of $[Ar]_n$; besides R^1 and R^2 , $[Ar]_n$ may be substituted with other groups such as an alkyl having 1 to 8 carbon atoms.

In formula (1), examples of R^1 and R^2 include hydrogen, methyl, ethyl, n-propyl, i-propyl, n-butyl, i-butyl, sec-butyl, t-butyl, amyl, hexyl, heptyl, octyl, nonyl, decyl, dodecyl, cetyl, and the like, but are not limited thereto; examples of Ar include a benzene ring, a furan ring, a pyridine ring, a thiophene ring, a pyrrole ring, an indole group, a purine group, an imidazole ring, a polyaromatic hydrocarbon (PAH), and a fused product of the above (for example, pentacene, benzothiophene, etc), but are not limited thereto.

In a most preferred embodiment of the method, the organic semiconductor material is mainly composed of C₈-BTBT.

In a preferred embodiment of the method, the pressure in the vacuum chamber may be any value below 10 Torr, preferably 10⁻³ Torr or less, more preferably 10⁻⁵ Torr or less.

The support in the method according to the present invention is not specifically limited, and any material can be used as the support as long as it can provide a substantially atomically smooth crystalline surface and van der Waals interactions

allowing for epitaxial growth of organic molecules. In a preferred embodiment, the support is graphene. In this case, any kinds of graphene can be used, for example, mechanically exfoliated graphene, CVD graphene, or epitaxial graphene. The thickness of graphene can be from monolayer to about 100 nm, but not limited thereto.

5 In another preferred embodiment of the method, the support is hBN.

In an embodiment of the method, the vacuum chamber may be tube like and the support and the source of the organic semiconductor material are arranged horizontally in the tube-shaped chamber and are spaced from each other at a distance
10 allowing for epitaxy. In another embodiment of the method, the support and the source of the organic semiconductor may be arranged vertically and spaced from each other at a distance allowing for epitaxy. The chamber can also have other shapes, for example, prism-shaped. The distance between the source and the support is not specifically limited, as long as the distance allows the evaporated or sublimed
15 molecules of the organic semiconductor material to reach the crystalline surface of the support and epitaxially grow thereon. For example, when C₈-BTBT is used as the organic semiconductor material, the distance may be 1 to 50 cm, preferably 5-40 cm, more preferably 10-30 cm, but not limited thereto.

20 In an embodiment of the method, the deposition time of the organic semiconductor varies depending on the source temperature, the type of the organic semiconductor material, and the intended total thickness of the crystalline layers to be deposited. In a specific embodiment, the organic semiconductor material is C₈-BTBT and the deposition time is about 10 to 100 minutes, preferably 15 to 80 minutes, but not
25 limited thereto.

Without being bound to theory, it is considered that, at the interface of the organic crystal/support layered structure, the interaction between the crystalline monolayer having π -conjugate systems and the crystalline surface of the support (e.g. graphene
30 or hBN) is a vdW interaction, or more specifically, a vdW interaction mainly composed of non-covalent π - π interactions of the dispersion type. The inventors have found that support flatness and the weak vdW interaction are crucial for high-performance monolayer organic transistors because of the minimal disturbance in both crystal growth and charge transport.

35 A specific embodiment of the method will be described below with reference to Figures 1 and 2.

Figure 1 shows a schematic configuration of the apparatus and the conditions for
40 implementing the method in accordance with an embodiment of the present invention. As shown in Figure 1, the apparatus is a tube furnace comprising a quartz tube 4. A

source 1 of an organic semiconductor material and a support 2 on a substrate 3 are placed horizontally at a distance inside a quartz tube 4 under vacuum, preferably below 10^{-5} Torr. A turbo molecular pump (not shown) is connected to the tube 4 to evacuate the inside of the tube and maintain the pressure. The source 1 is placed in the center of the tube furnace. A temperature gradient is established inside the tube, with the temperature declining from the source 1 to the support 2 as indicated by the arrow. The molecules of the organic semiconductor material diffuse along the temperature gradient to the crystalline surface of the support 2 and epitaxially form one or more crystalline layers on the crystalline surface.

In the apparatus and process illustrated in Figure 1, the temperature of the source 1 is maintained by a heater (not shown) such that the organic semiconductor material begins to evaporate or sublime. The temperature of the support 2 is controlled by its position apart from the source and may be approximate to room temperature but should be lower than the source temperature to ensure epitaxial growth on the support.

The source temperature is not specifically limited as long as it satisfies the above condition. For example, for C₈-BTBT as the organic semiconductor material, any source temperature between about 20°C and about 200°C may be adopted as long as it is higher than the temperature of the support 2. The growth speed of the organic semiconductor crystalline layer on the support 2 is primarily controlled by the source temperature. When the crystalline film reaches intended thickness, the growth is terminated by stopping the heating and allowing the heterostructure sample (i.e. the support 2 with the layer(s) deposited thereon) to cool down to ambient temperature while maintaining the vacuum condition.

The growth of the 2D layers of the organic semiconductor crystal by the method of the present invention can be confirmed by atomic force microscopy (AFM). Figure 2 shows AFM images of crystalline C₈-BTBT layers grown on a graphene support at different stages.

From Figure 2 it can be seen that the C₈-BTBT crystal preferentially grew on graphene, in a layer-by-layer fashion, with atomic smoothness. The thickness of the initial two layers (namely the interfacial layer, IL, and the first layer, 1L) is ~0.6 nm and ~1.7 nm, respectively, as measured by AFM (see Figure 2o), indicating that the molecular packing in the initial layers is different from bulk crystal of C₈-BTBT. However, the thickness of the subsequent layers (2L and further layers) was ~3 nm (see Figure 2o), the same as that of bulk crystal. Furthermore, for each layer, the growth initiated at certain nucleation sites, and then proceeded nearly isotropically as compact islands. The most common nucleation sites of each layer were disorders (such as cracks and wrinkles) from the previous layers (Figure 2d) or from the

substrate (Figure 2a, 2f, 2m), as well as edges (Figure 2i, 2k, 2n), probably owing to their high surface energy. Such a growing process strongly indicates epitaxy.

In addition, although each snapshot was taken after interruption of the growth and removal of the sample into the ambient environment, the frequent interruptions and ambient exposure of the sample did not significantly affect the growth, which indicates that the crystal are of pristine quality and stable against photo oxidation in ambient environments.

Large-area mono-layered or bi-layered C₈-BTBT single crystal completely covering the graphene sample was repeatedly obtained after careful control of the growth parameters on defect-free (e.g. crack and wrinkle-free) graphene. Figure 3a shows a continuous single piece of mono-layered uniform C₈-BTBT crystal over about 30 μm long and 5 μm wide (IL not counted) grown on a graphene sample, as confirmed by the total thickness of C₈-BTBT/graphene of 3.7 nm and Raman mapping (Figure 3b). Cross-polarized optical micrographs showed that the entire piece was a single crystal except a small portion at the bottom (Figure 3c, 3d), and the optical intensity had a four-fold symmetry as expected for high-quality single crystal (Figure 1e). The low nucleation density and island growth mode (as opposed to fractal growth) indicate a high diffusion coefficient of C₈-BTBT molecules both on surface and along the island edges. This is a natural result of the substrate flatness and relatively weak vdW forces from the substrate, in clear contrast to the conventional epitaxy where strong chemical bonds are formed at the interface.

The thickness of ~0.6 nm of the IL reveals a novel form of molecular packing at the interface. Scanning tunneling microscopy (STM) showed that C₈-BTBT molecules in IL were packed in a rectangular lattice with $d_1=2.52$ nm and $d_2=0.66$ nm in two orthogonal directions (Figure 4a). Based on density functional theory (DFT) studies, it is postulated that the most stable single-molecule configuration of C₈-BTBT in IL has both its octyl chains and benzothiophene plane in closest proximity to and parallel to graphene, such that both CH- π interactions and the π - π interactions are maximized. When forming periodic crystal, however, the fully-relaxed benzothiophene plane is expected to be slightly tilted to form a 10° angle with the graphene plane because of inter-molecular interactions, as calculated in DFT (Figure 4b).

High-resolution AFM in ambient environments shows that the crystal structure for both 1L and 2L is monolithic with herringbone-type packing as in bulk crystal (Figure 4c, 4d). The lattice constants are $a=6.24\pm0.25\text{Å}$ ($6.69\pm0.13\text{Å}$), $b=8.31\pm0.05\text{Å}$ ($7.89\pm0.25\text{Å}$) for C₈-BTBT crystal on graphene, and no statistical difference of lattice constants between 1L and 2L was observed. The C₈-BTBT molecules in 1L (thickness ~1.7 nm) are more inclined than bulk crystal (thickness ~3 nm). Figure 4e shows a

schematic layered structure of IL, 1L and 2L of C₈-BTBT crystal stacked on graphene. The AFM and STM results confirm the epitaxy of C₈-BTBT crystal.

As mentioned above, the support is not limited to graphene. In one embodiment of the method of the present invention, the support is hexagonal boron nitride (hBN). Figure 5 shows the results of epitaxial growth of C₈-BTBT crystalline monolayers on hBN. The thickness of each layer is similar to that of C₈-BTBT/graphene.

The method of the present invention can also be applied to patterned growth of ultrathin organic crystal for device integration. Figure 6 shows that, on (6a) graphene patterns etched by oxygen plasma, a (6b) C₈-BTBT crystal can be readily grown with excellent uniformity over an area of about 1200 μm^2 . The uniform color change over the entire area confirms that C₈-BTBT forms a single crystal. When combined with CVD graphene or BN, large-area integration of devices is feasible.

Layered hetero-structure comprising a ultrathin organic crystal and a 2D support

Another aspect of the present invention relates to a layered structure produced by the above-described method, the layered structure comprising a support having a crystalline surface; and

one or more two-dimensional layers of crystal of an organic semiconductor material epitaxially grown on the crystalline surface of the support; wherein the total thickness of the crystalline layers is 100 nm or less.

In an embodiment of the layered structure, the number of the 2D crystalline layers formed on the support may be 20 or less, preferably 10 or less, more preferably 5 or less. Each monolayer formed may appear as one whole piece or discrete pieces on the underlying layer or the graphene, and each piece may be a single crystal of pristine quality. Each monolayer may be a whole piece of single crystal of pristine quality having a dimension (length or width) of at least tens of micrometers, for example, at least 30 μm , 40 μm , or 50 μm .

In an embodiment, the 2D crystalline layer in direct contact with the support (referred to as the interfacial layer) is thinner than all other layers stacked thereabove. In an embodiment, the 2D crystalline layer stacked directly over the interfacial layer (referred to as the first layer), if present, is thicker than the interfacial layer, but thinner than other layers (if present) stacked thereabove. In one embodiment of the layered structure, there may be only one, two, or three 2D crystalline layers grown on the support. The total thickness of the 2D crystalline layers may be 100 nm or less, preferably 90 nm or less, more preferably 80, 70, 60, 50, 40, 30, 20, 15, 10 or 5 nm or less. In an embodiment, the π -planes of the organic molecules in the interfacial layer are nearly parallel to the crystalline surface of the support.

In a preferred embodiment of the layered structure, the organic semiconductor material to be deposited may be primarily composed of molecules having π -conjugate systems. Examples of such molecules include aromatic polycyclic compounds (such as polyphenylene, pentacene, oligothiophene, and polythiophene), compounds comprising one or more porphyrin cores (such as porphyrin), and compounds comprising one or more phthalocyanine cores (such as phthalocyanine salts). In another embodiment of the layered structure, the organic semiconductor material can be doped. Further examples of the organic semiconductor material have been described in previous paragraphs.

In a preferred embodiment, the organic semiconductor material is C₈-BTBT. In this case, the π -planes (i.e. benzothiophene planes) of C₈-BTBT molecules in the interfacial layer are preferably at an angle of about 10° to the crystalline surface of the support. The C₈-BTBT interfacial layer has a thickness of about 0.6 nm. The first layer on the interfacial layer has a thickness of about 1.7 nm, and the further layers above the first layer each have a thickness of about 3 nm.

The support in the layered structure is not specifically limited, and any material can be used as the support as long as it can provide a substantially atomically smooth crystalline surface and van der Waals interactions allowing for epitaxial growth of the organic molecules. In a preferred embodiment, the support is graphene. In this case, any kinds of graphene can be used, for example, mechanically exfoliated graphene, CVD graphene, or epitaxial graphene. The thickness of graphene can be from monolayer to about 100 nm, but not limited thereto. In another preferred embodiment of the method, the support is hBN.

Transistors employing the layered structure

The layered structure of the present invention can be used as a unit or element of an electronic device, such as OFET. Figure 7 shows a proposed device structure of a bottom-gate top-drain graphene/C₈-BTBT vertical OFET.

In Figure 7, “Graphene” refers to a graphene sheet that serves as the support for organic semiconductor crystal described above and may be up to 10 nm thick. The size of the graphene sheet can be from micrometers to centimeters or even meters. Synthetic methods for the graphene sheet include mechanical exfoliation, chemical vapor deposition, and chemically derived graphene thin films. “Metal” refers to any electrically conducting substance including, but not limited to, metals such as Au, Ti, Pd, Cu, Al; conducting oxides such as “ITO”; and conducting polymers and paints. “C₈-BTBT” refers to a crystal (up to 100 nm thick) of C₈-BTBT grown on the graphene by above-mentioned epitaxy method. The fabrication process of the above

device starts with preparation of graphene, either by mechanical exfoliation on a target substrate, or by chemical vapor deposition and transfer onto a substrate. A metal electrode is connected to graphene by lithography. C₈-BTBT is then epitaxially grown on the graphene using the above-mentioned method according to the present invention.

5 Finally a top metal electrode is deposited.

In a specific example of Figure 7, a 100-nm thick Au layer is deposited on the C₈-BTBT crystal and serves as the top drain electrode, a graphene sheet serves as the bottom source electrode, the Si/SiO₂ substrate includes the dielectric layer (SiO₂) and the gate electrode (Si), and the C₈-BTBT crystal serves as the channel.

Figure 8 shows the transfer (J_{ds} - V_g) and output (J_{ds} - V_{ds}) characteristics of a typical vertical OFET as shown in Figure 7 which comprises 5 monolayers of C₈-BTBT on graphene. The on/off ratio of this OFET is about 1.5×10^3 at room temperature. The device exhibited a diode-like rectifying behavior similar to graphene barristers [8, 12], indicating different conduction mechanisms for the two bias polarities.

Figure 9 shows the characteristics of a planar p-type OFET with a monolayer of C₈-BTBT crystal grown on insulating hBN. Despite the monolayer thickness (~1.7 nm), the devices exhibits several features of ideal OFETs: linear I_{ds} - V_g ($I_{ds}^{1/2}$ - V_g) characteristics in the linear (saturation) regime, Ohmic contact, and negligible hysteresis. The room-temperature peak field-effect mobility μ could reach as high as ~5 cm²/(V·s), much higher than previously reported values for monolayer OFETs (which are in the range from ~10⁻⁶ to 10⁻¹ cm²/(V·s)). The value of μ is still underestimated due to contact resistance, which is estimated to be quite low (~500 $\Omega \cdot \text{cm}$) at on-state using the Y function method. Such a dramatic improvement is strong evidence that the density of charge traps and grain boundaries have been significantly reduced. This can be attributed to the pristine, ultrasmooth crystal and their weak coupling interaction with the support.

Compared to bulk-crystal devices, the I_{ds} - V_{ds} characteristic curves in Figure 9b reveals two unique features: (i) the absence of non-linearity at low bias, and (ii) complete saturation with extremely small saturation voltage (<-1V). Both features are direct consequence of the monolayer nature of the C₈-BTBT channel. The former feature is because the source/drain electrodes are in direct contact with the charge transporting layer, leading to extremely efficient carrier injection. The latter one is due to easy and complete channel pinch-off without interlayer screening effects. With scaled dielectric thickness and other optimized device parameters, the operation voltage of these OFETs can be reduced to 1V, which makes these devices compatible with silicon CMOS in circuits. In addition, it is found that the mobility decreases slightly at low temperatures, but still maintains very high, e.g. ~2.3 cm²/(V·s) at 250K.

Figure 10a and 10b show the characteristics of another planar OFET device with a much thicker piece of C₈-BTBT crystal grown on hBN by the method of the present invention. The on-state current of this device is over 100 A/cm² and its on/off ratio is about ~10⁶.

Therefore, another aspect of the invention relates to use of the layered structure describe above in the fabrication of an OFET or diode. Yet another aspect of the invention relates to an OFET or diode comprising the layered structure described above. In particular, the planar OFET employing monolayer semiconductor crystal on hBN can achieve a carrier mobility as high as ~5 cm²/(V·s) and an aggressively scaled saturation voltage below 1V, which is highly promising for electronic and photonic applications.

Logic gates employing the layered structure

The inventors also made more complex circuits based on two graphene/C₈-BTBT vertical diodes described above. By connecting two such structures in different ways, OR and AND logic gates can be successfully achieved. Figure 11 schematically shows (a) an OR gate and (b) an AND gate and their output characteristics. For the AND gate, two pieces of C₈-BTBT crystal were grown on two spaced graphene pieces as inputs, and they were connected with a common top electrode as the output. Either diode under forward bias (with a low input) would be closed with a much lower resistance than the pull-up resistor, thereby creating a low output. The gate showed excellent logic function, with the high and low outputs close to V_{dd} (4 V) and 0 respectively (Figure 11b). For the OR gate, two pieces of C₈-BTBT crystal were grown on a single piece of graphene as the output, and two top electrodes as inputs were deposited on the two pieces of C₈-BTBT crystal respectively. Either diode under forward bias (with a high input) would be closed with a much lower resistance than the pull-down resistor, thereby creating a high output. The outputs of the OR gate for (4, 0) and (0, 4) are between 2 V and 3 V, which are not as ideal as 4 V because of the finite leakage current under reverse bias, but are sufficient for effective functioning of the OR gate (Figure 11a). Clearly, more complex functionality can be created with lithographic patterning.

Therefore, the present invention further relates to an OR gate, comprising one support having a crystalline surface;
two separate pieces of crystal of an organic semiconductor material epitaxially deposited on the crystalline surface of the support, each piece having one or more two-dimensional layers of the organic semiconductor material and a total thickness of 100 nm or less;
two separate electrically conductive covers covering the top of the two crystal pieces

respectively; and
a substrate underneath the support.

- The present invention further relates to an AND gate, comprising
- 5 two separate supports each having a crystalline surface;
two separate pieces of crystal of an organic semiconductor material epitaxially deposited on the crystalline surface of the two supports respectively, wherein each of the two crystal pieces has one or more two-dimensional layers of the organic semiconductor material and a total thickness of 100 nm or less;
- 10 one electrically conductive cover covering the top of both crystal pieces of the organic semiconductor material; and
a substrate underneath the supports.

- In the OR and AND gates of the present invention, the organic semiconductor/support
- 15 layered structure may be the layered structure of the present invention describe above. The conductive cover may be a layer of any electrically conducting substance including, but not limited to, metals such as Au, Ti, Pd, Cu, Al; conducting oxides such as “ITO”; and conducting polymers and paints.

- 20 The demonstrated transistor/diode structure will have potential applications in display drive circuits, display drive circuits, LEDs, solar cells and other complementary circuitry.

- The present invention solves several critical issues in the application of graphene
- 25 vertical heterostructures in electronic devices. First, the coating deposition method of organic layers on graphene/BN can be scaled up, which solves the problem of manual transfer of two-dimensional layered materials. Second, both graphene/BN and the ultrathin organic layers are transparent in visible wavelength, and therefore such structure can be used in transparent displays and LEDs. Third, the channel length in
- 30 the vertical transistor is only a few nm to tens of nm, much reduced compared to conventional planar OFET structures. Hence, the structure of the present invention will dramatically improve the OFET transistor performance compared to conventional OFET structures.

35 **Examples**

Example 1 *Growth of C₈-BTBT crystal on graphene*

- Graphene was exfoliated on a 285-nm SiO₂/Si substrate without further thermal treatment, to prepare a graphene sample having a surface area of about 500 μm². The
- 40 exfoliated graphene was characterized by optical microscope, AFM and Raman spectroscopy before growth to obtain its thickness and topology information. The

growth was carried out in a tube furnace as shown in Figure 1. In the tube furnace, an open container (about 1 cm in size) containing C₈-BTBT powder (from NIPPON KAYAKU co., Ltd. without further purification) was placed in the middle of the quartz tube chamber (1.5 meters long and 10 cm in diameter). Then the graphene sample was placed about 20 cm away from the source. The quartz tube chamber was sealed and evacuated by a turbo molecular pump to about 4×10^{-6} Torr. The distance between source and the graphene sample was accurately measured each time to obtain good reproducibility. The C₈-BTBT powder was then heated to 100°C to start the growth. After 50 minutes of growth, the furnace was turned off and the sample was cooled down to room temperature with the vacuum condition maintained. As a result, about three monolayers of C₈-BTBT crystal epitaxially grew on the graphene, as confirmed by AFM and STM.

Example 2

C₈-BTBT crystal was grown by the same method as in Example 1 except that the distance between the support and the source was changed to 10 cm. As a result, about three monolayers of C₈-BTBT crystal epitaxially grew on the graphene.

Example 3

C₈-BTBT crystal was grown by the same method as in Example 1 except that the distance between the support and the source was changed to 25 cm. As a result, about two monolayers of C₈-BTBT crystal epitaxially grew on the graphene.

Example 4

C₈-BTBT crystal was grown by the same method as in Example 1 except that the source temperature was changed to 110°C. As a result, about six monolayers of C₈-BTBT crystal epitaxially grew on the graphene.

Example 5

C₈-BTBT crystal was grown by the same method as in Example 1 except that the source temperature was changed to 120°C. As a result, about ten monolayers of C₈-BTBT crystal epitaxially grew on the graphene.

Example 6

C₈-BTBT crystal was grown by the same method as in Example 1 except that the deposition time was changed to 90 minutes. As a result, about four monolayers of C₈-BTBT crystal epitaxially grew on the graphene.

Example 7

C₈-BTBT crystal was grown by the same method as in Example 1 except that the deposition time was changed to 30 minutes. As a result, about two monolayers of

C₈-BTBT crystal epitaxially grew on the graphene.

Example 8 *Growth of C₈-BTBT crystal on hBN*

C₈-BTBT crystal was grown by the same method as in Example 1 except that hBN
5 was used as the support instead of graphene. As a result, about three monolayers of
C₈-BTBT crystal epitaxially grew on the hBN.

The terminology used in this specification is for the purpose of describing particular
example embodiments only and is not intended to be limiting. As used herein, the
10 singular forms "a", "an" and "the" may be intended to include the plural forms as well,
unless the context clearly indicates otherwise. The terms "comprises", "comprising",
"including", and "having" are inclusive and therefore specify the presence of stated
features, layers, steps, pieces, groups, compounds, elements, and/or components, but
do not preclude the presence or addition of one or more other features, layers, steps,
15 pieces, groups, compounds, elements, components and/or combinations thereof.

In addition, the disclosure of particular values (e.g., pressures, times, dimensions,
number of atoms, number of layers, electronic characteristics, etc.) and particular
ranges of values herein are not exclusive of other values or ranges of values that may
20 be useful in other embodiments depending, for example, on particular growing
processes or devices, or in one or more of the examples disclosed herein. Moreover, it
is envisioned that any two particular values for a specific parameter stated herein may
define the endpoints of a range of values that may be suitable for the given parameter.
The disclosure of a first value and a second value for a given parameter can be
25 interpreted as disclosing that any value between the first and second values could also
be employed for the given parameter.

The foregoing description of the embodiments has been provided for purposes of
illustration and description. It is not intended to be exhaustive or to limit the
30 disclosure. For a person skilled in the art, the embodiments and examples disclosed
herein may be varied or modified in many ways without departing from the scope of
the disclosure and such variations and modifications are included in the scope defined
by the appended claims.

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Claims

1. A method for epitaxially growing two-dimensional layers of crystal of an organic semiconductor material on a crystalline surface of a support, the method comprising
- 5 1) placing a support and a source of an organic semiconductor material in a vacuum chamber, in which the source and the support are spaced from each other,
- 2) applying a temperature gradient between the source and the support, wherein the temperature of the source is set such that the organic semiconductor material begins to
- 10 evaporate or sublime, and the source temperature is higher than that of the support,
- 3) allowing the molecules of the organic semiconductor material to evaporate or sublime at the source temperature and grow on the crystalline surface of the support, and
- 4) controlling the time, pressure, and/or temperature of deposition such that a
- 15 crystalline layer of desired thickness and morphology can be deposited on the support.
2. The method according to claim 1, wherein the organic semiconductor material is mainly composed of organic molecules having π -conjugate systems.
- 20 3. The method according to claim 2, wherein the organic molecules having π -conjugate systems are selected from a group consisting of aromatic polycyclic compounds, compounds comprising one or more porphyrin cores, and compounds comprising one or more phthalocyanine cores.
- 25 4. The method according to claim 2, wherein the organic molecule having π -conjugate systems is represented by general formula (1):
- $$R^1-[Ar]_n-R^2 \quad (1)$$
- where R^1 and R^2 are each independently hydrogen or a linear or branched alkyl group having 1 to 12 carbon atoms; Ar represents a monocyclic aromatic group or a fused
- 30 polycyclic aromatic group; n is an integer from 1 to 4.
5. The method according to claim 2, wherein the organic molecule having π -conjugate systems is dioctylbenzothienobenzothiophene (C_8 -BTBT).
- 35 6. The method according to claim 5, wherein the source temperature is about 20°C to about 200°C.
7. The method according to claim 1, wherein the pressure in the vacuum chamber is 10^{-3} Torr or less.
- 40 8. The method according to any one of claims 1-7, wherein the support is graphene.

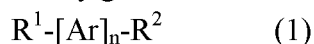
9. The method according to any one of claims 1-7, wherein the support is hexagonal boron nitride.

5 10. A layered structure, the layered structure comprising a support having a crystalline surface; and one or more two-dimensional layers of crystal of an organic semiconductor material epitaxially grown on the crystalline surface of the support; wherein the total thickness of the one or more two-dimensional layers is 100 nm or
10 less.

11. The layered structure according to claim 10, wherein the organic semiconductor material is mainly composed of organic molecules having π -conjugate systems.

15 12. The layered structure according to claim 11, wherein the organic molecules having π -conjugate systems are selected from a group consisting of aromatic polycyclic compounds, porphyrin derivatives, and phthalocyanine derivatives.

20 13. The layered structure according to claim 11, wherein the organic molecule having π -conjugate systems is represented by general formula (1):



where R^1 and R^2 are each independently hydrogen or a linear or branched alkyl group having 1 to 12 carbon atoms; Ar represents a monocyclic aromatic group or a fused polycyclic aromatic group; n is an integer from 1 to 4.

25 14. The layered structure according to claim 11, wherein the organic molecules having π -conjugate systems is C₈-BTBT.

30 15. The layered structure according to claim 10, wherein the length or width of at least one two-dimensional crystalline layer is at least 30 μ m.

16. The layered structure according to any one of claims 10-15, wherein the support is graphene.

35 17. The layered structure according to any one of claims 10-15, wherein the support is hexagonal boron nitride.

40 18. Use of the layered structure according to any one of claims 10-17 in the fabrication of an electronic device.

19. An electronic device comprising the layered structure according to any one of

claims 10-17.

20. The electronic device according to claim 19, wherein the electronic device is an organic field-effect transistor or diode.

5

21. An OR gate, comprising

a layered structure according to any one of claims 10-17, wherein the crystal of the organic semiconductor material is present as two separate pieces on the crystalline surface of the support, each piece having one or more two-dimensional layers and a total thickness of 100 nm or less;

10

two separate electrically conductive covers covering the top of the two crystal pieces respectively; and

a substrate underneath the support of the layered structure.

15

22. An AND gate, comprising

two separate layered structures according to any one of claims 10-17;

one electrically conductive cover covering the top of the crystal of the organic semiconductor material of both layered structures; and

a substrate underneath the supports of the layered structures.

20

AMENDED CLAIMS
received by the International Bureau on 03 June 2015 (03.06.2015)

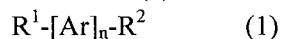
1. A method for epitaxially growing one or more two-dimensional layers of crystal of ~~one organic semiconductor material on a crystalline surface of a support, the method comprising~~

- 1) placing a support and a source of an organic semiconductor material in a vacuum chamber, in which the source and the support are spaced from each other,
- 2) applying a temperature gradient between the source and the support, wherein the temperature of the source is set such that the organic semiconductor material begins to evaporate or sublime, and the source temperature is higher than that of the support,
- 3) allowing the molecules of the organic semiconductor material to evaporate or sublime at the source temperature and grow on the crystalline surface of the support, and
- 4) controlling the time, pressure, and/or temperature of deposition such that a crystalline layer of desired thickness and morphology can be deposited on the support, wherein, the support is a two-dimensionally layered material, and the total thickness of the one or more two-dimensional layers of crystal of the organic semiconductor material is 20 nm or less.

2. The method according to claim 1, wherein the organic semiconductor material is mainly composed of organic molecules having π -conjugate systems.

3. The method according to claim 2, wherein the organic molecules having π -conjugate systems are selected from a group consisting of aromatic polycyclic compounds, compounds comprising one or more porphyrin cores, and compounds comprising one or more phthalocyanine cores.

4. The method according to claim 2, wherein the organic molecule having π -conjugate systems is represented by general formula (1):



where R^1 and R^2 are each independently hydrogen or a linear or branched alkyl group having 1 to 12 carbon atoms; Ar represents a monocyclic aromatic group or a fused polycyclic aromatic group; n is an integer from 1 to 4.

5. The method according to claim 2, wherein the organic molecule having π -conjugate systems is dioctylbenzothienobenzothiophene (C_8 -BTBT).

6. The method according to claim 5, wherein the source temperature is about 20°C to about 200°C.

7. The method according to claim 1, wherein the pressure in the vacuum chamber is 10^{-3} Torr or less.

8. The method according to any one of claims 1-7, wherein the support is graphene.
9. The method according to any one of claims 1-7, wherein the support is hexagonal boron nitride.
10. A layered structure, the layered structure comprising
a support having a crystalline surface; and
one or more two-dimensional layers of crystal of one organic semiconductor material epitaxially grown on the crystalline surface of the support;
wherein the total thickness of the one or more two-dimensional layers is 20 nm or less, and the support is a two-dimensionally layered material.
11. The layered structure according to claim 10, wherein the organic semiconductor material is mainly composed of organic molecules having π -conjugate systems.
12. The layered structure according to claim 11, wherein the organic molecules having π -conjugate systems are selected from a group consisting of aromatic polycyclic compounds, porphyrin derivatives, and phthalocyanine derivatives.
13. The layered structure according to claim 11, wherein the organic molecule having π -conjugate systems is represented by general formula (1):
$$R^1-[Ar]_n-R^2 \quad (1)$$

where R^1 and R^2 are each independently hydrogen or a linear or branched alkyl group having 1 to 12 carbon atoms; Ar represents a monocyclic aromatic group or a fused polycyclic aromatic group; n is an integer from 1 to 4.
14. The layered structure according to claim 11, wherein the organic molecules having π -conjugate systems is C₈-BTBT.
15. The layered structure according to any one of claims 10-14, wherein the support is graphene.
16. The layered structure according to any one of claims 10-14, wherein the support is hexagonal boron nitride.
17. Use of the layered structure according to any one of claims 10-16 in the fabrication of an electronic device.
18. An electronic device comprising the layered structure according to any one of claims 10-16.

19. The electronic device according to claim 18, wherein the electronic device is an organic field-effect transistor or diode.

20. An OR gate, comprising
a layered structure according to any one of claims 10-16, wherein the crystal of the organic semiconductor material is present as two separate pieces on the crystalline surface of the support, each piece having one or more two-dimensional layers with a total thickness of 20 nm or less;
two separate electrically conductive covers covering the top of the two crystal pieces respectively; and
a substrate underneath the support of the layered structure.

21. An AND gate, comprising
two separate layered structures according to any one of claims 10-16;
one electrically conductive cover covering the top of the crystal of the organic semiconductor material of both layered structures; and
a substrate underneath the supports of the layered structures.

Statement under Article 19(1)

This is a statement regarding the amendments of claims of the above-reference patent application under PCT Article 19.

The applicant believes that amended claim 1 under Article 19 is distinguished from and therefore novel and inventive over D1 (US5738720A), because the support in D1 is crystal of an inorganic salt which does not have a two-dimensionally layered structure like graphene or hBN in the present application. The force between the support and the crystal layer thereon that supports the growth is accordingly distinguished from that in D1 and not taught in D1. By the same token, the other claims in the amended claim set are believed to be novel and inventive over D1 as well.

Drawings

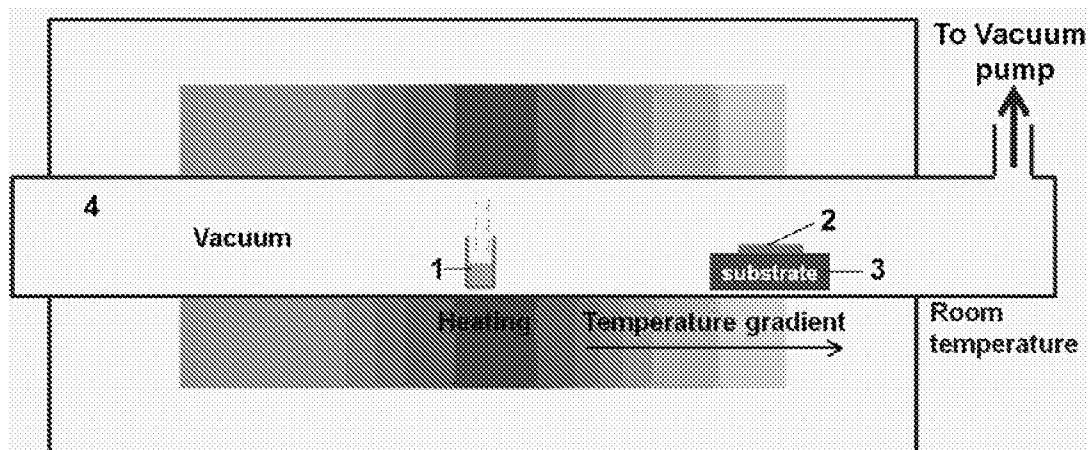


Figure 1

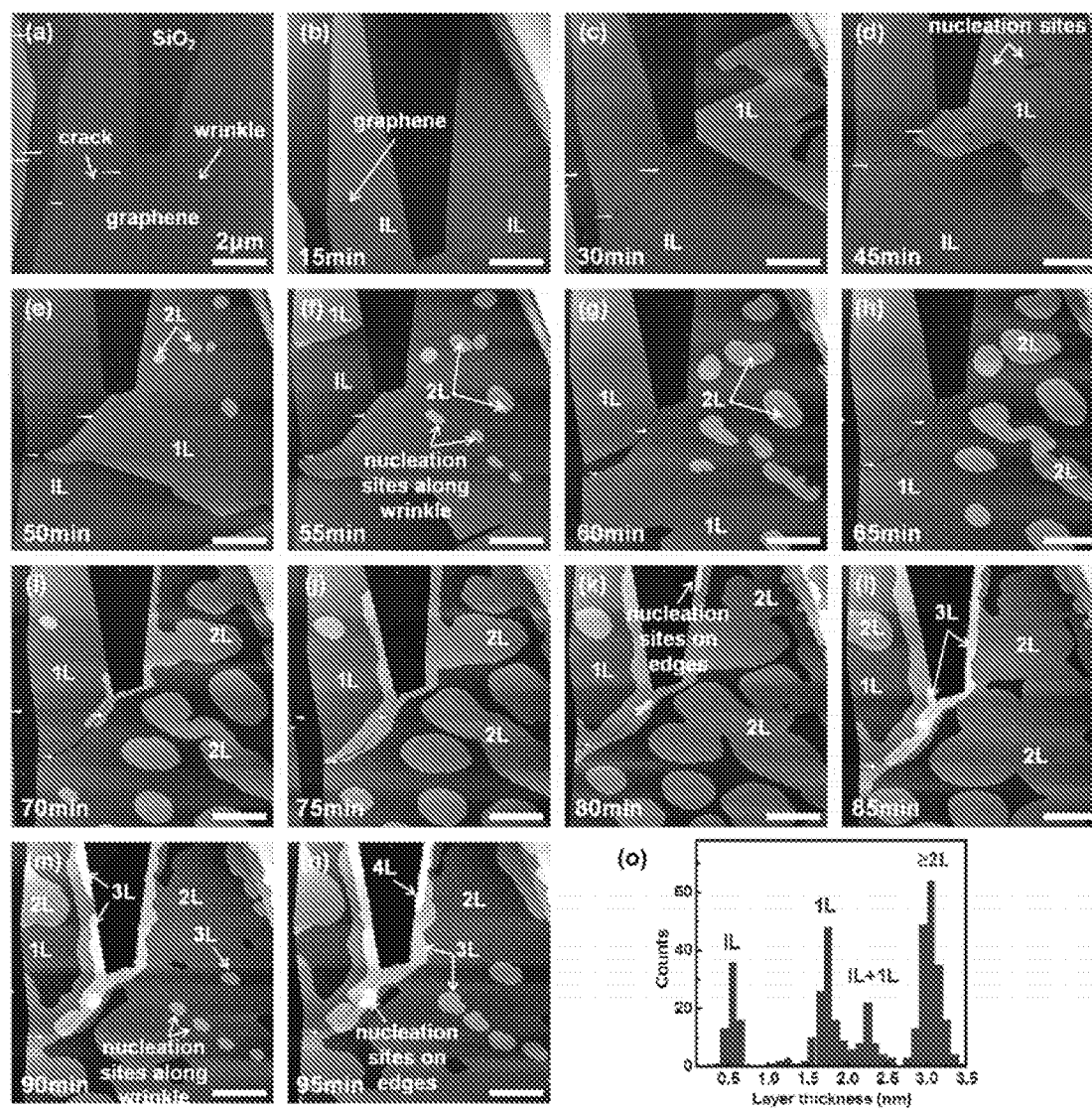


Figure 2

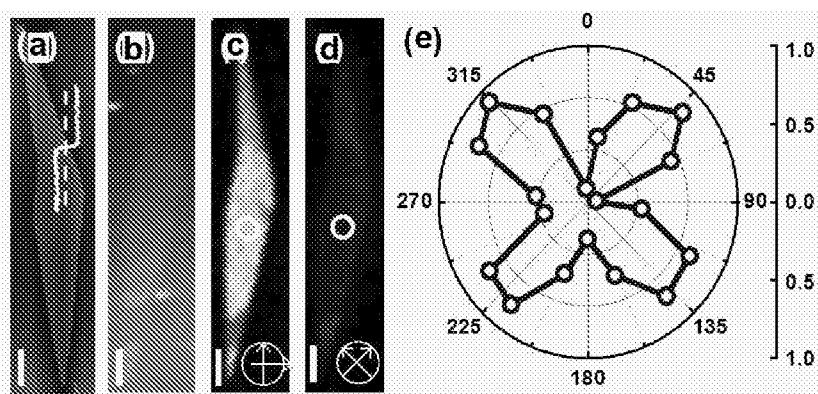


Figure 3

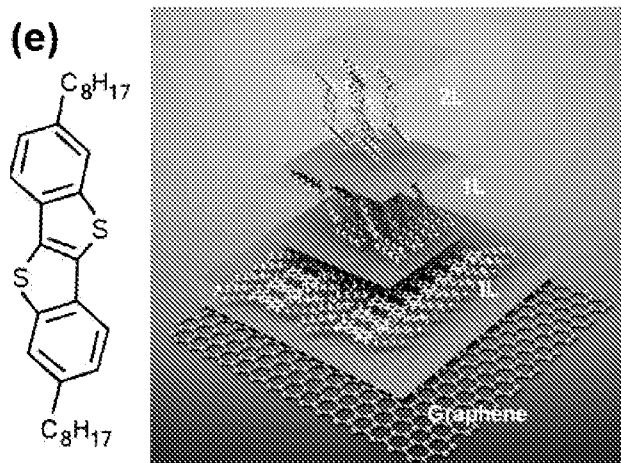
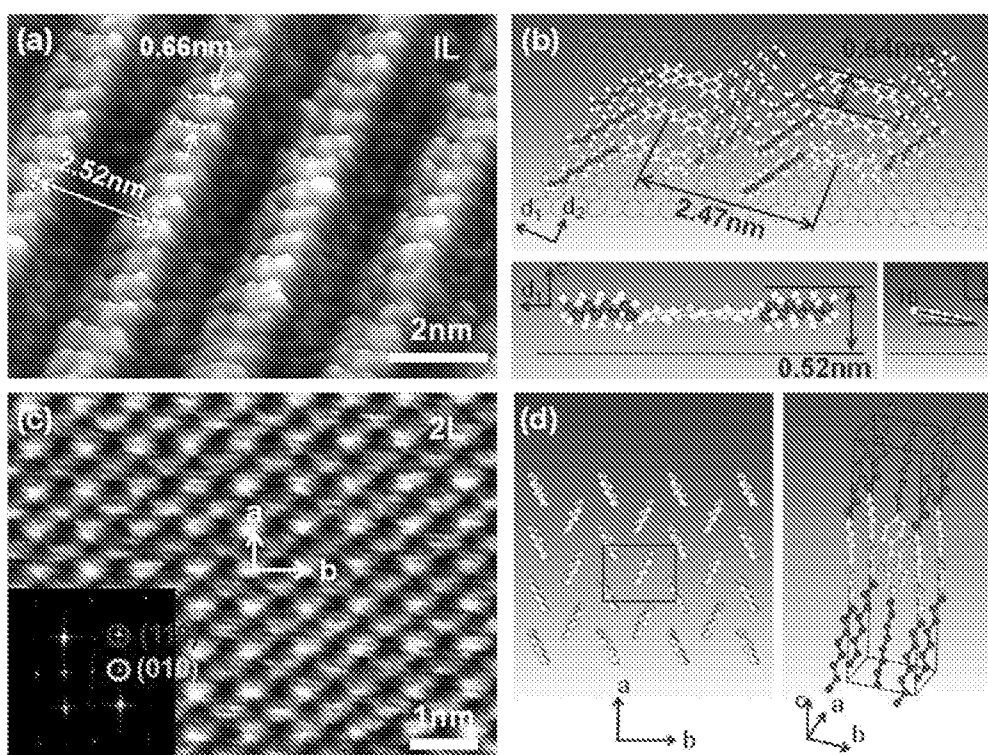


Figure 4

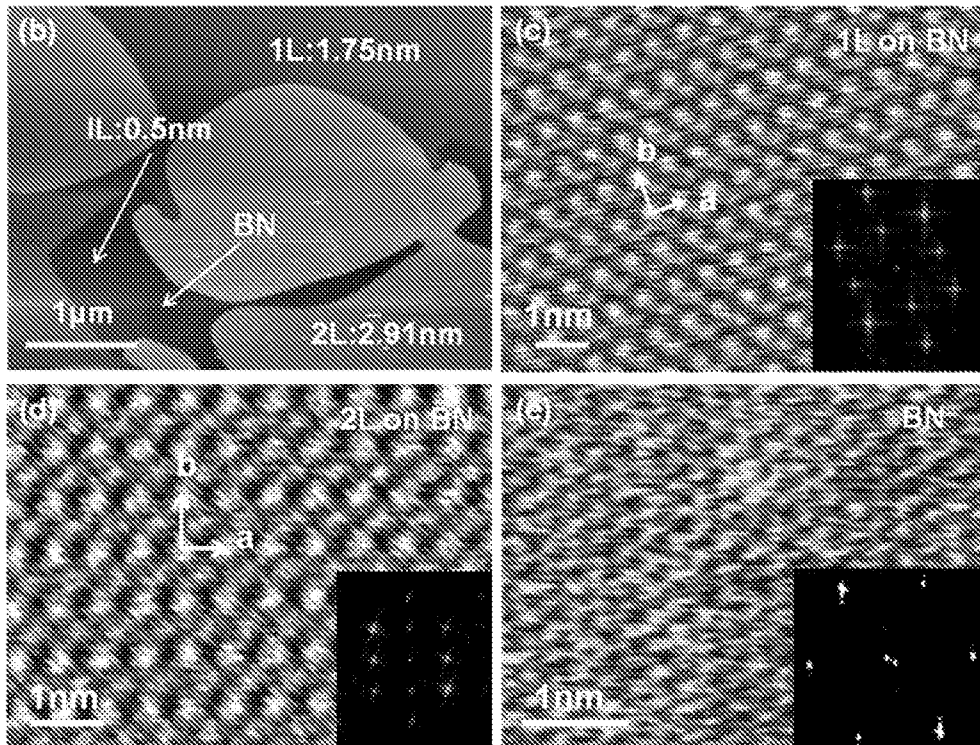


Figure 5

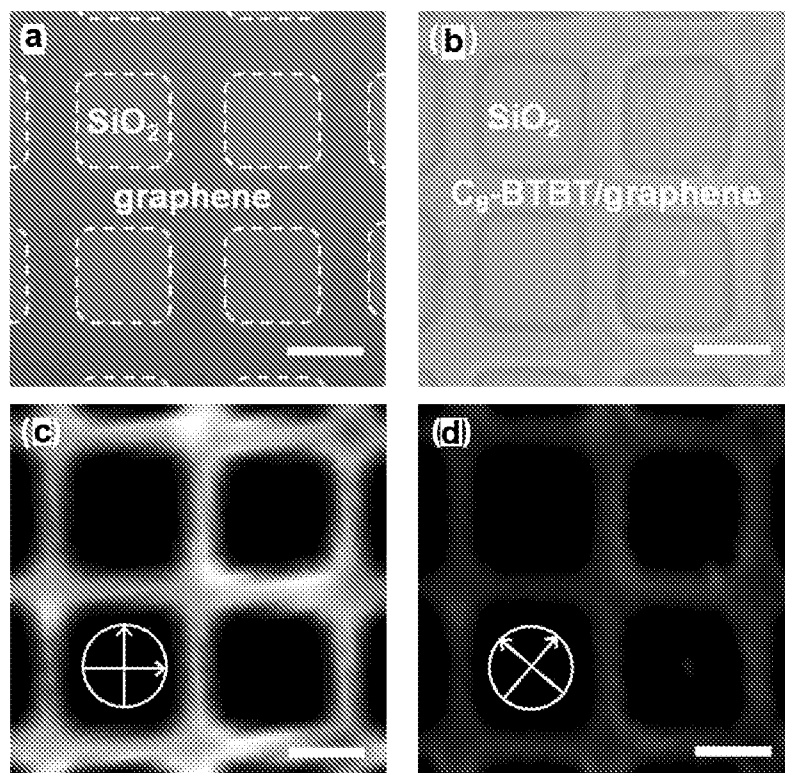


Figure 6

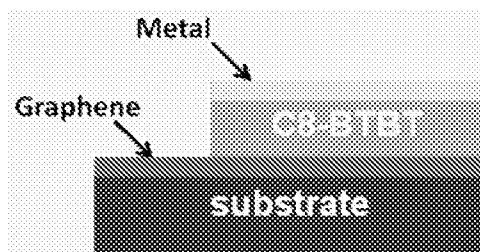


Figure 7

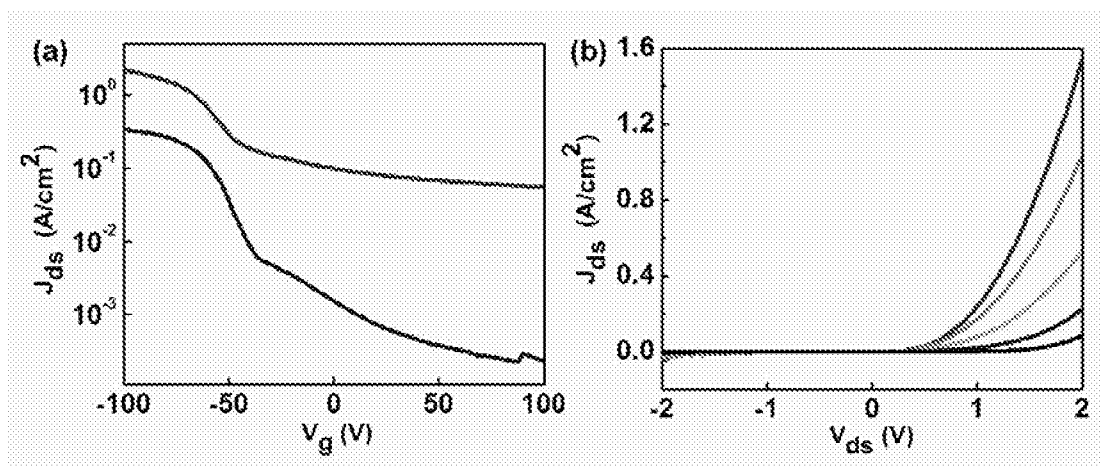


Figure 8

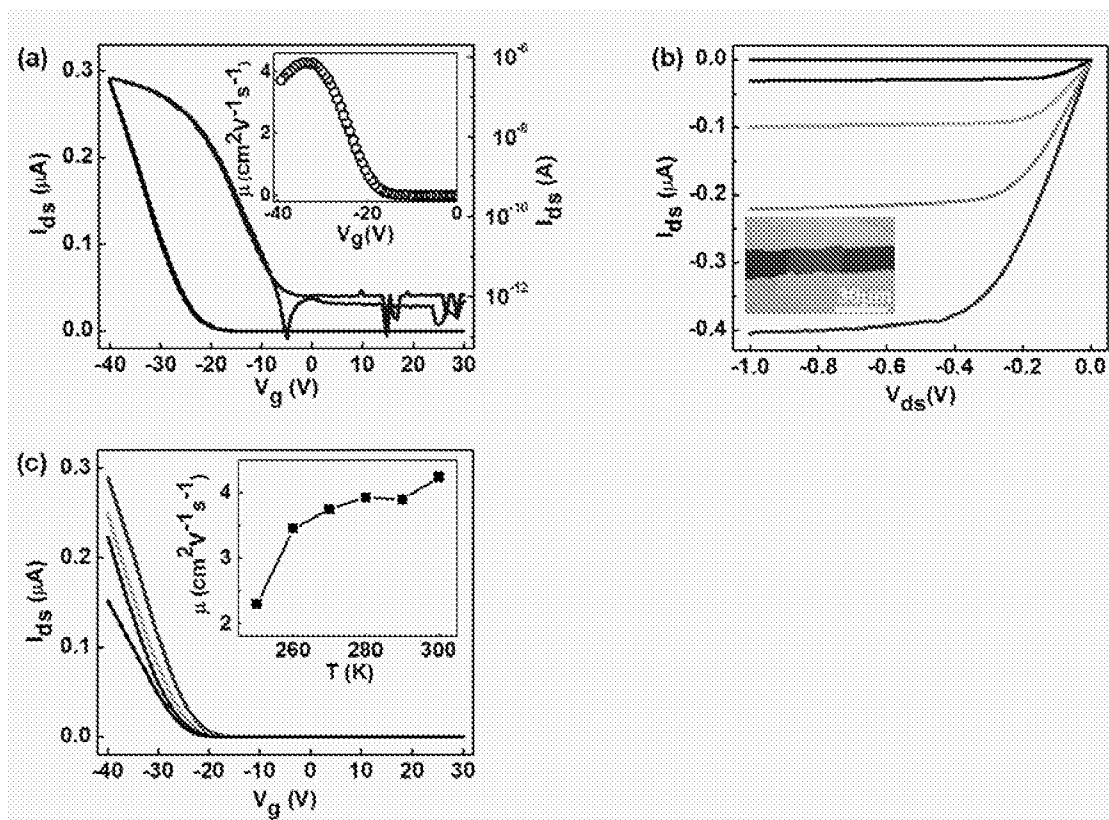


Figure 9

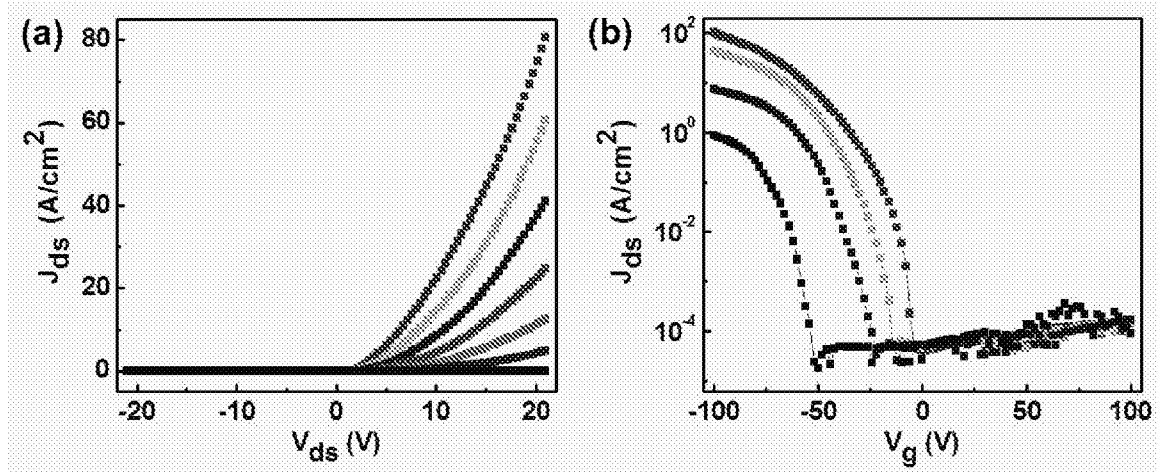


Figure 10

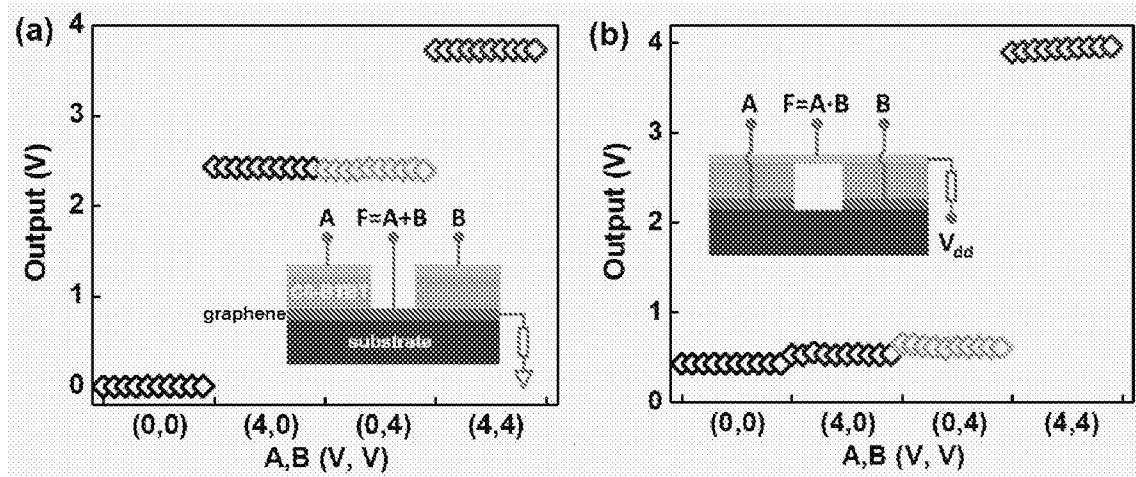


Figure 11

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2014/074947

A. CLASSIFICATION OF SUBJECT MATTER

C30B 29/54(2006.01)i; C30B 23/06(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

C30B 29/-; C30B 23/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS, CNKI, EPODOC, WPI, ???BTBT, epitaxial+, boron, polycyclic, ??conjugate?, epitaxy, BN, graphene, gradient?, nitride, porphyrin, temperature, evaporat+, sublime, crystal+, grow+, phthalocyanine?, semiconductor, aromatic

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5738720 A (UNIV TOKYO) 14 April 1998 (1998-04-14) description, col. 1, lines 10-23, col. 3, lines 11-28, col. 4, line 52 to col. 5, line 16, col. 5, lines 45-55	1-22
A	CN 101260566 A (CHANGCHUN INSTITUTE OF APPLIED CHEMISTRY CHINESE ACADEMY OF SCIENCES) 10 September 2008 (2008-09-10) claims 1-5	1-22
A	CN 101955491 A (SHANGHAI CASAIL DISPLAY TECHNOLOGY LTD) 26 January 2011 (2011-01-26) claims 1-3	1-22



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

04 December 2014

Date of mailing of the international search report

30 December 2014

Name and mailing address of the ISA/CN

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Telephone No. (86-10)82245537

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2014/074947

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	5738720	A	14 April 1998	JP	H08264445	A	11 October 1996
				JP	2762046	B2	04 June 1998
CN	101260566	A	10 September 2008	CN	101260566	B	14 September 2011
CN	101955491	A	26 January 2011	WO	2011075932	A1	30 June 2011
				CN	101955491	B	12 November 2014
				EP	2518075	A1	31 October 2012
				EP	2518075	A4	29 May 2013
				US	2011152541	A1	23 June 2011
				JP	2013515016	A	02 May 2013