Figure 4B

Abstract: A memory cell with an internal supply feedback loop is provided herein. The memory cell includes a latch having two storage nodes Q and QB, and a supply node. A gating device couples the supply node of the latch to the supply voltage. The gating device is controlled by a feedback loop coming from storage node QB. Due to the aforementioned asymmetric topology, the writing of logic “1” and the writing of logic “0” are carried out differently. Contrary to standard SRAM cells, in the hold states, only the QB storage node presents a valid value of stored data. The feedback loop cuts off the supply voltage for the latch such that the latch is no longer an inverting latch. By cutting off the supply voltage at the stable hold states, while maintaining readability of the memory cell, leakage currents associated with the hold states are eliminated altogether.
before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(88) Date of publication of the international search report:
24 January 2013
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8): G 11 C 11/00, 11/22 (2012.01)
USPC: 365/156, 154

According to International Patent Classification (IPC) or to both national classification and IPC

B.FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8): G 11 C 11/00, 11/22, 7/6; H 01 L 21/8234 (2012.01)
USPC: 365/156, 154, 181, 182, 49, 11

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database consulted during the international search (name of database and, where practicable, search terms used)


C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US 7710674 B2 (PRADHAN, D et al.) April 27, 2010, Fig. 1, column 3, lines 25-28, Figure 5, column 4, lines 21-29, column 2, lines 44-55, Figure 5, column 6, lines 13-21</td>
<td>1-7</td>
</tr>
</tbody>
</table>

Further documents are listed in the continuation of Box C.

Date of the actual completion of the international search: 12 November 2012 (12.1.2012)

Date of mailing of the international search report: 3 NOV 2012

Name and mailing address of the ISA/US:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-3201

Authorized officer: Shane Thomas
PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774

Form PCT/ISA /210 (second sheet) (July 2009)
### INTERNATIONAL SEARCH REPORT

**International application No.**
PCT/IB 12/52265

**Box No. II** Observations where certain claims were found unsearable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. □ Claims Nos.:
   because they relate to subject matter not required to be searched by this Authority, namely:

2. □ Claims Nos.:
   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. □ Claims Nos.:
   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box No. II** Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

*Group I: Claims 1-7; Group II: Claims 8-15*

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1; in order for all inventions to be examined, the appropriate additional examination fee must be paid.

*Group I: Claims 1-7 are directed toward a memory cell comprising: a latch having a supply node, a ground node, a storage node Q, and a storage node QB; a gating device having a control node and further connected to a voltage supply and to the supply node of the latch; and a feedback loop connecting the storage node QB with the control node of the gating device, wherein the ground node of the latch is connected to ground and wherein the storage node Q and the storage node QB are each connected to a separate write circuitry, wherein responsive to a writing of a logic "0" or a logic "1" into the memory cell, the feedback loop and the gating device are configured to cut off the voltage supply to the latch when the storage nodes reach steady state in which only one of the storage nodes stores a valid value while maintaining readability, and wherein leakage currents through the latch are reduced in the steady state.*

- Continued Within the Extra Page...**+

   □ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

   2. □ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

   3. □ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

   4. ✗ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

   Claims 1-7

**Remark on Protest**

□ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

□ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

□ No protest accompanied the payment of additional search fees.

Form PCT/ISA/210 (continuation of first sheet (2)) (July 2009)
-Continued from Box No. III: Observations where unity of invention is lacking-

Group II: Claims 8-15 are directed toward a memory cell comprising: a first nMOS device having a gate, a source, and a drain; a first pMOS device having a gate, a source, and a drain; a second nMOS device having a gate, a source, and a drain; a second pMOS device having a gate, a source, and a drain; and an nMOS gating device having a gate, a source, and a drain, wherein the source of the second pMOS device, the drain of the second nMOS device, and the gates of the first nMOS and the first pMOS devices are connected together forming a storage node QB, wherein the source of the first pMOS device, the drain of the first nMOS device, and the gates of the second nMOS and the second pMOS devices are connected together forming a storage node Q, wherein the sources of the first and the second nMOS devices are connected to ground, wherein the drains of the first and the second pMOS devices are connected to the source of the gating device, wherein the drain of the nMOS gating device is connected to a supply voltage, and wherein the gate of the nMOS gating device is connected to the storage node QB.

The common technical feature shared by Groups I and II are a memory cell comprising: a latch having a supply node, a ground node, a storage node Q, and a storage node QB; a gating device having a control node and further connected to a voltage supply and to the supply node of the latch. However, this common feature is previously disclosed by US 7,548,456 B2 (Chiu). Chiu discloses a memory cell (a SRAM cell, abstract) comprising: a latch having a supply node (supply voltage Vcc, abstract, figure 3A), a ground node (ground GND, figure 3A), a storage node Q, and a storage node QB (combo memory cell 200, figure 2); a gating device (gates of first pMOS and nMOS, abstract) having a control node and further connected to a voltage supply and to the supply node of the latch (the sources of the first and second nMOS transistors N1 and N2 are coupled to the ground GND or the supply voltage Vcc, abstract, figure 3A, column 3, lines 53-67).

Since the common technical feature is previously disclosed by the Chiu reference, this common feature is not special and so Groups I and II lack unity.