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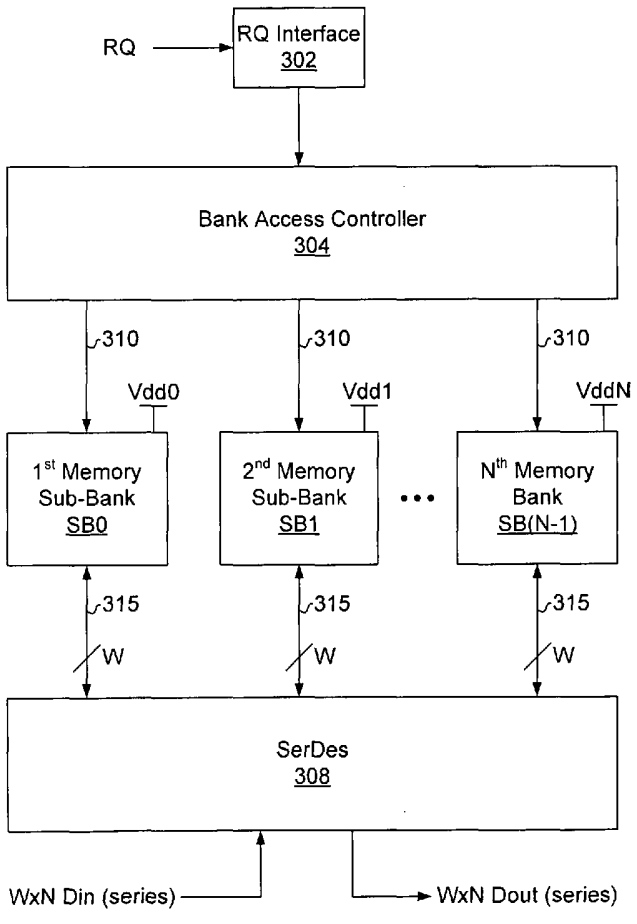

(57) Abstract: A memory system includes logical banks divided into sub-banks or collections of sub-banks. The memory system responds to memory-access requests (e.g., read and write) directed to a given logical bank by sequentially accessing sub-banks or collections of sub-banks. Sequential access reduces the impact of power-supply spikes induced by memory operations, and thus facilitates improved system performance. Some embodiments of the memory system combine sequential sub-bank access with other performance-enhancing features, such as wider power buses or increased bypass capacitance, to further enhance performance.

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MEMORY DEVICE HAVING STAGGERED MEMORY OPERATIONS

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BACKGROUND

[0001] Figure 1 (prior art) shows a block diagram of a basic memory component 100, which includes a control interface 102 and a collection of four logical banks B0-B3 distributed among four quadrants 104. Each logical bank includes left and right sub-banks: for example, bank B0 includes a left sub-bank LB0 in the upper left quadrant and a right sub-bank RB0 in the lower right quadrant 104. As discussed in more detail below, physically separating banks reduces local power-supply fluctuations resulting from memory accesses, and consequently reduces deleterious noise and the resultant adverse impact on speed performance.

[0002] Each quadrant 104 includes a two-dimensional array of storage cells (not shown), a row/column address decoder 105, and sense amplifiers 106. Decoders 105 activate specified rows and access columns of the memory cells, while sense amplifiers 106 sense and temporarily store data extracted from a specified row in the associated banks or sub-banks. Data moved to or from the storage cells through a sense amplifier by an "activate" operation are available for access by read and write operations. Data is delivered to and extracted from memory component 100 via respective write pipes 107 and read pipes 108.

[0003] A "column" is the quanta of data accessed in a given row currently residing in the sense amplifier during a read or write operation. An external device, typically a memory controller, accesses the storage cells in one logical bank (e.g., sub-banks LB0 and RB0) by issuing an appropriate data-access request (read request or write request) to control interface 102, which in turn presents the appropriate address and control signals to the specified sub-banks via internal address and control buses 110.

[0004] Figure 2A (prior art) illustrates the movement of data during three steps for accessing data in one of the logical banks introduced in Figure 1. Step one is an activate operation in which data from a selected row in each of a corresponding pair of sub-banks are selected and placed into the associated sense amplifiers. Step two is a data-access (read or write) operation in which one column of the selected row (held in the sense amplifiers) is selected and accessed. Data from the sense amplifiers are transferred to read pipes 108 (read

data), or data in write pipes 107 is transferred into the sense amplifiers. In Figure 2A, the label "c" means "column."

[0005] Step three is a precharge operation. The sub-banks and sense amplifiers are deselected and left in a state in which another activate operation can access a different row. Prior to deselection, the data in the sense amplifiers, including any data modified by a write operation, are copied back to the storage cells of the selected row of the selected logical bank. In the present disclosure, an "operation" refers to memory operations, for example, one of the above mentioned steps (activate, read, write, precharge). A "transaction" specifies a sequence of one or more operations that accesses a memory component. The following examples assume that transactions are directed to precharged banks and that each transaction performs a precharge operation after each read or write operation.

[0006] Figure 2B (prior art) is a timing diagram illustrating a read transaction directed to a precharged logical bank. A clock signal CLK is shown across the top of the diagram for reference. The "RQ" label identifies a collection of control/address signals that convey transaction requests to control interface 102, the label "DATA" identifies information conveyed to an external requestor, and the label "READ" identifies data conveyed to read pipes 108. The illustrative read transaction includes the following events:

1. At clock edge 0, interface 102 receives an ACT (activate) command specifying one row of a logical bank, logical bank B0 in this example. Via control buses 110, control interface 102 asserts a bit-sense signal BSen to specified logical bank B0, and thus opens one corresponding row in each sub-bank LB0 and RB0. Opening the rows requires power, and thus produces a power spike 210 on supply voltage Vdd. As shown in Figure 1, each quadrant 104 is connected locally to supply voltage Vdd, and sub-banks are physically separated. The physical separation reduces the combined impact of accessing the sub-banks, but each quadrant 104 nevertheless suffers some supply-voltage degradation.
2. At clock edge 5, control interface 102 receives a read command RD for a given column of the now active logical bank B0. Control interface 102 responds by issuing a column-selection signal CSel via buses 110 to selected sub-columns within the selected sub-banks LB0 and RB0. Column accesses are power intensive, and thus produce another power spike 215. In this example, the column access causes 32 bits of read data RD from each sub-bank of the selected logical bank to be conveyed to read pipes 108. The two

32-bit data words from the read pipes together make up a single 64-bit data word DQ.

3. At clock edge 9, control interface 102 receives a PRE (precharge) command for the logical bank B0. Control interface 102 responds by issuing a precharge signal Pre via buses 110 to sub-banks LB0 and RB0 to deselect the logical banks in preparation for subsequent read and write transactions. The precharge operation once again draws supply power, and consequently produces yet another power spike 220. (The shapes and sizes of spikes 210, 215, and 220 are merely illustrative.)

Write transactions, similar to read transactions and producing similar power spikes, are well understood and are therefore omitted here for brevity.

[0007] Power-supply spikes of the type described above limit device performance. As noted above, the amplitude of such spikes is limited by dividing memory banks into widely separated sub-banks. Other approaches include the use of more and wider power buses and increased local bypass capacitance. Unfortunately, these approaches consume die area, and are thus undesirable.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0009] Figure 1 (prior art) shows a block diagram of a basic memory component 100, which includes an control interface 102 and a collection of four logical banks B0-B3 distributed among four quadrants 104.

[0010] Figure 2A (prior art) illustrates the movement of data during three steps for accessing data in one of the logical banks introduced in Figure 1.

[0011] Figure 2B (prior art) is a timing diagram illustrating a read transaction directed to a precharged logical bank.

[0012] Figure 3 depicts an integrated-circuit (IC) memory component 300 in accordance with one embodiment.

[0013] Figure 4A describes a read transaction performed by component 300 of Figure 3 in response to a read request received on lines RQ.

[0014] Figure 4B depicts the response of component 300 of Figure 3 to a write request on lines RQ.

[0015] Figure 5 depicts a memory component 500 in accordance with another embodiment.

[0016] Figure 6 is a timing diagram illustrating a read transaction directed to a pre-charged logical bank of component 500 (i.e., one sub-bank from each of the four quadrants) to retrieve 512 bits of information.

[0017] Figure 7 is a functional block diagram of memory component 500 of Figure 5. Interface 510 is broken into a request interface 700 and bank-access control logic 705.

DETAILED DESCRIPTION

[0018] In several embodiments of the present disclosure, memory device, apparatus, and methods of performing memory accesses in sequential fashion are described. For example, a memory access, such as one initiated in response to an activate command, a read command and/or a write command effectuates a divided or sequenced internal response. In an example of an activate command, received on the pins of the memory device, internal row activation and sensing is sequenced into two or more row sense operations. Here a delay time is inserted between row sense operations or the divided row operations can be timed using a clock signal (e.g., rising edges of the clock or both falling and rising edges of the clock signal). In the case

of a read or write command, an internal prefetch of a plurality of data bits, based on a locality given by a column address, is staggered using delay circuitry or sequenced on consecutive timing events referenced by an external clock signal. One benefit of performing memory accesses in sequential fashion internally is that power spikes can be reduced. Another benefit of performing memory accesses in sequential fashion internally is that memory bandwidth may be increased.

[0019] Figure 3 depicts an integrated-circuit (IC) memory component 300 in accordance with one embodiment. One benefit realized in component 300 is that the impact of power-supply spikes induced by memory transactions can be reduced. To accomplish this reduction, component 300 sequentially accesses sub-banks of the core memory in response to memory access requests directed to a given bank. A memory access request may also be referred to as a command. The sequential core access offsets the memory operations in time, and in an embodiment, reduces the amplitude of the resulting power-supply spikes. In this embodiment, memory component 300 can thus be used at higher data rates without wider power buses or increased bypass capacitance. Other embodiments combine sequential sub-bank access with other performance-enhancing features, such as wider power buses or increased bypass capacitance, to further enhance performance.

[0020] Component 300 includes a request interface 302, a bank-access controller 304, N memory sub-banks SB[0:N-1], and a serializer/de-serializer (SerDes) 308. In the depicted embodiment, data Din is received as a series of WxN-bit data symbols, where N is the number of sub-banks and W is the width of each sub-bank. How many bits of data are provided in a given access to a particular sub-bank depends on the width. SerDes 308 divides these symbols into N sub-words, each of W bits. Bank access controller 304 then conveys access-control signals on access-control ports 310 to successive ones of memory banks SB[0:N-1] to sequentially store each sub-word into a corresponding one of the sub-banks. Assuming, for example, that W is 128 and N is 2, data Din arrives in words of 128x2=256 bits. SerDes 308 divides received data into the two constituent sub-words, 128-bits each, and controller 304 issues the appropriate control signals to store the first sub-word into memory sub-bank SB0 and then the second sub-word into the second sub-bank SB1 via respective parallel data ports 315. In this embodiment, controller 304 offsets the storage operations used during the write transaction to offset the supply-voltage spikes caused by the sub-bank accesses, and thus reduces the amplitude of the resulting power-supply noise. Component 300 likewise offsets the operations used in read transactions to minimize power-supply noise. By reducing supply noise, component 300 supports higher data bandwidth and otherwise

improves device performance; alternatively, the reduced impact on local supply voltages can be used to reduce supply line width, local bypass capacitance, or both, to save valuable die area. Conventional methods of reducing supply noise may be used in conjunction with sequential sub-bank access to further improve performance.

[0021] In various embodiments, circuits and methods described above in relation to the integrated circuit component 300 are applied to integrated circuit memory devices having a dynamic random access memory (DRAM) core such as Extreme Data Rate (XDR™) DRAM architecture, or Double Data Rate (DDR) Synchronous DRAM architecture. Other integrated circuit memory technologies are applicable to the apparatus and circuits described herein, for example, Flash memory device technology.

[0022] Figure 4A describes a read transaction performed by component 300 of Figure 3 in response to a read request received on lines RQ. Figure 4B describes a similar write transaction. Both examples assume only the first and second sub-banks SB0 and SB1 are accessed, but the sequence of operations can easily be extended to three or more sub-banks.

[0023] In Figure 4A, at step 400, request interface 302 receives an activate command on request bus RQ and conveys a form of this command to bank access controller 304. Controller 304 activates first memory sub-bank SB0 by applying the appropriate signals on the leftmost access-control port 310 (step 405). This memory access draws supply current, so the voltage at local supply node Vdd0 (Figure 3) drops slightly during step 405. Shortly after step 405, e.g. one memory clock cycle later, bank access controller 304 activates the second memory sub-bank SB1 (step 410), resulting in a supply spike at local supply node Vdd1. Sub-banks SB0 and SB1 are physically separated and their respective accesses are spread over time, both of which tend to reduce the overall amplitude of the supply noise. In other embodiments, bank access controller 304 activates the second memory sub-bank two or more clock cycles after step 405.

[0024] In another embodiment, bank access controller inserts a delay time to activate the second memory sub-bank SB1 (step 410). That is, respective accesses to sub-banks SB0 and SB1, that occur in response to an activate command, can be separated by a delay time. For example, accesses separated in time by a delay may be initiated by delaying an internal command using an inverter chain or by inserting resistive and capacitive elements to introduce a resistive capacitive time constant to the internal command.

[0025] Next, and still in response to the same read request, bank access controller 304 sequentially accesses first sub-bank SB0 (step 415) and second sub-bank SB1 (step 420). Access steps 415 and 420 once again impact local supply voltages Vdd0 and Vdd1, and are

again separated in time to minimize the combined effects. Controller 304 then successively pre-charges sub-bank SB0 (step 425) and sub-bank SB1 (step 430), with the timing offset yet again minimizing the combined effects on the local supply voltages. At some point after access steps 415 and 420, SerDes 308 serializes the parallel data provided from first and second sub-banks SB0 and SB1 and conveys the resulting serialized data from memory component 300 on output port Dout (step 435). Alternative embodiments employ parallel input data, output data, or both.

[0026] Figure 4B depicts the response of component 300 to a write request on lines RQ. To begin with, interface 302 receives an activate command (step 440). SerDes 308 breaks a WxN-bit word to be written to memory into separate W-bit sub-words (step 445). Controller 304 then activates first sub-bank SB0 (step 450) and next activates second sub-bank SB0 (step 455) to sequentially prepare them to receive respective ones of the sub-words from SerDes 308. Controller 304 then issues access control signals to the first and second memory sub-banks to select the addressed columns in those sub-banks. These accesses are done sequentially, in steps 460 and 465, to reduce the impact of the resulting power supply glitches. The sequential accesses, such as the ones performed in steps 460 and 465, can also be performed to achieve other benefits, for example; internal read and/or write pipeline resources may be reduced by multiplexing sequential accesses in time. Internal read/write pipelines refer to internal data paths, including associated circuitry, used to move data between the interface (e.g., interface circuitry coupled to terminals such as pins, balls, etc.) and the sense amplifiers. Finally, the first and second memory sub-banks are each pre-charged, again in sequence (steps 470 and 475) to complete the write cycle.

[0027] Figure 5 depicts a memory component 500 in accordance with another embodiment. Component 500 is similar to memory component 100 of Figure 1, but is adapted in accordance with one embodiment to provide offset read and write access to the various sub-banks. The resulting reduction in the amplitude of power supply spikes allows for increased bandwidth and facilitates the extension of the core width of component 500 from 32 bits to 128 bits, where core width is a measure of the number of bits moved to or from memory component 500 in response to one write or read request.

[0028] Component 500 has, in this embodiment, four quadrants, one in each of the four corners. Each quadrant includes 16 discreet sub-banks. Sub-banks from all four quadrants are combined to reduce the amplitude of power-supply spikes resulting from memory operations. Each quadrant includes additional conventional memory circuitry, such as sense amplifiers, row decoders, and column decoders, but these are omitted here for ease of

illustration. Memory control circuitry 510 provides timing and control signals to the four quadrants, left and right read pipes 515, and left and right write pipes 520.

[0029] Each read transaction produces two successive 256-bit collections of data, for a total of 512 bits of information. The first 256 bits produced in a read transaction are provided from corresponding sub-banks from quadrant L0 (for "left-quadrant zero") and quadrant R0 (for "right quadrant zero"), each of which provides 128 bits; the second 256 bits are similarly provided from quadrants LQ1 and RQ1. The circuitry that responds to the first half of each read request can be physically separated into opposite corners to reduce local supply spikes, while staggering the operations in time further reduces such spikes.

[0030] Figure 6 is a timing diagram illustrating a read transaction directed to a pre-charged logical bank of component 500 (i.e., one sub-bank from each of the four quadrants) to retrieve 512 bits of information. A clock CLK is shown across the top of the diagram for reference. The RQ label identifies the transactional request conveyed to interface 510 and the label DATA provides information conveyed from left and right read pipes 515, collectively. The illustrative read transaction includes the following events and operations.

[0031] At clock edge 0, interface 510 receives an activate command ACT specifying one row of a logical bank. The present example assumes that the logical bank comprises sub-banks L0B[0], R0B[0], L1B[0], and R1B[0]. Interface 510 activates the row specified in the read request by issuing appropriate row-access control signals to the appropriate sub-banks. Among these signals, a bit-sense signal BSen0 to quadrants LQ0 and RQ0 on buses 525 activates the sense amplifiers of those quadrants, causing a Vdd spike 605. A number of clock cycles later, one clock cycle in this embodiment, interface 510 issues a second bit-sense signal BSen1 to quadrants LQ1 and RQ1 on buses 530 to activate the sense amplifiers of those quadrants, causing a second Vdd spike 610. A third spike 615 illustrates the theoretical combined impact of accessing all four quadrants simultaneously instead of offsetting the accesses in the manner described: the relatively lower amplitudes resulting from the offset memory operations reduce the amplitude of the maximum Vdd spikes.

[0032] The read and precharge operations are offset in the manner of the activate operation. Namely, interface 510 responds (1) to a read request RD with a column select command CSel0 to quadrants LQ0 and RQ0 and, a clock cycle later, with a second column select command CSel1 to quadrants LQ1 and RQ1; and (2) to a precharge request PRE with a precharge command Pre0 to quadrants LQ0 and RQ0 and, a clock cycle later, with a second precharge command Pre1 to quadrants LQ1 and RQ1. Supply voltage Vdd exhibits a pair of consecutive spikes for each of the read and precharge requests.

[0033] As a result of the single read operation, read pipes 515 together produce two 256-bit words separated by one clock cycle. A serializer (not shown) combines words RD0 and RD1 into a single, serial, 512-bit data word DQ0. In some embodiments, the serializer begins transmitting the first 256 bits of data DQ0 before the second 256 bits are available for transmit. Write transactions are accomplished in the same manner as read transactions, and the spacing of the pre-charge, activate, and sense operation similarly reduces the impact of write transactions on power supply voltage. Write transactions are therefore omitted here for brevity.

[0034] Component 500 separately controls sub-sets of each logical bank, and thus requires additional control lines as compared with conventional systems. Offsetting this increased overhead, read and write pipes 515 and 520 sequentially produce the output data over two clock cycles, and are thus only half the length of the output data.

[0035] Figure 7 is a functional block diagram of memory component 500 of Figure 5. Interface 510 is broken into a request interface 700 and bank-access control logic 705. Interface 700 receives requests RQ, for example, in the form of operation codes, or "op-codes," for control logic 705. The operation codes may be received sequentially or in parallel. Control logic 705 includes an op-code decoder 710 that decodes the op-codes and issues appropriate control signals to activation logic 715, column-select logic 720, and precharge logic 725. Decoder 710 additionally provides row and column addresses and other control signals well understood by those of skill in the art, but these are omitted here for brevity.

[0036] Activation logic 715, column logic 720, and precharge logic 725 issue respective bit-sense control signals BSen0, column select signals CSel0, and precharge signals Pre0 to sub-banks LQ0 and RQ0, depicted as one block, and issue respective bit-sense control signals BSen1, column select signals CSel1, and precharge signals Pre1 to sub-banks LQ1 and RQ1, also depicted as one block. As detailed above in connection with Figures 5 and 6, memory operations are performed sequentially, first on sub-banks LQ0 and RQ0 and then on sub-banks LQ1 and RQ1. Each of the control signals from bank-access control logic 705 is timed accordingly.

[0037] Read pipes 515 each include a multiplexer 730 feeding a 128-bit register 735. When transferring data from the sub-banks to read pipes 515, column logic 720 asserts a select signal on line Q0/Q1b, coupling the outputs of quadrants LQ0 and RQ0 to respective left and right registers 735, and asserts a load signal LD that latches the outputs of the selected quadrants into registers 735. Then, during the next clock cycle, column logic 720 de-asserts the select signal on line Q0/Q1b, coupling the outputs of quadrants LQ1 and RQ1 to

respective left and right registers 735, and once again asserts load signal LD to latch the outputs of quadrants LQ1 and RQ1. 512 bits of data are thus presented to a serializer 740 over two clock cycles. Serializer 740 combines the two 256-bit sequences into 512-bit serial data. In some embodiments, serializer 740 transmits some or all of the first-received 256 bits before registers 715 are loaded with the second set of data provided in response to the single memory request. Serializer 740 may be integrated with or separated from component 500, and registers 735 can be part of serializer 740.

[0038] The concepts illustrated in Figure 7 and the associated discussion can be extended to write and refresh transactions, as will be evident to those of skill in the art. A detailed discussion of write and refresh transactions is therefore omitted for brevity.

[0039] The foregoing embodiments reduce power-supply noise, and consequently facilitate core accesses that produce large numbers of bits. This advantage may be expected to grow in importance over time, as the speed performance of memory interfaces is increasing more rapidly than that of memory cores. Pipeline depths can thus be expected to deepen, with consequent increases in peak power, as larger chunks of data from the memory core are made available to support ever faster memory interfaces. The embodiments described herein can be used to bridge the widening performance gap between memory cores and memory interfaces.

[0040] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols are set forth to provide a thorough understanding of the present invention. In some instances, the terminology and symbols may imply specific details that are not required to practice the invention. For example, the interconnection between circuit elements or circuit blocks may be shown or described as multi-conductor or single conductor signal lines. Each of the multi-conductor signal lines may alternatively be single-conductor signal lines, and each of the single-conductor signal lines may alternatively be multi-conductor signal lines. Signals and signaling paths shown or described as being single-ended may also be differential, and vice-versa. Similarly, signals described or depicted as having active-high or active-low logic levels may have opposite logic levels in alternative embodiments. With respect to terminology, a signal is said to be "asserted" when the signal is driven to a low or high logic state (or charged to a high logic state or discharged to a low logic state) to indicate a particular condition. Conversely, a signal is said to be "deasserted" to indicate that the signal is driven (or charged or discharged) to a state other than the asserted state (including a high or low logic state, or the floating state that may occur when the signal driving circuit is transitioned to a high impedance condition, such as an open

drain or open collector condition). A signal driving circuit is said to "output" a signal to a signal receiving circuit when the signal driving circuit asserts (or deasserts, if explicitly stated or indicated by context) the signal on a signal line coupled between the signal driving and signal receiving circuits. A signal line is said to be "activated" when a signal is asserted on the signal line, and "deactivated" when the signal is deasserted. Whether a given signal is an active low or an active high will be evident to those of skill in the art.

[0041] Various aspects of the subject-matter described herein are set out in the following numbered clauses:

1. An integrated circuit comprising:
   a. a bank-access controller adapted to receive memory access requests, including a first memory access request, and adapted to provide first and second access-control signals sequentially in response to the first memory access request;
   b. a first memory bank having:
      i. a first plurality of memory cells;
      ii. a first access-control port coupled to the bank-access controller and adapted to receive the first access-control signals from the bank-access controller; and
      iii. a first plurality of parallel data lines adapted to convey first data read in parallel from the first plurality of memory cells;
   c. a second memory bank having:
      i. a second plurality of memory cells;
      ii. a second access-control port coupled to the bank-access controller and adapted to receive the second access-control signals from the bank-access controller; and
      iii. a second plurality of parallel data lines adapted to convey second data read in parallel from the second plurality of memory cells; and
   d. a serializer coupled to the bank-access controller, the first plurality of data lines, and the second plurality of data lines, wherein the serializer is adapted to combine the first and second data into a series of data.

2. The integrated circuit of clause 1, further comprising a third plurality of parallel data lines adapted to convey first write data in parallel to the first memory bank and a fourth plurality of parallel data lines adapted to convey second write data in parallel to the second memory bank.

3. The integrated circuit of clause 2, further comprising a deserializer adapted to separate serial input data into the first and second write data.

4. The integrated circuit of clause 1, further comprising a memory-access request bus adapted to receive memory-access requests and a request interface coupled between the memory-access request bus and the bank-access controller.

5. The integrated circuit of clause 1, wherein the first and second memory banks are two of N memory banks, where N is at least two.

6. The integrated circuit of clause 1, wherein the bank-access controller is adapted to issue read and write control signals to the first and second memory banks.

7. The integrated circuit of clause 6, wherein the read and write control signals include column selection signals.

8. The integrated circuit of clause 1, further comprising a multiplexer having first multiplexer input terminals coupled to the first plurality of data lines, second multiplexer input terminals coupled to the second plurality of data lines, and multiplexer output terminals coupled to the serializer, wherein the serializer is coupled to the first and second pluralities of data lines via the multiplexer.

9. The integrated circuit of clause 8, further comprising a register disposed between the multiplexer output terminals and the serializer.

10. The integrated circuit of clause 1, wherein the first and second memory banks each include first and second sub-banks.

11. The integrated circuit of clause 1, wherein each of the first and second memory banks is a sub-bank of a logical bank.

12. A method of reading a set of data from an integrated-circuit memory, the method comprising:
    a. receiving a read request for the set of data;
    b. activating, in response to the read request, a first sub-bank containing a first subset of the data;
    c. activating, in response to the read request, a second sub-bank containing a second subset of the data;

d. reading, after activating the second sub-bank, the first sub-bank to obtain the first subset of data;
e. reading the second sub-bank to obtain the second subset of data; and
f. combining the first and second subsets of data into a serial data word.

13. The method of clause 12, further comprising precharging the first sub-bank and the second sub-bank.

14. A method of writing a set of data to an integrated-circuit memory, the method comprising:
a. receiving a write request;
b. receiving the set of data;
c. dividing the set of data into first and second parallel data words;
d. activating, in response to the write request, a first sub-bank;
e. activating, after activating the first sub-bank and in response to the write request, a second sub-bank;
f. writing the first parallel data word to the first sub-bank; and
g. writing, after writing the first parallel data word to the first sub-bank, the second parallel data word to the second sub-bank.

15. The method of clause 14, further comprising precharging the first sub-bank and the second sub-bank.

16. The method of clause 14, wherein activating one of the first and second sub-banks includes activating a plurality of bit sense amplifiers and selecting a plurality of memory columns.

17. A memory system comprising:
a. a request interface adapted to receive memory requests;
b. bank-access control circuitry coupled to the request interface, the bank-access control circuitry including:
i. a decoder coupled to the request interface and adapted to decode the memory requests;
ii. activation logic coupled to the decoder and adapted to issue first and second activation commands via respective first and second activation ports;
c. a first sub-bank including:

i. a first plurality of memory cells;

ii. a first plurality of data lines coupled to the memory cells; and

iii. a first memory control port coupled to the first activation port;

iv. wherein the first sub-bank activates the first plurality of memory cells in response to the first activation command; and

d. a second sub-bank including:

i. a second plurality of memory cells;

ii. a second plurality of data lines coupled to the memory cells; and

iii. a second memory control port coupled to the second activation port;

iv. wherein the second sub-bank activates the second plurality of memory cells in response to the second activation command.

18. The memory system of clause 17, further comprising a serializer coupled to the first and second pluralities of data lines.

19. The memory system of clause 17, further comprising a deserializer coupled to the first and second pluralities of data lines.

20. A memory module comprising:

a. a plurality of logical memory banks, each logical memory bank divided into a corresponding plurality of sub-banks, including a first sub-bank having a first plurality of data lines and a second sub-bank having a second plurality of data lines;

b. a request interface adapted to receive operation requests directed to the logical memory banks; and

c. bank-access control logic coupled to the request interface and adapted to receive and decode the operation requests, the bank access control logic including a first control port coupled to a first sub-bank and a second control port coupled to the second sub-bank, the bank-access control logic issuing, in response to one of the operation requests, a first activate command to the first sub-bank on a first clock cycle and a second activate command to the second sub-bank on a second clock cycle.

21. The memory module of clause 20, wherein the activate command is part of a read transaction that sequentially produces first and second read data.

22. The memory module of clause 21, further comprising a serializer adapted to combine the first and second read data into a serial data stream.

23. A memory circuit comprising:
    a. a plurality of logical memory banks, each logical memory bank divided into a corresponding plurality of sub-banks, including a first sub-bank and a second sub-bank;
    b. means for sequentially activating, in response to a memory request directed to one of the logical memory banks, the first sub-bank and the second sub-bank; and
    c. means for sequentially accessing, in response to the memory request, the first sub-bank and the second sub-bank.

24. The memory circuit of clause 23, wherein the memory request is a read request.

25. The memory circuit of clause 24, wherein the first sub-bank produces first data in response to the read request and the second sub-bank produces second data in response to the read request.

26. The memory circuit of clause 25, further comprising means for combining the first and second data into a serial data stream.

27. The memory circuit of clause 23, wherein the memory request is a write request.

28. The memory circuit of clause 27, wherein the first sub-bank receives first data in response to the write request and the second sub-bank receives second data in response to the write request.

29. The memory circuit of clause 28, further comprising means for receiving the first and second data as serial input data and separating the first and second data prior to receipt of the first and second data by the respective first and second sub-banks.

[0042] While the present invention has been described in connection with specific embodiments, variations of these embodiments will be obvious to those of ordinary skill in the art. For example, the IC memory components described herein can be collected on a common printed-circuit board to form a memory module, or can be integrated with other types of circuitry to form myriad computational systems, including e.g. graphics cards, set-top boxes, game consoles, line cards, and wireless phones. Moreover, the IC memory

components need not be discrete memory ICs, but can instead be implemented and integrated with other types of circuitry, for example, in an embedded dynamic random access memory (DRAM) approach or in a system-on-chip (SOC) type of integrated circuit implementation. Embedded DRAM may be included with other circuits on an application specific integrated circuit (ASIC). Alternatively, multiple discrete integrated circuit memory devices, such as integrated circuit devices of the DRAM type, may be disposed in a single package using a multi-chip package (MCP) approach. Here the DRAM ICs are positioned within the package, either in a staked configuration or disposed on a two dimensional plane.

[0043] Some components are shown directly connected to one another while others are shown connected via intermediate components. In each instance the method of interconnection, or "coupling," establishes some desired electrical communication between two or more circuit nodes, or terminals. Such coupling may often be accomplished using a number of circuit configurations, as will be understood by those of skill in the art. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description. Only those claims specifically reciting "means for" or "step for" should be construed in the manner required under the sixth paragraph of 35 U.S.C. Section 112.

CLAIMS

What is claimed is:

1. An integrated circuit comprising:
first and second memory banks each including a respective plurality of memory cells;
a bank-access controller to provide, in response to a first memory access request, first and second access-control signals in sequence to the first and second memory banks, respectively, to enable the first and second memory banks to output in sequence, first read data and second read data, respectively; and
a serializer to receive the first and second read data from the first and second memory banks, respectively, and to combine the first and second read data into a series of data.

2. The integrated circuit of claim 1 wherein the serializer is coupled to the bank-access controller.

3. The integrated circuit of claim 1 further comprising a deserializer to separate serial input data into first and second write data and to output the first and second write data sequentially to the first and second memory banks, respectively.

4. The integrated circuit of claim 1, further comprising a memory-access request bus adapted to receive memory-access requests and a request interface coupled between the memory-access request bus and the bank-access controller.

5. The integrated circuit of claim 1, wherein the first and second memory banks are physically separated from one another.

6. The integrated circuit of claim 1, wherein the bank-access controller is adapted to issue read and write control signals to the first and second memory banks.

7. The integrated circuit of claim 6, wherein the read and write control signals include column selection signals.

8. The integrated circuit of claim 1, further comprising:
a first plurality of data lines to convey the first read data from the first memory bank to the serializer;
a second plurality of data lines to convey the second read data from the second memory

bank to the serializer; and

a multiplexer having first multiplexer input terminals coupled to the first plurality of data lines, second multiplexer input terminals coupled to the second plurality of data lines, and multiplexer output terminals coupled to the serializer, wherein the serializer is coupled to the first and second pluralities of data lines via the multiplexer.

9. The integrated circuit of claim 8, further comprising a register disposed between the multiplexer output terminals and the serializer.

10. The integrated circuit of claim 1, wherein the first and second memory banks each include first and second sub-banks.

11. The integrated circuit of claim 1, wherein each of the first and second memory banks is a sub-bank of a first logical bank.

12. A method of reading a set of data from an integrated-circuit memory, the method comprising:

activating, in response to a request to read data, a first sub-bank containing a first subset of the data and a second sub-bank containing a second subset of the data;

reading, after activating the second sub-bank, the first sub-bank to obtain the first subset of data;

reading the second sub-bank to obtain the second subset of data; and

combining the first and second subsets of data into a serial data word.

13. The method of claim 12, further comprising precharging the first sub-bank and the second sub-bank.

14. A method of writing a set of data to an integrated-circuit memory, the method comprising:

receiving a write request and a corresponding set of data;

dividing the set of data into first and second parallel data words;

activating a first sub-bank and a second sub-bank in sequence in response to the write request;

writing, in sequence, the first parallel data word to the first sub-bank and the second parallel data word to the second sub-bank.

15. The method of claim 14, further comprising precharging the first sub-bank and the second sub-bank.

16. The method of claim 14, wherein activating one of the first and second sub-banks includes activating a plurality of bit sense amplifiers and selecting a plurality of memory columns.

17. A memory system comprising:
    a. a request interface adapted to receive memory requests;
    b. bank-access control circuitry coupled to the request interface, the bank-access control circuitry including:
        i. a decoder coupled to the request interface and adapted to decode the memory requests;
        ii. activation logic coupled to the decoder and adapted to issue first and second activation commands via respective first and second activation ports;
    c. a first sub-bank including:
        i. a first plurality of memory cells;
        ii. a first plurality of data lines coupled to the memory cells; and
        iii. a first memory control port coupled to the first activation port;
        iv. wherein the first sub-bank activates the first plurality of memory cells in response to the first activation command; and
    d. a second sub-bank including:
        i. a second plurality of memory cells;
        ii. a second plurality of data lines coupled to the memory cells; and
        iii. a second memory control port coupled to the second activation port;
        iv. wherein the second sub-bank activates the second plurality of memory cells in response to the second activation command.

18. The memory system of claim 17, further comprising a serializer coupled to the first and second pluralities of data lines.

19. The memory system of claim 17, further comprising a deserializer coupled to the first and second pluralities of data lines.

20. A memory module comprising:

a plurality of logical memory banks, each logical memory bank divided into a corresponding plurality of sub-banks, including a first sub-bank having a first plurality of data lines and a second sub-bank having a second plurality of data lines;

a request interface adapted to receive operation requests directed to the logical memory banks; and

bank-access control logic coupled to the request interface and adapted to receive and decode the operation requests, the bank access control logic including a first control port coupled to a first sub-bank and a second control port coupled to the second sub-bank, the bank-access control logic issuing, in response to one of the operation requests, a first activate command to the first sub-bank on a first clock cycle and a second activate command to the second sub-bank on a second clock cycle.

21. The memory module of claim 20, wherein the activate command is part of a read transaction that sequentially produces first and second read data.

22. The memory module of claim 21, further comprising a serializer adapted to combine the first and second read data into a serial data stream.

23. A memory circuit comprising:

a plurality of logical memory banks, each logical memory bank divided into a corresponding plurality of sub-banks, including a first sub-bank and a second sub-bank;

means for sequentially activating, in response to a memory request directed to one of the logical memory banks, the first sub-bank and the second sub-bank; and

means for sequentially accessing, in response to the memory request, the first sub-bank and the second sub-bank.

24. The memory circuit of claim 23, wherein the memory request is a read request.

25. The memory circuit of claim 24, wherein the first sub-bank produces first data in response to the read request and the second sub-bank produces second data in response to the read request.

26. The memory circuit of claim 25, further comprising means for combining the first and

second data into a serial data stream.

27. The memory circuit of claim 23, wherein the memory request is a write request.

28. The memory circuit of claim 27, wherein the first sub-bank receives first data in response to the write request and the second sub-bank receives second data in response to the write request.

29. The memory circuit of claim 28, further comprising means for receiving the first and second data as serial input data and separating the first and second data prior to receipt of the first and second data by the respective first and second sub-banks.

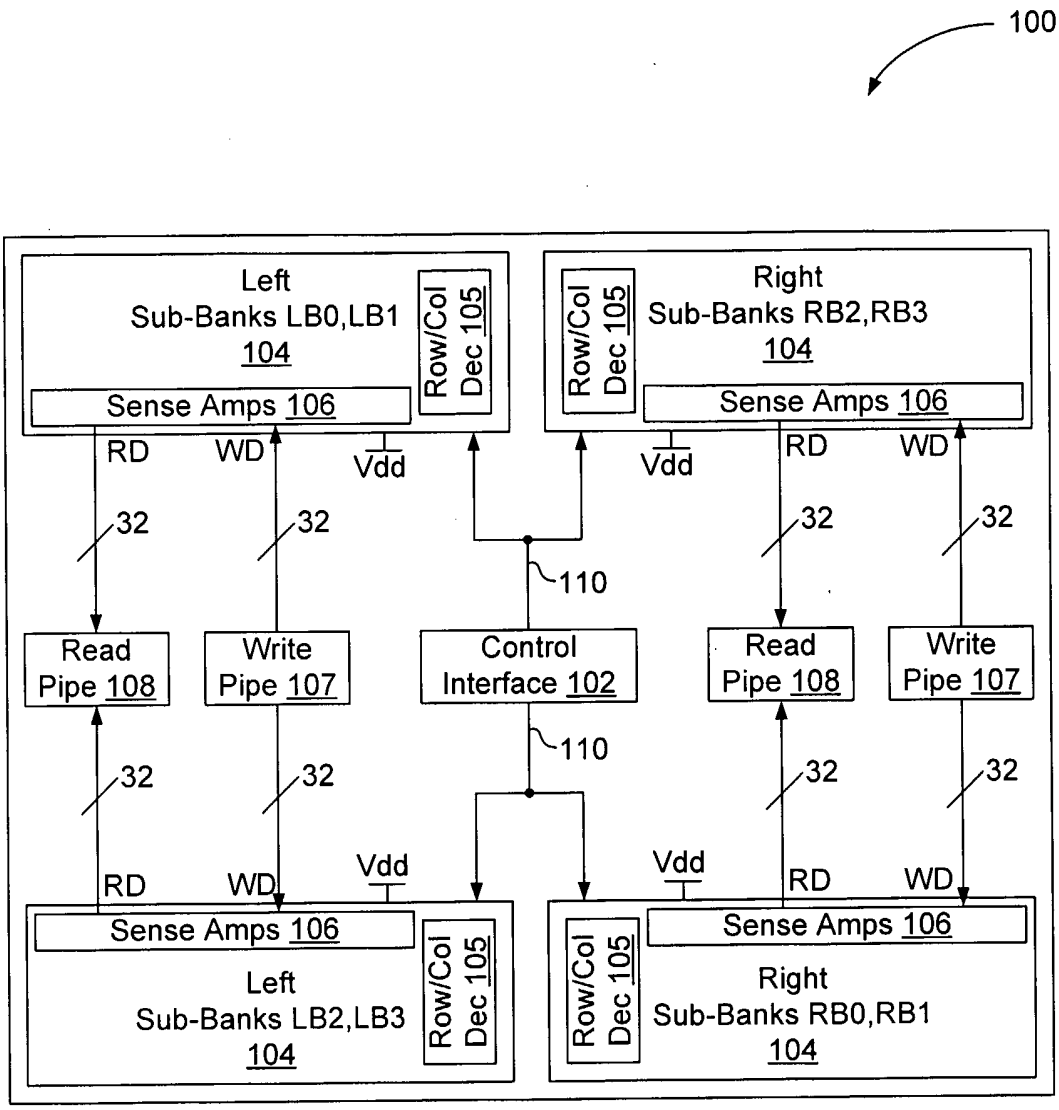


Fig. 1
(Prior Art)

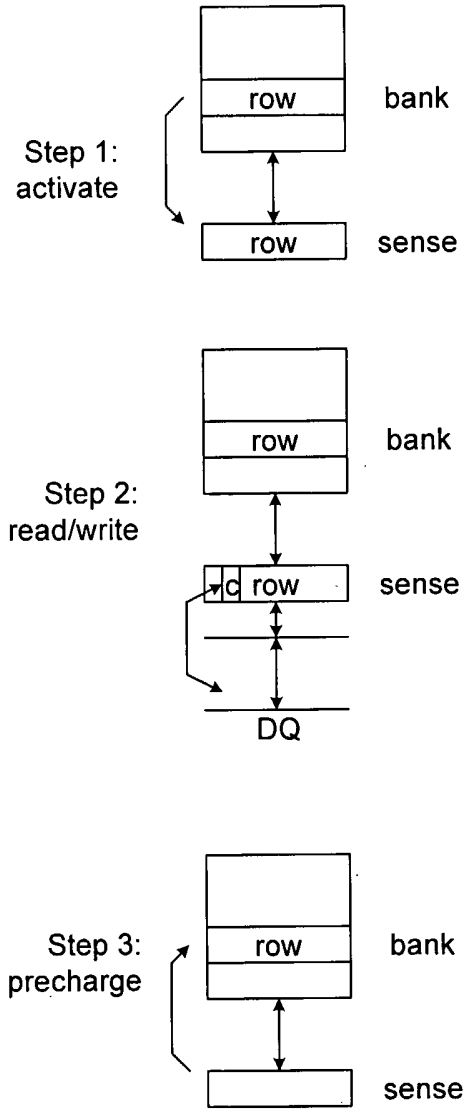


Fig. 2A (Prior Art)

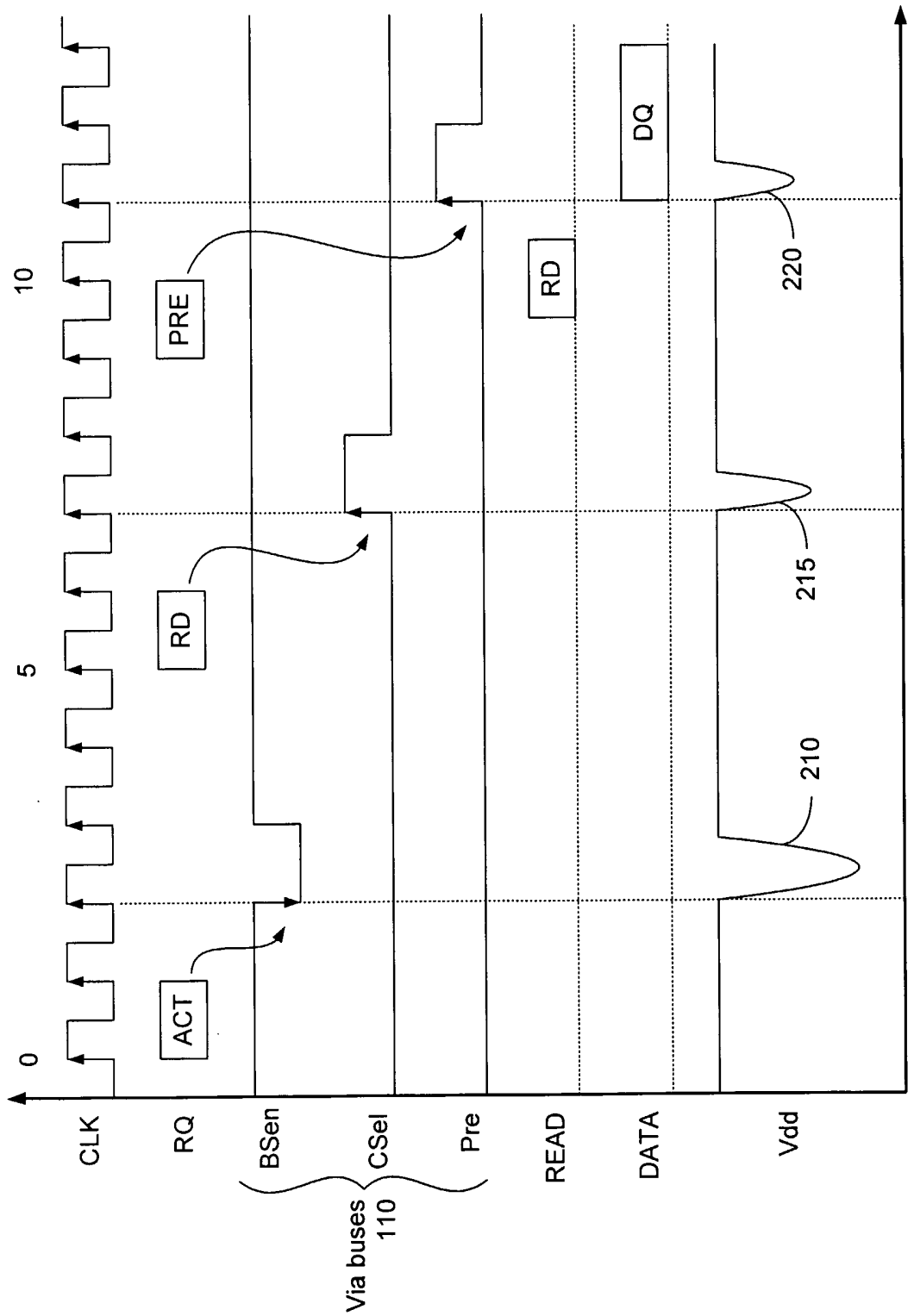
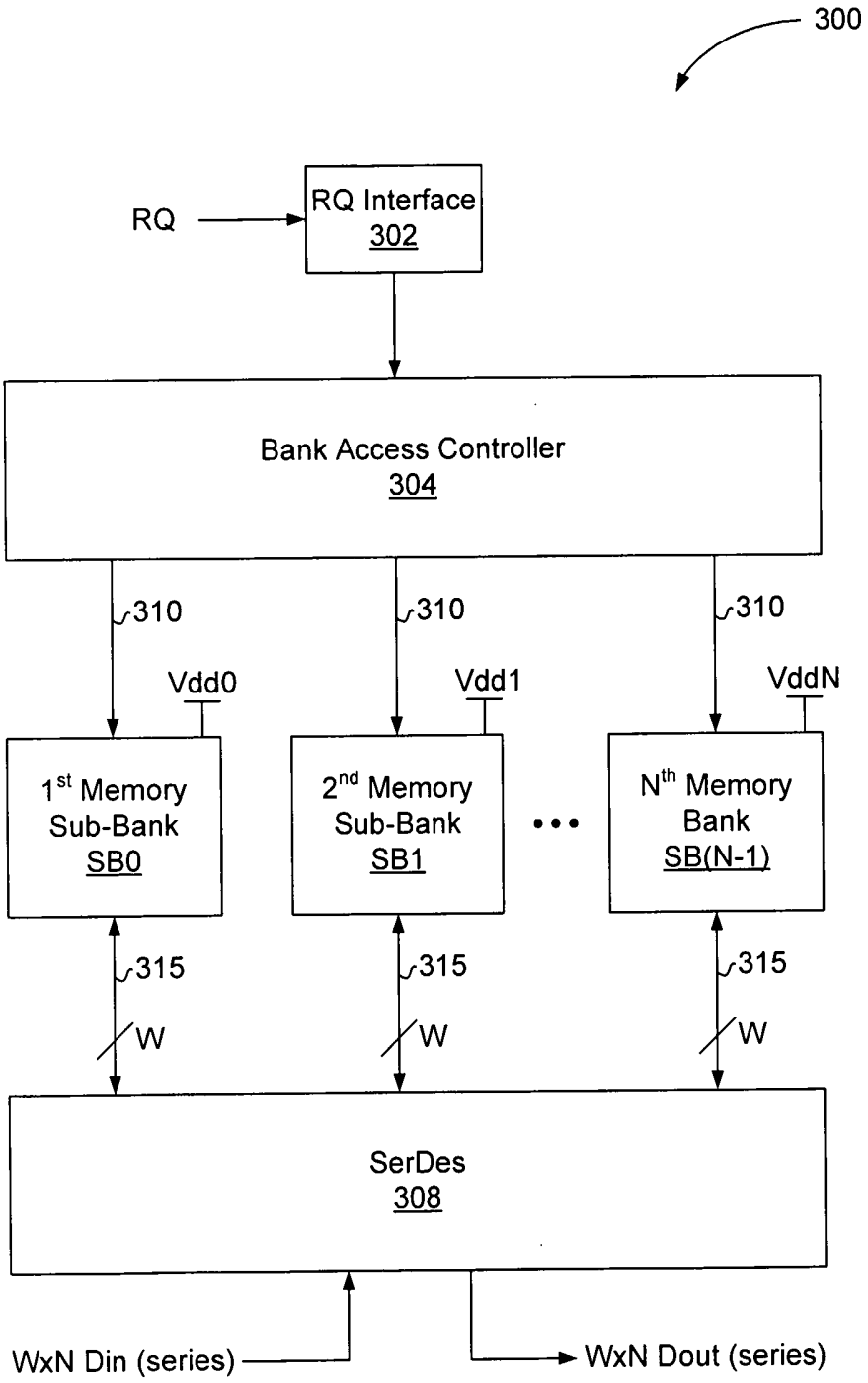


Fig. 2B (Prior Art)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RQ
RQ Interface
302
Bank Access Controller
304
310
310
310
Vdd0
Vdd1
VddN
1st Memory
Sub-Bank
SB0
2nd Memory
Sub-Bank
SB1
Nth Memory
Bank
SB(N-1)
315
315
315
W
W
W
SerDes
308
WxN Din (series)
WxN Dout (series)

Fig. 3

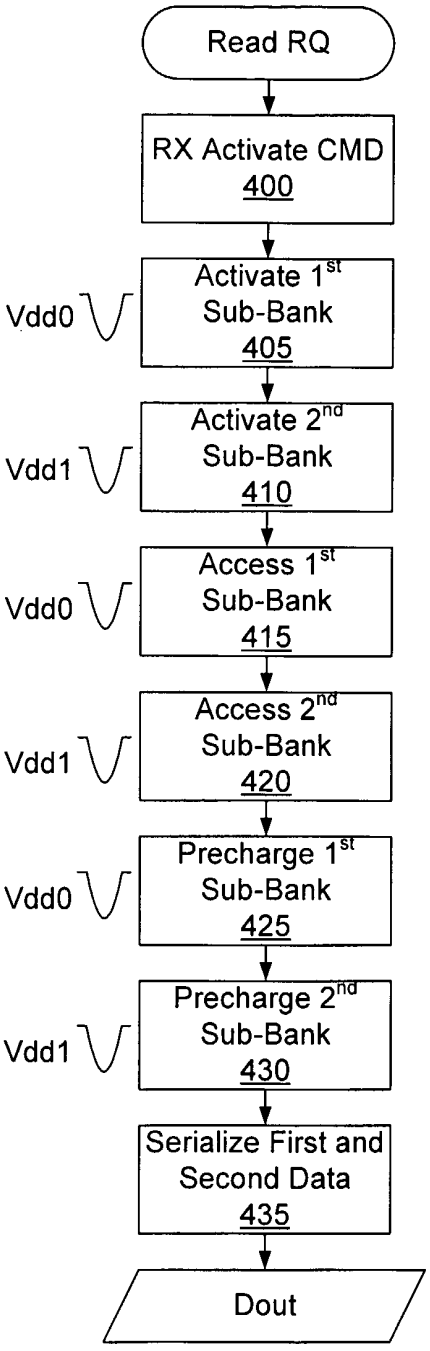

Read RQ
RX Activate CMD 400
Vdd0
Activate 1st Sub-Bank 405
Vdd1
Activate 2nd Sub-Bank 410
Vdd0
Access 1st Sub-Bank 415
Vdd1
Access 2nd Sub-Bank 420
Vdd0
Precharge 1st Sub-Bank 425
Vdd1
Precharge 2nd Sub-Bank 430
Serialize First and Second Data 435
Dout

Fig. 4A

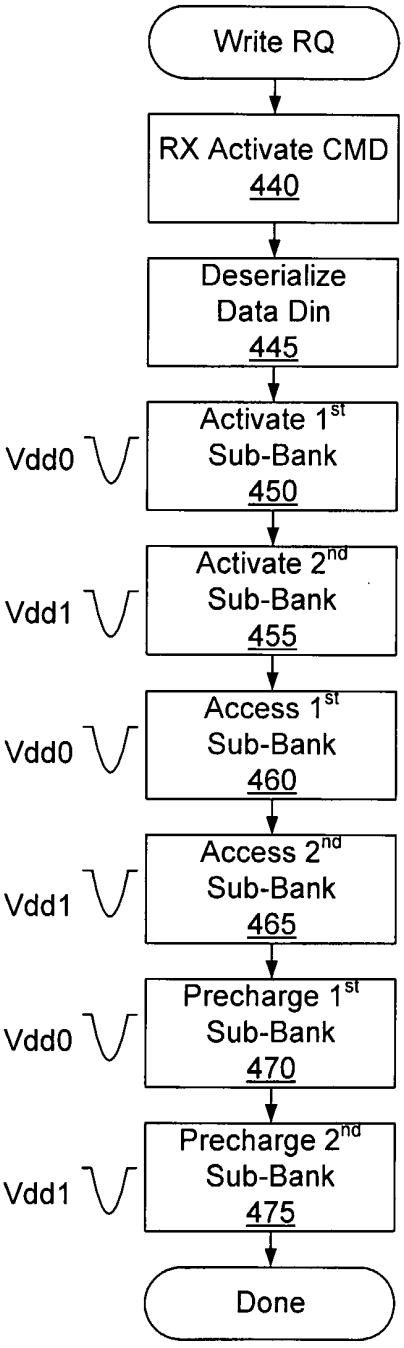
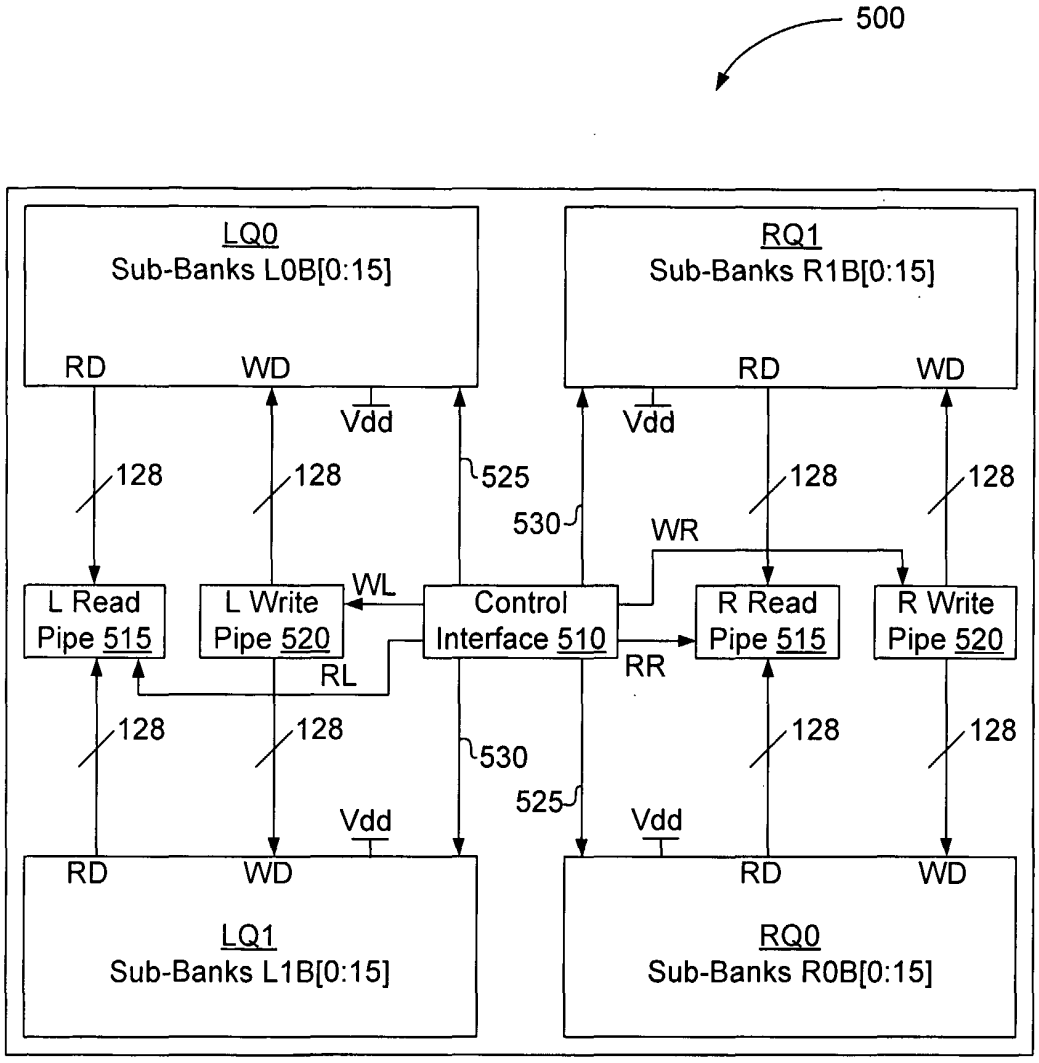

Write RQ
RX Activate CMD 440
Deserialize Data Din 445
Vdd0
Activate 1st Sub-Bank 450
Vdd1
Activate 2nd Sub-Bank 455
Vdd0
Access 1st Sub-Bank 460
Vdd1
Access 2nd Sub-Bank 465
Vdd0
Precharge 1st Sub-Bank 470
Vdd1
Precharge 2nd Sub-Bank 475
Done

Fig. 4B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RQ1
Sub-Banks R1B[0:15]
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530
WR
WL
L Read Pipe 515
L Write Pipe 520
Control Interface 510
R Read Pipe 515
R Write Pipe 520
RL
RR
LQ1
Sub-Banks L1B[0:15]
RQ0
Sub-Banks R0B[0:15]

Fig. 5

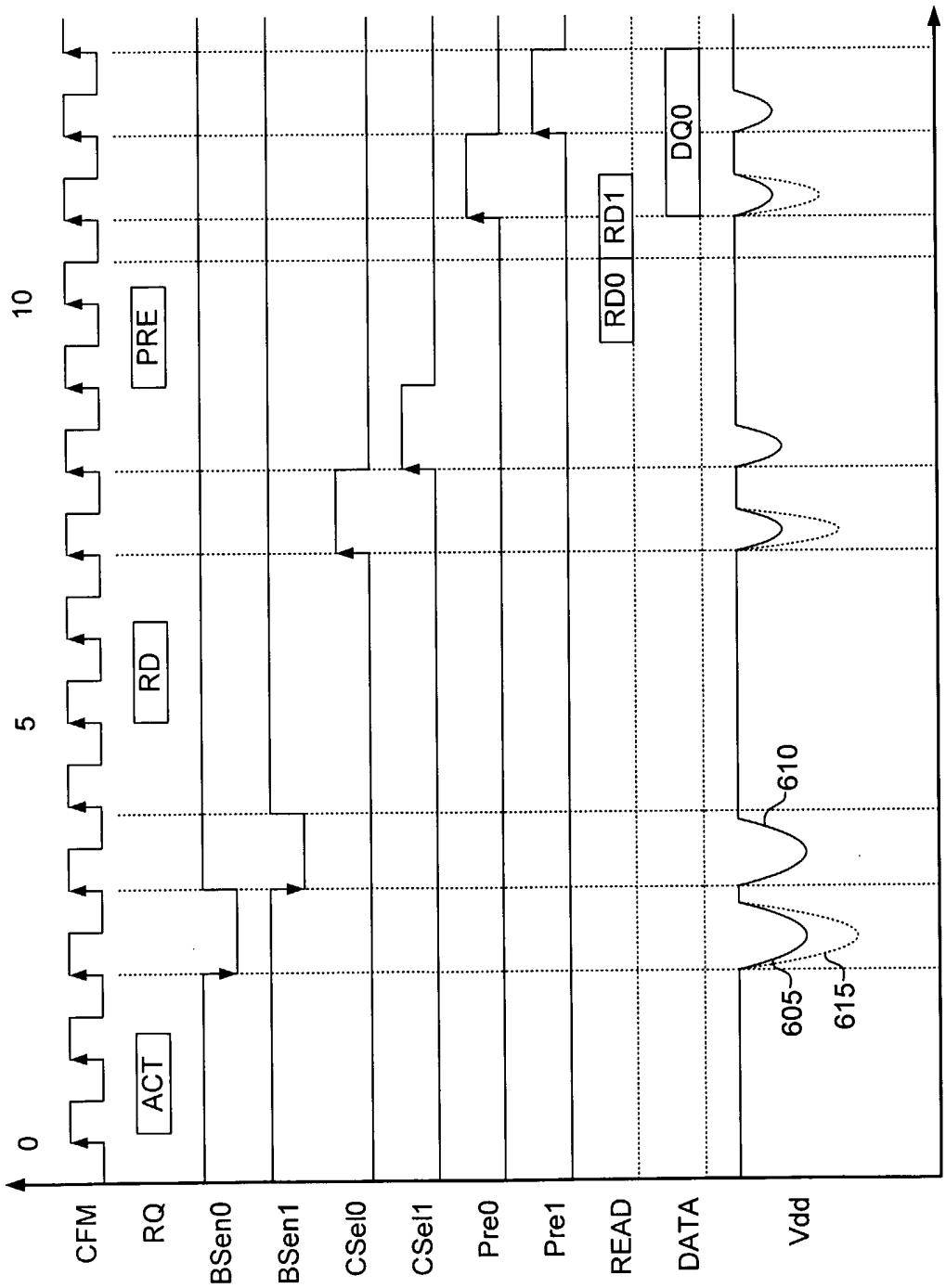
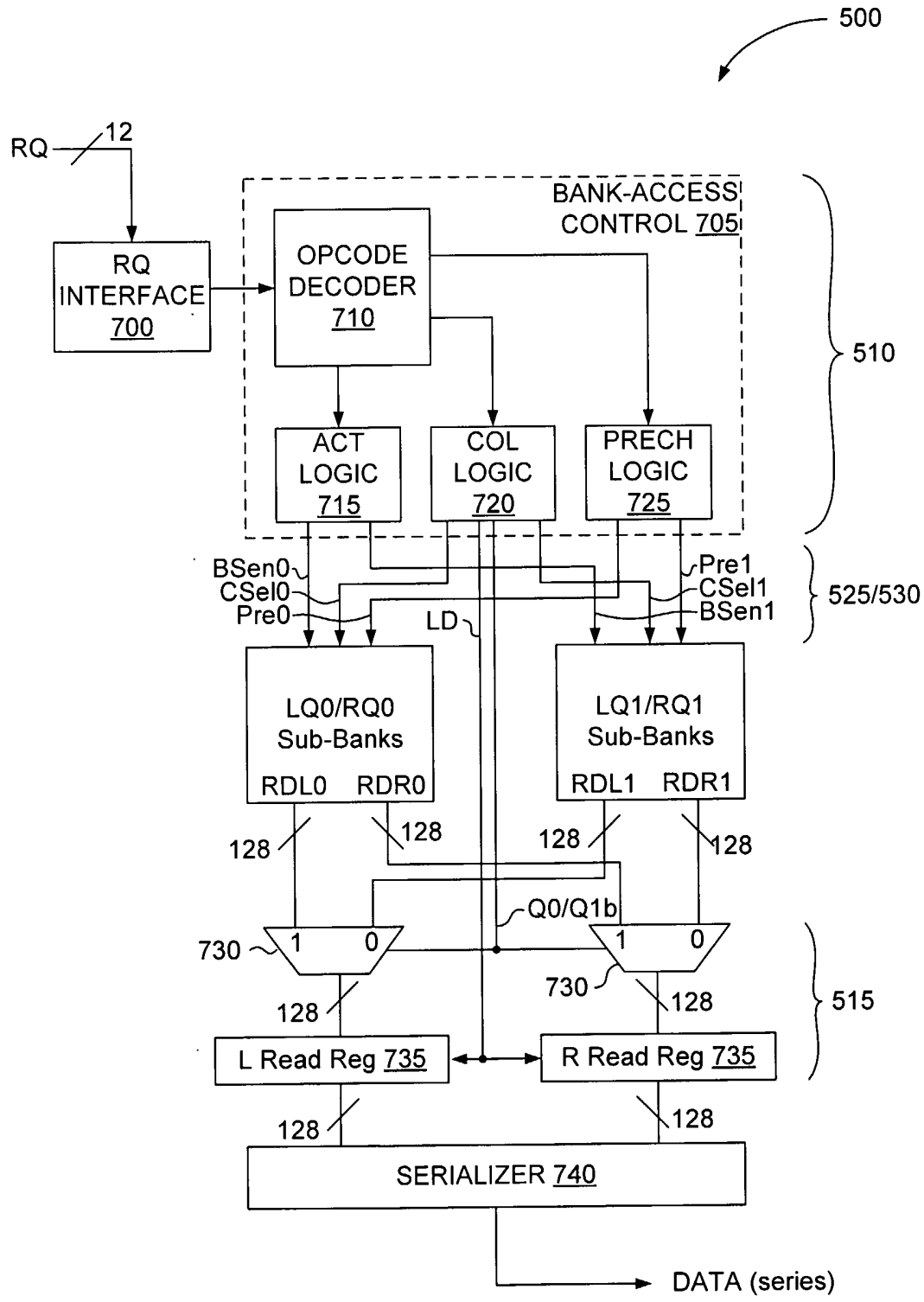

0
5
10
CFM
RQ
BSen0
BSen1
CSel0
CSel1
Pre0
Pre1
READ
DATA
Vdd
ACT
RD
PRE
RD0
RD1
DQ0
610
605
615
TIME

Fig. 6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RQ
12
RQ INTERFACE 700
BANK-ACCESS CONTROL 705
OPCODE DECODER 710
ACT LOGIC 715
COL LOGIC 720
PRECH LOGIC 725
510
BSen0
CSel0
Pre0
LD
Pre1
CSel1
BSen1
525/530
LQ0/RQ0 Sub-Banks
RDL0 RDR0
LQ1/RQ1 Sub-Banks
RDL1 RDR1
128
128
128
128
Q0/Q1b
730
1 0
730
1 0
128
128
515
L Read Reg 735
R Read Reg 735
128
128
SERIALIZER 740
DATA (series)

Fig. 7

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/028728

A. CLASSIFICATION OF SUBJECT MATTER
G11C7/10 G11C7/22 G11C8/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 222 047 A (MATSUDA ET AL) 22 June 1993 (1993-06-22) the whole document	1-29
A	EP 1 248 267 A (FUJITSU LIMITED) 9 October 2002 (2002-10-09) the whole document	1-29
A	US 2003/174573 A1 (SUZUKI HIDEAKI ET AL) 18 September 2003 (2003-09-18) the whole document	1-29
A	US 4 636 982 A (TAKEMAE ET AL) 13 January 1987 (1987-01-13) the whole document	1-29

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 December 2005	04/01/2006

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Czarik, D

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/028728

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