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(54) **Title:** SYSTEM FOR MAINTAINING EEPROM ENABLE DURING DE-ENERGIZED STATE
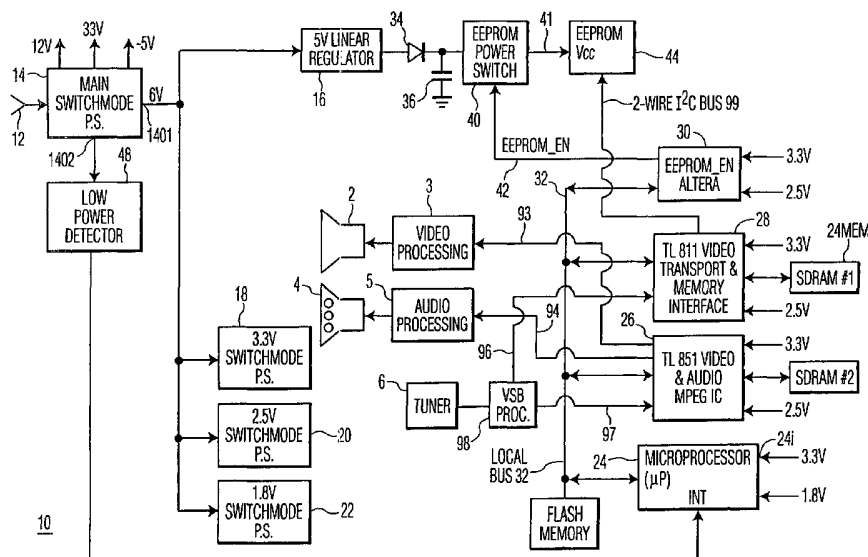
(57) **Abstract:** A system (10) including a processor (24) is energized from a source (18, 22) which is subject to power failure. To allow the state of the system (10) to be restored after the power failure, at least portions of the volatile data of the processor (24) are stored in non-volatile electrically erasable programmable read-only memory (Eeprom) (44). In order to effectuate the data transfer, storage capacitors (36) must provide power to the Eeprom and to the processor (24). In order to minimize the amount of storage capacitance, the processor power is maintained only until the data to be stored is transferred to the buffer (24MEM) of the Eeprom. Eeprom power is maintained until after a later time at which the buffer (24MEM) transfers the data to non-volatile storage of the Eeprom.

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SYSTEM FOR MAINTAINING EEPROM ENABLE DURING DE-ENERGIZED STATE

[0001] This application claims the priority of Provisional application serial number 60/376,443 filed April
5   29, 2002 and US Patent Application 10/339,421 filed January 9, 2003 in the name of William John Testin.

Field of the Invention

[0002] This invention relates to storage of data in
10   electronic systems, and more particularly to storage of data in systems subject to power outages.

Background of the Invention

[0003] Televisions do not typically remember the last
15   operating state of the set in the event of a power failure. Thus, the occurrence of a power failure may necessitate reprogramming of the set to restore it to the same state it had at the time of the power outage. One piece of data which may not be stored is the time of day, which is typically counted by
20   a clock. In order to save money, the clock does not have its own power source, and so the clock loses the current time upon power failure. There are other pieces of data which might be useful in restoring the state of a television receiver after a power failure, such as the ON or OFF state of the set, the
25   audio volume level and the channel.

[0004] In one prior-art scheme, an Eeprom was used to store data from a microprocessor of the receiver during a power failure. The video processor and Eeprom were powered until the transfer of the data to non-volatile storage occurred. As the
30   processing power of the video processors increases for providing high definition television, so does the cost of powering the various elements required to transfer data to non-volatile storage.

[0005] Improved data storage arrangements are
35   desired.

[0006] An Electrically Erasable Programmable Read-

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Only-Memory (Eeprom) may include a volatile input data buffer and a non-volatile data storage region. The time required for transfer of data into non-volatile portions of the Eeprom includes the sum of the time required to store the data in the
5   buffer, plus the time required to transfer the data from the buffer to the non-volatile storage region. According to an aspect of the invention, power is applied to the processor of the system upon the occurrence of a power failure for only so long as is required in order to sense the power failure and to
10 transfer the data to be stored from the processor to the buffer of the Eeprom. Power is provided to the relatively high-power processor for only the minimum time required for the data transfer, and the relatively low-power Eeprom can be maintained operative for an additional length of time to allow it to
15 complete the transfer of data from the buffer to the non-volatile storage portion of the Eeprom.

Summary of the Invention

[0007] A data storage arrangement of a video display
20 according to an aspect of the invention) comprises a volatile memory containing data used for controlling an operational parameter of the video display, during normal operation. A buffer memory has an input coupled to an output of the volatile memory. A non-volatile memory has an input coupled to an
25 output of the buffer memory. A detector detects a loss of power and initiates a first data transfer from the volatile memory to the buffer memory, when the loss of power is detected, and initiates a second data transfer from the buffer memory to the non-volatile memory, such that at least a portion
30 of the second data transfer occurs after the first data transfer has been completed. A first power supply energizes the volatile memory, during the first data transfer, such that, during the second data transfer portion, the volatile memory is in a de-energized state. A second power supply energizes the
35 non-volatile memory, during at least the second data transfer portion, such that, after the second data transfer has been

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completed, the non-volatile memory is in a de-energized state.
In a preferred embodiment according to an aspect of the
invention, the non-volatile memory comprises an electrically
erasable programmable read-only memory. According to another
5   aspect of the invention, the second power supply also energizes
the buffer memory, during said second data transfer portion,
such that, after the second data transfer has been completed,
the buffer memory is in a de-energized state.

10   Brief Description of the Drawing
         [0008] FIGURE 1a is a simplified block diagram of a
video or television apparatus according to an aspect of the
invention, and FIGURE 1b is a simplified block diagram of a
non-volatile storage element of FIGURE 1a;
15   FIGURE 2 is a simplified diagram in schematic form
illustrating details of a switch element of FIGURE 1a;
                 FIGURES 3 and 4 are simplified timing diagrams
illustrating the temporal relationships of the various steps,
waveforms, and voltages according to aspects of the invention.
20
                   Description of the Invention
         [0009] FIGURE 1a is a simplified block diagram of a
portion 10 of a video or television device according to an
aspect of the invention, in which a picture tube 2 receives and
25   displays signals from analog video processing illustrated as a
block 3, and a speaker 4 produces sound from analog signals
produced by an audio processor 5. A tuner 6 receives the
channel to be viewed. Also in FIGURE 1a, power is applied by
way of a port 12 to a block 14, which represents a main switch-
30   mode power supply. Supply 14 produces various direct output
voltages, including -5 volts, 12 volts, and 33 volts, for
powering various portions of the device. Supply 14 also
produces a 6-volt output at a port 14o1 and a sense voltage at
a port 14o2. The 6-volt output of the main switchmode power
35   supply 14 is applied from port 14o1 to a 5-volt linear
regulator 16, and to a 3.3-volt switch mode power supply 18, a

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2.5-volt switch mode power supply 20, and a 1.8-volt switch
mode power supply 22, for producing energizing voltages for
portions of the device.

[0010] Also in FIGURE 1a, a processor illustrated as
5 24 and using an instruction set receives 1.8 and 3.3 volt
energization from switch mode power supplies 18 and 22,
respectively, and, with the aid of an associated volatile
random-access SDRAM memory (RAM) 24Mem, accessible by way of a
local bus 32 and through a video transport and memory interface
10 integrated circuit 28, performs the main control processing for
the digital television device. Memory block 24Mem may be
considered to be the output buffer of the microprocessor 24
onto the local data bus 32. The microprocessor 24 commands
tuner 6 to receive a particular channel as determined by a
15 user. The received signals on the selected channel are applied
to a Vestigial Side Band (VSB) block 98, which couples high-
definition Advanced Television System Committee (ATSC) or 2H
signals by way of path 96 to integrated circuit 28, and
digitizes standard-definition (NTSC) signals for application by
20 way of a path 97 directly to an integrated circuit 26.
Integrated circuit 28 receives the processed information from
VSB block 98. Integrated circuit 26 processes the digitized 1H
standard-definition signals to produce audio, 2H video, and
control parameters. Also, integrated circuit (IC) 26 coacts
25 with integrated circuit 28 to process Moving Pictures [Image
Coding] Experts Group (MPEG) signals to produce audio, 2H
video, and control parameters. From whichever source, the
audio signals are applied from MPEG IC 26 to audio processor
block 5 by way of a path 94, and the video signals are applied
30 to video processor block 3 by way of a path 93. The audio
control parameters, such as audio volume, channel separation,
and the like, are coupled to audio processor 5. Integrated
circuit 26 receives 3.3 volts and 2.5 volts from switch mode
power supplies 18 and 20, respectively. Integrated circuit 28
35 receives 3.3 volts and 2.5 volts from switch mode power
supplies 18 and 20, respectively, and performs the video

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processing for the device. An ALTERA Field Programmable Gate
Array (FPGA) is illustrated as a block 30. This ALTERA FPGA
has part number EPIK30WC208-3, but other types or brands of
FPGA may be used. FPGA 30 receives energization at 3.3 volts

5   and 2.5 volts from switch mode power supplies 18 and 20,
respectively. FPGA 30 contains "glue" logic elements in the
form of gates for interconnecting the remainder of the logic by
way of signal paths which are not illustrated. Blocks 24, 26,
28, and 30 are connected to a local data bus designated 32.

10   [0011] The 5-volt energization produced by linear
regulator 16 of FIGURE 1a is applied by way of a rectifier or
diode illustrated as 34 to a storage capacitor 36. An Eeprom
power control switch illustrated as a block 40 is energized
with the voltage appearing across capacitor 36, which under

15   ordinary circumstances is maintained by the 5 volt energization
produced by linear regulator 16. Eeprom power control switch
40 is controlled by the state of an Eeprom_EN signal applied
from FPGA 30 by way of a path 42, and provides power by way of
a path 41 to enable an Eeprom 44. Eeprom 44 is coupled to bus

20   32 by way of I^2C bus 99 and integrated circuit 28, and so is
effectively coupled to the volatile memory 24Mem associated
with microprocessor 24. Consequently, Eeprom 44 is able to
receive the data to be stored in the event of a power loss.
             [0012] The Eeprom 44 in one embodiment of the

25   invention is a type M24C64-WMN6T fabricated by ST, but other
types may be used. FIGURE 1b illustrates some details of
Eeprom 44 of FIGURE 1a. In FIGURE 1b, Eeprom 44 receives
energizing power or potential from path 41, and applies the
energizing power in common to a buffer 50 and non-volatile

30   storage 52. Buffer 50 has a port 50_1 connected to two-wire I^2C
bus 99 for receiving data therefrom when commanded by processor
24 of FIGURE 1a, and for transferring the data from a second
port 50_2 to a port 52_1 of non-volatile memory or storage 52.
As mentioned, there is a time lag between the time at which

35   buffer 50 accepts or receives the data to be stored and the
later time at which the data stored in buffer 50 is fully

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transferred to non-volatile storage 52.

[0013] A power outage sensing arrangement illustrated as a block 48 in FIGURE 1a is connected to port 14o2 of main switch mode power supply 14, for producing a signal which

5   anticipates a total power outage. The voltage at output port 14o2 is taken to be 6 volts, as an example, under normal conditions. So long as the voltage of the 6-volt supply at port 14o2 of switch mode power supply 14 exceeds a given value, taken for example as being 5.5 volts, the power is deemed to be

10 ON, and power outage sensing arrangement 48 produces a first state of a control signal. However, when the voltage goes below the given value, detector 34 produces a signal, which is sent to an interrupt (INT) terminal of microprocessor 24, to begin the storage of data to be saved, preparatory for the

15 complete loss of power.

[0014] FIGURE 2 is a simplified schematic diagram of Eeprom power switch 40 of FIGURE 1a. In FIGURE 2, the emitter of a PNP transistor 210 is connected to the cathode of diode or rectifier 34 and to the hot terminal of storage capacitor 36.

20 When transistor 210 is conductive, a voltage near the capacitor voltage is applied across a voltage divider designated generally as 212, which includes the serial combination of resistors 214 and 216, and a tap 212t. The voltage at tap 212t is filtered by a capacitor 218. The value of resistor 214 is

25 selected to limit the inrush current of capacitor 218. The voltage across capacitor 218 is applied to the Vcc input port of Eeprom 44 (FIGURE 1a) for energization thereof. In the arrangement of FIGURE 2, transistor 210 is enabled only when an NPN transistor 220 is conductive. Transistor 220 has its

30 emitter grounded and its collector connected to capacitor 36 by way of a resistor 222. The voltage at the collector of transistor 220 is communicated to the base of transistor 210 by a resistor 224. The Eeprom_EN signal from FPGA 30 of FIGURE 1a is applied by way of path 42 of FIGURE 2 and a resistor 226 to

35 the base of transistor 220. A pull-up resistor 228 pulls the base of transistor 220 positive during those intervals when a

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high or "tristate" impedance is applied to path 42. The
tristate condition occurs when the power source to FPGA 30
drops below a given value, such as one volt. Thus, transistor
220, and consequently transistor 210, is rendered conductive
5   when a positive voltage (a logic "1" or logic "high") is
applied over path 42, or when path 42 is tristate. Transistor
220, and consequently transistor 210, is nonconductive when a
logic "0" or logic "low" is applied by way of path 42 from FPGA
30 of FIGURE 1a.

10   [0015] When switch 40 of FIGURE 2 is open, which is
when a logic low level is applied to path 42, energizing
voltage to Eeprom 44 is cut off, and Eeprom 44 is cleared.
During those intervals in which Eeprom power switch 40 is
conductive, power flows from capacitor 36 and/or linear
15   regulator 16 of FIGURE 1a, and the Eeprom is energized for
accepting commands and for storing data.

             [0016] "FIGURE 3" is a term applied to FIGURES 3a,
3b, 3c, 3d, 3e, 3f, 3g, and 3h, taken as a whole. The
waveforms of FIGURE 3 are those occurring at initial turn-on or
20   boot-up of the device. In FIGURE 3, t0 represents the turn-on
time. At turn-on time t0, the 6-volt supply voltage rises to 6
volts as indicated by FIGURE 3a, the 5-volt linear regulator
output rises to 5 volts as indicated by FIGURE 3b, and the 3.3,
2.5, and 1.8-volt supply voltages rise, as indicated by FIGURES
25   3c, 3d, and 3e, respectively. In FIGURE 3, times t1 and t2
represent the times between which FPGA 30 of FIGURE 1a produce
a logic low level on signal path 42, as suggested by FIGURE 3f,
to turn OFF transistors 210 and 220, to thereby disable the 5-
volt supply to Eeprom 44, which allows resistor 216 to
30   discharge capacitor 218 to thereby remove energization voltage
from Eeprom 44, to thereby clear its input register or buffer.
The energization Vcc of the Eeprom 44 is illustrated in FIGURE
3h, and can be seen to drop to zero in the time just before
time t2. In effect, the logic low level initiated at time t1
35   disables Eeprom enable switch 40 of FIGURE 1a, and as a result
the voltage at the power input pin of the Eeprom 44 ramps

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toward zero voltage, as illustrated between times t1 and t2 in
FIGURE 3h. The processor comes out of the reset (inoperative)
state shortly after the initial turn-on of the device at time
t0, as suggested by FIGURE 3g. The reset of the microprocessor
5   is performed in order to set all the logic gates to known
conditions, and to allow any internal clock time in which to
stabilize. The reset state is the logic low or logic 0 level
of FIGURE 3g, and the logic high or logic 1 state is designated
by reset bar represents the operational state of the
10   microprocessor. After time t2 of FIGURE 3, the device is in
its normal operating state, and the various voltages and
signals remain in the states illustrated to the right of time
t2 until a power loss is detected.
        [0017] The term "FIGURE 4" is used to refer jointly
15   to FIGURES 4a, 4b, 4c, 4d,4e, 4f, 4g, 4h, and 4i. The
waveforms, states and voltages of FIGURE 4 are those which are
relevant in the context of a power failure beginning at a time
designated as t6. Plot 410 of FIGURE 4a represents the voltage
produced at the 6 volt output 14o1 of main switch mode power
20   supply 14 of FIGURE 1a. As illustrated by plot 410 of FIGURE
4a, the 6-volt supply begins to drop at time t6, representing
the time at which a power failure occurs. The 5-volt supply 16
of FIGURE 1a has a one-volt inherent offset between its 6-volt
input and its 5-volt output. At a time illustrated as t8 in
25   FIGURE 4, the 5-volt supply voltage represented by plot 418 of
FIGURE 4e begins to decrease in magnitude or "drop", because
the 5-volt supply 16 of FIGURE 1a is fed from the 6-volt
source, which began dropping at time t6. After time t8, the 5-
volt supply decreases in correspondence with the 6-volt supply.
30   Shortly thereafter, at a time illustrated as t10 in FIGURE 4,
the Eeprom supply voltage, which is represented by plot 422 of
FIGURE 4g, begins to drop, because its 5-volt source is
decreasing in magnitude. Thus, the Eeprom 44 of FIGURE 1a is
powered by the 5-volt supply 16 until time t10, and is
35   thereafter powered by the voltage remaining on capacitors 36
and 218. The source of power to the Eeprom is illustrated by

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the state diagram 426 of FIGURE 4i, which shows a low level, representing powering by the 5-volt supply, until time t10, and thereafter shows powering from C36/218 until a time t26. The decreasing voltage of the six-volt supply 14 of FIGURE 1a

5   crosses the 5.5-volt trigger level of low power detector 48 of FIGURE 1a at a time illustrated in FIGURE 4 as t12. Beginning at time t12 of FIGURE 4, low power detector 48 of FIGURE 1a produces an interrupt command, illustrated as 412 of FIGURE 4b, which is applied to processor 24 of FIGURE 1a to initiate data

10   transfer to non-volatile storage. Beginning at time t14 of FIGURE 4, processor 24 of FIGURE 1a responds to the interrupt command by transmitting over bus 32, integrated circuit 28, and path 99 to Eeprom 44 of FIGURE 1b both storage commands and data to be stored, as suggested by the microprocessor (:P) data

15   transfer state 414 of FIGURE 4c in the interval t14-t16. The data transferred during the time interval illustrated as 414 of FIGURE 4c puts data into the buffer 50 of Eeprom 44 of FIGURE 1b. The data transfer to buffer is completed at a time illustrated as t16 in FIGURE 4. At some slightly later time

20   illustrated as time t18 in FIGURE 4, Eeprom 44 of FIGURE 1b internally initiates the transfer of data from the buffer to nonvolatile memory upon reception of the standard "stop bit" of the I^2C bus 99 (not illustrated). The internal data transfer interval from buffer 50 to nonvolatile storage 52 in the Eeprom

25   44 of FIGURE 1b is suggested by the time period designated as 424 of FIGURE 4h, which extends from time t18 to time t20.

         [0018] At a time illustrated as time t19 in FIGURE 4, the voltage of the 6-volt supply drops to a level, illustrated as around 5 volts in FIGURE 4a, such that :P 24 is reset, as

30   suggested by state 416 of FIGURE 4d, and :P 24 becomes inoperative. The switching regulators 18, 20, and 22 of FIGURE 1a also derive their power from the six-volt supply, so their voltage also begins to drop after the six-volt supply begins its drop, as suggested by waveform 420 of FIGURE 4f; this time

35   is not critical to the invention and is not designated.
         [0019] Power for the Eeprom 44 of FIGURE 1a is

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derived from the 5-volt supply 16 prior to time t10 of FIGURE
4. Since there is a diode 34 of FIGURE 1a in series with
supply 16, the 5 volts available to Eeprom 44 during this time
is reduced by the forward offset voltage of the diode to around
5   4.2 volts, as indicated by plot 422 of FIGURE 4g. After time
t10 of FIGURE 4, the 5-volt supply voltage represented by 418
of FIGURE 4e has dropped low enough so that the Vcc energizing
voltage available to Eeprom 44 of FIGURE 2 is provided by
capacitors C36 and C218. The voltage available to Eeprom 44 of
10 FIGURE 1 from capacitors C36 and C218 of FIGURE 2 continues,
albeit at decreasing voltage, from time t10 until a later time
t26, as suggested by voltage plot 422 of FIGURE 4g. The Eeprom
44 of FIGURE 1a is rated to operate at some minimum supply
voltage, illustrated as being 2.8 volts in FIGURE 4g. Thus,
15 Eeprom 44 of FIGURE 1a is enabled or energized by capacitors
C36/218 of FIGURE 1b and FIGURE 2 for the interval t10 through
t24 of FIGURE 4, and can therefore perform all of its
functions, including transfer of data from the buffer 50 of
FIGURE 1b to non-volatile storage 52, even after :P 24 of
20 FIGURE 1a has ceased to function at time t19. The period
during which the Eeprom buffer 50 of FIGURE 1b writes to non-
volatile storage 52 is illustrated as extending from time t18
to a time which may be selected within the range of ranging
from t20 to t22, as suggested by 424 in FIGURE 4h. As may be
25 deduced, there is a guard time between the latest time for
transfer of data from buffer to nonvolatile storage, which is
time t22, and the time at which the buffer supply voltage
decreases below its rated operating value, which is illustrated
as t24 in FIGURE 4. In addition to this guard time, there may
30 be in most manufactured units an additional guard time,
attributable to the potential for operating at least some of
the buffers at values of energizing voltage lower than their
minimum rated values. The time allowable for transfer of data
from buffer 50 of FIGURE 1b to non-volatile store 52 is decided
35 during the design of the device 10. The nominal capacitance of
capacitor 36 in relation to the current drain of the worst

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(highest current drain) Eeprom (as well as other parameters) is
selected so that the lowest-capacitance capacitor will maintain
the Eeprom energized until after the time at which data
transfer from buffer to non-volatile storage is accomplished.
5   Since the distribution of component variation and tolerance
will in the average apparatus be much greater than the minimum
allowable value, there will ordinarily be some time after
transfer of data from buffer to non-volatile memory is
completed during which the Eeprom continues to be energized
10   sufficiently to operate. Thus, the continued energization time
during which Eeprom 44 of FIGURE 1 continues to be energized
after the 5-volt regulator 16 fails to produce useful output
lies between times t8 and a time later than time t24 of FIGURE
4, as suggested by the energization state 426 of FIGURE 4i.
15   [0020] In one embodiment of the invention, the
interval t10-t24 is a minimum of 10 milliseconds (msec).
Between the time t19 at which the processor resets and a time
later than time t22, Eeprom 44 can perform transfers of data
stored in buffer to non-volatile memory.
20   [0021] Thus, the relatively high-power processor 24
need not be powered for any longer a time than is required to
transfer the data to be stored to an input buffer associated
with the Eeprom 44, and the processor 24 can be allowed to
become de-energized at a time before the Eeprom 44 has
25   completed transfer of the data from volatile buffer to non-
volatile storage. This advantageously reduces the cost of
energy storage which would be required if the processor 24 were
kept in operation until the Eeprom 44 was finished with its
operation. Only the relatively low-power Eeprom 44 is powered
30   until the time at which the data is stored in non-volatile
memory. Thus, the data is available from the non-volatile
memory of Eeprom 44 at the next power-up following the power
failure. The initial clearing of the buffer by Eeprom_En at
power-up does not affect the non-volatile portions of the
35   Eeprom, which remain available.

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WHAT IS CLAIMED IS

1.   A data storage arrangement of a video display, comprising:

a volatile memory containing data used for
5   controlling an operational parameter of said video display, during normal operation;

a buffer memory having an input coupled to an output of said volatile memory;

a non-volatile memory having an input coupled to an
10 output of said buffer memory;

a detector for detecting a loss of power and for initiating a first data transfer from said volatile memory to said buffer memory, when said loss of power is detected, and a second data transfer from said buffer memory to said non-
15 volatile memory, such that at least a portion of said second data transfer occurs after said first data transfer has been completed;

a first power supply for energizing said volatile memory, during said first data transfer, such that, during said
20 second data transfer portion, said volatile memory is in a de-energized state; and

a second power supply for energizing said non-volatile memory, during at least said second data transfer portion, such that, after said second data transfer has been
25 completed, said non-volatile memory is in a de-energized state.

2.   A data storage arrangement according to claim 1, wherein said non-volatile memory comprises an electrically erasable programmable read-only memory.

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3.   A data storage arrangement according to claim 1, wherein said second power supply also energizes said buffer memory, during said second data transfer portion, such that,
35 after said second data transfer has been completed, said buffer memory is in a de-energized state.

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4.   A data storage arrangement according to claim 1, wherein a supply voltage energizes, in common, said buffer and non-volatile memories.

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5.   A data storage arrangement, comprising:

a source of volatile data, said source of volatile data requiring power application to prevent loss of said volatile data;

10   an Eeprom including a data input buffer and a non-volatile data storage portion, said input buffer of said Eeprom being coupled to said source of volatile data, said Eeprom also requiring power application to prevent loss of data in said input buffer; and

15   a source of energization coupled to energization inputs of said source of volatile data and said Eeprom, for normally energizing said source of volatile data and said Eeprom, and for, in a power-loss condition, powering said Eeprom for a period of time including the sum of the time

20   during which data is transferred from said source of volatile data to said buffer of said Eeprom plus the time during which said data is transferred from said buffer to said non-volatile data storage, and for, in said power-loss condition, powering said source of volatile data for said period of time during

25   which data is transferred from said source of volatile data to said buffer of said Eeprom but not until the end of said time during which said data is transferred from said buffer to said non-volatile storage.

30   6.   A data storage arrangement according to claim 5, wherein said source of energization comprises:

a source of power which is subject to said power loss;

a first regulator coupled to said source of power and

35   to said energization input of said source of volatile data for providing energization thereto;

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a second regulator coupled to said source of power
for generating a second energization voltage, said second
regulator further including energy storage for tending to
maintain said second energization voltage; and

5   controllable switch means coupled to said second
regulator and to said Eeprom, for selectively (a) momentarily
withholding said second energization voltage from said Eeprom
during boot-up to clear said buffer, (b) coupling said second
energization voltage to said Eeprom during normal operation,

10   and (c) coupling said energy storage of said second regulator
to said Eeprom during a time interval following detection of
said power loss.

7.   An electronic system which is subject to power

15   failures, said system comprising:

a processor including at least a power input port,
and also including at least data output ports coupled to a bus,
the data at said data output ports being subject to loss when
power to said power input port fails, said processor also

20   including an input port for accepting a low-voltage signal and
for initiating storage of data in response thereto;

a first power source (6v) subject to temporary
failure;

a second power source (3.3v, 1.8v) derived from said

25   first power source for powering said processor;

sensing means coupled to said first power source and
to said processor, for producing and coupling to said processor
a voltage-low signal indicating that the voltage of said first
power source is below a particular value;

30   a third power source (5v) derived from said first
power source;

an eeprom coupled to said bus, said eeprom including
a power input port, said eeprom being for storing data applied
over said bus under the control of commands applied over said

35   bus;

a storage capacitor;

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a nonlinear impedance coupled to said storage
capacitor and to said third power source, for coupling voltage
to said capacitor during those intervals in which the voltage
of said capacitor is lower than the voltage of said third power
5   source, and for isolating said storage capacitor from said
third power supply during those intervals in which said
capacitor has a higher voltage than said third power source;
controllable switch means coupled to said storage
capacitor and to said power input port of said eeprom, for, in
10   response to a first state of a command signal, coupling power
from said storage capacitor to said power input port of said
eeprom, and for, in response to a second state of said command
signal, isolating said storage capacitor from said power input
port of said eeprom;
15   said second power source including sufficient energy
storage to be capable of operating said processor for a
selected period of time following generation of said voltage-
low signal sufficient for said processor to initiate data
storage and to couple the data to be stored to said eeprom; and
20   the magnitude of said storage capacitor being
selected to provide energizing voltage to said eeprom for a
second period of time, greater than said selected period of
time, sufficient for said eeprom to accept said data to be
stored and to couple said data to be stored to non-volatile
25   memory.

8.   An electronic system according to claim 7,
wherein said controllable switch means comprises:
a transistor arrangement including a controlled
30   current path having one end coupled to said storage capacitor
and a second end coupled to said power input port of said
eeprom, and also including a control electrode which controls
the current flow in said controlled current path in response to
enable and disable signals;
35   means for generating an enable signal, said means for
generating an enable signal being coupled to said control

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electrode, for operating in the absence of said enable signal and said disable signal, whereby said eeprom is enabled at all times, except in the presence of said disable signal.

5   9.   A method for operating a system subject to power outage, said method comprising the steps of:
      providing stored energy to a processor and to an Eeprom;
      beginning transfer of data to be stored from said
10   processor to a buffer of said Eeprom when a power failure is sensed;
      after said beginning transfer of data, transferring said data from said buffer to non-volatile storage of said Eeprom;
15   maintaining said stored energy to said Eeprom until a time at which said data is transferred from said buffer to said non-volatile storage; and
      maintaining said stored energization of said processor until a time after said beginning of transfer of data
20   to said Eeprom, but not so long as said time at which said data is transferred from said buffer to said non-volatile storage.
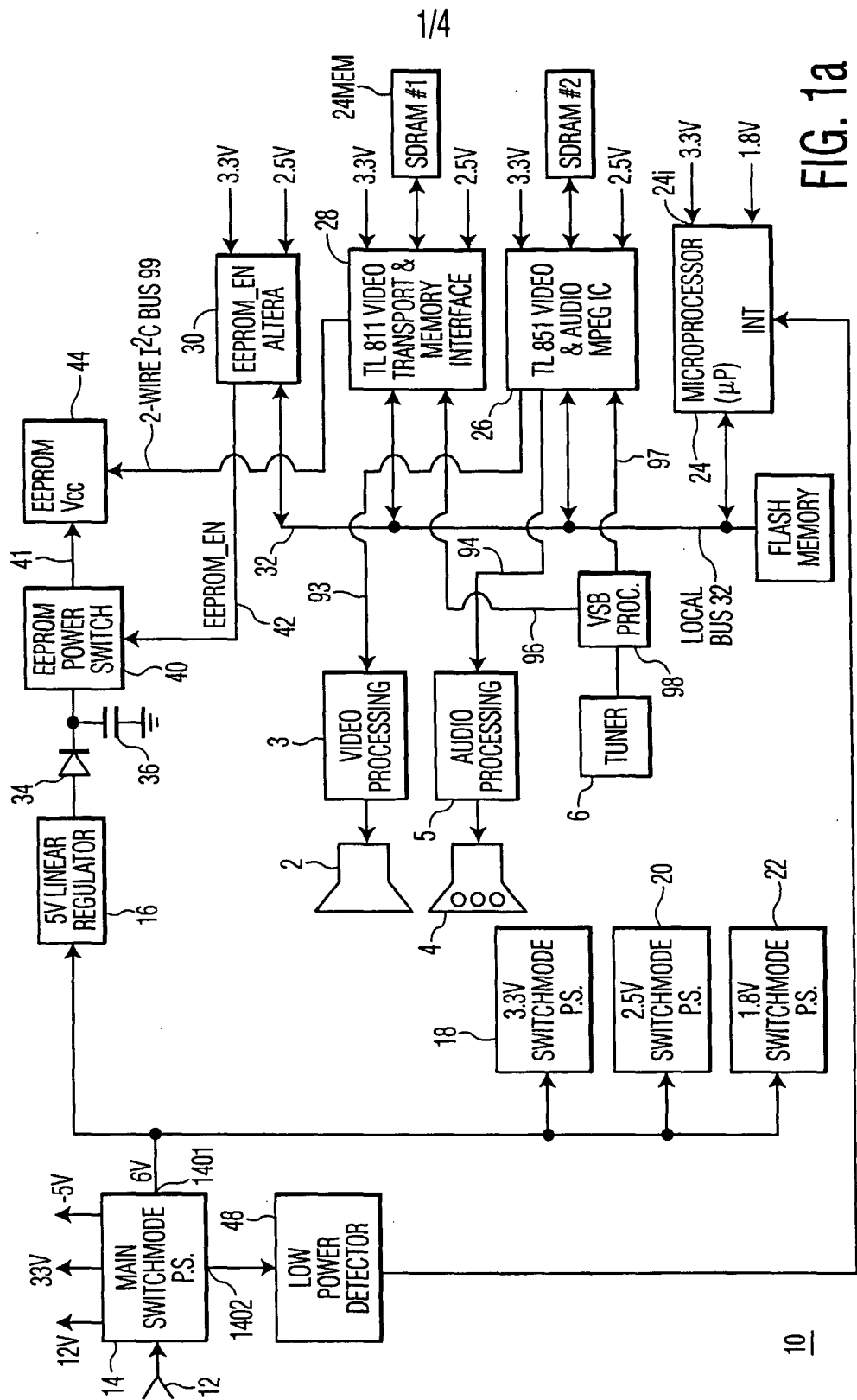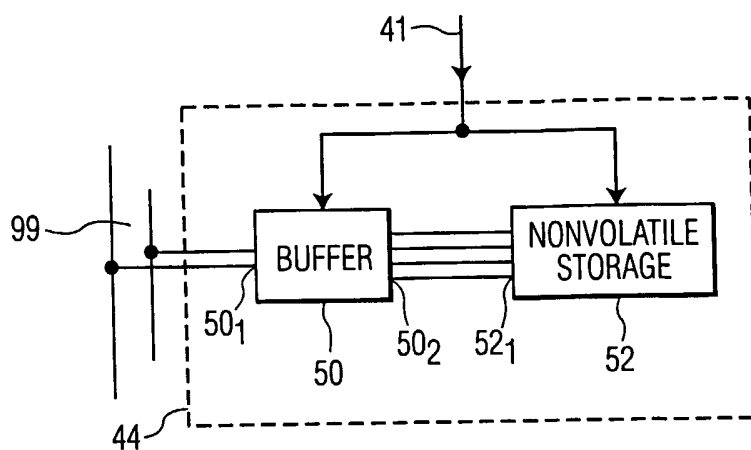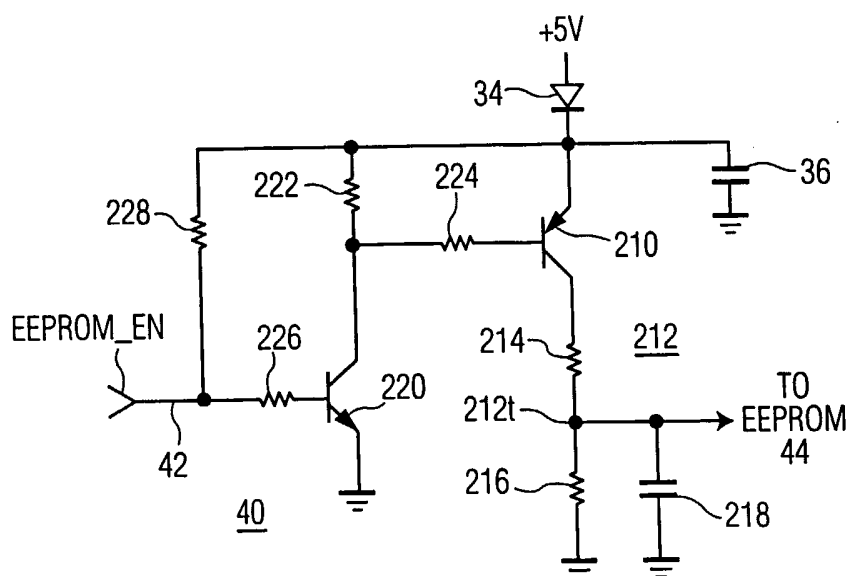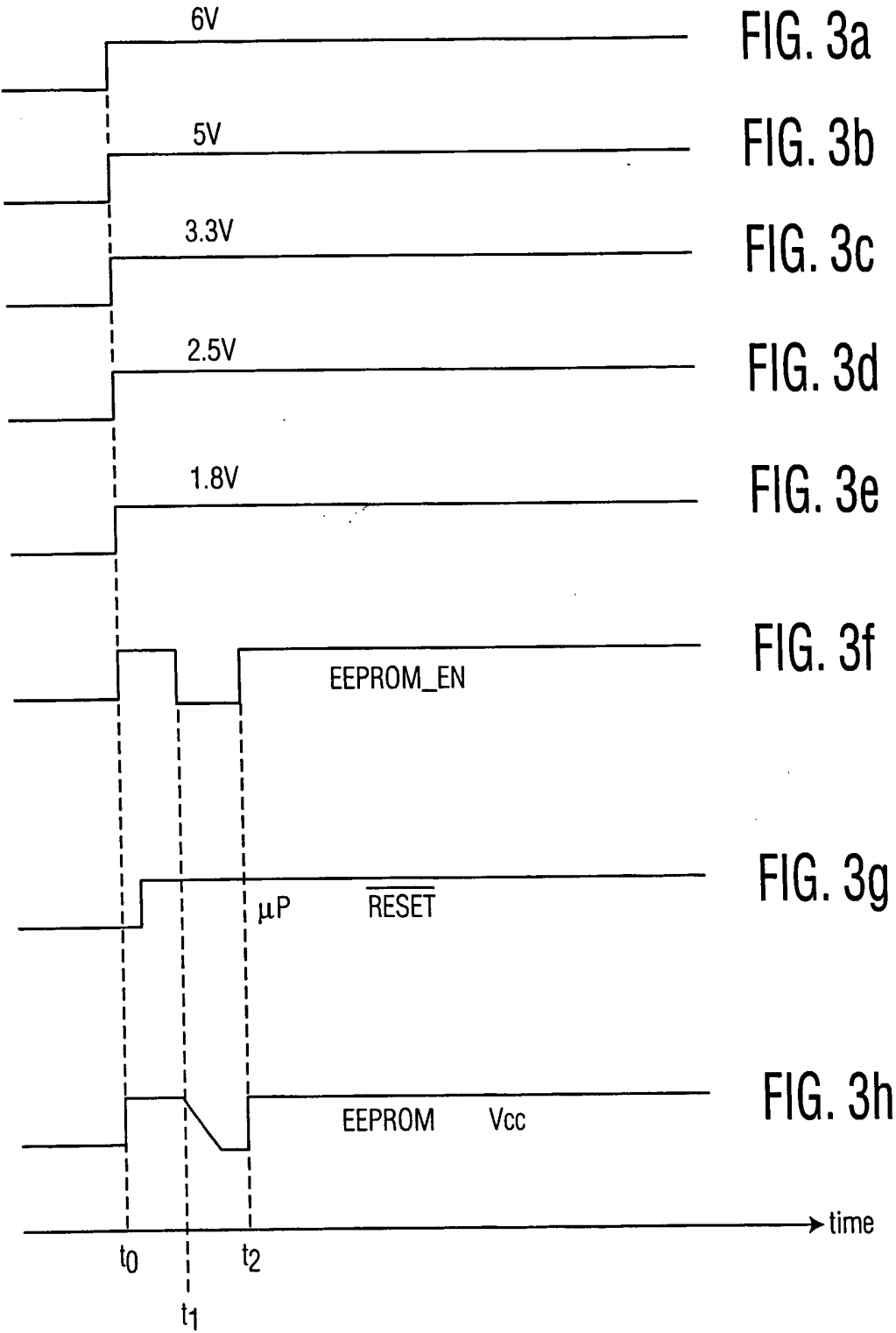
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FIG. 1a

FIG. 1b

FIG. 2

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FIG. 3a

FIG. 3b

FIG. 3c

FIG. 3d

FIG. 3e

FIG. 3f

FIG. 3g

FIG. 3h

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FIG. 4a

FIG. 4b

FIG. 4c

FIG. 4d

FIG. 4e

FIG. 4f

FIG. 4g

FIG. 4h

FIG. 4i
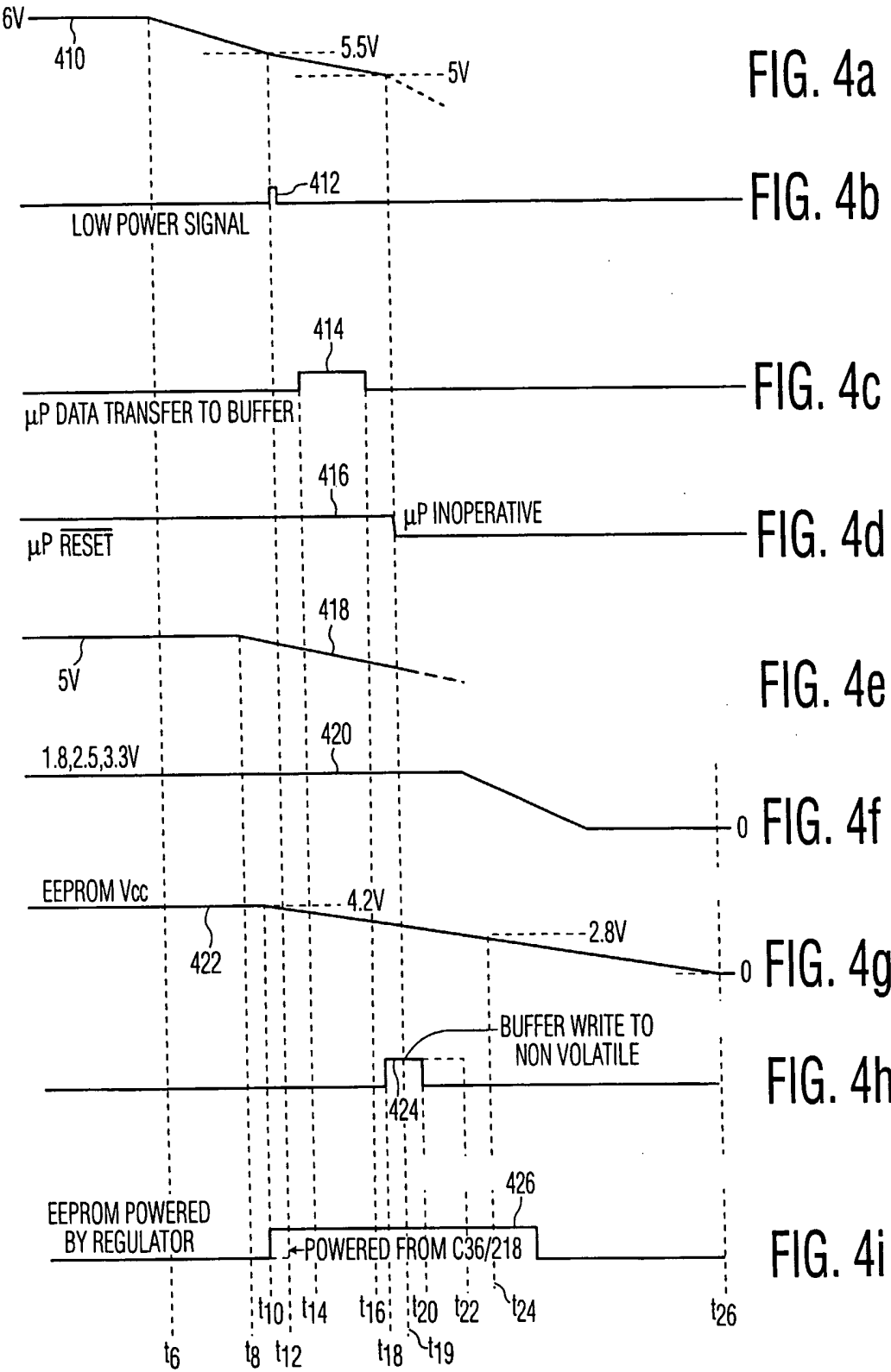
INTERNATIONAL SEARCH REPORT

A.	CLASSIFICATION OF SUBJECT MATTER

IPC(7)   :G06F 12/06; G11C 13/00
US CL   : 711/167, 100, 1, 154; 365/226, 227, 228, 229, 230.01, 230.08
According to International Patent Classification (IPC) or to both national classification and IPC

B.	FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. :   711/167, 100, 1, 154; 365/226, 227, 228, 229, 230.01, 230.08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
GOOGLE ONLINE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

IEEE ONLINE

C.	DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,151,541 A (IIZUKA) 21 November 2000, col. 2, lines 1-25; col. 4, lines 39-56.	9
A	US 5,586,334 A (MIYAZAKI et al) 17 December 1996, abstract, col. 3, lines 22-49.	1-9
A	US 5,519,663 A (HARPER, Jr. et al) 21 May 1996, abstract, col. 6, lines 29-50.	1-9
A	EP 0 518 622 A1 (ENOKI et al) 16 December 1992, abstract, fig. 2, col. 1, line 46 to col. 2, line 34.	1-9

☐ Further documents are listed in the continuation of Box C.   ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 JUNE 2003	**11 JUL 2003**

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