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I.E.E.E. JOURNAL OF SOLID-STATE CIRCUITS
vol. 24, no. 1, February 1989, pages 181-183,
New York, NY, US; K. NAGARAJ:
"Large-Swing CMOS Buffer Amplifier"

58 References cited :
IEEE JOURNAL OF SOLID-STATE CIRCUITS
vol. SC-20, no. 6, December 1985, pages
1200-1205; J.A. FISHER: "A High-Performance
CMOS Power Amplifier"

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Description

Amplifier circuitry having relatively low output impedance is necessary for driving large capacitive or resistive loads, such as the relatively low impedance of a telephone line, typically an impedance of about 600 ohms or less. In prior art, such amplifier circuitry typically is composed of a low impedance unity-gain buffer output stage fed by one or more voltage-gain stages. This amplifier circuitry typically is integrated in a semiconductor chip; whereas the load is situated off-chip.

For example, as shown in the textbook by P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits (John Wiley & Sons, second edition, 1984) at page 759, Figure 12.43, a buffer stage for class B (push-pull) operation can be formed by a pair of error operational amplifiers (error op-amps) which are connected to receive feedback from a pair of serially connected output transistors in such a manner as to assure unity voltage gain. The operation is class AB (push-pull) in cases where in the quiescent (no signal) state both output transistors conduct current, but one of them does not conduct any current whenever the input voltage goes outside a narrow range, typically the range of about ± 0.5 volt around ground potential. As known in the art, class AB operation in general is desirable from the standpoints of low standby power consumption and of no missing output signals for small input signals (no "dead zone") which would distort the output. However, the circuit design of the aforementioned buffer stage is undesirably sensitive to semiconductor processing variations, so that either excessive power dissipation or circuit instability (oscillations) caused by poor feedback control over the quiescent current, or both, may result. Too high a quiescent current is wasteful of power, whereas too low a quiescent current can result in the above-mentioned circuit instability.

GB 2180710 discloses a CMOS output stage comprising complementary push-pull connected MOS transistors each fed by a respective differential amplifier whose negative input is fed by the input signal and whose positive input is fed by the output signal appearing at the node between the MOS transistors. Such an arrangement suffers from the disadvantage that the output quiescent current level is greatly affected by offsets in the differential amplifiers.

According to this invention there is provided amplifier circuitry as claimed in claim 1.

The buffer stage can be operated class AB and advantageously be fed by a high voltage gain stage of amplifier circuitry. Also, a pair of serially connected third and fourth transistors, having much higher channel width-to-length ratios than the first and second transistors, can be connected in parallel with the first and second transistors, in order to make the output voltage swing more nearly approximate the rail-to-rail

power supply voltage. Furthermore, for full rail-to-rail output capability, a separate switching transistor is inserted between the first and second rails, respectively, and the first and second transistors; and each such switching transistor has its control terminal respectively connected to the first and second nodes.

The invention will now be described with reference to the accompanying drawing which is a circuit schematic including a buffer stage in amplifier circuitry.

Detailed Description

The FIGURE shows a low impedance buffer stage 20 embodying the invention. Advantageously this buffer stage 20 is supplied with voltages V1 and V2 by a high voltage gain stage 10. The circuitry of both the stages 10 and 20 can be integrated into a single silicon semiconductor chip, as known in the art and as further discussed below.

In the FIGURE, power lines ("rails") V_{DD} and V_{SS} are set at typically +5 volt dc and -5 volt dc, respectively, as known in the art. A fixed electrical current source of current I_S is connected serially with a resistor R_S and an n-channel MOS transistor M7 between the power rails, in order to form the high gain stage 10. During operation, this high gain stage 10 receives an input voltage V_{IN} at its input terminal 11 and delivers voltages V1 and V2 to the buffer stage 20.

Each of a pair of standard op-amps A1 and A2 (each of which can be formed by a simple differential pair of transistors) is connected in the stage 20, and each of these op-amps has its respective negative input terminal connected to receive the voltages V1 and V2. Serially connected from rail to rail are n-channel MOS transistors M5 and M1, a resistor R1, a resistor R2, and p-channel transistors M2 and M6. A node between the resistors R1 and R2 develops an output voltage V_{OUT} at an output terminal 21 of the stage 20. Optionally, for reasons discussed below, another n-channel MOS transistor M3 and another p-channel MOS transistor M4 are added to the buffer stage 20 in parallel with the branch formed by the serially connected M5, M1, R1, R2, M2 and M6. The transistors M3 and M4 are serially connected from rail to rail. A node between these transistors M3 and M4 is connected to the output terminal 21.

Advantageously, the parameters of the transistors M3 and M4 are selected so as to equalize their transconductances. The channel width to length ratio (W/L) of each of M3 and M4 advantageously is at least about five times as large as that of M1 and M2, respectively. Likewise, advantageously the transistors M1 and M2 are formed with equal transconductances. The resistors R1 and R2 advantageously are a matched pair ($R1=R2$). The requirements of matched pairs for R1 and R2, as well as for equal transconductances of M1 and M2, M3 and M4, need not be satisfied, at

some penalty of signal distortion. Indeed, one of the resistances R1 and R2 could be zero (short circuit).

The purpose of M5 and M6 is to enable full rail-to-rail output voltage swing at the output terminal 21, for such full rail-to-rail operation tends to be prevented by the voltage drop(s) across R1 and R2. For example, because of the voltage drop across R2, the output voltage V_{OUT} cannot attain V_{DD} regardless of how high V_2 rises, so long as current can flow through R2. In the presence of M6, however, when V_2 rises and causes the potential at the node N2 to rise to a threshold below V_{DD} , the transistor M6 turns off, whereby the voltage drop across R2 vanishes and hence the transistor M4 can then bring the output voltage V_{OUT} fully to V_{DD} . If, on the other hand, such full rail-to-rail output is not required, then the transistors M5 and M6 can be omitted, with the source terminals of M1 and M2, respectively, being connected directly to V_{SS} and V_{DD} .

Each of the op-amps A1 and A2, respectively, has its output terminal coupled (connected) to a low current carrying control terminal (gate terminal) of the pair M1, M3 and the pair M2, M4.

In practice, the op-amps A1 and A2 are biased (not shown) so that there is an adequate safety margin of non-zero quiescent current in a neighborhood of the quiescent state (no signal region), in order to avoid the signal distortion problem otherwise caused by a "dead zone" in which a change in the input signal would not produce any change in the output.

The buffer stage 20 operates as follows. Because the op-amp A1 and A2, being operational amplifiers, cannot support any significant differences in the voltages applied to their positive vs. negative input terminals, the feedback to their positive input terminals supplied by node N1 located between R1 and M1 (to A1) and by node N2 located between R2 and M2 (to A2) makes the quiescent current i_Q well-defined and controlled, i.e., adjustable to the desired value by proper selection of parameters. More specifically, assuming that the source-drain voltage drop across M5 and M6 are both much less than a threshold of n-channel and p-channel transistors, the quiescent current i_Q is given by:

$$i_Q = I_S R_S (1 + a)/(R1 + R2) \quad (1)$$

where the R's are the resistances of the respective designated resistors, and where a is equal to the ratio of the width-to-length ratio $(W/L)_3$ of M3 to that $(W/L)_1$ of M1, and equally of M4 to M2 (assuming matched pairs of transistors):

$$a = (W/L)_3/(W/L)_1 = (W/L)_4/(W/L)_2 \quad (2)$$

Note that from eq. (1) it follows the quiescent current i_Q is thus well-controllable and insensitive to semiconductor processing variations: the resistances of the resistors track one another, as do the W/L ratios. Although the current I_S supplied by the current source varies with semiconductor processing conditions, it does so in a well-defined non-critical way, so that the

quiescent current is relatively stable with respect to variation in semiconductor processing conditions: the feedback in the operational amplifiers does not introduce any significant circuit instability.

By selecting $R1=R2=R$, then, in the quiescent state:

$$V_{OUT} = (V_1 + V_2)/2; \quad (3)$$

i.e., the output voltage of the buffer stage 20 then is conveniently equal to the common mode voltage of the inputs V_1 and V_2 to this buffer stage.

As noted above, the transistors M3 and M4, as well as M6 and M5, can be omitted, but then during class AB operation (push-pull) the output voltage V_{OUT} could not swing as closely from V_{DD} to V_{SS} as it can when these transistors are present. Note that the larger the value of a , as given by eq. (2), the closer the output voltage swing becomes equal to rail to rail.

In order to assure stable operation with sufficient quiescent current, and hence to assure class AB operation, I_S and R_S should be selected to be large enough to make $I_S R_S$ greater than the sum of the maximum expected absolute values of the operational amplifier offset voltages of A1 and A2 by a factor of about 5 to about 10 or more, lest chip-to-chip variations of the offset in A1 or A2 or both should cause undesirably large chip-to-chip variations in the quiescent current i_Q .

The resistors R_1 , R_2 , R_S can be formed, for example, by standard diffused regions in semiconductor or by standard deposited polysilicon resistors. The current source I_S can be formed by an MOS transistor biased in its saturation region, as known in the art.

Note that in the presence of signal applied to the gate terminal of M7, the voltage drop (V_2-V_1) across R_S remains fixed ($I_S R_S$). That is, the difference mode $(V_2-V_1)/2$ is fixed; whereas the common mode $(V_2 + V_1)/2$ varies with signal.

In a typical case, only by way of illustration, approximate values for the various parameters are:

$R1 = R2 = 2000$ ohm; $R_S = 1000$ ohm; $I_S = 50$ microamp;

$$a = 30.$$

With signal, the output current at the output terminal 21 can go as high as 10 milliamp.

The gate terminal of M7, to which V_{IN} is applied, can be connected, for example, to the output terminal of a differential gain stage (not shown); and the output terminal 21 of the stage 20 can then be connected, for the purpose of feedback, to the negative input terminal of the differential gain stage. In that way, overall unity gain of V_{OUT} relative to the input voltage applied to a positive input terminal of the differential gain stage can be achieved, in combination with overall high input impedance and low output impedance, as is desired in amplifier circuitry for driving large currents into large loads (line drivers).

Although the invention has been described in detail in terms of a specific embodiment, various modi-

fications can be made within the scope of the claims.

For example, instead of n-channel and p-channel MOS transistors, npn and pnp bipolar transistors can be used.

Claims

1. Amplifier circuitry comprising a buffer stage (20) which comprises first and second amplifiers (A1,A2) each having an output terminal and a first and a second input terminal, first and second connection means (R1,R2), first and second transistor devices (M1,M2) respectively having first and second relatively high current carrying controlled paths and respectively having first and second relatively low current carrying control terminals, first and second power rails (V_{SS} , V_{DD}), the first high current path of the first transistor device (M1), the first connection means (R1), the second connection means (R2), and the second high current path of the second transistor device (M2) being serially connected, in the order stated, in a path between the first power rail and the second power rail, means for connecting the output terminal of the first amplifier to the control terminal of the first transistor device (M1), and means for connecting the output terminal of the second amplifier to the control terminal of the second transistor device (M2), CHARACTERIZED IN THAT the first and second amplifiers (A1,A2) are operational amplifiers, at least one of the first and second connection means comprises resistance means (R1,R2), there is provided means for connecting a first node (N1) located between the first transistor device (M1) and the first connection means (R1) to the second input terminal of the first amplifier, and means for connecting a second node (N2) located between the second transistor device (M2) and the second connection means (R2) to the second input terminal of the second amplifier (A2), and there is provided a voltage gain stage (10) comprising current source means (I_s) for supplying a constant current, further resistance means (R_s) having first and second terminals (V1, V2), a third transistor device (M7) having a control terminal that is connected to a circuitry input terminal (11) for receiving an input signal voltage, the third transistor device having a third relatively high current path suitable for carrying the constant current, means for connecting, from the first rail to the second rail, serially, in the order stated, the current source means, the further resistance means, and the third relatively high current path, and means for connecting the first and second terminals of the further resistance means to the first input terminal of the first and second operational amplifiers,

respectively.

2. Circuitry as claimed in claim 1, wherein each of said first and second connection means comprises resistance means (R1, R2), and there is provided means for connecting a node located between the first and second connection means to an output terminal (21) of the buffer stage.
3. Circuitry as claimed in claim 1 or 2 comprising fourth and fifth transistor devices (M3, M4) having respectively third and fourth relatively low current carrying control terminals that are coupled respectively to the first and second control terminals of the first and second transistor devices, respectively, the fourth and fifth transistor devices having respectively fourth and fifth relatively high current paths that are connected serially from the first power rail to the second power rail.
4. Circuitry as claimed in claim 3 wherein the channel width to length ratio of the fourth transistor device and of the fifth transistor device is at least five times greater than that of the first transistor device and of the second transistor device, respectively.
5. Circuitry as claimed in claim 3 or 4 comprising sixth and seventh transistor devices (M5,M6) whose high current paths are respectively connected in series with that of the first and second transistor devices, and whose control terminals are respectively connected to the first and second nodes (N1,N2).
6. Circuitry as claimed in any preceding claim wherein the constant current multiplied by the resistance of the further resistance means is at least about 5 times the input offset voltage of the first and second amplifiers.
7. A semiconductor integrated circuit comprising circuitry as claimed in any preceding claim.

Patentansprüche

1. Verstärkerschaltung mit einer Pufferstufe (20), die erste und zweite, je einen Ausgangsanschluß sowie einen ersten und zweiten Eingangsanschluß aufweisenden Verstärkern (A1, A2), einer ersten und zweiten Verbindungseinrichtung (R1, R2), einem ersten und zweiten Transistorbauteil (M1, M2), die je einen ersten und einen zweiten, verhältnismäßig hohe Ströme führende Steuerwege und je einen ersten und einen zweiten, verhältnismäßig niedrige Ströme führende Steueranschlüsse aufweisen,

- einer ersten und zweiten Stromversorgungsschiene (V_{SS} , V_{DD}), wobei der erste Hochstromweg des ersten Transistorbauteil (M1), die erste Verbindungseinrichtung (R1), die zweite Verbindungseinrichtung (R2) und der zweite Hochstromweg des zweiten Transistorbauteil (M2) in der angegebenen Reihenfolge auf einem Weg zwischen der ersten und der zweiten Stromversorgungsschiene in Reihe geschaltet sind, einer Einrichtung zur Verbindung des Ausgangsanschlusses des ersten Verstärkers mit dem Steueranschluß des ersten Transistorbauteils (M1) und einer Einrichtung zur Verbindung des Ausgangsanschlusses des zweiten Verstärkers mit dem Steueranschluß des zweiten Transistorbauteils (M2), dadurch gekennzeichnet, daß der erste und der zweite Verstärker (A1, A2) Operationsverstärker sind, daß wenigstens eine der ersten und der zweiten Verbindungseinrichtungen eine Widerstandseinrichtung (R1, R2) umfaßt, und daß vorgesehen sind:
- eine Einrichtung zur Verbindung eines ersten Knotens (N1), der sich zwischen dem ersten Transistorbauteil (M1) und der ersten Verbindungseinrichtung (R1) befindet, mit dem zweiten Eingangsanschluß des ersten Verstärkers,
- eine Einrichtung zur Verbindung eines zweiten Knotens (N2), der sich zwischen dem zweiten Transistorbauteil (M2) und der zweiten Verbindungseinrichtung (R2) befindet, mit dem zweiten Eingangsanschluß des zweiten Verstärkers (A2),
- eine Spannungsverstärkerstufe (10) mit einer Stromquelleneinrichtung (I_S) zur Lieferung eines Konstantstroms, einer weiteren Widerstandseinrichtung (R_S), die einen ersten und einen zweiten Anschluß (V_1 , V_2) aufweist, einem dritten Transistorbauteil (M7) mit einem Steueranschluß, der mit einem Schaltungseingangsanschluß (11) zur Aufnahme einer Eingangssignalspannung verbunden ist, wobei das dritte Transistorbauteil einen dritten Weg für einen verhältnismäßig hohen Stroms aufweist, der zur Führung des Konstantstroms geeignet ist,
- eine Einrichtung zur Reihenschaltung der Stromquelleneinrichtung, der weiteren Widerstandseinrichtung und des dritten Weges für einen verhältnismäßig hohen Strom in der angegebenen Reihenfolge von der ersten zur zweiten Stromversorgungsschiene, und
- eine Einrichtung zur Verbindung des ersten und zweiten Anschlusses der weiteren Widerstandseinrichtung mit dem ersten Eingang des ersten und zweiten Operationsverstärkers.
- Schaltung nach Anspruch 1, bei der die erste und die zweite Verbindungseinrichtung je eine Wider-

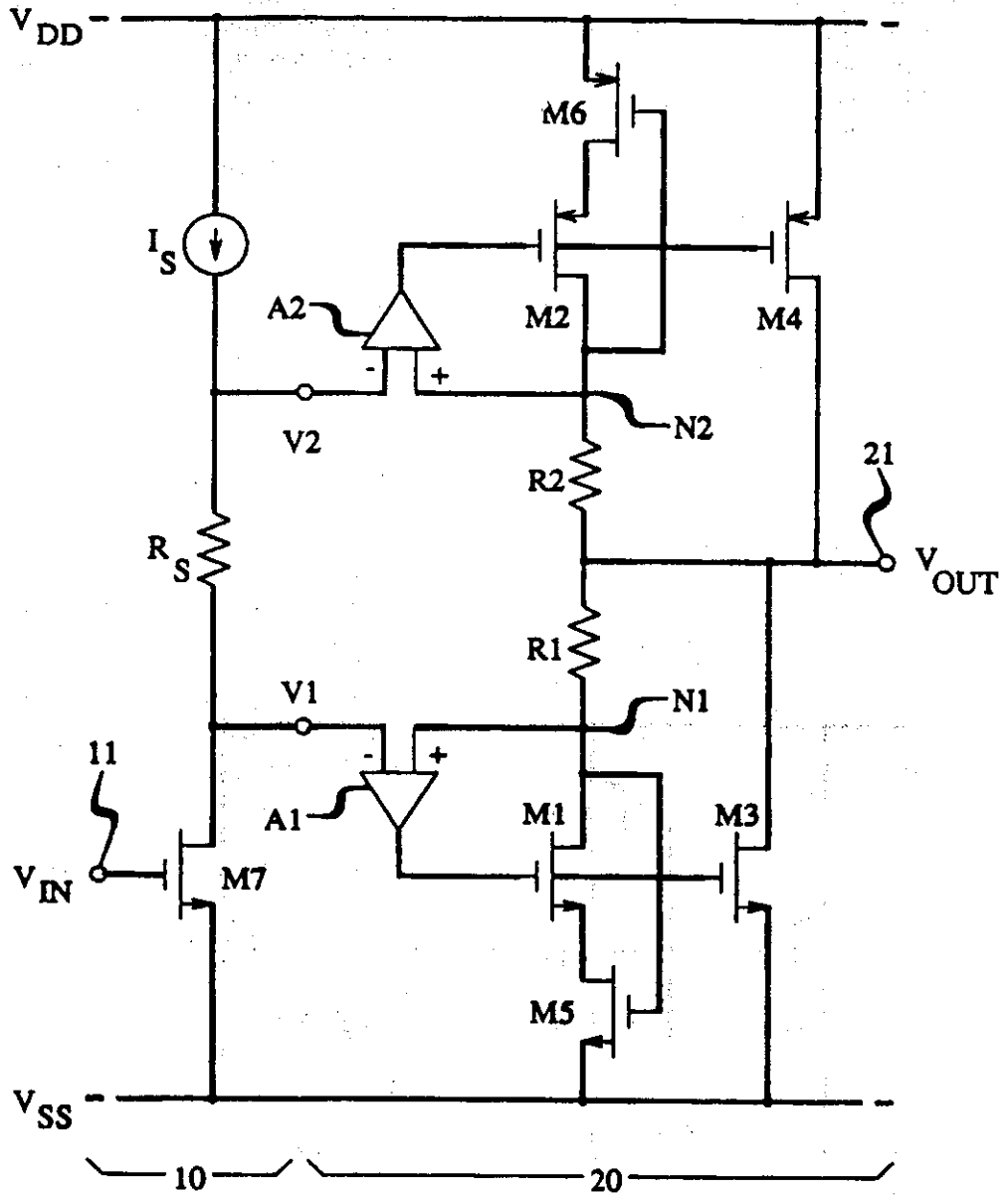
standseinrichtung (R1, R2) umfassen und eine Einrichtung zur Verbindung eines Knotens, der sich zwischen der ersten und der zweiten Verbindungseinrichtung befindet, mit einem Ausgangsanschluß (21) der Pufferstufe vorgesehen ist.

- Schaltung nach Anspruch 1 oder 2 mit einem vierten und einem fünften Transistorbauteil (M3, M4), die einen dritten bzw. vierten, einen verhältnismäßig niedrigen Strom führenden Steueranschluß besitzt und mit dem ersten bzw. zweiten Steueranschluß des ersten bzw. zweiten Transistorbauteils verbunden sind, wobei das vierte und das fünfte Transistorbauteil einen vierten bzw. einen fünften, verhältnismäßig hohen Strom führende Wege besitzen, die seriell zwischen die ersten und die zweite Stromversorgungsschiene geschaltet sind.
- Schaltung nach Anspruch 3, bei der das Verhältnis der Kanalbreite zur Kanallänge des vierten und des fünften Transistorbauteils wenigstens fünf mal größer als das des ersten bzw. zweiten Transistorbauteils ist.
- Schaltung nach Anspruch 3 oder 4 mit einem sechsten und siebten Transistorbauteil (M5, M6), deren Hochstromwege jeweils in Reihe mit denen des ersten und zweiten Transistorbauteils geschaltet sind und deren Steueranschlüsse mit dem ersten bzw. zweiten Knoten (N1, N2) verbunden sind.
- Schaltung nach einem der vorhergehenden Ansprüche, bei der der Konstantstrom multipliziert mit dem Widerstandswert der weiteren Widerstandseinrichtung wenigstens etwa gleich dem Fünffachen Wert der Eingangs-Offset-Spannung des ersten und zweiten Verstärkers ist.
- Integrierte Halbleiterschaltung mit einer Schaltung nach einem der vorhergehenden Ansprüche.

Revendications

- Circuit amplificateur comprenant un étage séparateur (20) qui comprend des premier et second amplificateurs (A1, A2) ayant chacun une borne de sortie et des première et seconde bornes d'entrée, des premier et second moyens de connexion (R1, R2), des premier et second dispositifs à transistors (M1, M2), ayant respectivement des premier et second chemins commandés acheminant un courant relativement élevé, et ayant respectivement des première et seconde bornes de commande acheminant un courant re-

- lativement faible, des première et seconde lignes d'alimentation (V_{SS} , V_{DD}), le premier chemin à courant élevé du premier dispositif à transistor (M1), le premier moyen de connexion (R1), le second moyen de connexion (R2) et le second chemin à courant élevé du second dispositif à transistor (M2) étant connectés en série, dans l'ordre indiqué, dans un chemin qui s'étend entre la première ligne d'alimentation et la seconde ligne d'alimentation, des moyens pour connecter la borne de sortie du premier amplificateur à la borne de commande du premier dispositif à transistor (M1), et des moyens pour connecter la borne de sortie du second amplificateur à la borne de commande du second dispositif à transistor (M2),
- CARACTERISE EN CE QUE** les premier et second amplificateurs (A1, A2) sont des amplificateurs opérationnels, l'un au moins des premier et second moyens de connexion comprend des moyens à résistance (R1, R2), il existe des moyens pour connecter un premier noeud (N1) se trouvant entre le premier dispositif à transistor (M1) et le premier moyen de connexion (R1), à la seconde borne d'entrée du premier amplificateur, et des moyens pour connecter un second noeud (N2) se trouvant entre le second dispositif à transistor (M2) et le second moyen de connexion (R2), à la seconde borne d'entrée du second amplificateur (A2), et il existe un étage de gain en tension (10) comprenant des moyens constituant une source de courant (I_S) pour fournir un courant constant, des moyens à résistance supplémentaires (R_S) ayant des première et seconde bornes ($V1$, $V2$), un troisième dispositif à transistor (M7) ayant une borne de commande qui est connectée à une borne d'entrée de circuit (11) destinée à recevoir une tension de signal d'entrée, le troisième dispositif à transistor ayant un troisième chemin à courant relativement élevé qui convient pour acheminer le courant constant, des moyens pour connecter en série, dans l'ordre indiqué, de la première ligne d'alimentation à la seconde ligne d'alimentation, les moyens constituant une source de courant, les moyens à résistance supplémentaires et le troisième chemin à courant relativement élevé, et des moyens pour connecter les première et seconde bornes des moyens à résistance supplémentaires à la première borne d'entrée respectivement des premier et second amplificateurs opérationnels.
2. Circuit selon la revendication 1, dans lequel chacun des premier et second moyens de connexion comprend des moyens à résistance (R1, R2), et des moyens sont prévus pour connecter un noeud se trouvant entre les premier et second moyens de connexion, à une borne de sortie (21) de l'étage séparateur.
 3. Circuit selon la revendication 1 ou 2, comprenant des quatrième et cinquième dispositifs à transistors (M3, M4) ayant respectivement des troisième et quatrième bornes de commande acheminant un courant relativement faible, qui sont respectivement connectées aux première et seconde bornes de commande des premier et second dispositifs à transistor, respectivement, les quatrième et cinquième dispositifs à transistor ayant respectivement des quatrième et cinquième chemins à courant relativement élevé qui sont connectés en série de la première ligne d'alimentation à la seconde ligne d'alimentation.
 4. Circuit selon la revendication 3, dans lequel le rapport entre la largeur et la longueur de canal du quatrième dispositif à transistor et celui du cinquième dispositif à transistor sont respectivement au moins cinq fois supérieurs à celui du premier dispositif à transistor et à celui du second dispositif à transistor.
 5. Circuit selon la revendication 3 ou 4, comprenant des sixième et septième dispositifs à transistor (M5, M6) dont les chemins à courant élevé sont respectivement connectés en série avec ceux des premier et second dispositifs à transistor, et dont les bornes de commande sont respectivement connectées aux premier et second noeuds (N1, N2).
 6. Circuit selon l'une quelconque des revendications précédentes, dans lequel le produit du courant constant par la résistance des moyens à résistance supplémentaires est au moins 5 fois supérieur à la tension de décalage d'entrée des premier et second amplificateurs.
 7. Un circuit intégré à semiconducteurs comprenant un circuit selon l'une quelconque des revendications précédentes.



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