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[Continued on next page]

(54) Title: DOPING IN III-NITRIDE DEVICES

(57) Abstract: Doping in Ill-nitride devices can be used for effective polarization field screening, wherein doped layers are adjacent to the outermost extents of light-emitting layers, or the doped layers are offset more than 1 nm from the furthest extents of the light-emitting layers, or the doped layers are within a multiple quantum well active region comprising the light-emitting layers. In addition, germanium (Ge) can be used as an n-type dopant in highly-doped Ill-nitride layers, because it does not add significant strain to a Ill-nitride lattice while maintaining smooth morphology beyond a concentration of 1E20 cm^{-3}.

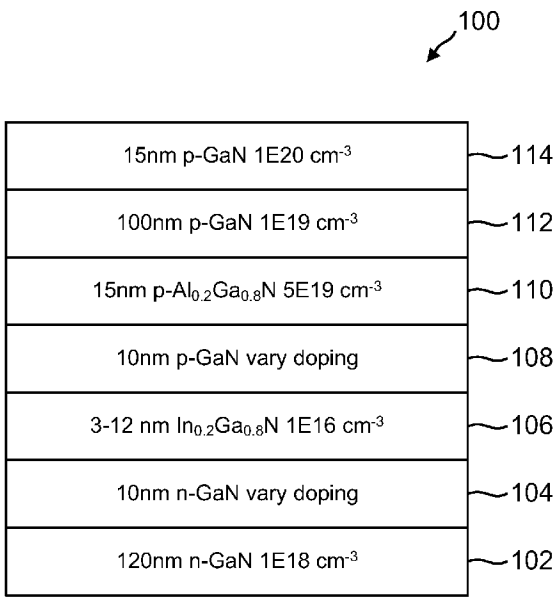

FIG. 1

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DOPING IN III-NITRIDE DEVICES

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit under 35 U.S.C Section 119(e) of the following co-pending and commonly-assigned applications:

U.S. Provisional Application Serial No. 61/993,804, filed on May 15, 2014, by Nathan G. Young, Robert M. Farrell, Claude C. A. Weisbuch, James S. Speck, Steven P. DenBaars, and Shuji Nakamura, entitled "DOPING IN (0001) III-NITRIDE LIGHT-EMITTING DEVICES FOR EFFECTIVE POLARIZATION FIELD SCREENING," attorneys' docket number 30794.553-US-P1 (2014-722-1); and

U.S. Provisional Application Serial No. 62/074,950, filed on November 4, 2014, by Nathan G. Young, James S. Speck, Steven P. DenBaars, Shuji Nakamura, and Umesh K. Mishra, entitled "DOPED III-NITRIDE ELECTRONIC DEVICES," attorneys' docket number 30794.578-US-P1 (2015-301-1);

which applications are incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates to doping in III-nitride devices.

2. Description of the Related Art.

(Note: This application references a number of different publications as indicated throughout the specification by one or more reference numbers within brackets, e.g., [Ref. x]. A list of these different publications ordered according to these reference numbers can be found below in the section entitled "References." Each of these publications is incorporated by reference herein.)

Current commercially-available III-nitride are typically grown along the polar [0001] c-direction and the associated polarization-induced electric fields are detrimental to the device performance. Reducing or eliminating polarization-induced

electric fields in the active region of c-plane devices should significantly improve device performance.

For typical c-plane devices, the net polarization in the active region is greater than zero and in the opposite sense to the built-in field due to the p-n or n-p junction. However, the impurity doping profile can be designed so that the built-in field effectively screens the polarization field, resulting in a near zero net field in the active region of a properly doped device.

Silicon (Si) and germanium (Ge) are suitable n-type dopants in III-nitride semiconductors with low activation energy. Silicon has been the n-type dopant of choice in all III-nitride devices since they were first developed, but there are issues with highly Si-doped layers above 1E19 cm^{-3}. Because of the large polarization discontinuities on c-plane, very large dopant concentrations up to 1E20 cm^{-3} may be necessary to screen fixed polarization charges at heterointerfaces and to cause polarization charges that contribute to a conductive two-dimensional electron gas (2DEG) channel.

Heavy Si doping leads to dislocation incline, resulting in a buildup of tensile stress that can lead to cracking and other morphological degradation. Germanium, on the other hand, has recently been shown to not add significant strain to the Gallium Nitride (GaN) lattice while maintaining smooth morphology beyond a concentration of 1E20 cm^{-3}. [Ref. 11] Thus, the use of Ge as an n-type dopant, rather than Si, may be necessary to achieve such high dopant densities without compromising material quality. [Ref. 1]

Consequently, there is a need in the art for improvements in the fabrication of III-nitride devices in order to increase dopant concentrations. The present invention satisfies this need.

SUMMARY OF THE INVENTION

To overcome the limitation in the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding the present specification, the present invention describes doping in III-nitride devices.

In one aspect, the present invention describes doping in c-plane (0001) III-nitride light emitting devices for effective polarization field screening. The devices include one or more light-emitting layers and one or more doped layers, wherein: the doped layers are adjacent to the light-emitting layers' outermost extents, or the doped layers are offset more than 1 nm from the light-emitting layers' furthest extents, or the light-emitting layers comprise a multiple quantum well (MQW) active region and the doped layers are within the multiple quantum well active region.

In another aspect, the present invention describes a III-nitride semiconductor device comprised of two or more III-nitride layers, wherein germanium (Ge) is used as an n-type dopant in one or more of the layers. Germanium does not add significant strain to a III-nitride lattice while maintaining smooth morphology beyond a concentration of 1E20 cm^{-3}. Germanium is a more suitable dopant for highly doped layers in III-nitride electronic devices, especially transistors involved in high voltage, high power or high frequency operation, such as high electron mobility transistors (HEMTs), current aperture vertical electron transistors (CAVETs), heterojunction bipolar transistors (HBTs), metal-semiconductor field effect transistors (MESFETs) or junction field effect transistor (JFETs).

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIG. 1 is a cross-sectional schematic of a (0001) single quantum well (SQW) LED structure.

FIGS. 2(a), 2(b), 2(c) and 2(d) are simulated energy band diagrams and ground state electron and hole wavefunctions under equilibrium (J = 100 A/cm^2) for

SQW LEDs with quantum well (QW) thicknesses of: 3 nm in FIG. 2(a), 5 nm in FIG. 2(b), 8 nm in FIG. 2(c), and 12 nm in FIG. 2(d), respectively.

FIG. 3 is a graph of the simulated dependence of the square of the wavefunction overlap on current density for SQW LEDs with a range of QW thicknesses.

FIGS. 4(a), 4(b), 4(c) and 4(d) are simulated energy band diagrams and ground electron and hole wavefunctions under forward bias (J = 100 A/cm^2) for SQW LEDs with doping levels of: 1E19 cm^{-3} in FIG. 4(a), 4E19 cm^{-3} in FIG. 4(b), 7E19 cm^{-3} in FIG. 4(c), and 1E20 cm^{-3} in FIG. 4(d).

FIG. 5 is a graph of the simulated dependence of the square of the wavefunction overlap on current density for SQW LEDs with a range of doping levels.

FIG. 6 is a schematic representation of a III-nitride high electron mobility transistor (HEMT).

FIG. 7 is a schematic representation of a III-nitride current aperture vertical electron transistor (CAVET).

FIG. 8 is a schematic representation of a III-nitride heterojunction bipolar transistor (HBT).

FIG. 9 is a schematic representation of a III-nitride metal-semiconductor field effect transistor (MESFET).

FIGS. 10(a) and 10(b) are schematic representations of a structure for van der Pauw and Hall effect measurements on GaN:Ge layers, wherein FIG. 10(a) shows a cross-section view and FIG. 10(b) shows a top down view.

FIG. 11 is the experimental relation between carrier concentration, mobility, and IBGe carrier flow for GaN:Ge layers grown with the structure of FIGS. 10(a) and 10(b).

FIGS. 12(a) and 12(b) are schematic representations of a III-nitride HEMT with a GaN:Ge layer in the AlGaN barrier, wherein the Ge doped layer can either

have a definite thickness as shown in FIG. 12(a) or be a delta-doped layer as shown in FIG. 12(b).

FIG. 13 is a schematic representation of a III-nitride gate-recessed HEMT with a GaN:Ge delta doped layer just above the $Al_xGa_{1-x}N$ / $Al_yGa_{1-y}N$ interface.

FIG. 14 is a schematic representation of a III-nitride CAVET with a GaN:Ge layer in the AlGaN barrier region above the channel.

DETAILED DESCRIPTION OF THE INVENTION

In the following description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

I. DOPING IN (0001) III-NITRIDE LIGHT-EMITTING DEVICES FOR EFFECTIVE POLARIZATION FIELD SCREENING

A. Background

This invention describes a structure for improving the performance of c-plane (0001) III-nitride light-emitting or light-absorbing devices. As noted above, current commercially-available III-nitride light emitting diodes (LEDs) and laser diodes (LDs) are typically grown along the polar [0001] c-direction and the associated polarization-induced electric fields are detrimental to the device performance. Reducing or eliminating polarization-induced electric fields in the active region of c-plane devices should significantly improve device performance.

For typical c-plane devices, the net polarization in the active region is greater than zero and in the opposite sense to the built-in field due to the p-n or n-p junction. This leads to a reduction in electron-hole wavefunction overlap in the active layer and a corresponding decrease in radiative efficiency; however, the impurity doping profile can be designed so that the built-in field effectively screens the polarization field,

resulting in a near zero net field in the active region of a properly doped device. Because of the large polarization discontinuities on c-plane, very large dopant concentrations up to 1E20 cm^{-3} may be necessary to screen fixed polarization charges at heterointerfaces. The use of Ge as an n-type dopant, rather than Si, may be necessary to achieve such high dopant densities without compromising material quality. [Ref. 1]

Decreasing the net electric field in the active region should increase the wavefunction overlap at a given active region thickness, and allow growth of thicker active regions without a damaging loss of wavefunction overlap. Increased wavefunction overlap and active region thickness should increase recombination rates and decrease carrier density, resulting in less efficiency droop at a given current density. [Ref. 2] LEDs with a properly designed doping profile should result in minimal net field in the active region, maximum wavefunction overlap, allowing thicker active volume, and thus droop onset at high currents.

C-plane III-nitride LEDs are a commercially proven technology and can be grown on a variety of low cost substrates, including sapphire, silicon, and silicon carbide. A reduction in efficiency droop in c-plane III-nitride LEDs could significantly improve device performance at higher drive current densities. Operating at higher drive current densities allows proportionally less material use for the same light output, as one usually limits the operating current of LEDs to have maximum light generation efficiency. Decreasing polarization-induced electric fields by the proper doping described in the present invention should increase the current at which III-nitride LEDs have their maximum efficiency. Likewise, decreasing polarization-induced electric fields should decrease the current densities necessary to generate optical gain in III-nitride LDs. This should lead to significantly less heating in III-nitride LEDs and LDs, which should result in longer device lifetimes and higher production yields for device manufacturers.

B. Overview

The usefulness of III-nitrides has been well established for the fabrication of visible and ultraviolet optoelectronic devices and high power electronic devices. Current state-of-the-art III-nitride thin films, heterostructures, and devices are grown along the [0001] axis. The total polarization of such films consists of spontaneous and piezoelectric polarization contributions, both of which originate from the single polar [0001] axis of the wurtzite III-nitride crystal structure. When III-nitride heterostructures are grown pseudomorphically, polarization discontinuities are formed at surfaces and interfaces within the crystal. These discontinuities lead to the accumulation or depletion of carriers at surfaces and interfaces, which in turn produce electric fields. Since the direction of these polarization-induced electric fields coincides with the typical [0001] growth direction of III-nitride thin films and heterostructures, these fields have the effect of "tilting" the energy bands of III-nitride devices.

In c-plane wurtzite III-nitride quantum wells, the "tilted" energy bands spatially separate the electron and hole wavefunctions. This spatial charge separation reduces the oscillator strength of radiative transitions and red-shifts the emission wavelength. These effects are manifestations of the quantum confined Stark effect (QCSE) and have been thoroughly analyzed for III-nitride quantum wells (QWs). [Refs. 3-6] Under device operation, the large polarization-induced electric fields can be partially screened by injected carriers. [Ref. 7] While this partially diminishes the internal electric field inside the quantum wells, it leads to emission characteristics, such as the emission wavelength, that are difficult to engineer accurately.

For typical c-plane devices, the net polarization in the active region is greater than zero, which can lead to a reduction in electron-hole wavefunction overlap in the active layer and a corresponding decrease in radiative rate which results in diminished radiative efficiency. For light-emitting devices grown on c-plane, the polarization field is in the opposite sense to the built-in field due to the p-n junction. Therefore, in the growth of c-plane devices, the impurity doping profile can be designed so that the

built-in field effectively screens the polarization field, resulting in a near zero net field in the active region of a properly doped device. These doping profiles can be designed so the net field is near zero for current densities of interest for device operation. Because of the large polarization discontinuities between different compositions of (Ga,Al,In,B)N semiconductor alloys on the polar (0001) plane, very large dopant concentrations up to 1E20 cm^{-3} may be necessary to screen fixed polarization charges at heterointerfaces. The use of Ge as an n-type dopant, rather than Si, may be necessary to achieve such high dopant densities without adding strain and negatively impacting epitaxial surface morphology during growth. [Ref. 1]

Decreasing the net electric field in the active region should increase the wavefunction overlap, which should increase both the radiative and nonradiative recombination rates in the active region. [Ref. 2] It might seem that nothing has been gained; however, increasing the recombination rate should decrease the carrier density in the active region for a given current density, resulting in less efficiency droop at a given current density. Indeed, a one-to-one correlation has been found between the net electric field in the active region and the magnitude of efficiency droop for c-plane III-nitride LEDs. [Ref. 2] Decreasing the net electric field in the active region also allows for the growth of thicker active regions without a damaging loss of wavefunction overlap. Thicker active region designs will also decrease the carrier density in the active region, resulting in less efficiency droop for a given current density. LEDs with a properly designed doping profile should result in a minimal net field in the active region, maximum wavefunction overlap, allowing thicker active volume, and thus droop onset at high currents.

This invention describes a structure for decreasing the net electric field in the active region of (0001) single quantum well (SQW), multiple quantum wells (MQW) or double heterostructure (DH) LEDs and lasers. By DH, this specification means devices where the single light emitting layer is thick enough that electron and hole energy levels are approximately continuous.

C. Technical Description

FIG. 1 shows a cross-sectional schematic of the (0001) SQW LED structure 100. This structure 100 was used for simulating the effects of QW thickness and doping on the net electric field and wavefunction overlap in the active region. The structure is comprised of a 120 nm n-GaN layer 102 with [Si] = 1E18 cm^{-3}, a 10 nm n-GaN barrier layer 104 with varying doping level, an n-$In_{0.20}Ga_{0.80}N$ SQW 106 of varying thickness with an n-type background doping level of 1E16 cm^{-3}, a 10 nm p-GaN barrier layer 108 with varying doping level, a 15 nm p-$Al_{0.20}Ga_{0.80}N$ electron blocking layer 110 with [Mg] = 5E19 cm^{-3}, a 100 nm p-GaN layer 112 with [Mg] = 1E19 cm^{-3}, and a 15 nm p-GaN contact layer 114 with [Mg] = 1E20 cm^{-3}.

Since equal fixed positive and negative sheet charges exist at the top and bottom interfaces of the SQW 106, respectively, the doping levels in the n-GaN and p-GaN barrier layers 104, 108 were varied equally and concurrently. For the purposes of the simulation, LEDs with four SQW thicknesses of 3, 5, 8, and 12 nm were considered with nominally undoped (1E16 cm^{-3} n-type) GaN barrier layers. Additionally, LEDs with four barrier layer doping levels of 1E16 cm^{-3}, 1E17 cm^{-3}, 1E18 cm^{-3}, and 1E19 cm^{-3} were considered with a 12 nm SQW. For the sake of simplicity, this specification only describes effects on the longitudinal (along (0001)) ground state of the SQW structure. While it is an excellent approximation for the thinnest QW structure, an exact rendition would also need to model excited states in thicker layer samples. This would add unnecessary complexity without changing the arguments developed below. This specification also only models SQW structures, but the arguments would apply equally well to MQW structures.

All simulations were performed using the SiLENSe version 5.4 software. [Ref. 7]

FIGS. 2(a), 2(b), 2(c) and 2(d) show simulated energy band diagrams and ground state electron and hole wavefunctions under forward bias (at a current density, J = 100 A/cm^2) for LEDs with varying QW thicknesses and nominally undoped barrier layers (1E16 cm^{-3} n-type). The low doping in the barrier layers will not screen

the polarization fields in the QW. As shown in FIG. 2(a), the ground state electron and hole wavefunctions are pressed together by the wide bandgap barrier confinement even though the electric field in the QW is very high. This high degree of confinement in a 3 nm SQW LED maintains a sizeable carrier wavefunction overlap, about 18% at zero current injection (described below with regard to FIG. 3). In FIGS. 2(b), 2(c), and 2(d), as the QW thickness increases, the separation of the ground state electron and hole wavefunctions also increases, resulting in decreased wavefunction overlap. The electric field in the QW remains large in the case of 5, 8, and 12 nm QW LEDs even at the relatively high forward current density of $J = 100$ A/cm^2 as injected carriers only partially screen the polarization-induced electric field. In the case of the 12 nm QW LED, the field is nearly flat in the middle of the QW, but increases significantly at the right and left edges, causing the electron and hole ground state wavefunctions to be confined at the edges of the well rather than spreading across the entire width of the well. Well-designed n-type and p-type barrier layer doping is necessary to fully screen the polarization charges at the QW interfaces and flatten the electric field in the QW, thereby increasing wavefunction overlap.

Increasing the wavefunction overlap in the active region of c-plane devices should have a number of potential benefits for device operation. FIG. 3 summarizes the simulated dependence of the square of the wavefunction overlap on current density for LEDs with a range of active region thicknesses and no intentional barrier layer doping. As shown in FIG. 3, the LEDs with QW thicknesses of 3, 5, and 8 nm exhibited wavefunction overlap that increased monotonically as a function of current density. There was, however, a dramatic decrease in the values of wavefunction overlap between the 3 nm QW LED and the 5 nm QW LED, and again between the 5 nm QW LED and the 8 nm QW LED. The LED with a thickness of 12 nm exhibited nearly zero wavefunction overlap with little dependence on current density. The increase in wavefunction overlap with increasing current density is indicative of the expected partial screening of polarization by injected carriers. Nevertheless, the maximum overlap of all four LEDs with nominally undoped barriers was still less

than less than 0.35 at 1 kA/cm^2 due to incomplete screening of the polarization, which is worse for thicker active layers due to their increased separation between the electron and hole ground state wavefunctions.

Larger QW thicknesses are desired, however, in order to reduce efficiency droop by reducing active region carrier density at a given drive current density. This is due to the nonlinear dependence on carrier density of the Auger non radiative process, which causes droop. [Ref. 8] Therefore, two main effects are expected from the present invention of increased electron hole pair overlap for thick active layers: (i) the possibility to retain large electron hole pair overlap even for thick active layers; (ii) increased electron hole pair overlap compared to the value reached in thin QWs.

FIGS. 4(a), 4(b), 4(c) and 4(d) show simulated energy band diagrams and ground state electron and hole wavefunctions under forward bias (at J = 100 A/cm^2) for LEDs with varying n and p barrier doping levels and a QW thickness of 12 nm. FIG. 4(a) shows that even with n and p barrier layer doping of 1E19 cm^{-3}, there is little difference from the undoped case (FIG. 3): the electric field in the QW is still in the opposite sense to the built-in field since the polarization field remains largely unscreened, and this leads to a spatial separation of the ground state electron and hole wavefunctions, yielding a near zero wavefunction overlap. FIG. 4(b) shows that upon increasing the doping to 4E19 cm^{-3}, the electric field in the QW begins to decrease and the energy bands begin to flatten, bringing the electron and hole wavefunctions closer together and increasing the overlap, though it is apparent that the wavefunctions are still spatially separated. Increasing the doping slightly more to 7E19 cm^{-3}, as shown in FIG. 4(c), results in nearly zero electric field in the QW, indicating that the polarization field in the QW was fully screened. The wavefunction overlap in this case is very high. In contrast, FIG. 4(d) once again shows some spatial separation between the electron and hole wavefunctions and a non-zero electric field in the QW. The doping level of 1E20 cm^{-3} was high enough to be degenerate on the n-side of the QW and cause an accumulation of electrons. This resulted in a lowering of the bands on the n-side of the well, which lead to a non-zero electric field and

localization of the electron wavefunction nearer to the n-side of the well. The hole wavefunction remained largely unchanged between FIGS. 4(c) and 4(d). According to these simulations, the condition of near zero electric field in the QW is met at a doping level near 7E19 cm^{-3}.

FIG. 5 summarizes the simulated dependence of the square of the wavefunction overlap on current density for LEDs with a SQW width of 12 nm and a range of doping levels. The LED with a doping level of 1E19 cm^{-3} exhibited nearly zero wavefunction overlap over a large range of current densities. The LED with a doping of 4E17 cm^{-3} exhibited a relatively low but non-zero wavefunction overlap that increased monotonically with increasing current density. Likewise, the LED with a doping level of 1E20 cm^{-3} showed a similar, albeit much higher, dependence of the wavefunction overlap on current density. In contrast, the LED with a doping level of 7E19 cm^{-3} exhibited a high wavefunction overlap with little dependence on current density above J = 100 A/cm^2. This behavior is similar to that expected for a nonpolar LED with the same structure and indicates that the polarization field in the QW was fully screened with a doping level of 7E19 cm^{-3}. It should be noted that, in the case of a doping level of 7E19 cm^{-3}, the overlap has a local maximum near J = 100 A/cm^2. Increasing the doping further pushes that maximum point to higher overlaps and higher current densities. No maximum is evident in the curve for the case of an LED with a doping level of 1E20 cm^{-3}, but above J = 400 A/cm^2, the wavefunction overlap is actually higher than the case of 7E19 cm^{-3} doping. However, it is desirable to design a structure that has high overlap, and therefore high radiative efficiency, at both low and high drive current densities. A structure like the one described above, with a wide active region and high wavefunction overlap over a wide range of drive current densities, is likely to exhibit a minimal amount of efficiency droop.

The above section described a structure for decreasing the net electric field in the active region of a (0001) SQW LED. However, the scope of this invention also covers the N-face (000-1) orientation when used in an n-p junction, with the p-type

material underneath the active region so that the polarization is in the opposite sense to the built-in field due to the n-p junction.

The scope of this invention also covers III-nitride devices with active regions designs other than the 12 nm $In_{0.20}Ga_{0.80}N$ SQW active region design cited in the technical description. This idea is also pertinent to III-nitride devices with multiple quantum well (MQW) active regions, active regions with QWs of any thickness, active regions with QWs of any alloy composition, active regions with QWs of a graded alloy composition, active regions with barriers of any thickness, active regions with barriers of any alloy composition, and active regions with barriers of a graded alloy composition. It has already been shown that doping adjacent to MQW active regions in InGaN/GaN c-plane solar cells is beneficial for current collection. [Ref. 9] Similar improvements could be expected for current injection into MQW c-plane LED active regions.

The scope of this invention also covers III-nitride devices with doping profiles other than the profile cited above in the technical description. The LED cited above in the technical description had 10 nm n-type and p-type doped layers that were immediately adjacent to the light-emitting layers in the active region. However, the scope of this invention also covers doped layers that are offset slightly (e.g. more than 1 nm) from the light-emitting layers. Offsetting the doped layers decreases the effectiveness of the polarization screening, but may be necessary for other reasons related to the device growth or fabrication. This idea is also pertinent to doped layers that are offset by asymmetric distances from the light-emitting layers, doped layers with asymmetric doping levels, doped layers with graded doping profiles, and doped layers of asymmetric thicknesses.

The scope of this invention also covers III-nitride devices with MQW active regions where the layers between light-emitting QWs (referred to hereafter as internal barrier layers) are intentionally doped. In a MQW active region there is more than one pair of polarization sheet charge layers, each of which must be compensated in order to screen the electric field in all of the light emitting QW layers. Doping of internal

barrier layers, which are immediately adjacent to QWs in the MQW active region, may be more effective at screening polarization-induced fields in a MQW active region than only doping layers outside of the active region. This idea is pertinent to cases where all internal barrier layers between QWs are intentionally doped, where some internal barrier layers are intentionally doped and others are not, where one or more internal barrier layers are intentionally doped by different amounts, and where internal barrier layers have graded doping profiles.

Additional impurities or dopants can also be incorporated into the c-plane III-nitride thin films described in this invention. For example, Fe, Mg, Si, Ge, and Zn are frequently added to various layers in III-nitride heterostructures to alter the conduction properties of those and adjacent layers. These dopants can also be incorporated in the vicinity of the active region so that built-in field due to the p-n junction effectively screens the polarization field of the active region. The use of such dopants and others not listed here are within the scope of the invention.

Moreover, substrates other than free-standing c-plane GaN could be used for III-nitride thin film growth. The scope of this invention includes the growth of III-nitride thin films on all possible crystallographic orientations of all possible foreign substrates. These foreign substrates include, but are not limited to, sapphire, silicon carbide, silicon, zinc oxide, boron nitride, lithium aluminate, lithium niobate, germanium, aluminum nitride, lithium gallate, partially substituted spinels, and quaternary tetragonal oxides sharing the γ-$LiAlO_2$ structure.

Furthermore, variations in c-plane III-nitride nucleation (or buffer) layers and nucleation layer growth methods are acceptable for the practice of this invention. The growth temperature, growth pressure, orientation, and composition of the nucleation layers need not match the growth temperature, growth pressure, orientation, and composition of the subsequent thin films and heterostructures. The scope of this invention includes the growth of c-plane III-nitride thin films on all possible substrates using all possible nucleation layers and nucleation layer growth methods.

The scope of this invention also covers c-plane III-nitride thin films grown on epitaxial laterally overgrown (ELO) III-nitride templates. The ELO technique is a method of reducing the density of threading dislocations (TD) in subsequent epitaxial layers. Reducing the TD density leads to improvements in device performance. For c-plane III-nitride LEDs and LDs, these improvements include increased output powers, increased internal quantum efficiencies, longer device lifetimes, and reduced threshold current densities. [Ref. 10]

II. DOPED III-NITRIDE ELECTRONIC DEVICES

A. Background

To date, modern power semiconductor devices, including devices such as Si Power Metal-Oxide-Semiconductor Field-Effect Transistors (Power MOSFETs) and Si Insulated Gate Bipolar Transistors (IGBT), have been typically fabricated with silicon semiconductor materials. More recently, silicon carbide (SiC) power devices have been researched due to their superior properties. GaN semiconductor devices are now emerging as an attractive candidate to carry large currents and support high voltages providing very low on resistance and fast switching times.

A high electron mobility transistor (HEMT) is one type power semiconductor device that can be fabricated based on III-nitride materials. A GaN HEMT device can include a III-nitride semiconductor body with at least two III-nitride layers formed thereon. Different materials formed on the body or on a buffer layer causes the layers to have different band gaps. The different materials in the adjacent III-nitride layers also causes polarization, which contributes to a conductive two-dimensional electron gas (2DEG) region near the junction of the two layers, specifically in the layer with the narrower band gap. One of the layers through which current is conducted is the channel layer. Herein, the narrower band gap layer in which the current carrying channel, or the 2DEG is located is referred to as the channel layer. The device also includes a gate electrode, a Schottky contact, and Ohmic source and drain electrodes on either side of the gate.

FIG. 6 shows a standard Ga-face GaN HEMT structure 600 comprised of a substrate 602, GaN buffer layer 604, $Al_xGa_{1-x}N$ layer 606, source (S) 608, drain (D) 610 and gate (G) 612. The substrate 600 may be GaN, SiC, sapphire, Si, or any other suitable substrate for GaN device technology. The conducting channel is comprised of a 2DEG 614 formed in the GaN layer 604 near the interface with the $Al_xGa_{1-x}N$ layer 606, which is shown as a dotted line in FIG. 6. The region between the source 608 and gate 612 is referred to as the source access region, and the region between the drain 610 and gate 612 is referred to as the drain access region.

In conventional III-V HEMTs, the barrier layer (for example, AlGaAs on GaAs) must be doped in order to pull the conduction band energy down far enough to form a 2DEG at the heterointerface. The delta-doped sheet or doped region is usually separated from the heterointerface by an undoped cap layer. In III-nitride HEMTs, the barrier layer is often left undoped since a 2DEG forms naturally due to polarization. This allows for higher channel mobility due to the lack of ionized impurity scattering. In this case, the charge in the channel comes from surface donor states.

Having the channel charge provided by surface states can present problems. There is the problem of DC-to-RF dispersion, in which the static I-V characteristics of the device predict a higher output power than is seen in load pull measurements. Surface traps with slow response times are believed to be responsible this dispersion. Surface passivation, for example by SiN, can improve performance, but the reliability and reproducibility of dispersion elimination as well as breakdown voltage and gate leakage is poor and depends strongly on processing.

One method of overcoming the problems presented by surface donor states is to dope the barrier layer with an n-type dopant. This doping can take the form of a delta-doped layer or a thicker region of the barrier layer. There is a trade-off involved in the placement of this doped layer. The closer the donors are to the channel, the more charge they can contribute because surface states are also competing for charges. On the other hand, having donors close to the channel decreases the channel mobility due to ionized impurity scattering.

A current aperture vertical electron transistor (CAVET) is another type power semiconductor device that can be fabricated based on III-nitride materials. FIG. 7 is a schematic illustration of a CAVET 700, including higher/heavily n-type doped GaN (n+ -GaN) 702, lower or lightly n-type doped GaN (n~- GaN) 704, aperture 706, Current Blocking Layer (CBL) 708, unintentionally doped (UID) GaN 710, $Al_xGa_{1-x}N$ 712, source (S) 714, gate (G) 716, and drain (D) 718. The CAVET 700 is a vertical device comprised of an n-type doped drift region to hold voltage and a horizontal 2DEG 720 to carry current flowing from the source 714, under a planar gate 716, and then in a vertical direction to the drain 718 through the aperture 706. As shown in FIG. 7, electrons flow horizontally from the source 714 through the 2DEG 720, which is represented as dashed lines, and then vertically through the aperture 706 region to the drain 718, and are modulated by the gate 716. A fundamental part of a CAVET 700 is the CBL 708, which blocks the flow of the current and causes on-state current to flow through the aperture 706.

Similar to a HEMT, a CAVET's performance relies on high frequency modulation of current in a 2DEG channel 720. The same issues of dispersion apply, and it is desirable to dope the AlGaN barrier 712 in such a way as to provide charge to the channel 720 while avoiding impurity scattering.

An additional issue arises from heavy Si doping in the n-type buffer region 702. Heavy Si doping can result in an increase in the tensile strain of epitaxial layers. Subsequent growth of AlGaN layers 712 adds additional tensile strain, which can lead to cracking. It is desirable to have a structure with a heavily n-doped buffer region 702 for low contact resistance, but to also avoid adding strain to the subsequent layers during growth.

A heterojunction bipolar transistor (HBT) is another type of power semiconductor device that can be fabricated based on III-nitride materials. FIG. 8 is a schematic illustration of an HBT 800, including an n-type doped GaN emitter region 802, a p-type doped GaN base region 804, a lightly n-type doped GaN collector region 806, a heavily n-type doped GaN sub-collector region 808, and emitter 810,

base 812, and drain 814 contacts. The substrate 816 may be GaN, SiC, sapphire, Si, or any other suitable substrate for GaN device technology. The HBT 800 is a vertical device comprised of an n-type emitter region 802, a p-type base region 804, and an n-type collector region 806. Electrons are provided by the emitter 810 and they flow across the base 812 and to the collector 814. On-state current flows in the device 800 when the emitter-base junction is forward biased, and the base-collector junction is reverse biased. It is desirable to have a structure with a heavily n-doped sub-collector region 808 for low contact resistance, but to also avoid adding strain to the subsequent layers during growth.

A metal-semiconductor field effect transistor (MESFET) or junction field effect transistor (JFET) is another type power semiconductor device that can be fabricated based on III-nitride materials. The key difference between a MESFET and a JFET is that, in a JFET, a p^+- n junction is used to create a barrier between the metal gate and the semiconductor, while, in the MESFET, the Schottky barrier between the metal and semiconductor is used. FIG. 9 is a schematic illustration of a MESFET 900 with a lightly n-type doped GaN channel region 902, a source 904, a drain 906, and a gate 908. The substrate 910 may be GaN, SiC, sapphire, Si, or any other suitable substrate for GaN device technology. Electrons flow through the channel region 902 from source 904 to drain 906 when the bias on the gate 908 is such that the channel 902 is not completely depleted.

The channel region 902 in a MESFET must be doped in order to ensure a low turn-on voltage; however, it is desirable to have high mobility in the channel 902. Doping tends to lower mobility due to ionized impurity scattering, so it would be desirable to use an n-type dopant in the channel 902 with a high mobility at the same doping concentration.

Thus, there is a need in the art for improved n-type dopants for III-nitride layers in III-nitride electronic devices, such as HEMTs, CAVETs, HBTs, and MESFETs. The present invention discloses III-nitride electronic devices with n-type layers doped with germanium. Germanium has been shown to not add significant

strain to a GaN lattice while maintaining smooth morphology beyond a concentration of 1E20 cm^{-3}. Consequently, germanium is a more suitable dopant for highly doped layers in III-nitride electronic devices, such as HEMTs, CAVETs, HBTs, and MESFETs.

B. Overview

This invention describes a structure for improving the performance and reliability of III-nitride electronic devices, especially transistors involved in high voltage, high power, or high frequency operation in such applications, where the use of III-nitride materials would be suitable. Many such devices suffer from a problem known as dispersion, in which the output power at high frequency operation is significantly lower than at DC operation. Properly placed doped layers can help overcome the problem of dispersion.

As noted above, silicon and germanium are suitable n-type dopants in III-nitride semiconductors with low activation energy. Silicon has been the n-type dopant of choice in all III-nitride devices since they were first developed, but there are issues with highly Si-doped layers with concentrations above 1E19 cm^{-3}. Heavy Si doping leads to dislocation incline, resulting in a buildup of tensile stress that can lead to cracking and other morphological degradation. Germanium, on the other hand, has recently been shown to not add significant strain to the GaN lattice while maintaining smooth morphology beyond a concentration of 1E20 cm^{-3}. [Ref. 11] Germanium should be a more suitable dopant than silicon for many highly doped layers in III-nitride electronic devices.

The addition of a highly doped layer in the wide bandgap barrier of a HEMT device replaces surface states as the source of charge in the channel of the transistor, which is comprised of a 2DEG formed because of the band discontinuity at the heterostructure interface between channel material and the wider bandgap barrier material. This prevents dispersion, which is thought to be caused by surface traps. A HEMT device using Ge instead of Si in the AlGaN barrier layer, either in a delta

doped layer or a layer of definite thickness, would allow higher doping concentrations before the onset of strain related degradation. The doped layer could be placed closer to the channel, separated by a wide bandgap cap layer, allowing higher charge concentration, or further from the channel with the same charge concentration, allowing higher mobility. Ge doping can also be applied to a gate-recessed HEMT just above the AlGaN barrier, which is contacted by the gate, and below the AlGaN cap, which screens the channel from the surface states that cause dispersion.

Similarly, in a CAVET structure, doping in the AlGaN barrier can eliminate dispersion. A CAVET device using Ge instead of Si in the AlGaN barrier layer, either in a delta doped layer or a layer of definite thickness, would allow higher doping concentrations before the onset of strain related degradation. The doped layer could be placed closer to the channel, separated by a wide bandgap cap layer, allowing higher charge concentration, or further from the channel with the same charge concentration, allowing higher mobility. Ge doping can also be applied to a gate-recessed CAVET just above the AlGaN barrier, which is contacted by the gate, and below the AlGaN cap, which screens the channel from the surface states that cause dispersion.

Additionally, Ge can be used in place of Si in highly doped layers in vertical transistor devices. In a CAVET, the highly n-type layer that makes contact with the backside drain electrode can be improved using Ge doping. At the same dopant concentration, there will be less strain added and better morphology than in a Si-doped layer. This will improve the layers grown above it and lead to better overall device performance. Similarly, in an HBT, the sub-collector layer can be improved using Ge doping. It needs to be highly n-type to spread current laterally and make low resistance contact to the collector electrode. At the same dopant concentration, there will be less strain added and better morphology than in a Si-doped layer. This will improve the layers grown above it and lead to better overall device performance.

Germanium can also be used in a MESFET to dope the GaN channel region. The inventors have shown that GaN:Ge has a higher mobility at the same carrier

concentration compared to GaN:Si. This is likely due to the similar size of Ge and Ga atoms, and it should hold even at low concentrations between 1E16 cm^{-3} and 1E18 cm^{-3} that are used in a MESFET channel.

Incorporation of Ge doping into III-nitride electronic devices, such as HEMTs, CAVETs, HBTs, and MESFETs, could significantly improve device performance by decreasing DC-to-RF power dispersion, increasing channel mobility and charge density, and decreasing epitaxial strain. Eliminating dispersion in HEMTs and CAVETs by Ge doping in the barrier region above the 2DEG channel would significantly improve output power at microwave frequencies. Increasing channel mobility and carrier density in 2DEG channels of HEMTs, CAVETs, and MESFETs would increasing operating frequencies and decrease on-resistance. Decreasing epitaxial strain in highly n-type doped layers near the bottom of an epitaxial stack in an HBT or CAVET structure by using Ge would limit the strain in the structure, limit strain-induced defect formation, and improve the quality of other layers, leading to higher performance devices.

C. Technical Description

This invention describes a structure with one or more layers of III-nitride material doped with Ge instead of Si for the purpose of supplying charge to a 2DEG channel while maintaining high mobility, and/or creating a heavily doped contact layer, and/or creating a high mobility doped channel, where the mobility achieved with Ge is fundamentally higher than can be met with Si and where the growth of the structure is unaffected by strain common in Si-based devices.

The inventors have demonstrated Ge doping of GaN grown by metal organic chemical vapor deposition (MOCVD). During GaN:Ge growth, a precursor containing Ga (trimethyl gallium [TMGa] or triethyl gallium [TEGa]), a precursor containing N (NH_3), and a precursor containing Ge (isobutyl germane [IBGe]) are injected into the reactor chamber. These precursor gasses are mixed with H_2 and/or N_2 carrier gas and directed to flow over the substrate material, which is heated to

between 500°C and 1200°C during growth. The concentration of Ge in the GaN:Ge film increases with an increasing molar flow ratio of Ge to Ga. The concentration of Ge in the GaN:Ge film is not affected strongly by temperature between 800°C and 1200°C.

The inventors measured the properties of GaN:Ge layers grown by MOCVD by Hall measurements using a special epitaxial structure and measurement system, shown in FIGS. 10(a) and 10(b). The epitaxial structure 1000 shown in FIG. 10(a) is comprised of a sapphire substrate 1002, a thick layer of intrinsic GaN 1004 (4 μm in this case) for isolation of a top conductive GaN:Ge layer 1006, which must be thick enough to provide low resistance (300 nm in this case), and metal contacts 1008. FIG. 10(b) shows a top-down view of the sample 1000 prepared for van-der Pauw resistivity and Hall effect measurements.

FIG. 11 shows the dependence of carrier concentration and mobility on the IBGe flow rate during growth of the GaN:Ge layer 1006 in the structure 1000 from FIG. 10(a). IBGe flow rates were varied in the study from 0.06 sccm to 10 sccm. Carrier concentration is assumed to be equal to Ge concentration due to the low donor activation energy of Ge in GaN. Molar flow ratios of Ge to Ga ranged between 0.0026 and 0.44, and resulting carrier concentrations (Ge concentrations) ranged between 8.8E17 cm^{-3} to 1.3E20 cm^{-3}, respectively. Over that range of carrier concentrations, the mobility ranged from 337 to 109 cm^2/Vs. Over the studied range of doping concentrations, the mobility of GaN:Ge is higher than that of GaN:Si. [Ref. 12] This is likely the result of the Ge atom closer size than the Si atom to the Ga atom that it replaces in the GaN lattice. The size similarity results in less impurity scattering, which would decrease mobility. Higher mobility in n-doped GaN:Ge layers compared to GaN:Si layers in III-nitride semiconductor devices would benefit performance in terms of speed and power.

A Ge doped layer can be added to the $Al_xGa_{1-x}N$ barrier region of the III-nitride HEMT from FIG. 6. This device 1200 is shown in FIGS. 12(a) and 12(b), and is comprised of a substrate 1202, GaN buffer 1204, $Al_xGa_{1-x}N$ 1206, $Al_xGa_{1-x}N$:Ge

1208, source 1210, drain 1212 and gate 1214. The $Al_xGa_{1-x}N$:Ge layer 1208 can comprise either a layer of defined thickness that makes up part or all of the $Al_xGa_{1-x}N$ barrier region 1206 shown in FIG. 12(a), or a delta-doped layer 1208 represented by a dotted line in FIG. 12(b). Doping in the barrier region 1206, 1208 will eliminate dependence on surface states for supplying charge to the 2DEG channel 1216 as well as the dispersion and poor reliability and reproducibility of processing that plague HEMTs with undoped barriers. The advantage of a delta-doped layer or thin doped layer is that the donors can be located on average closer to the channel 1216 and therefore give more of their charge to the channel 1216 instead of to surface states. This results in a higher channel carrier concentration. The main advantage of Ge instead of Si in the n-doped layer 1208 is that a higher concentration of Ge can be supported in the layer 1208 without adverse strain effects or morphological breakdown. Therefore, the doped layer 1208 can be separated by a greater distance from the channel 1216, causing less ionized impurity scattering and leading to a higher mobility.

An AlN spacer layer can be optionally added at the barrier/channel interface in order to better confine charges in the 2DEG channel 1216 as well as reduce ionized impurity scattering in the channel 1216, and should be between 0.5 and 2 nm thick. If an AlN spacer is present, an additional undoped AlGaN layer may be added before the Ge doped AlGaN layer 1208 to provide additional separation between dopant atoms and the channel. For example, a 1 nm AlN spacer may be followed by a 3 nm $Al_{0.2}Ga_{0.8}N$ layer before a delta doped sheet charge where the Ge concentration is above 1E13 cm^{-2}.

Another method of overcoming the problems presented by surface donor states is the deep-recessed GaN HEMT 1300 design shown in FIG. 13, which includes a substrate 1302, GaN buffer 1304, $Al_xGa_{1-x}N$ layer 1306, $Al_yGa_{1-y}N$ layer 1308, $Al_xGa_{1-x}N$:Ge layer 1310, source 1312, drain 1314 and gate 1316. In this design, a thick cap layer of GaN or $Al_yGa_{1-y}N$ 1308 isolates the surface from the 2DEG channel 1318, while a selective etch allows the gate 1316 metal to be deposited on a thin

$Al_xGa_{1-x}N$ barrier 1306. In this structure, x and y can, but need not, be the same. Charge is supplied to the channel 1318 by a highly n-doped layer 1310 (delta-doped or with a small thickness) at the interface between the $Al_xGa_{1-x}N$ layer 1306 and the $Al_yGa_{1-y}N$ layer 1308. This layer 1310 can be Ge doped to reduce impurity scattering in the channel 1318 again by increasing the $Al_xGa_{1-x}N$ barrier 1306 thickness while maintaining the same channel 1318 carrier concentration without morphological degradation or increase in strain.

A Ge doped layer can be added to the $Al_xGa_{1-x}N$ barrier region of the III-nitride CAVET from FIG. 6. Such a device 1400 is shown schematically in FIG. 14, and includes a higher/heavily n-type doped GaN (n+ -GaN) layer 1402, a lower or lightly n-type doped GaN (n~ -GaN) layer 1404, an aperture 1406, a Current Blocking Layer (CBL) 1408, an unintentionally doped (UID) GaN layer 1410, an $Al_xGa_{1-x}N$ layer 1412, an $Al_xGa_{1-x}N$:Ge layer 1414, source 1416, gate 1418, and drain 1420. The CAVET 1400 is a vertical device comprised of an n-type doped drift region to hold voltage and a horizontal 2DEG 1422 to carry current flowing from the source 1416, under the planar gate 1418, and then in a vertical direction to the drain 1420 through the aperture 1406.

The $Al_xGa_{1-x}N$:Ge layer 1414 can comprise either a layer of defined thickness that makes up part or all of the $Al_xGa_{1-x}N$ barrier region 1412 or a delta-doped layer like the one depicted in the HEMT in FIG. 12(b). Doping in the barrier region 1412 will eliminate dependence on surface states for supplying charge to the channel 1422 as well as the dispersion and poor reliability and reproducibility of processing that plague CAVETs with undoped barriers. Like in the case of the HEMT, the main advantage of Ge instead of Si in the n-doped layer 1414 is that a higher concentration of Ge can be supported in the layer without adverse strain effects or morphological breakdown. Therefore, the doped layer 1414 can be separated by a greater distance from the channel 1422, causing less ionized impurity scattering and leading to a higher mobility.

Like in the HEMT, an AlN spacer layer can be optionally added at the barrier/channel interface of the CAVET 1400 in order to better confine charges in the 2DEG channel 1422 as well as reduce ionized impurity scattering in the channel 1422, and should be between 0.5 and 2 nm thick.

The CBLs 1408 are a fundamental part of the CAVET structure 1400. They can be made from any layer that will block vertical current flow, such as a buried dielectric layer, a buried p-GaN layer, or a buried AlGaN layer. The remaining structure must be regrown on top of the buried layer after patterning and etching an opening for the aperture 1406.

Ge doping can also be incorporated into the back contact n^+-GaN layer 1402 of the CAVET 1400 shown in FIG. 14. Since the CAVET 1400 is a vertical device, it must have a highly n-doped layer 1402 beneath the aperture 1406 and the channel 1422. The more highly this layer 1402 can be doped, the lower the contact resistance between the layer 1402 and the drain 1420 metal. The main advantage of Ge instead of Si in the n-doped layer 1402 is that a higher concentration of Ge can be supported in the n^+-GaN layer 1402 without adverse strain effects or morphological breakdown. The strain state of the layers above the n^+-GaN layer 1402 is important for device performance and high quality epitaxial growth. With Ge, this layer 1420 can be doped between 5E18 cm^{-3} and 1E20 cm^{-3}.

Ge doping can also be incorporated into the sub-collector of an HBT 800, shown in FIG. 8. Since an HBT is a vertical device, it must have a highly n-doped layer below the collector. The more highly this layer can be doped, the lower the contact resistance between the layer and the collector contact. The main advantage of Ge instead of Si in the sub-collector is that a higher concentration of Ge can be supported without adverse strain effects or morphological breakdown. The strain state of the layers above the sub-collector is important for device performance and high quality epitaxial growth. With Ge, this layer can be doped between 5E18 cm^{-3} and 1E20 cm^{-3}.

Ge doping can also be incorporated into the GaN channel region of a MESFET 9000, shown in FIG. 9. The channel is this device is doped lightly n-type. It is desirable to maximize the mobility in the channel while maintaining a low turn-on voltage. The advantage of doping with Ge instead of Si in the GaN channel region is that for the same doping level, and hence the same turn-on voltage, the mobility should be higher, as we have seen from comparing mobility values for GaN:Ge from FIG. 11 to known mobility values for GaN:Si. Ge doping in the channel should be in the range from 1E16 cm^{-3} and 1E18 cm^{-3}.

Typical material growth methods for the GaN devices include but are not limited to MOCVD and MBE. Additionally, certain device structure improvements that benefit all embodiments are described. These can be applied to each of the embodiments, either together or one at a time. In some embodiments, the devices are passivated by a suitable dielectric, such as SiN. Passivation by SiN or a suitable dielectric can minimize the effect of trapped charge and ensure good device operation. In some embodiments, field plating by single or multiple field plates is included, which increase the breakdown voltage of the device and further minimizes the impact of trapping by reducing the peak electric field near the gate. Field plates (either separate or in conjunction with forming the gate layer) can be used for obtaining high breakdown voltages. In particular, slant field plates can maximize the benefits of the field plates. In some embodiments, a gate insulator is under the gate. The insulator reduces or eliminates the gate leakage current.

The above section described a structure for Ge doping the AlGaN barrier of a HEMT or CAVET oriented in the [0001] growth direction in order to supply carriers to the 2DEG channel with minimal scattering and an improvement in dispersion. The scope of this invention also covers devices in the N-face (000-1) orientation when the AlGaN back barrier lies underneath the GaN channel and the GaN:Ge sheet doping layer is located between the AlGaN back barrier and the GaN buffer. Heavy n-type doping above 1E13 cm^{-2} in this layer prevents the formation of a 2-dimentional hole gas at the back barrier/buffer interface, which would act as a parasitic channel. The

use of Ge as an n-type dopant is advantageous compared to Si because a higher concentration of Ge can be supported without adverse strain effects or morphological breakdown. The strain state of the layers above the sub-collector is important for device performance and high quality epitaxial growth.

The scope of this invention also covers devices with non-polar or semipolar orientations of GaN. Nonpolar planes include the {11-20} planes, known collectively as a-planes, and the {10-10} planes, known collectively as m-planes. Such planes contain equal numbers of gallium and nitrogen atoms per plane and are charge-neutral. The term "semipolar plane" can be used to refer to any plane that cannot be classified as c-plane, a-plane, or m-plane. In crystallographic terms, a semipolar plane would be any plane that has at least two nonzero h, i, or k Miller indices and a nonzero l Miller index.

The scope of this invention also covers III-nitride devices with doping profiles other than the profile cited in the technical description. The Ge doped layer in the barrier of a HEMT or CAVET can be of any reasonable thickness, from a delta-doped layer to several tens of nanometers. The Ge doped layer can be offset from the channel by any reasonable distance, up to several tens of nanometers and at a minimum 1 nm. An ideal position of the GaN:Ge can be found in the barrier region that maximizes the charge in the channel and the mobility of the channel. Doping in the GaN:Ge layer can be graded. There can be multiple GaN:Ge layers in the barrier region.

Additional impurities or dopants can also be incorporated into the c-plane III-nitride thin films described in this invention. For example, Fe, Mg, Si, Ge, and Zn are frequently added to various layers in III-nitride heterostructures to alter the conduction properties of those and adjacent layers. The use of such dopants and others not listed here are within the scope of the invention.

Moreover, substrates other than free-standing c-plane GaN could be used for III-nitride thin film growth. The scope of this invention includes the growth of III-nitride thin films on all possible crystallographic orientations of all possible foreign

substrates. These foreign substrates include, but are not limited to, sapphire, silicon carbide, silicon, zinc oxide, boron nitride, lithium aluminate, lithium niobate, germanium, aluminum nitride, lithium gallate, partially substituted spinels, and quaternary tetragonal oxides sharing the γ-$LiAlO_2$ structure.

Furthermore, variations in c-plane III-nitride nucleation (or buffer) layers and nucleation layer growth methods are acceptable for the practice of this invention. The growth temperature, growth pressure, orientation, and composition of the nucleation layers need not match the growth temperature, growth pressure, orientation, and composition of the subsequent thin films and heterostructures. The scope of this invention includes the growth of c-plane III-nitride thin films on all possible substrates using all possible nucleation layers and nucleation layer growth methods.

The scope of this invention also covers c-plane III-nitride thin films grown on epitaxial laterally overgrown (ELO) III-nitride templates. The ELO technique is a method of reducing the density of threading dislocations (TD) in subsequent epitaxial layers. Reducing the TD density leads to improvements in device performance. For c-plane III-nitride electronic devices, these improvements include increased channel mobility, increased gain, longer device lifetimes, and reduced gate and substrate leakage.

III. REFERENCES

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IV. NOMENCLATURE

The terms "Group-III nitride" or "III-nitride" or "III-N" or "nitride" as used herein refer to any alloy composition of the (Ga,Al,In,B)N semiconductors having the formula $Ga_wAl_xIn_yB_zN$ where $0 \leq w \leq 1$, $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$, and $w + x + y + z = 1$. These terms as used herein are intended to be broadly construed to include respective nitrides of the single species, Ga, Al, In and B, as well as binary, ternary and quaternary compositions of such Group III metal species. Accordingly, these terms include, but are not limited to, the compounds of AlN, GaN, InN, AlGaN, AlInN, InGaN, and AlGaInN. When two or more of the (Ga, Al, In, B)N component species are present, all possible compositions, including stoichiometric proportions as

well as off-stoichiometric proportions (with respect to the relative mole fractions present of each of the (Ga, Al, In, B)N component species that are present in the composition), can be employed within the broad scope of this invention. Further, compositions and materials within the scope of the invention may further include quantities of dopants and/or other impurity materials and/or other inclusional materials.

This invention also covers the selection of particular crystal orientations, directions, terminations and polarities of Group-III nitrides. When identifying crystal orientations, directions, terminations and polarities using Miller indices, the use of braces, { }, denotes a set of symmetry-equivalent planes, which are represented by the use of parentheses, ( ). The use of brackets, [ ], denotes a direction, while the use of brackets, < >, denotes a set of symmetry-equivalent directions.

Many Group-III nitride devices are grown along a polar orientation, namely a c-plane {0001} of the crystal, although this results in an undesirable quantum-confined Stark effect (QCSE), due to the existence of strong piezoelectric and spontaneous polarizations. One approach to decreasing polarization effects in Group-III nitride devices is to grow the devices along nonpolar or semipolar orientations of the crystal.

The term "nonpolar" includes the {11-20} planes, known collectively as *a*-planes, and the {10-10} planes, known collectively as *m*-planes. Such planes contain equal numbers of Group-III and Nitrogen atoms per plane and are charge-neutral. Subsequent nonpolar layers are equivalent to one another, so the bulk crystal will not be polarized along the growth direction.

The term "semipolar" can be used to refer to any plane that cannot be classified as *c*-plane, *a*-plane, or *m*-plane. In crystallographic terms, a semipolar plane would be any plane that has at least two nonzero h, i, or k Miller indices and a nonzero l Miller index. Subsequent semipolar layers are equivalent to one another, so the crystal will have reduced polarization along the growth direction.

V. CONCLUSION

This concludes the description of the preferred embodiment of the present invention. The foregoing description of one or more embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A III-nitride semiconductor device, comprising

a plurality of III-nitride layers;

wherein one or more of the III-nitride layers are doped layers; and

wherein one or more of the doped layers have a dopant concentration of at least about 1E19 cm^{-3}.

2. The device of claim 1, wherein the dopant is Germanium, Silicon or Magnesium.

3. An opto-electronic device, comprising:

a c-plane III-nitride light-emitting device comprised of a plurality of III-nitride layers,

the III-nitride layers including one or more light-emitting or light-absorbing layers and one or more doped layers, and

one or more of the doped layers having a dopant concentration of about 4E19 cm^{-3} to about 1E20 cm^{-3}, such that a built-in field due to a p-n or n-p junction in the light-emitting or light-absorbing layers screens a fixed polarization charge at a heterointerface of the light-emitting or light-absorbing layers, resulting in a polarization-induced electric field that is substantially zero.

4. The device of claim 3, wherein one or more of the doped layers are adjacent to the light-emitting or light-absorbing layers' outermost extents.

5. The device of claim 3, wherein one or more of the doped layers are offset more than 1 nm from the light-emitting or light-absorbing layers' furthest extents.

6. The device of claim 3, wherein one or more of the doped layers are offset by asymmetric distances from the light-emitting or light-absorbing layers.

7. The device of claim 3, wherein one or more of the doped layers on either side of the light-emitting or light-absorbing layers are of asymmetric thickness.

8. The device of claim 3, wherein one or more of the doped layers on either side of the light-emitting or light-absorbing layers are of asymmetric doping.

9. The device of claim 3, wherein one or more of the doped layers on either side of the light-emitting or light-absorbing layers have graded doping profiles.

10. The device of claim 1, wherein the light-emitting or light-absorbing layers comprise one or more quantum wells and one or more of the doped layers are within the quantum wells.

11. A III-nitride semiconductor device, comprising

a plurality of III-nitride layers;

wherein at least one of the III-nitride layers is a doped layer and Germanium is used as an n-type dopant in the doped layer.

12. The device of claim 11, wherein the Germanium has a concentration of about 8E17 cm^{-3} to about 1.3E20 cm^{-3}.

13. The device of claim 11, wherein:

at least two of the III-nitride layers are formed adjacent one another and have different bandgaps that cause polarization; and

the polarization contributes to a conductive two-dimensional electron gas (2DEG) channel near a junction of the at least two of the III-nitride layers and in one

of the at least two of the III-nitride layers with a narrower bandgap that comprises a channel layer.

14. The device of claim 13, wherein the device is a metal-semiconductor field effect transistor (MESFET), the channel layer is one of the doped layers, and the Germanium in the channel layer has a concentration of about 1E16 cm^{-3} to about 1E18 cm^{-3}.

15. The device of claim 11, wherein the device is a high electron mobility transistor (HEMT), and the doped layers include an AlGaN barrier layer.

16. The device of claim 15, wherein at least a portion of the AlGaN barrier layer is delta doped.

17. The device of claim 15, wherein the AlGaN barrier layer is spaced from the channel layer by an AlN and/or AlGaN layer.

18. The device of claim 15, wherein the AlGaN barrier layer is an $Al_xGa_{1-x}N$ barrier layer, a gate contact is recessed within an $Al_yGa_{1-y}N$ cap layer on top of the $Al_xGa_{1-x}N$ barrier layer, and x is not equal to y.

19. The device of claim 18, wherein one of the doped layers is a delta doped layer positioned at an interface between the $Al_yGa_{1-y}N$ cap layer and the $Al_xGa_{1-x}N$ barrier layer.

20. The device of claim 11, wherein the device is a current aperture vertical electron transistor (CAVET), one or more of the doped layers is in contact with a drain electrode, and the Germanium in the one or more of the doped layers in

contact with the drain electrode has a concentration of about 5E18 cm^{-3} to about 1E20 cm^{-3}.

21. The device of claim 11, wherein the device is a heterojunction bipolar transistor (HBT), one or more of the doped layers is a sub-collector, and the Germanium in the one or more of the doped layers that is the sub-collector has a concentration of about 5E18 cm^{-3} to about 1E20 cm^{-3}.

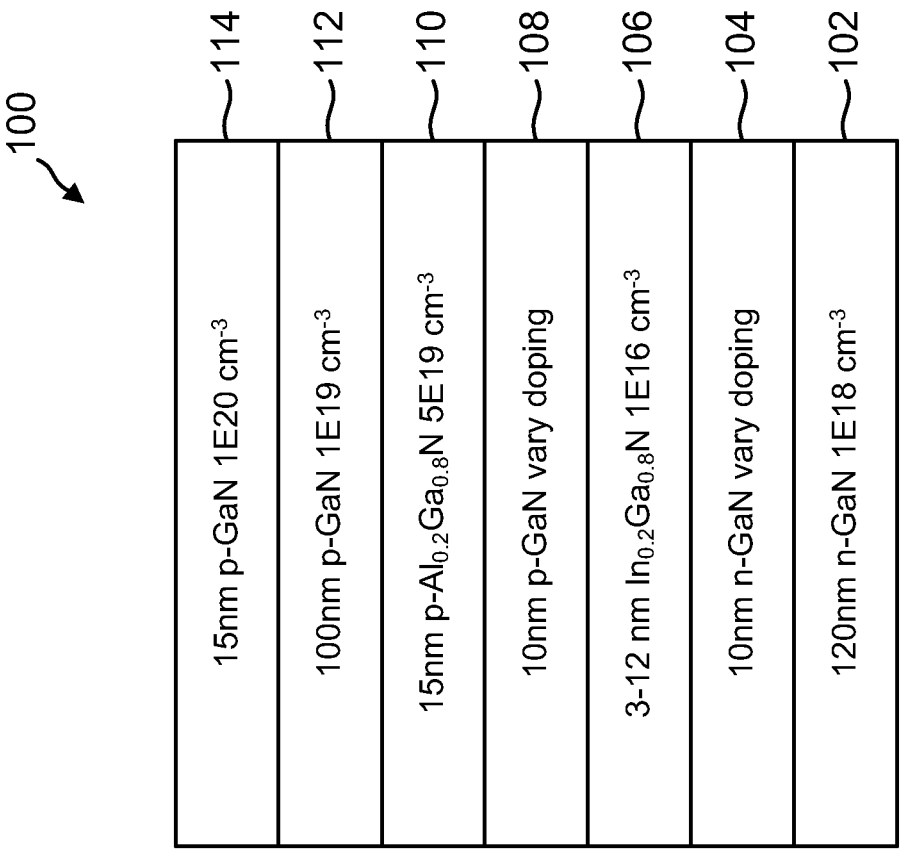
100
114
112
110
108
106
104
102
15nm p-GaN 1E20 cm-3
100nm p-GaN 1E19 cm-3
15nm p-Al0.2Ga0.8N 5E19 cm-3
10nm p-GaN vary doping
3-12 nm In0.2Ga0.8N 1E16 cm-3
10nm n-GaN vary doping
120nm n-GaN 1E18 cm-3

FIG. 1

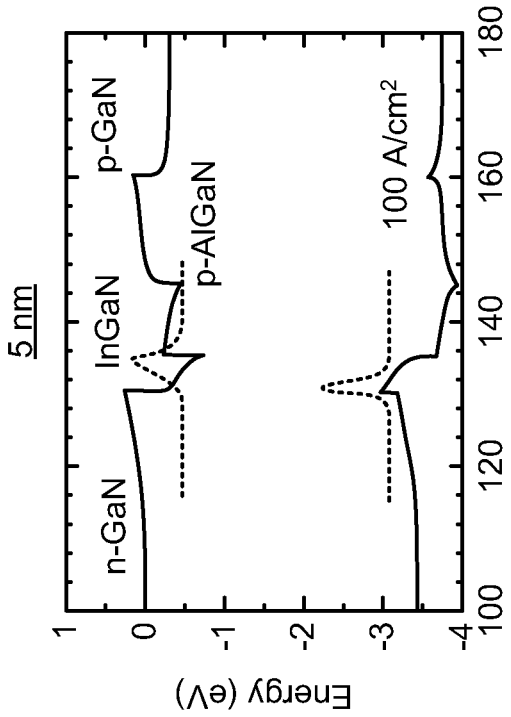

FIG. 2(b)

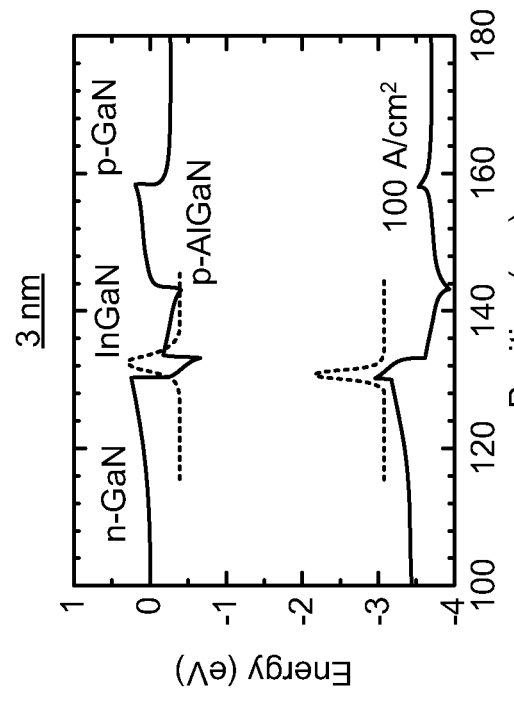

FIG. 2(a)

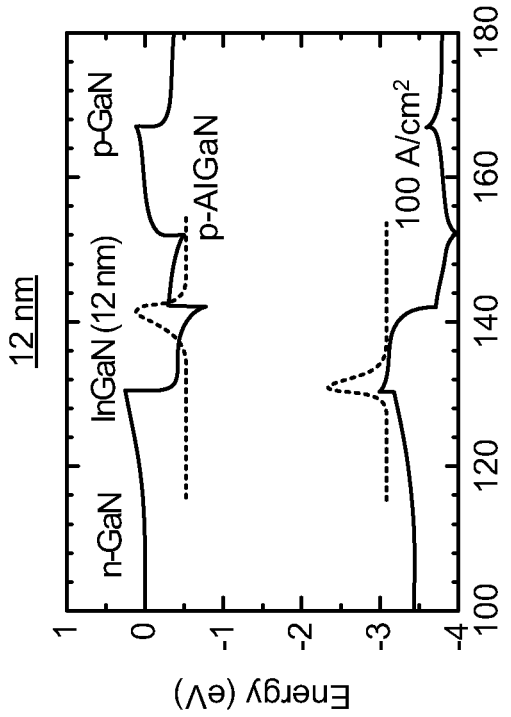

FIG. 2(d)

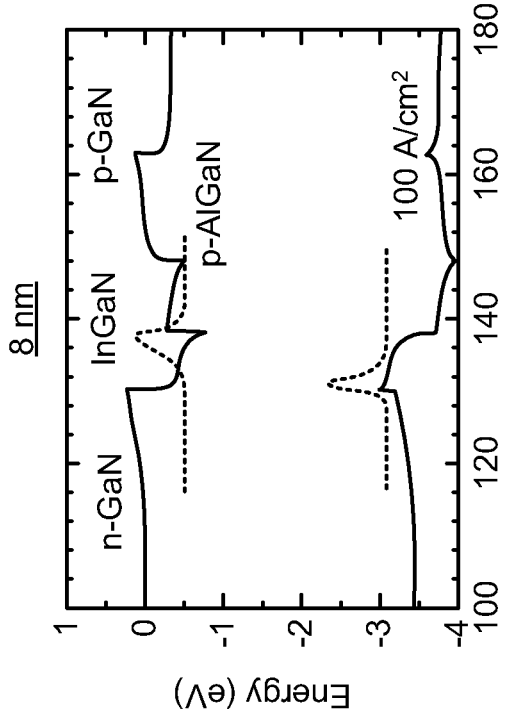

FIG. 2(c)

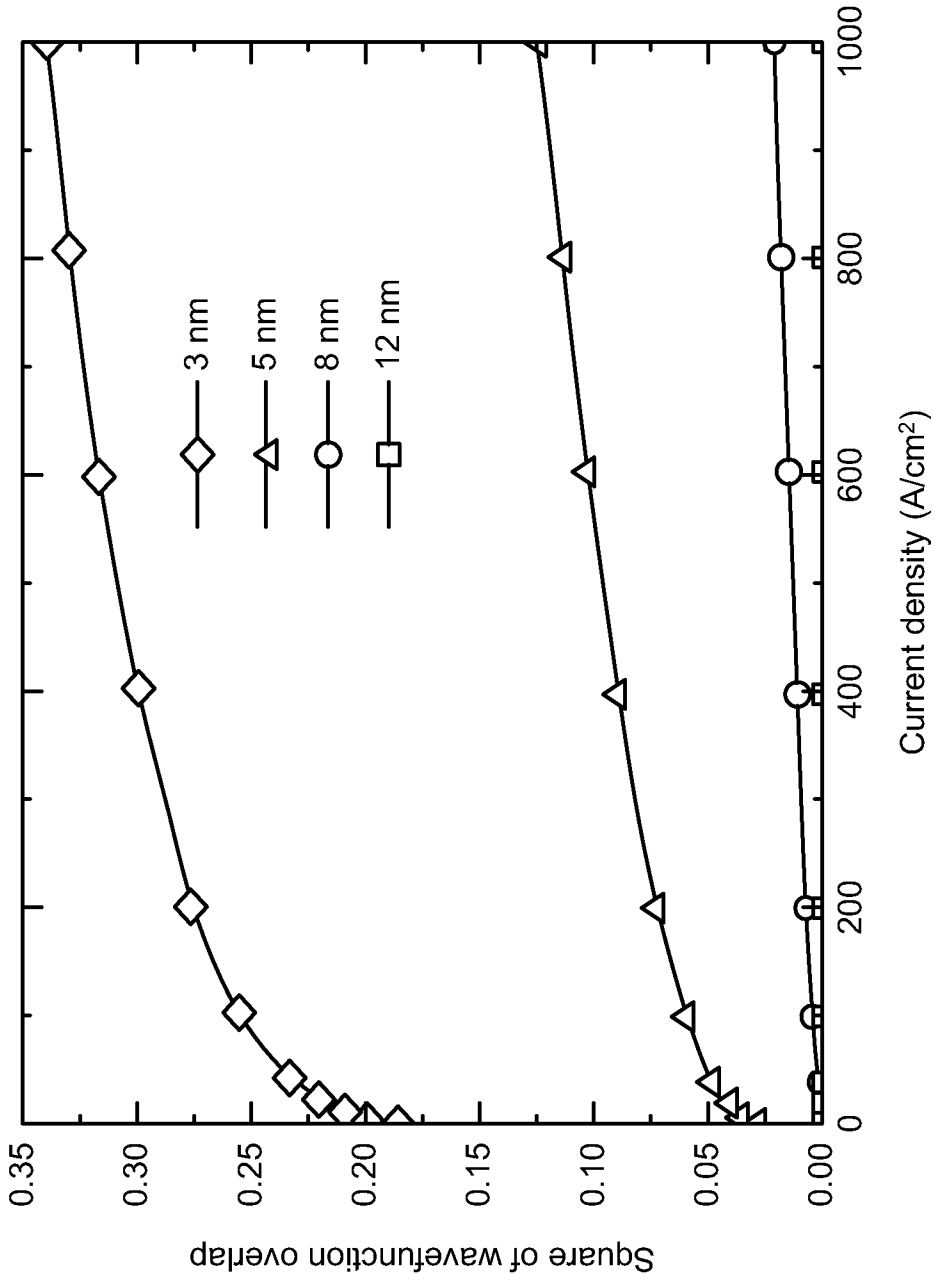
Square of wavefunction overlap
0.00
0.05
0.10
0.15
0.20
0.25
0.30
0.35
0
200
400
600
800
1000
Current density (A/cm2)
3 nm
5 nm
8 nm
12 nm

FIG. 3

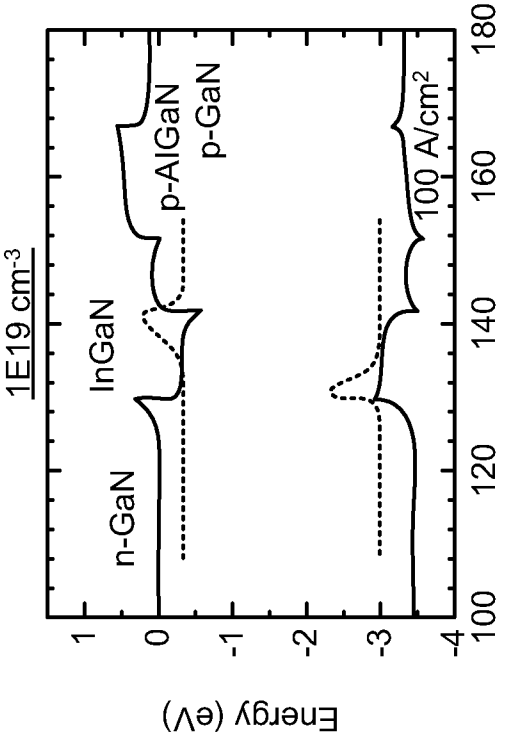

FIG. 4(a)

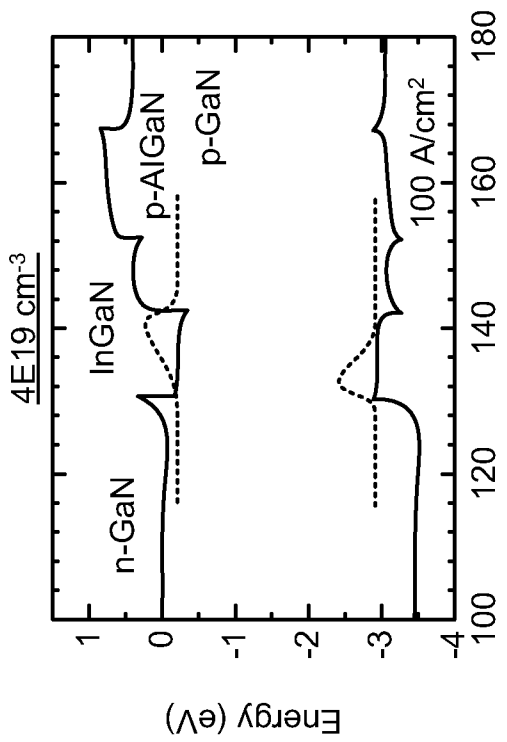

FIG. 4(b)

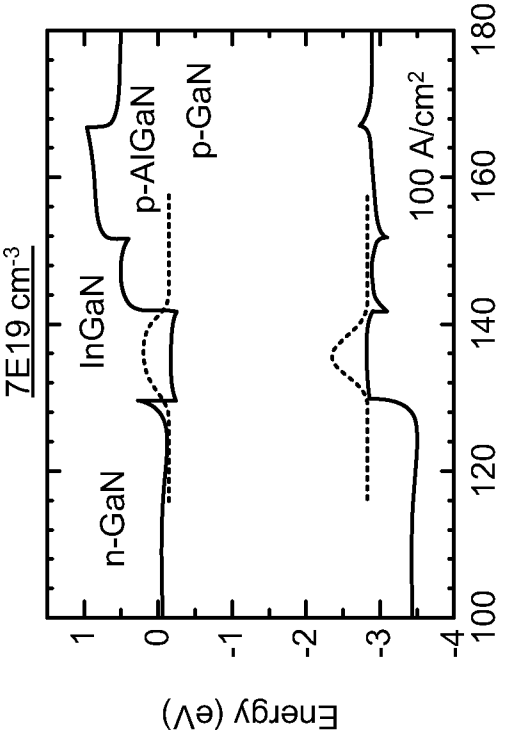

FIG. 4(c)

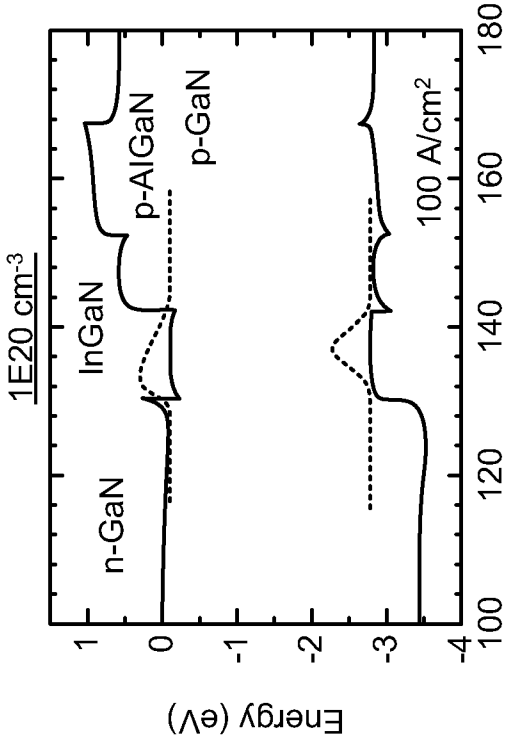

FIG. 4(d)

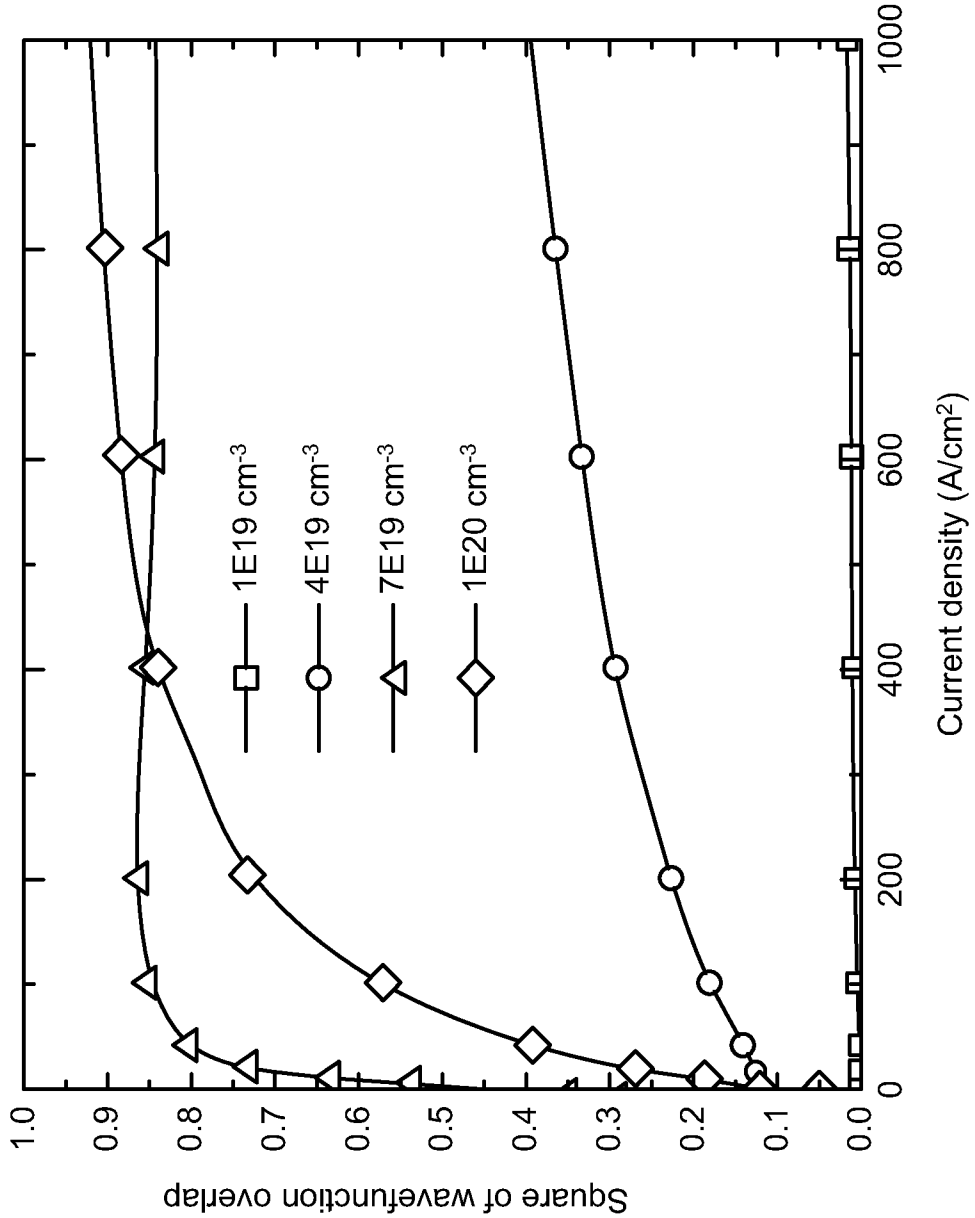
Square of wavefunction overlap
Current density (A/cm^2)
1E19 cm^{-3}
4E19 cm^{-3}
7E19 cm^{-3}
1E20 cm^{-3}
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
0
200
400
600
800
1000

FIG. 5

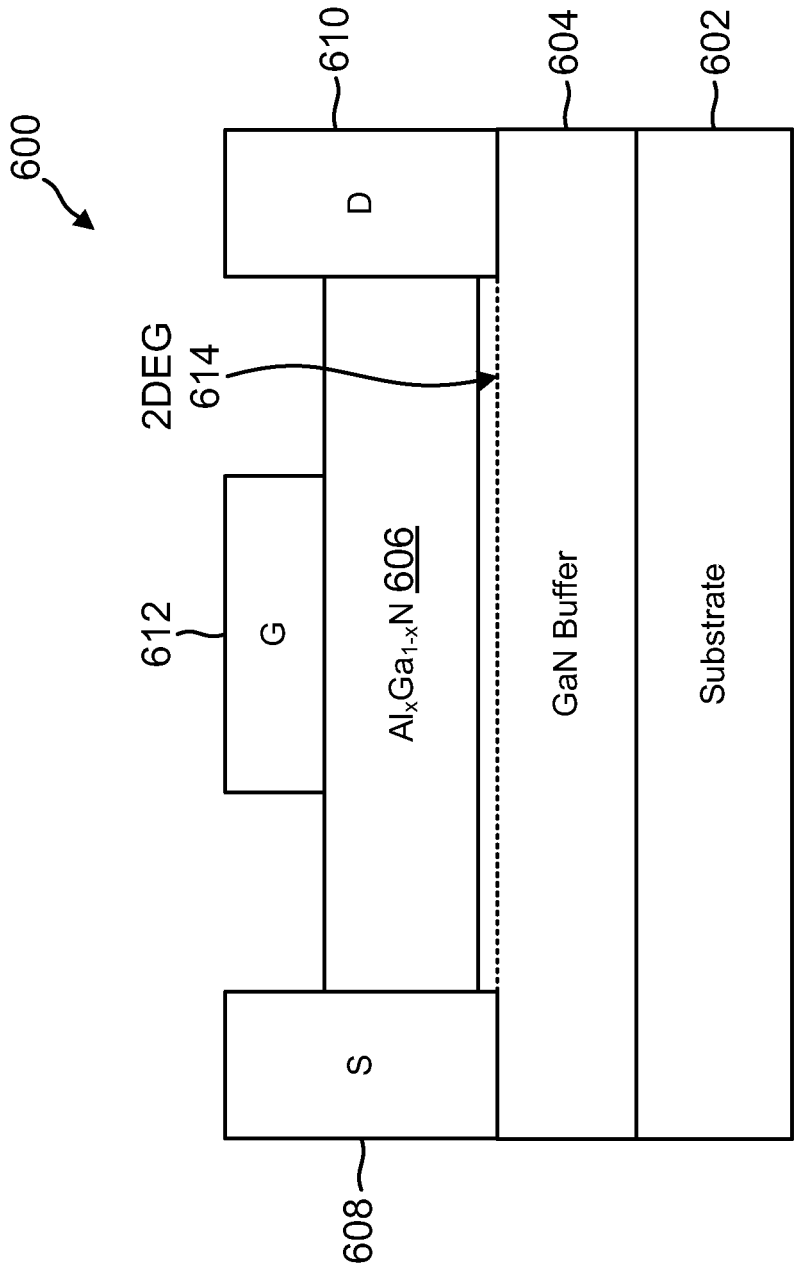
600
610
604
602
D
2DEG
614
612
G
$Al_xGa_{1-x}N$ 606
GaN Buffer
Substrate
S
608

FIG. 6

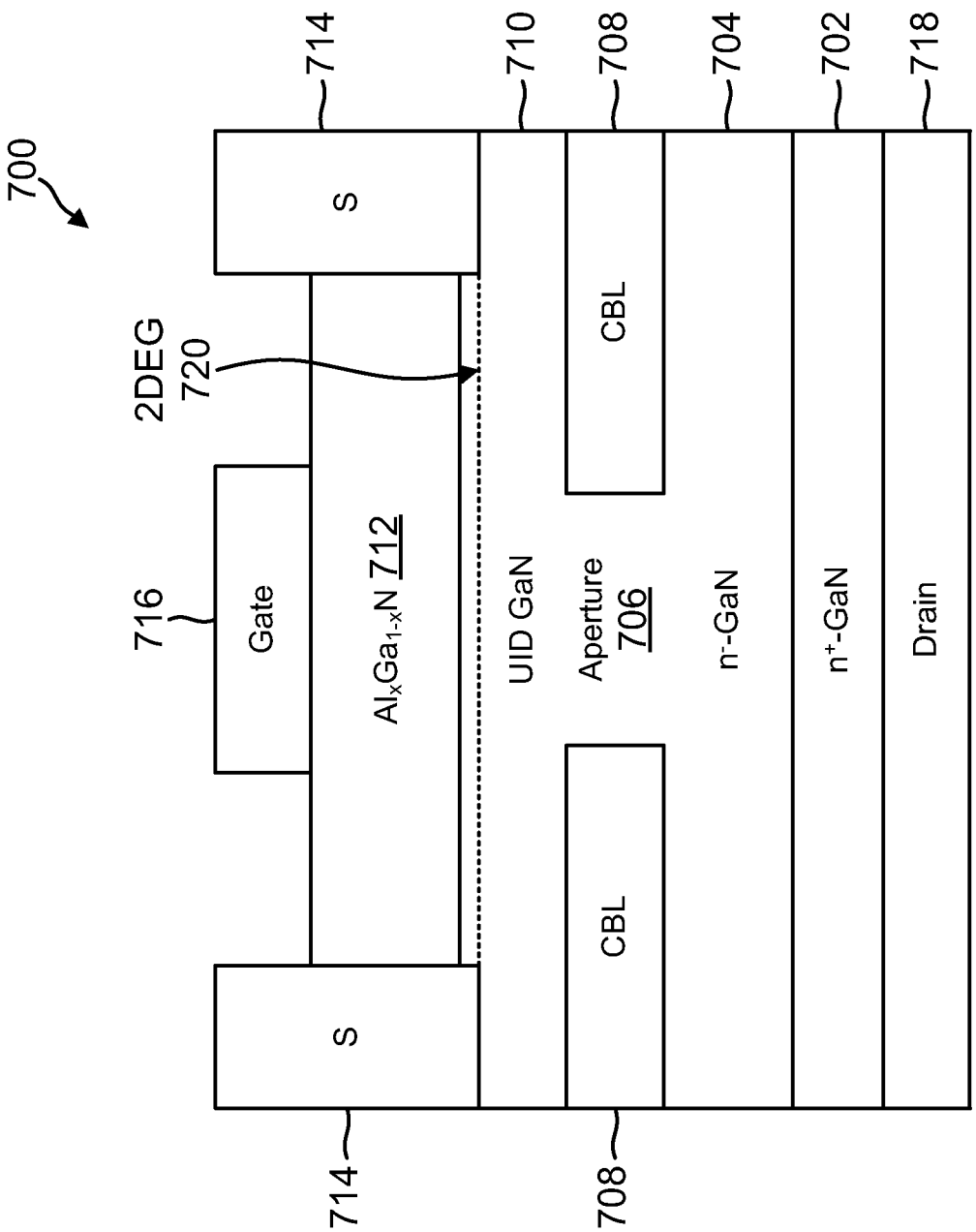
700
714
710
708
704
702
718
S
2DEG
720
CBL
716
Gate
$Al_xGa_{1-x}N$ 712
UID GaN
Aperture
706
n⁻-GaN
n⁺-GaN
Drain
S
CBL
714
708

FIG. 7

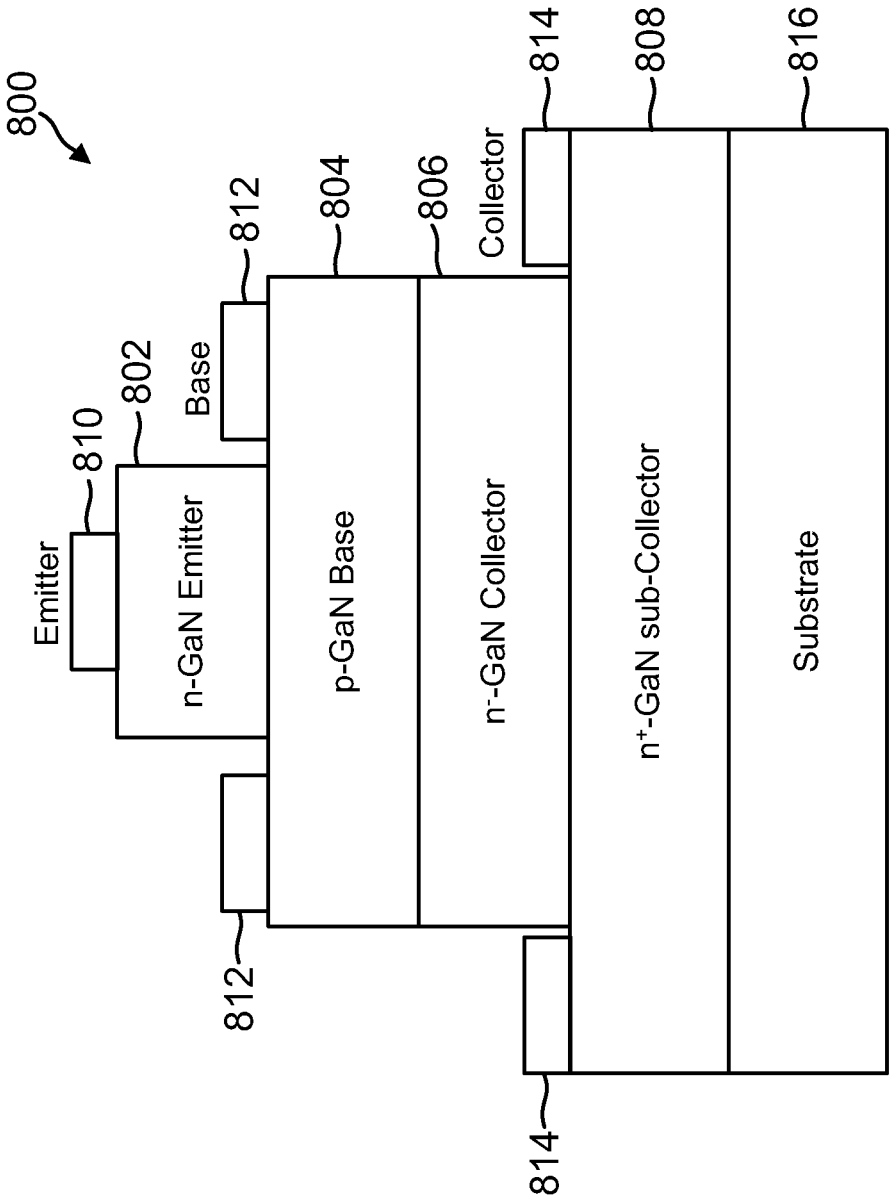
800
814
808
816
Collector
812
804
806
Base
802
810
Emitter
n-GaN Emitter
p-GaN Base
n⁻-GaN Collector
n⁺-GaN sub-Collector
Substrate
812
814

FIG. 8

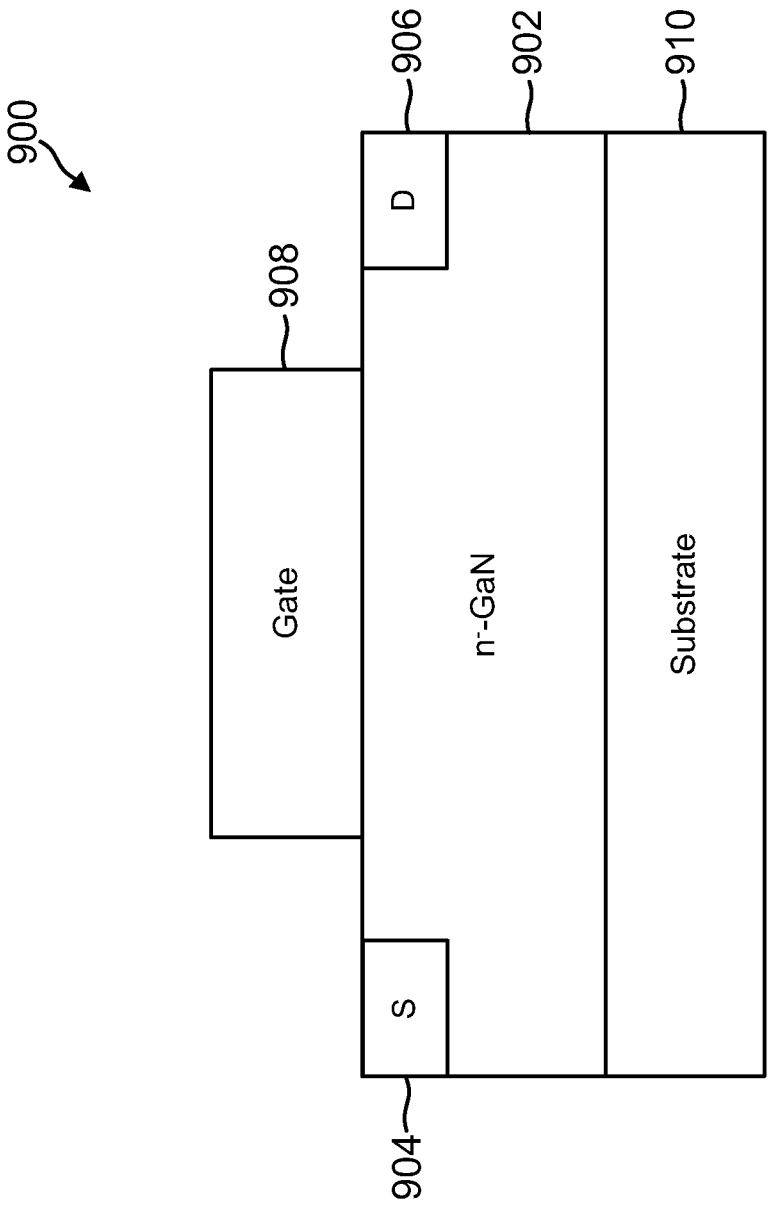

FIG. 9

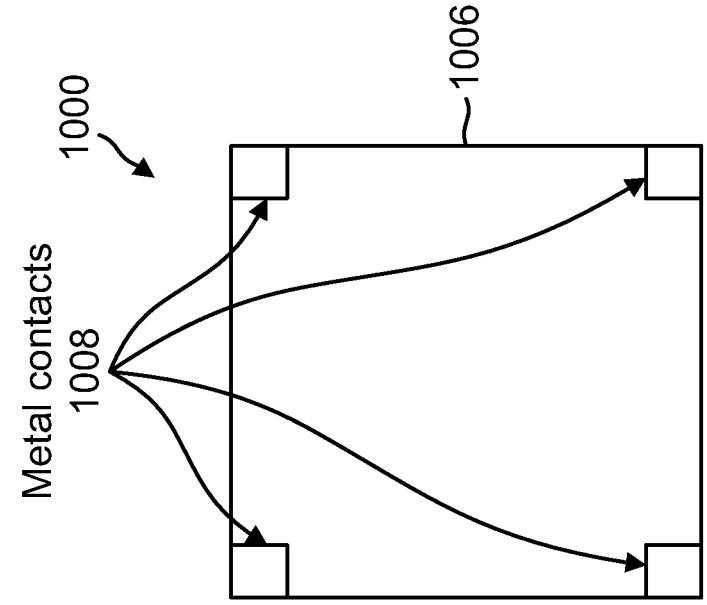

FIG. 10(b)

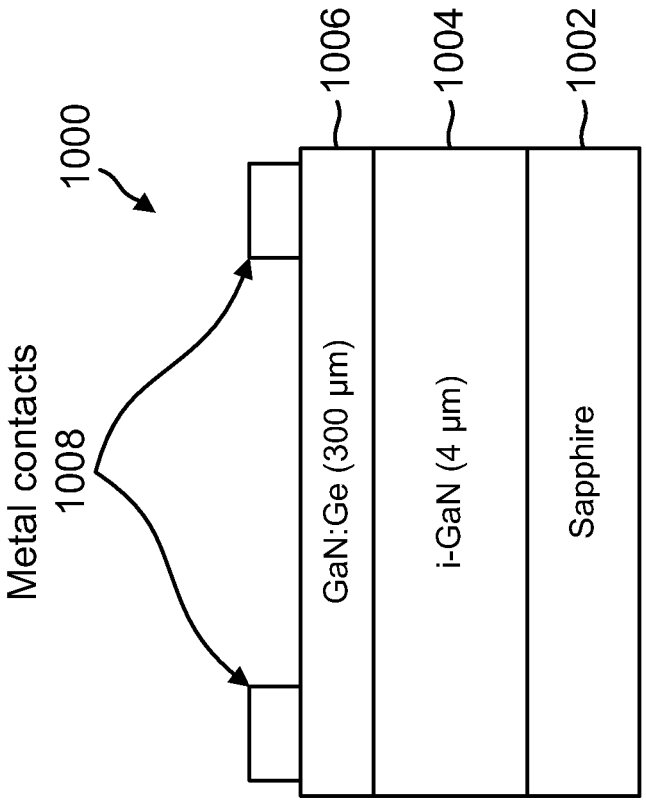

FIG. 10(a)

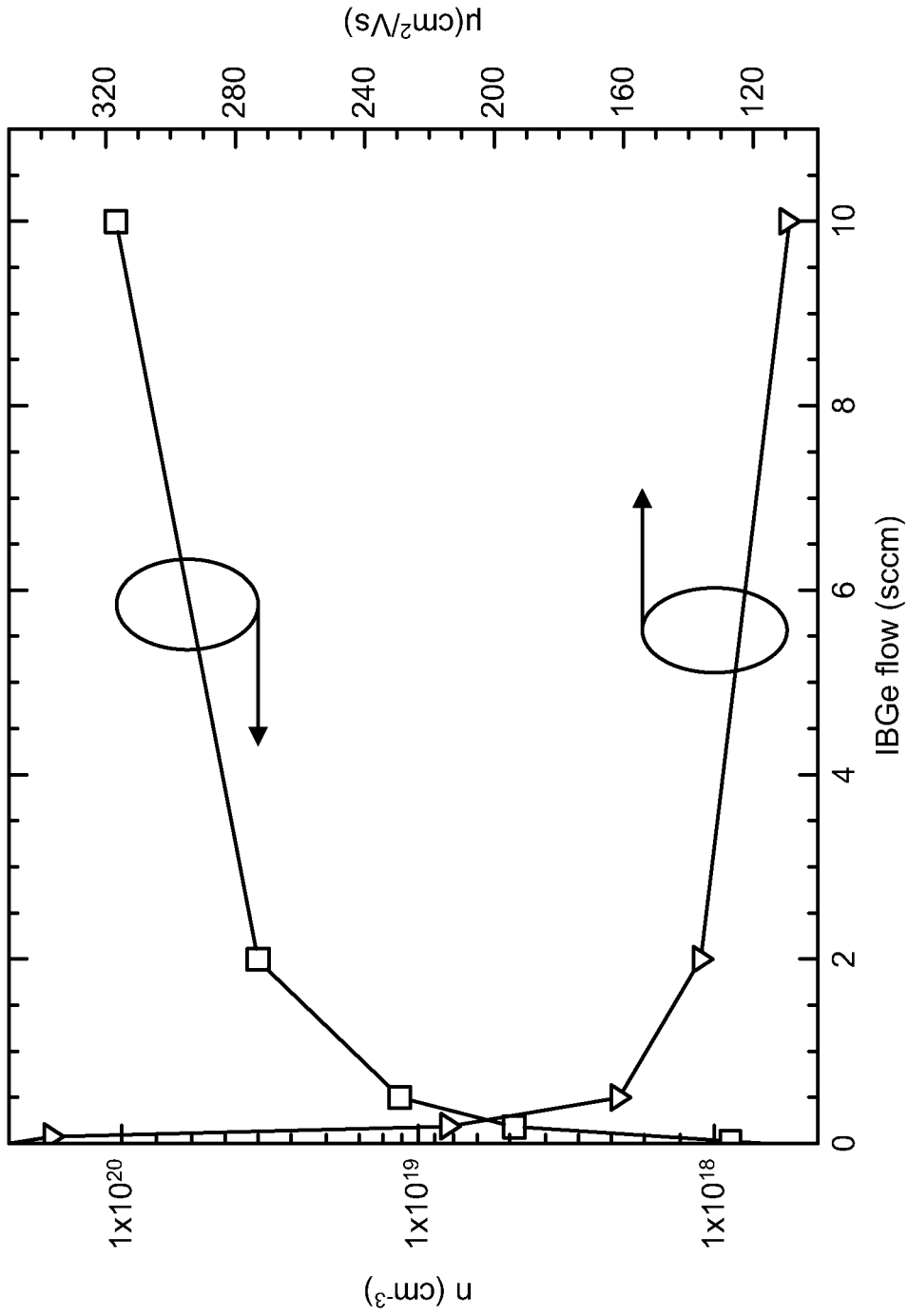
μ(cm²/Vs)
320
280
240
200
160
120
n (cm⁻³)
1x10²⁰
1x10¹⁹
1x10¹⁸
0
2
4
6
8
10
IBGe flow (sccm)

FIG. 11

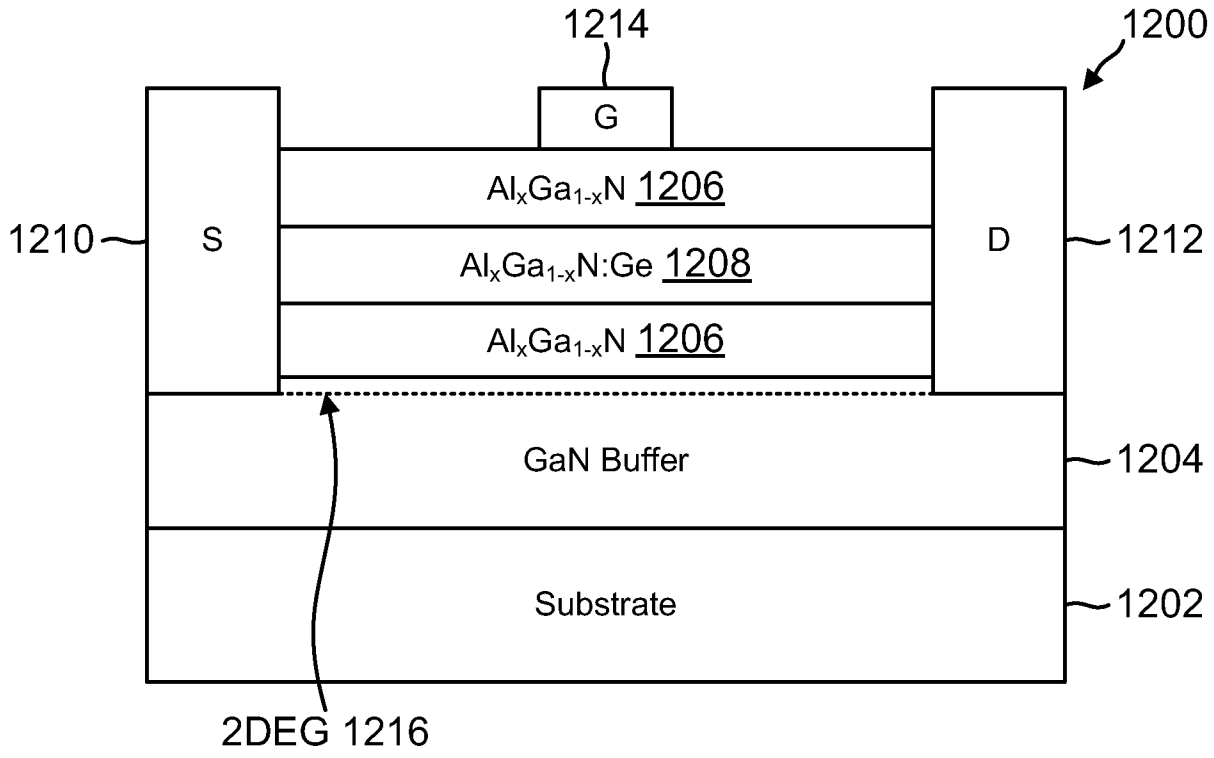

FIG. 12(a)

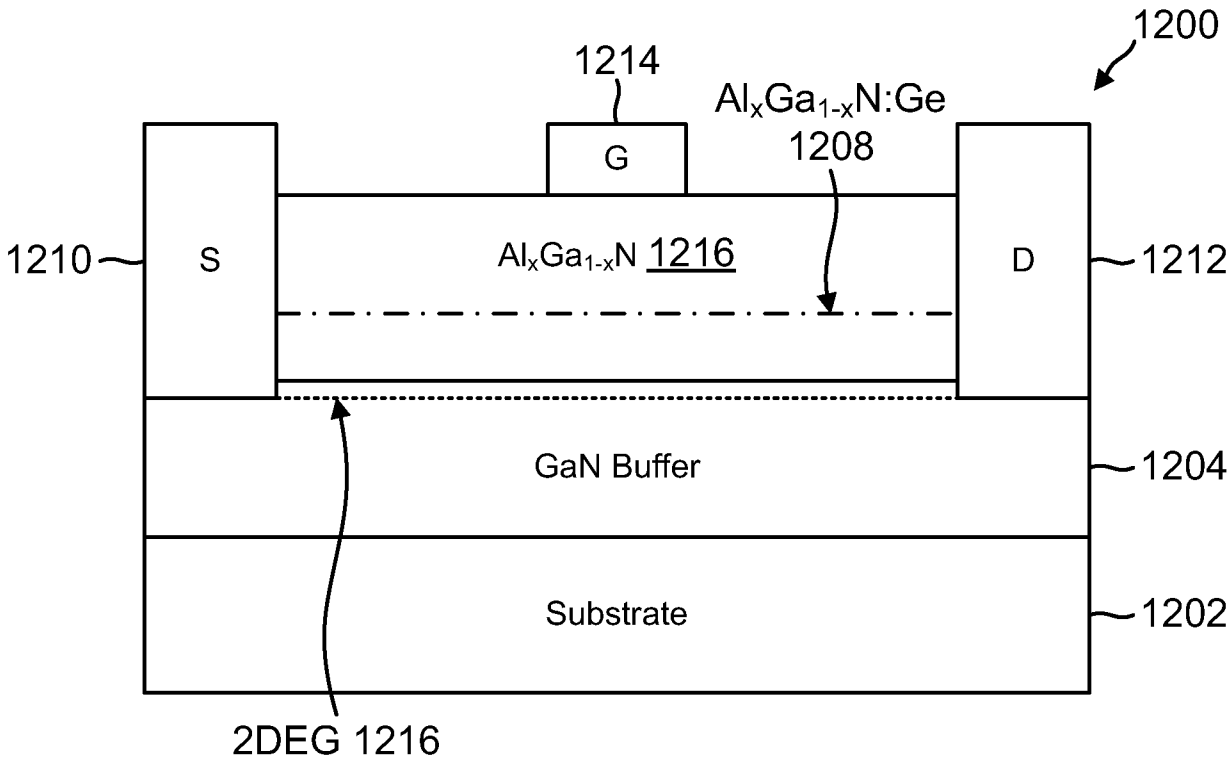

FIG. 12(b)

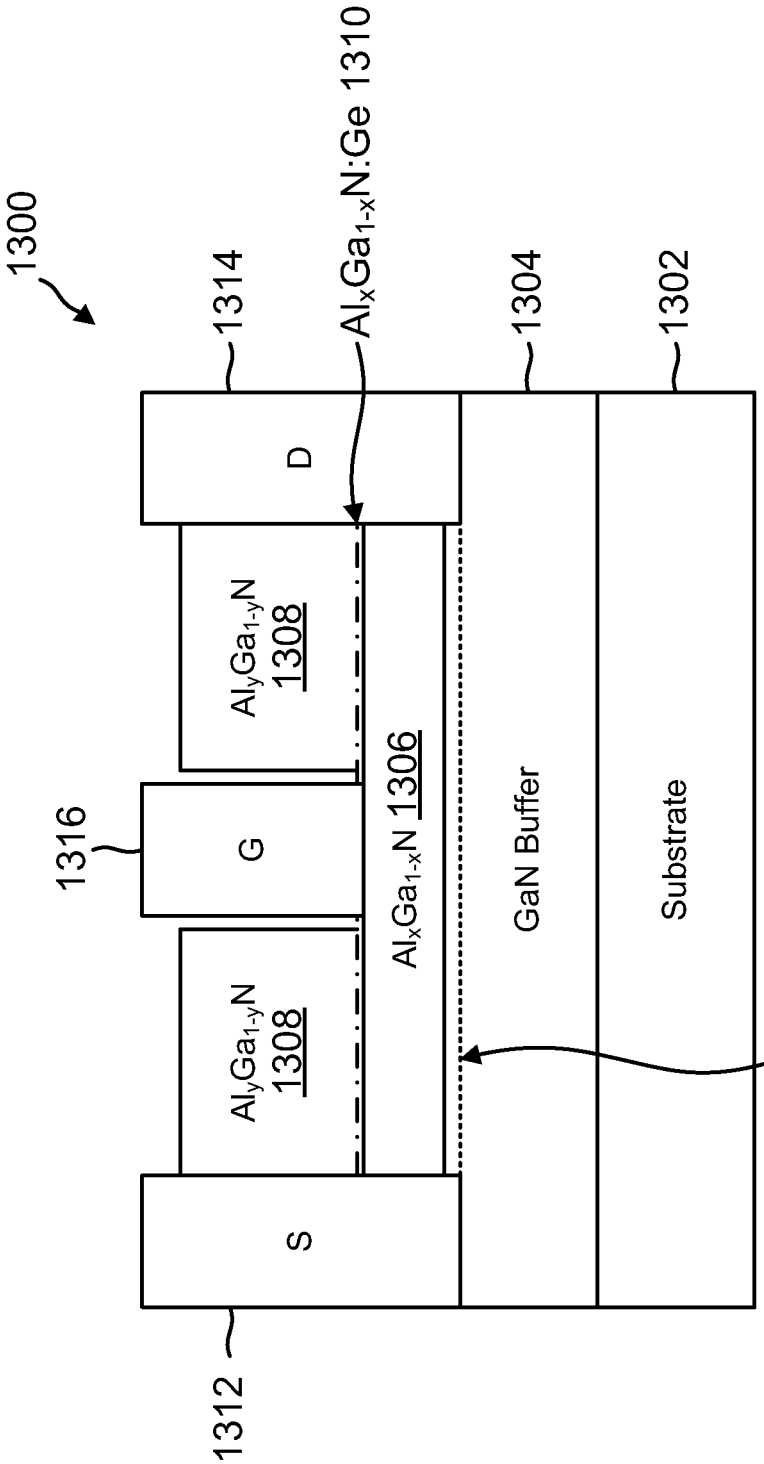
1300
1314
$Al_xGa_{1-x}N$:Ge 1310
1304
1302
D
$Al_yGa_{1-y}N$ 1308
$Al_xGa_{1-x}N$ 1306
1316
G
$Al_yGa_{1-y}N$ 1308
GaN Buffer
Substrate
S
1312
1318
2DEG

FIG. 13

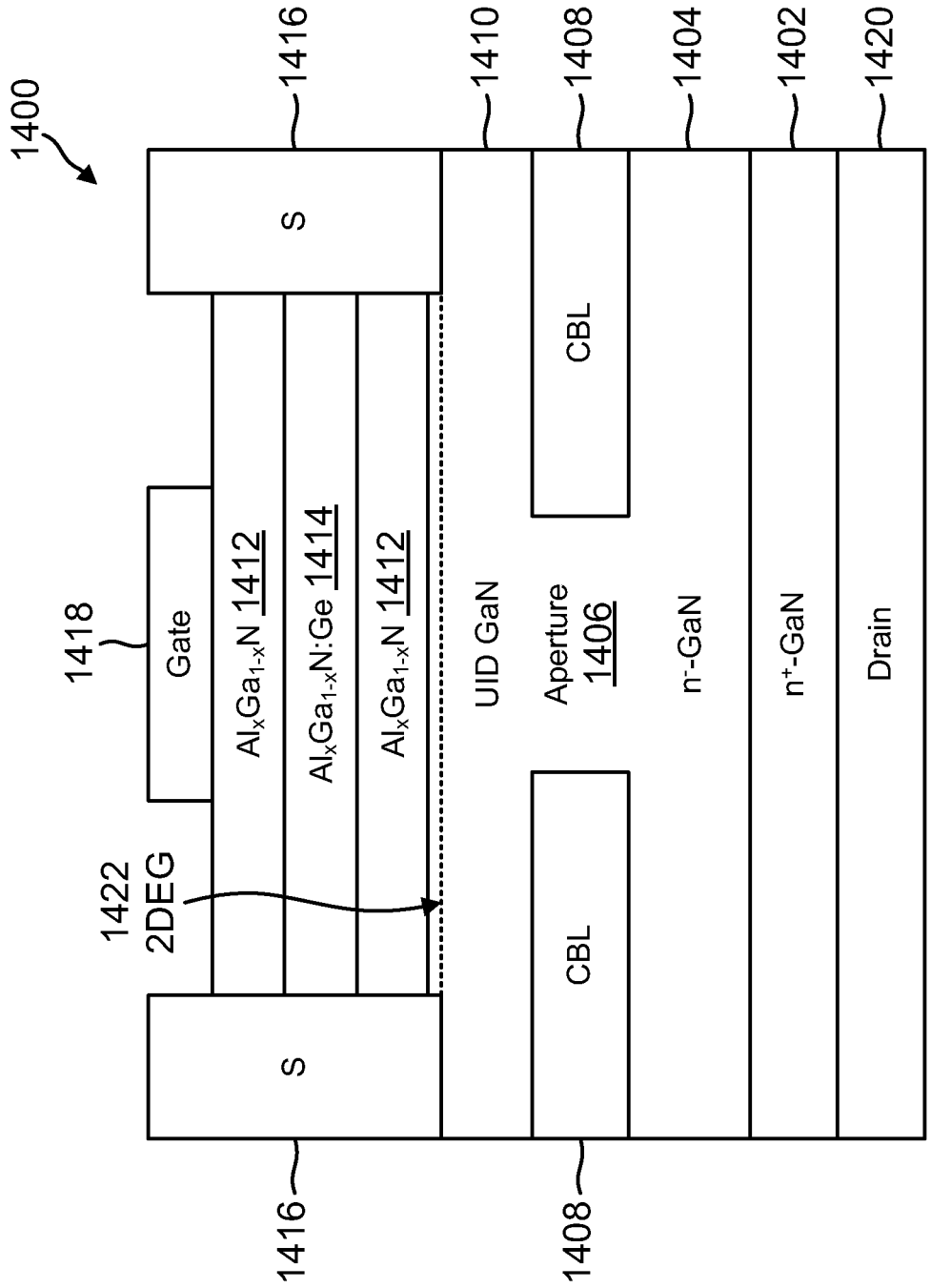
1400
1416
1410
1408
1404
1402
1420
S
CBL
Gate
1418
$Al_xGa_{1-x}N$ 1412
$Al_xGa_{1-x}N$:Ge 1414
$Al_xGa_{1-x}N$ 1412
UID GaN
Aperture 1406
n^--GaN
n^+-GaN
Drain
1422
2DEG
S
CBL
1416
1408

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US15/31190

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/207, 29/36, 29/778 (2015.01)
CPC - H01L 29/2003, 29/207, 29/36
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): H01L 29/15, 29/20, 29/207, 29/36, 29/778, 31/0304, 31/0328, 31/0336, 31/072, 31/109; H01S 5/32, 5/323, 5/34, 5/343 (2015.01);
CPC: H01L 29/15, 29/157, 29/20, 29/2003, 29/207, 29/36, 31/0304, 31/0328, 31/0336, 31/072, 31/109; H01S 5/32, 5/3213, 5/323, 5/34,

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatSeer (US, EP, WO, JP, DE, GB, CN, FR, KR, ES, AU, IN, CA, INPADOC Data); ProQuest (Derwent, INSPEC, NTIS, PASCAL, Current Contents Search, Dissertation Abstracts Online, Inside Conferences); EBSCO Discovery Service; Google Scholar; KEYWORDS: semiconductor, light emit, absorb, germanium, Ge, nitride, dop, quantum, well, asymmetric, thick, 2DEG, HEMT, "(0001)"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0018657 A1 (KOIKE, M et al.) January 29, 2004; abstract; figures 7a nd 8; paragraphs [0014, 0081, 0083]	1, 2, and 10
X --- Y	US 2002/0008245 A1 (GOETZ, W et al.) January 24, 2002; abstract; figure 3; paragraph [0007, 0036, 0039, 0048, 0049]	3 and 4 --- 5-9
Y	US 2005/0031000 A1 (BOTEZ, D) February 10, 2005; figures 1 and 5; paragraphs [0020, 0024, and 0042]	5-9
X --- Y	US 2007/0269968 A1 (SAXLER, A et al.) November 22, 2007; figures 1A-1F; paragraphs [0016, 0035, 0036, 0037, 0052]	11-13, 15, and 18 --- 14, 16, 17, 20, and 21
Y	US 4,636,822 A (CODELLA, C et al.) January 13, 1987; figure 2A; column 5, lines 2-10	14
Y	US 2010/0187570 A1 (SAXLER, A et al.) July 29, 2010; figure 1; paragraph [0081]	16
Y	US 2013/0307027 A1 (LU, J et al.) November 21, 2013; figure 2B; paragraphs [0040 and 0064]	17
Y	US 2008/0029789 A1 (SAXLER, A) February 7, 2008; abstract; figure 2; paragraphs [0034, 0036, 0044]	20

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 August 2015 (03.08.2015)	07 OCT 2015
Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US15/31190

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,767,540 A (SHIMIZU, M) June 16, 1998; abstract; figure 1; column 3, lines 21-29; column 4, lines 15-18 and 24-30	21
A	US 2010/0264461 A1 (RAJAN, S et al.) October 21, 2010; figures 1 and 2; paragraphs [0034 and 0038]	19