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[54] **ELECTRONIC MUSICAL INSTRUMENT KEYING SYSTEM WITH ENVELOPE SAMPLE MEMORIZING VOLTAGE DIVIDERS**

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Nov. 18, 1971 Japan 46-92562

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[51] **Int. Cl.** **G10h 1/02**
[58] **Field of Search** 84/1.01, 1.03, 1.24, 1.26, 84/DIG. 23; 307/251, 263, 264, 279

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Primary Examiner—Richard B. Wilkinson
Assistant Examiner—U. Weldon
Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57] **ABSTRACT**

An electronic musical instrument keying system comprises, for each tone signal to be keyed, a keyer constituted by a plurality of voltage dividers and switching elements, and a keyer drive circuit having an *n*-scale counter and a counter drive pulse generator associated with a key-operated switch. The keyer includes a sequentially changing-over voltage divider network having a common input resistor and a plurality of shunt resistors each with the series-connected switching element, wherein resistance values of the shunt resistors are so selected as to represent the sampled levels of the intended keying envelope for the tone signal, the tone signal being supplied through the input resistor and the output of the keyer being derived from the junction between the input resistor and the shunt resistors. Individual switching elements are sequentially rendered conductive by successive pulses from the counter to successively establish the voltage dividers one after another to determine the tone levels successively, thereby forming an envelope. Key touch-responsive tone level determining circuit constructed by a similar voltage divider network may be used with the keyer to control the input tone signal level to the keyer in response to the depression speed of the key. The keying system eliminates the use of a large capacity of capacitors which are required in RC timing circuits in the conventional system, and facilitates the fabrication in an integrated circuit form by mass production.

17 Claims, 13 Drawing Figures

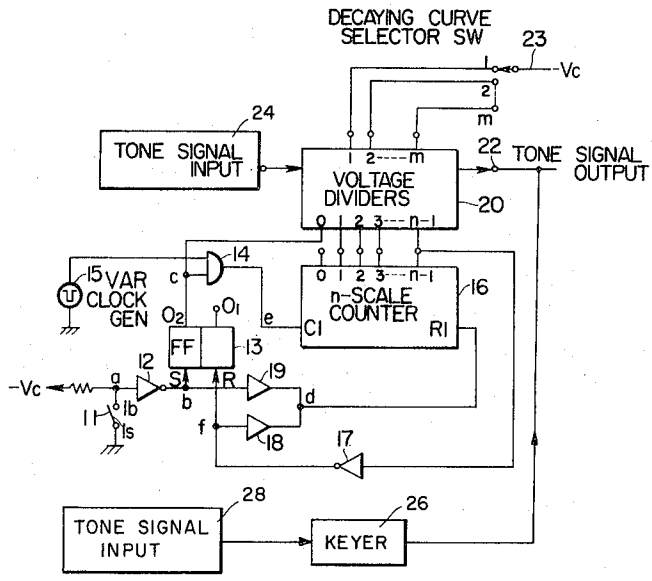


FIG. 1

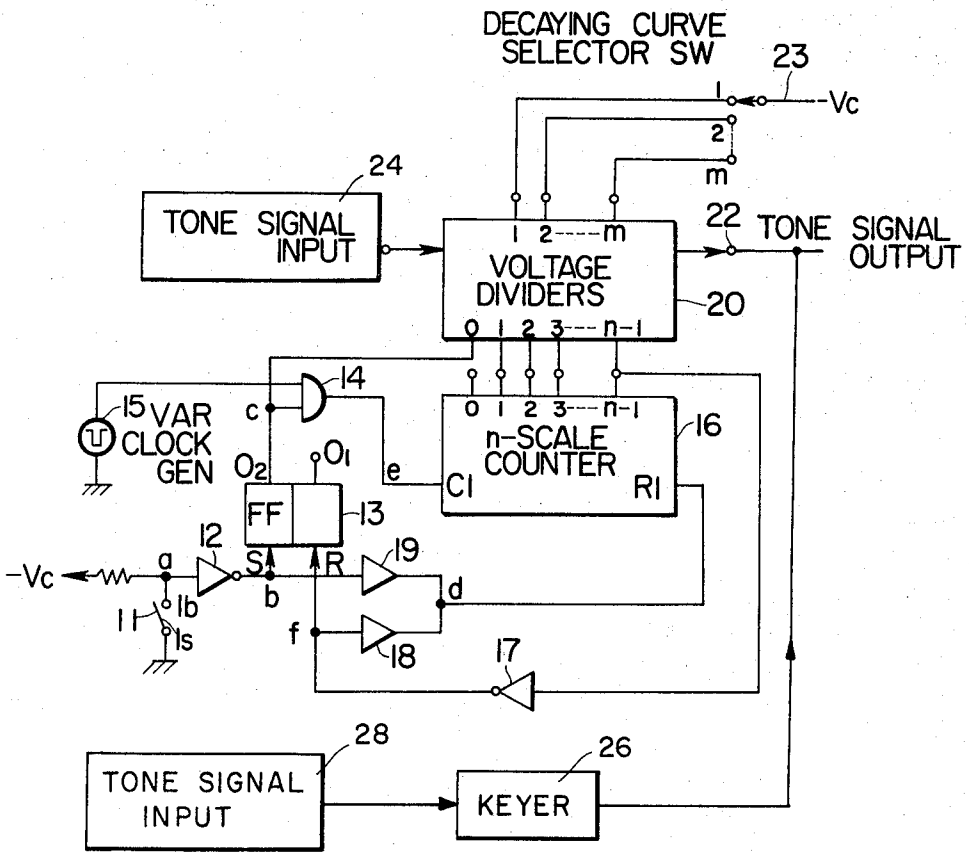

DECAYING CURVE SELECTOR SW
23
Vc
TONE SIGNAL INPUT
24
VOLTAGE DIVIDERS
20
22
TONE SIGNAL OUTPUT
VAR CLOCK GEN
15
14
16
n-SCALE COUNTER
FF
13
12
19
18
17
-Vc
TONE SIGNAL INPUT
28
KEYER
26

FIG. 2

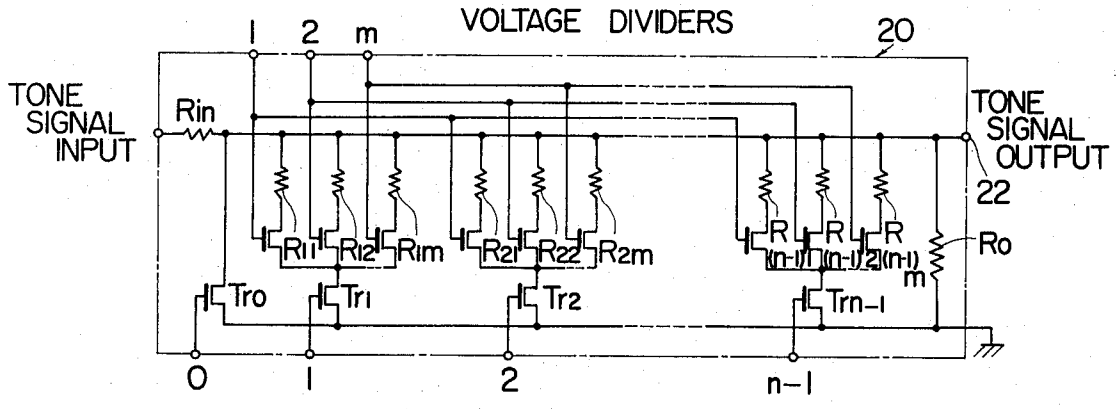

VOLTAGE DIVIDERS
20
TONE SIGNAL INPUT
Rin
TONE SIGNAL OUTPUT
22
Ro
Tro
Tr1
Tr2
Trn-1

FIG. 3

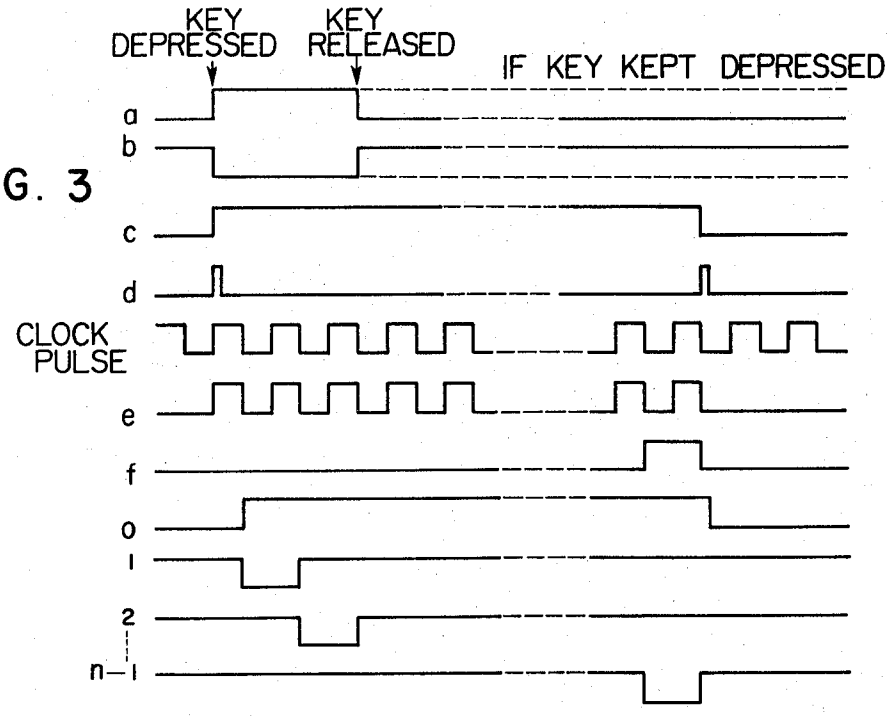

KEY DEPRESSED
KEY RELEASED
IF KEY KEPT DEPRESSED
a
b
c
d
CLOCK PULSE
e
f
o
1
2
n-1

FIG. 5

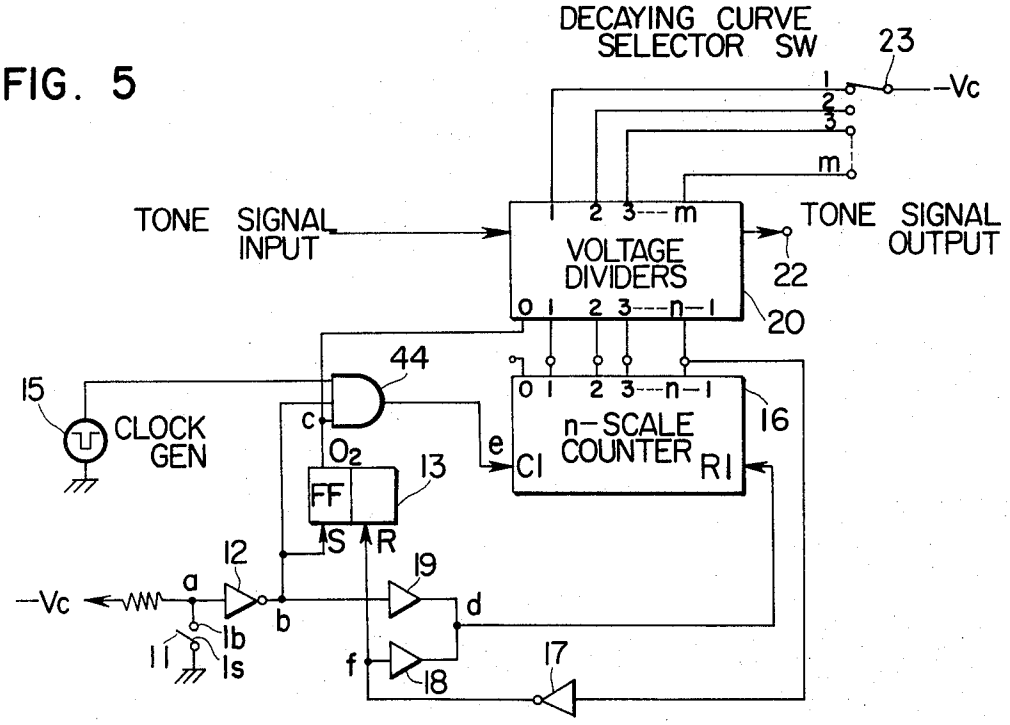

DECAYING CURVE SELECTOR SW
23
-Vc
1
2
3
m
TONE SIGNAL INPUT
1 2 3---m
VOLTAGE DIVIDERS
0 1 2 3---n-1
20
22
TONE SIGNAL OUTPUT
44
15
CLOCK GEN
c
e
O2
FF
13
S
R
0 1 2 3---n-1
n-SCALE COUNTER
16
C1
R1
12
19
-Vc
a
b
d
11
1b
1s
f
18
17

FIG. 4(a)

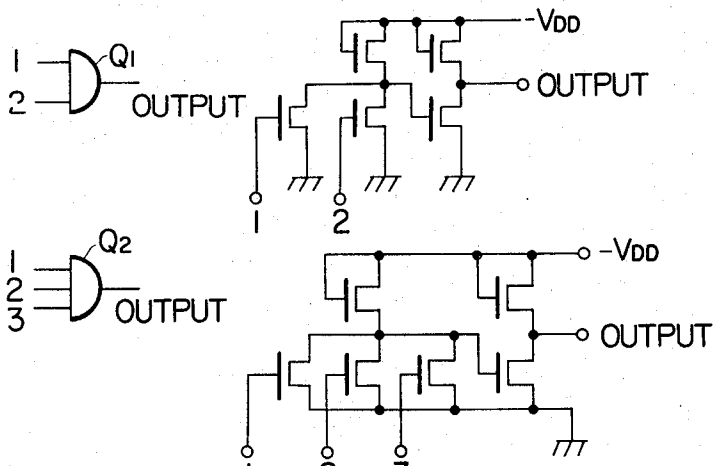


FIG. 4(b)

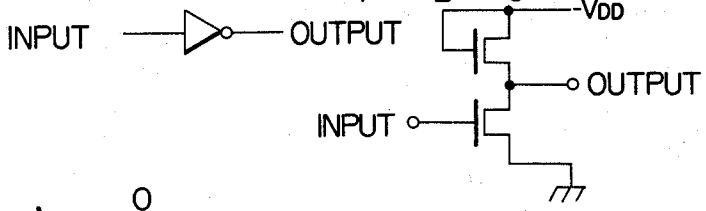


FIG. 4(c)

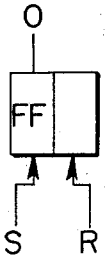
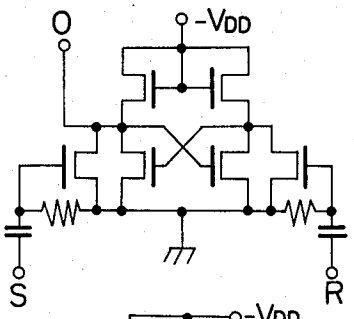


FIG. 4(d)



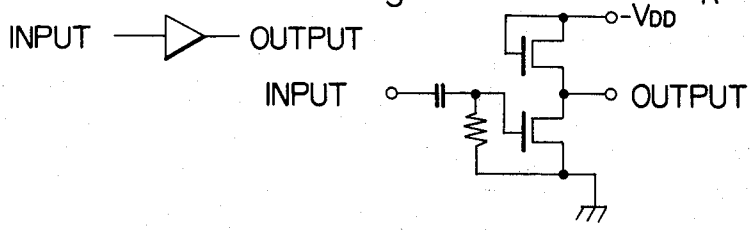


FIG. 6

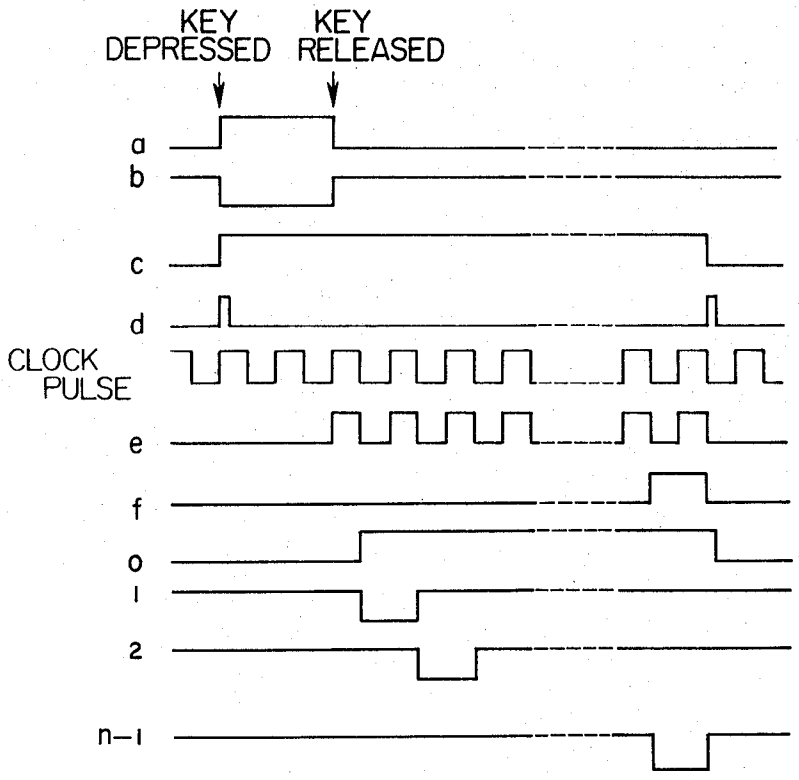

KEY DEPRESSED
KEY RELEASED
a
b
c
d
CLOCK PULSE
e
f
o
1
2
n-1

FIG. 7

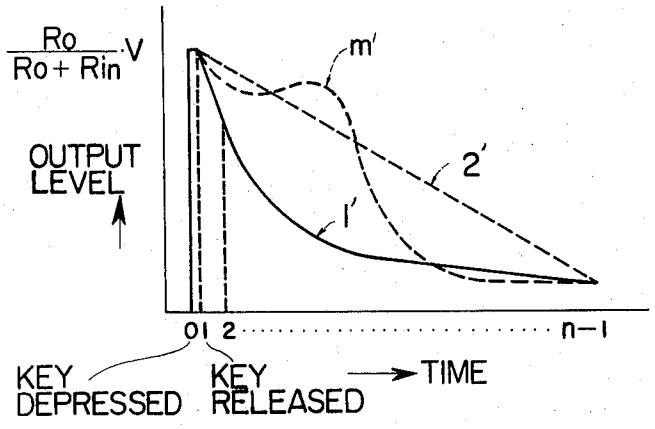

Ro / Ro + Rin · V
OUTPUT LEVEL
m'
2'
1'
0 1 2 ..... n-1
KEY DEPRESSED
KEY RELEASED
TIME

FIG. 8

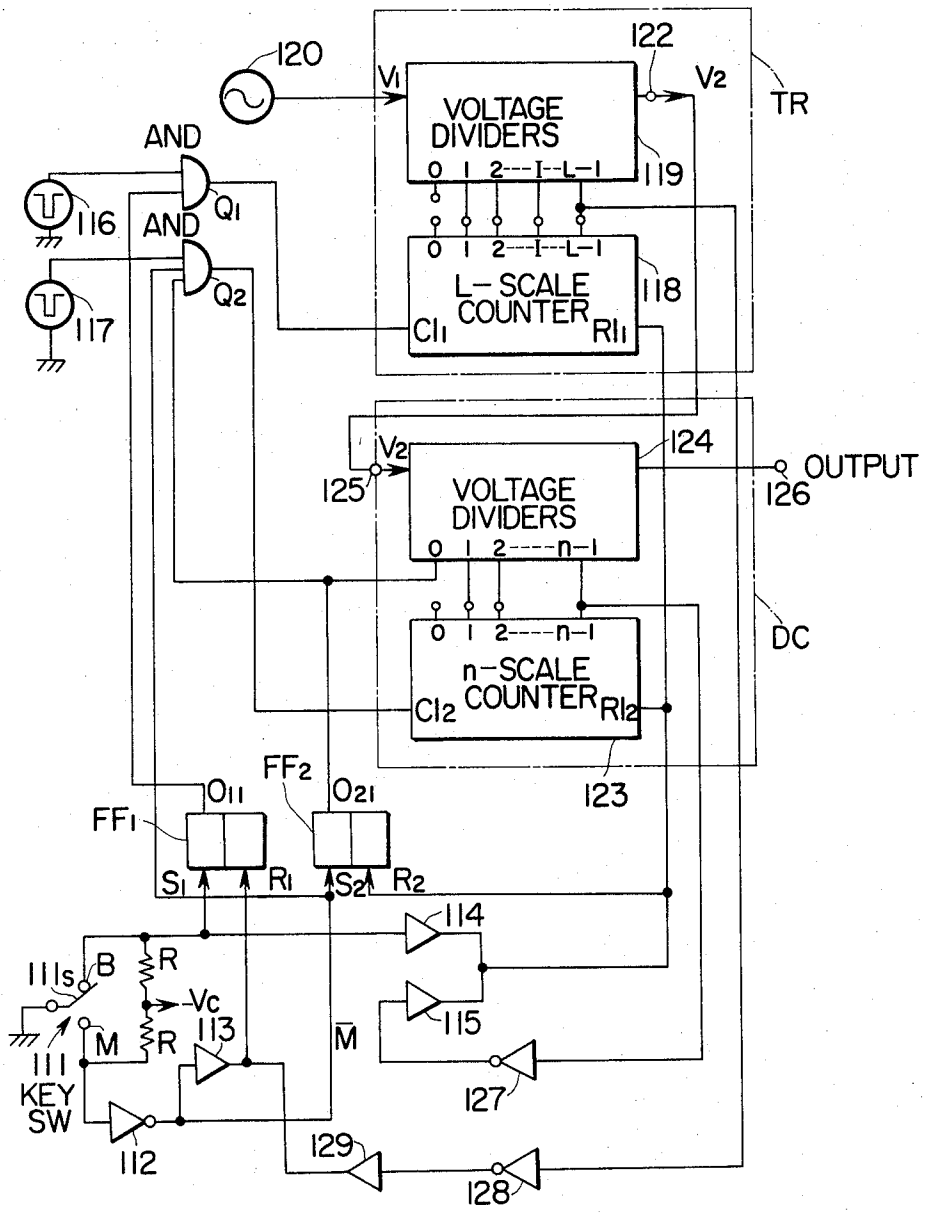

120
122
V1
V2
TR
VOLTAGE DIVIDERS
0 1 2---I--L-1
119
AND
Q1
116
AND
Q2
117
L-SCALE COUNTER
118
C11
R11
V2
125
124
OUTPUT
126
VOLTAGE DIVIDERS
0 1 2----n-1
DC
n-SCALE COUNTER
C12
R12
123
FF2
O11
O21
FF1
S1
R1
S2
R2
114
111s
B
R
Vc
M
R
113
M
115
111
KEY SW
127
112
129
128

FIG. 9

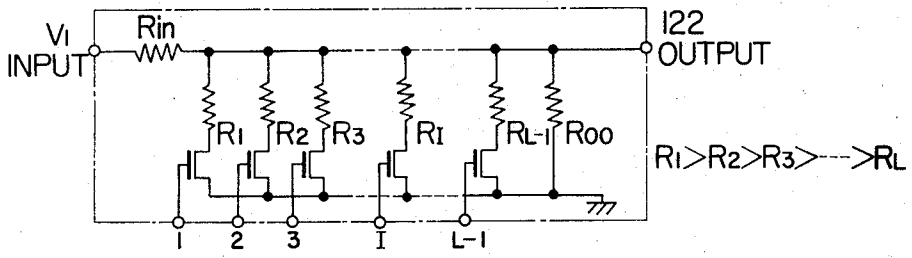
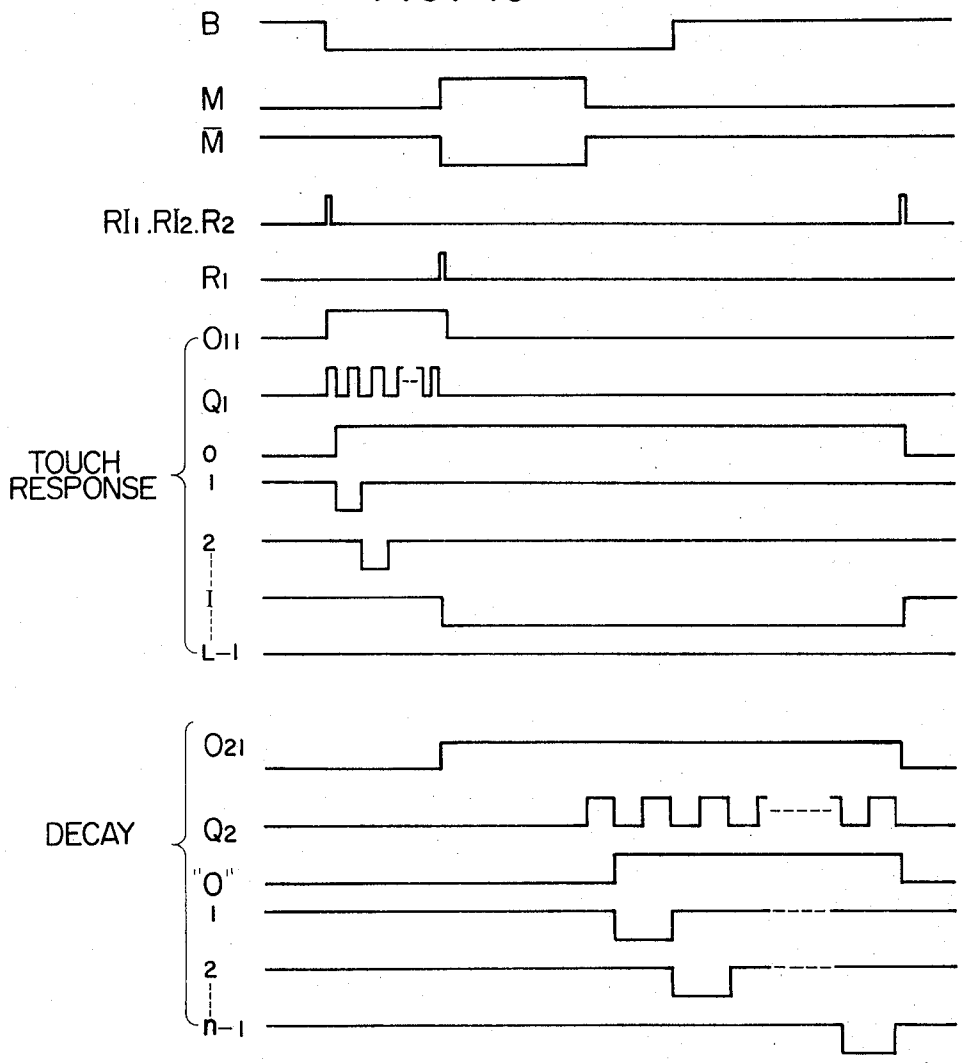

Vi
INPUT
Rin
122
OUTPUT
R1
R2
R3
RI
RL-1
Roo
R1>R2>R3>---->RL
1
2
3
I
L-1

FIG. 10


B
M
M̄
RI1.RI2.R2
RI
O11
Q1
TOUCH RESPONSE
0
1
2
I
L-1
O21
Q2
DECAY
"0"
1
2
n-1

ELECTRONIC MUSICAL INSTRUMENT KEYING SYSTEM WITH ENVELOPE SAMPLE MEMORIZING VOLTAGE DIVIDERS

BACKGROUND OF THE INVENTION

1. Field of the invention

The present invention relates to electronic musical instruments such as electronic organs and similar tone-producing apparatus, and more particularly to a keying system therefor including a sampled envelope memory utilizing voltage dividers and a counter.

2. Description of the prior art

In the conventional keying system for an electronic musical instrument of the key-actuated type, there have been proposed various types of tone keyers which employ RC timing circuits for providing percussion effect and/or sustain effect whereby the rate of change in amplitude of tone signals may be controlled. Such RC timing circuit constituting a charge-discharge circuit requires a capacitor of considerably large capacitance, and as a result, many inconveniences and disadvantages have been encountered in fabricating the whole keying system in the form of an integrated circuit and also in performing a low cost mass production since there were difficulties in forming capacitors of large capacitance in the integrated circuit and hence these capacitors had to be mounted in hybrid form. In addition, a large number of keyers, for example 60 keyers, are required in an electronic musical instrument, and accordingly, large capacitance capacitors of at least the same number are used in the RC timing circuits. However, such capacitors which are available fail to be uniform in quality and property, and therefore it has been difficult to arrange so that the decay characteristics of the whole keyers have a uniform decay time. Though this decay time can be varied by changing the values of capacitance and resistance which determine the time constant, the decay curve or the decay characteristic is considered to be determined inherently by the charge-discharge property of the large capacitance capacitor which is employed and therefore, it is impossible to vary this decay characteristic as required by the player. Even in the prior art keying system of this type, it also has been necessary to provide some means or other to eliminate unwanted click which will occur at the moment when a key begins to be depressed and released, namely, at the beginning as well as at the end of a key action.

Similar drawbacks as described above have also been true in a tone level determining circuit for use in the touch-responsive keying system, which makes use of such an effect that the level of tone signals depends on the depression speed of a playing key — which is generally called the "touch-responsive effect" — because of its employing a charge-discharge circuit consisting of a resistor and a capacitor of large capacitance.

SUMMARY OF THE INVENTION

Therefore, it is the primary object of the present invention to provide an apparatus for use with an electronic musical instrument for keying the tone signals coming from the tone generators, which comprises resistive voltage divider networks for effecting tone control, such as tone envelope control and tone level control, without using a charge-discharge circuit including a capacitor of large capacitance.

Another object of the present invention is to provide a keying system for an electronic musical instrument which is easy and inexpensive to fabricate in an integrated circuit form.

A further object of the present invention is to provide an integrable keying system for an electronic musical instrument, which is simple in construction and is high in quality and is very suitable for various commercial purposes.

Another object of the present invention is to provide an integrable keying system for use in an electronic musical instrument to provide percussive effects, which comprises: a resistive voltage divider network having a common input resistor and a bank of resistance elements each with a series-connected semiconductor switching element, the values of said resistance elements being preset in conformity with the predetermined decay amplitudes; an n-scale counter for providing drive pulse signals to the corresponding switching elements of the divider network to thereby sequentially enable the corresponding divider circuits; a counter drive pulse generator; and gate means which functions to deliver an output pulse from the pulse generator into the n-scale counter and at the same time to pass an input tone signal from a tone generator to an output terminal of the divider network at the beginning of depression of a playing key.

A further object of the present invention is to provide an integrable keying system for providing sustain effects to the tone signals, which comprises: a key-operated switch, a resistive voltage divider network having a common input resistor and a bank of parallel-connected resistance elements each with a series-connected semiconductor element, the respective values of the resistance elements being predetermined in conformity with the required sustain amplitudes; an n-scale counter whose output terminals are connected with the control terminals of the switching elements respectively for providing drive pulses therefor; a counter drive pulse generator for generating clock pulses to drive the counter; and gate means serving to enable a reference voltage divider circuit among the divider network to thereby develop a divided output voltage of an input tone signal upon the depression of a playing key and then to begin the feeding of clock pulses from the pulse generator to the n-scale counter whenever the release of the depressed key is detected.

A still further object of the present invention is to provide an electronic musical instrument keying system which can be produced in an MOS integrated circuit and in which two sets of resistive voltage divider networks each having series-connected electronic switching elements are arranged so as to produce a touch-responsive-level tone signal in response to the depression speed of a playing key and to provide the tone signal additively with a decay characteristic by detecting the release of the depressed key.

Other object, features and advantages of the present invention will be understood well from the following detailed description with respect to preferred embodiments when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram for schematically illustrating an embodiment of the present invention.

FIG. 2 is a circuit diagram illustrating an example of a resistive voltage divider network shown in FIG. 1.

FIG. 3 is a timing chart for explaining the operation of the circuit of FIG. 1.

FIGS. 4(*a*) – 4(*d*) are detailed circuit diagrams illustrating examples of parts shown in FIG. 1.

FIG. 5 is a schematic circuit diagram illustrating another embodiment of the keying system in accordance with the present invention.

FIG. 6 is a timing chart for explaining the operation of the circuit system shown in FIG. 5.

FIG. 7 is an illustration of the decay characteristic curves which are obtained in accordance with the embodiment shown in FIG. 5.

FIG. 8 is a schematic circuit diagram illustrating a further embodiment of a touch-responsive effect producing keying system in accordance with the present invention.

FIG. 9 is a detailed circuit diagram of a first voltage divider network shown in FIG. 9 only by way of example.

FIG. 10 is a graph illustrating a timing chart for explaining the operation of the circuit system shown in FIG. 8.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now particularly to FIG. 1, there is illustrated a block diagram of an essential part of a percussion-effect producing keying circuit for use in an electronic musical instrument in accordance with an embodiment of the present invention, in which reference numeral **11** represents a key-operated switch associated with a corresponding playing key of the instrument, **12** an inverter, **13** a flip-flop circuit, **14** an AND circuit with two input terminals, **15** a clock pulse generator for generating clock pulses whose frequency period is variable, **16** an *n*-scale counter with *n*-output terminals (No. **0** through *n*-**1**) where *n* is an integer, **17** another inverter, **18** and **19** modified differentiation circuits, **20** a resistive voltage divider network which is arranged to be driven by the output signals coming from the *n*-scale counter **16**, **22** an output terminal of the keying circuit, **23** a decaying curve selector switch for selecting one of the decaying patterns formed by the resistive divider network **20**, and **24** a source of a tone signal which is supplied to divider **20**. Normally, of course, a number of identical keyer or circuits, each receiving a different tone signal and each having its output coupled to the outputs of the other keyer circuits are provided. In FIG. **1**, a second keyer circuit **26** and tone source **28** are schematically illustrated.

Key-operated switch **11** is provided with a movable contact piece **1***s* having one end grounded and with a fixed contact **1***b* which is connected via a load resistor to a negative voltage source $-Vc$. The key-operated switch **11** is normally held open. The flip-flop **13** is normally rendered to a "low" level or "0" level at its set output end O_2, but is made in its reverse state upon receipt of a negative-going enabling pulse at its set terminal S. At this time, a "high" level or "1" level signal appears at the set output terminal O_2. This terminal O_2 is connected with one input terminal of the AND circuit **14** and simultaneously with a control terminal of a first-stage switching element Tr_0 (shown in FIG. **2**) one end of which is series-connected to a common tone input resistor R_{in} of the voltage divider network **20** and the other grounded. This switching element Tr_0 is normally rendered conductive, so that a tone source signal applied to the input terminal of the divider network **20** is shunted to ground, and thus no tone signal appears at the terminal **22**. The resistive voltage divider network **20** is constituted by the common input resistor R_{in}, a plurality of parallel-connected resistance elements each with a series-connected semiconductor switching element having one end grounded, one example of which is illustrated in FIG. **2**. Respective semiconductor switching elements are connected, at their control terminals, with the output terminals **1, 2, 3,** - - - , $n-1$ of the *n*-scale counter **16**, respectively, and they may be formed of MOS FET's (metal oxide semiconductor field effect transistors Tr_1, Tr_2, - - - , Tr_{n-1}). These switching elements and the *n*-scale counter are arranged in such a way that individual resistance elements R_{11}, R_{21} - - - R_{n-1} connected in series to the switching elements may sequentially be made to close individual potential divider circuits together with the common input resistor by sequentially operating the individual switching elements TR_1, TR_2, - - - , TR_{n-1}. As shown in FIG. **2** by way of example, the divider network **20** further comprises *m*-sets of divider-forming resistance elements R_{11}, R_{12} - - - , R_{1m}; R_{21}, R_{22} - - , R_{2m}; - - - ; and $R_{(n-1)1}$, $R_{(n-1)2}$ - - , $R_{(n-1)m}$, to whose elements are connected in series individual switching elements such as MOS FET's. The selection of the set of resistance elements is carried out by changing over the selector switch **23**. The values of divider-constituting resistance elements of each set are determined in conformity with the amplitudes of a decay curve of a tone signal. A reference resistance element R_0 having a relatively high resistance value is provided between the output terminal **22** and the ground and constitutes a part of a divider circuit with the common resistor R_{in} when one parallel-conneted resistance element is shunted to ground by the operation of the corresponding switching element connected to the *n*-scale counter **16**.

The operations and functions of the above-mentioned circuit arrangement will now be described with reference to the pulse waveform chart shown in FIG. **3**, in which each pulse waveform represents an output at a part indicated by the corresponding sign. When the key-operated switch **11** is kept in its OFF state, the potential at point *a* is in the 0 state lower than the ground potential, and thus the output side *b* of the inverter **12** is in 1 state, being at higher one of its available potential. At that time, the output terminal O_2 of the flip-flop circuit is maintained in the 0 state. Therefore, the AND circuit **14** is not enabled and the control terminal O of the divider network **20** is held in the 0 state, so that the conduction of corresponding switching element is maintained and all the input signals to the divider network **20** are shunted to the ground, thus no output signal appearing at its output terminal **22**. Now, when the key-operated switch **11** is closed by the depression of the key, namely, when it is brought to its ON state, the point *a* is of the ground potential, which is higher than the ngative voltage source $-Vc$ and the point *b* changes to the 0 level (state) in potential. At that time, the flip-flop circuit **13** is reversed in its state due to the change in potential at the set terminal S. Accordingly, the output terminal O_2 of the flip-flop circuit **13** and point *c* are rendered to the 1 state. This results in the cut-off state of the switching element Tr_0, so that

the tone source signal is no longer shunted to the ground. At that time, the amplitude of a tone source signal which has been passed through the divider network changes from $(r/R_{in} + r)$ V to $(R_0/R_{in} + R_0) \times V$, wherein V represents the amplitude of the signal at the input end of the network and r the ON resistance of the switching element Tr_0. The amplitude $(R_0/R_{in} + R_0) \times V$ of the output tone signal indicates that a stationary tone signal is present. As will be seen from the above-description, the leak level of tone source signals in the OFF state of the key-operated switch is determined by the quantity of resistance r. Accordingly, if the value of the resistance r is quite low as compared with that of the common input resistance R_{in}, the leak level will become low accordingly. In other words, no tone source signal substantially appears at the output terminal **22** at that time.

On the other hand, when the key-operated switch **11** is brought to its ON state, the flip-flop circuit **13** begins to develop an enabling signal, so that the point *c* is brought to the 1 state and the AND circuit **14** is rendered to its operative state to gate-on clock pulses from the clock pulse generator **15.** The clock pulses which have passed through the AND circuit **14** as shown by *e* in FIG. **3** are applied to the input terminal CI of the *n*-scale counter **16** to drive this counter. Various pulse waveforms occurring at the output terminals **1, 2,** - - , *n* of the *n*-scale counter are indicated by the same signs in FIG. **3.** Now, for the purpose of explanation, let us assume that the decay curve selector switch **23** is made to select the first set of divider-constituting resistance elements (i.e. R_{11}, R_{21} - - - , $R_{(n-1)1}$). Whereupon, the n-scale counter **16** successively energizes the switching elements Tr_1 through $Tr_{(n-1)}$ to render them to the ON state as long as clock pulses are applied thereto, and the output level of the tone source signal can be expressed by $(R'_0/R_{in} + R'_0) \times V$, wherein R'_0 represents the parallel resistance of R_0 and R_{11}; R_0 and R_{21}; - - - ; or R_0 and $R_{(n-1)1}$. From the above formula, it will be understood that the value R'_0 varies as the resistance elements successively constitute individual divider circuits with the common resistor R_{in} in response to the sequential pulse signals from the *n*-scale counter **16.** Accordingly, by setting the values of the resistance elements R_{11}, R_{21}, - - , $R_{(n-1)1}$ in conformity with the desired amplitudes of a tone signal with respect to time, a desired decay effect is given to the tone signal which is passed through the divider network **20.** The decay time of the keyed tone signal depends upon the frequency of the clock pulses from the clock pulse generator. Namely, if the frequency is high, the decay time is short; whereas if it is low, the decay time becomes long. Thus, the decay time can easily be controlled merely by adjusting the clock pulse generator to vary the frequency of the clock pulse train.

When a pulse signal develops at the last-stage $(n-1)$th output terminal of the *n*-scale counter **16,** it is fed through the inverter **17** not only to the reset terminal R of the flip-flop circuit **13** to thereby reset the circuit **13,** but also to a reset terminal CR of the counter **16** via the modified differentiator circuit **18** which produces a positive going pulse, for resetting the counter **16** thereby at the moment when this pulse falls down to the low level.

The modified differentiator circuit **19** is provided to reset the counter **16** whenever the key depression is repeated at a high speed, so that the counter always functions to develop pulse outputs from its first-stage successively.

The greater the number of parallelly-arranged divider-constituting resistance elements is, the richer is the decay curve.

FIGS. **4**(*a*) – **4**(*d*) show concrete constructions of the AND circuit **14,** the inverter **12,** the flip-flop circuit **13** and the modified differentiator circuits **18** and **19,** respectively, in which are employed MOS type transistors such as P channel enhancement mode transistors in view of the easiness of production in the form of an integrated circuit.

According to the circuit of the present invention, the problem of key click which appears in the conventional keying circuit using an RC timing circuit has been solved because of its requiring no charge and discharge capacitor.

Referring now to FIGS. **5** – **7,** there is illustrated a sustain effect producing keying circuit representing another embodiment of the present invention, which is similar to the circuit arrangement of the preceding embodiment except for the AND circuit and the associated connections. That is, in this circuit, a three-input AND circuit **44** is provided in place of a two-input AND circuit **14.** The third input terminal of the AND circuit **44** is connected with the set input terminal S of the flip-flop circuit **13.** Reference numerals **11** represents a key-operated switch having a movable contact **1***s* and a fixed contact **1***b*, **12** an inverter, **15** a variable frequency type clock pulse generator whose output terminal is connected to the first input terminal of the AND circuit **44, 16** an *n*-scale counter connected to the output end of the AND circuit **44** to receive clock pulses, **17** an inverter, **18** and **19** modified differentiator circuits, **20** resistor voltage divider network which operates by the output pulses produced from the counter **16** and is constructed as shown in FIG. **2,** and **23** a decay curve selector switch which selectively sets a combination of potential-divider forming resistor group of the network **20** by changing over parallel-connected resistor patterns through series-connected semiconductor switches.

The operation of the sustain effect producing keying circuit will be explained with reference to the timing chart of FIG. **6,** in which each pulse waveform is an output at a point indicated by a corresponding sign in the circuit arrangement of FIG. **5.**

The key-operated switch **11** is normally opened to be held in the OFF state, and the fixed contact point *a* is at a low level DC voltage with respect to the ground potential because this point *a* is connected through a load resistor to a negative DC voltage source −V. Accordingly, the output end *b* of the inverter **12** is at a high level DC voltage, but the flip-flop circuit **13** is not operated by the high level DC voltage since it is caused to operate upon receipt of a low level DC voltage (i.e. negative going moment) at its set input end. At that time, the output end of the flip-flop circuit **13** is held at a low level DC voltage. Therefore, the AND circuit **44** is not enabled, thus preventing any clock pulse from passing therethrough, and the first-stage terminal denoted by **0** in the resistor voltage divider network **20** is at the same low level voltage, whereby a switching element Tr_0 is maintained in its conductive state and the tone signal applied to the input end of the network **20** is shunted to the ground, thus no output appearing at its output end as will be seen from the operation of the

preceding embodiment. When the key-operated switch **11** is closed with the depression of the key, the point *a* is rendered to the ground potential which is higher than that of the negative DC voltage source $-Vc$, and the point *b* is rendered to a low level DC voltage. Reversal in the DC voltage at this point causes the operation of the flip-flop circuit **13** to turn the condition of its output to a high-level DC voltage. The high level output developed from the flip-flop circuit **13** renders the switching element Tr_0 to be cut-off, thereby disconnecting the flow of the input tone signal to ground. As a result, the divider network **20** causes a voltage divider circuit consisting of the common input resistor R_{in} and the reference divider resistor R_0 to stationarily produce at the output terminal **22** a keyed tone signal having a level of $(R_0/R_{in} + R_0) \times V$ when a tone signal having a level of V is applied to the input common resistor R_{in}. This is because other divider-constituting resistor elements in the divider network **20** are not conducting due to the fact that the AND circuit **44** is not enabled in the absence of the third input and hence the *n*-scale counter does not operate. On the other hand, when the key-operated switch is returned to its OPEN state by the release of the depressed key, the potentials at points *a* and *b* are in the initial levels respectively. However, the condition of the flip-flop circuit **13** remains because of its producing no reset pulse at that time, so that the AND circuit **44** is enabled to begin feeding clock pulses from the clock pulse generator **15** to the input terminal CI of the *n*-scale counter **16.** Then the *n*-scale counter **16** counts the clock pulses to develop a pulse voltage successively at sequentially arranged output terminals **1, 2, 3 - -**, *n* of the counter. Each pulse waveform with respect to time is shown in FIG. **6** by the same reference. In a similar manner as described above, these sequentially produced pulses render the divider network **20** operative, so that a keyed tone signal having a decay effect i.e., a decay envelope is produced through a set of voltage divider circuits having respectively predetermined resistance values, at the output terminal **22.** The decay envelope may be changed by changing over the selector switch **23** as required. As previously described, the decay time can be easily changed by varying the frequency of the clock pulses in the clock pulse generator. Three decay characteristics of a keyed tone signal are illustrated in FIG. **7,** which are determined by setting a pattern in values of parallel-connected divider-constituting resistor elements and also by setting the frequency of clock pulses. With the embodiment shown in FIG. **1,** the interval between time **0** and time **1** is very short, while with the embodiment shown in FIG. **5,** the interval between time **0** and time **1** is long as defined by the period of time when the key is being depressed.

Referring now to FIGS. **8 – 10,** there is shown an integrable touch-responsive keying circuit arrangement as a further embodiment of the present invention. In addition to the envelope forming arrangement as that shown in FIG. **5,** this embodiment further comprises a touch-responsive control arrangement constituted also by the combination of voltage dividers and a reading counter. The reference numeral **111** represents a key-operated change-over switch; **112, 127** and **128** inverters; **113 – 115** and **129** modified differentiator circuits each of which functions to generate a positive-going pulse when its input signal changes from a positive side potential to a negative side potential; FF_1, FF_2 flip-flop circuits respectively; Q_1, Q_2 a two-input AND gate circuit and a three-input AND gate circuit; **116, 117** variable frequency type clock pulse generators; **118** an L-scale counter having L-number output terminals, an input terminal CI_1 and a reset terminal RI_1 which is arranged to be cleared by a positive pulse at the falling moment thereof; **119** a resistor voltage divider network which comprises a common input resistor and a bank of parallel-connected resistor elements each with a switching element such as an MOS FET in such a manner that voltage divider circuits are successively constituted each time the corresponding switching elements are driven by the output pulses produced from the L-scale counter; **120** a tone generator for generating tone signals; **122** an output terminal of the divider network **119**; **123** an n-scale counter which has its input terminal CI_2 adapted to receive an input signal from the AND gate circuit Q_2 and its reset terminal RI_2 to receive a resetting positive pulse to reset the counter back to its original 0 state at the falling moment of the pulse; **124** another resistor voltage divider network which comprises a bank of parallel-connected resistor elements each with a series-connected MOS FET switching element, the switching elements being arranged to receive sequential pulses from the *n*-scale counter **123** and to establish voltage dividing resistor circuits successively; **125** an input terminal of the divider network **124,** and **126** an output terminal of the divider network **124** which constitutes an output of the keying circuit.

The key-operated switch **111** includes a movable contact **111**s with a movable arm, a make contact M and a break contact B. The movable contact **111**s connected to the ground interlocks with the key and is normally closed to the break contact B, so that the contact B is held at the ground potential even when a negative DC voltage $-V$ is applied across a load resistor R (upper one). The contact B in turn is connected with a set input terminal S_1 of the flip-flop circuit FF_1 and is connected via the modified differentiator circuit **114** to the reset terminals RI_1 and RI_2 of the counters **118** and **123,** respectively. On the other hand, the make contact M is connected through another load resistor R (lower one) to the negative DC voltage source and simultaneously is connected through the inverter **112** and the modified differentiator circuit **113** to the reset input terminal R_1 of the flip-flop circuit FF_1 and through the inverter **112** to the set input terminal S_2 of the flip-flop circuit FF_2 and the second input terminal of the AND gate circuit Q_2. The output terminal O_{11} of the flip-flop circuit FF_1 is normally rendered to a low level voltage and is connected with the first input terminal of the AND gate circuit Q_1. The AND gate Q_1 is enabled when the output of the flip-flop circuit FF_1 is rendered to a high level voltage to thereby gate-on clock pulses from the clock pulse generator **116,** whereas the output terminal O_{21} of the other flip-flop circuit FF_2 is normally rendered to a low level voltage, and therefore, no enabling signal is supplied to the first input terminal of the AND gate circuit Q_2. At that time, the flip-flop FF_2 gives a low level voltage to the decay effect producing divider network **124** such that an input tone signal is grounded. Accordingly, the AND gate Q_2 is rendered inoperative and no clock pulses enter the *n*-scale counter **123** from the clock pulse generator **117.** The L-scale counter **118** and the *n*-scale counter **123** may be of the recirculation type in which L-number output

terminals and n-number output terminals are arranged so as to produce a pulse sequentially each time a clock pulse is inputed, respectively, for example by combining a large number of cascaded flip-flops and a decoder. Each of the divider circuits **119** and **124** is constructed by a large number of resistor elements and MOS FET's so as to facilitate the fabrication of an integrated semiconductor circuit. An example of the circuit **119** is illustrated in FIG. **9** in which the terminals **1, 2, - - -, L−1** led from the control gates of MOS FET's as shown are connected to the output terminals of the L-scale counter, respectively. As the circuit **124**, the construction shown in FIG. **2** may be used by merely eliminating the common input resistor R_{in}. Alternatively, such a common input resistor R_{in} is provided in the preceding-stage circuit **119**, to receive a tone signal from the tone generator **120** in the present keying circuit. Thus, one resistor voltage divider network **119** and the L-scale counter constitute a key touch-responsive tone level control circuit TR, whereas the other resistor voltage divider network **124** and the n-scale counter **123** constitute a decaying envelope forming circuit DC by which a decaying envelope is given to a tone signal which has been subjected to a key touch-responsive level control in the preceding stage circuit TR. The last-stage output signal of the L-scale counter **118** is fed through the inverter **128** and the modified differentiator circuit **129** to the reset input terminal R_1 of the flip-flop FF_1, and the last-stage output signal of the n-scale counter **123** is supplied via the inverter **127** and the modified differentiator **115** to three reset terminals, namely, the terminal RI_2 of the n-scale counter, the terminal R_2 of flip-flop FF_2 and the terminal RI_1 of L-scale counter **118.**

Now, the operation of the touch-responsive keying circuit arrangement will be described hereunder with reference to the pulse waveforms indicated in FIG. **10** which are output waveforms at positions identified by the same legends in FIG. **8.**

The clock pulse generators **116** and **117** always generate clock pulse trains, preferably the pulse from the generator **116** being of a higher frequency than the pulse from the generator **117.** In FIG. **10,** waveforms Q_1 and Q_2 represent the clock pulses derived from the AND gates Q_1 and Q_2 respectively only during the gate-on periods. In the present embodiment, these clock pulse generators are individually provided, but they can be substituted by the single clock pulse generator combined with frequency dividers or frequency multipliers.

When the key is depressed, it takes T seconds for the movable arm **111***s* of the key-operated switch to travel from the break contact B to the make contact M. The traveling time is inversely proportional to the traveling speed of the contact **111***s*, viz. the depression speed of the key. In the usual key-actuated electronic musical instrument, the depression speed of key is about 1.5 to 20 milliseconds. At the time when the movable arm **111**s leaves the contact B, the contact B which has been at the ground potential is now brought to the negative voltage $-Vc$, namely, the contact B which was at a high level voltage is rendered to a low level voltage. This results in the delivery of an enabling pulse to the set input S_1 of flip-flop FF_1, the reset terminal R_2 of flip-flop FF_2 and the reset terminals RI_1 and RI_2 of the counters. As a result, the output O_{11} of flip-flop FF_1 is reversed to be of a high level voltage, and the high level voltage output of the flip-flop FF_1 renders the AND gate Q_1 to its operative state, so that it begins feeding clock pulses from the clock pulse generator **116** to the L-scale counter **118** to be driven thereby. The counter **118** continues counting of in-coming clock pulses until the AND gate Q_1 is disabled. When the movable arm **111**s of the key-operated switch **111** reaches the make contact M, the potential at the make contact M shifts from a negative voltage to the ground potential, namely from a low level to a high level. This results in providing, through the differentiator **113,** a reset pulse to the reset terminal R_1 of flip-flop FF_1 to thereby invert its output voltage condition at the falling moment of the pulse. In other words, the output terminal O_{11} is brought to a low level voltage. Thus, it will be seen that the L-scale counter which has been advancing step by step for a period of T seconds determined by the depression speed of the key, stops at a certain count, say at No. I. Assuming that a set of resistor elements $R_1, R_2, - - -, R_{L-1}$ of the divider network **119** as shown in FIG. **9** are set to have values as $R_1 > R_2 > R_3 > - - - > R_l > - - - > R_{L-1}$, an output voltage expressed by $(R'_0/R_{in} + R'_0) \times V_1$ is obtained at the terminal **122,** wherein R'_0 is a parallel resistance of the common output resistance R_{00} and the now selected resistance R_l, V_1 the voltage of an input tone signal. Since the extent in which the counter **118** advances depends on the period T, the output level of the divider network **119** is determined in accordance with the period T. Thus, the level V_1 of a tone signal produced by the generator **120** can be varied in accordance with the depression speed of the key into an output V_2 at the terminal **122.**

If the L-scale counter **118** advances up to the last output terminal, the flip-flop FF_1 is reset by a reset pulse obtained through the inverter **128** and a differentiator **129,** before the movable arms **111**s reaches the make contact M.

Then, when the movable arm **111**s has reached the make contact M, a negative going voltage change is applied to the set input terminal S_2 of flip-flop FF_2, so that its output O_{21} is turned to a high level state, i.e., to be of a high level voltage and this high level voltage is applied to the first stage terminal of the network **124,** and accordingly, the voltage is applied to the gate of the MOS FET switching element Tr_0, which has been in the ON state allowing an input tone signal to flow into the ground, so that the switching element Tr_0 is now cut off. As a result, the input tone signal appears at the output terminal **126** with a level expressed by $(R_0/R_{in} + R_0) \times V_2$, wherein R_0 is a common output resistance, and V_2 is the input level of tone signal to the circuit **124** (same as shown in FIG. **2,** although the decaying curve selector circuit is omitted here). This holds true so long as the key-operated switch **111** is held to close the make contact M by the depression of the key. During this period, the AND gate Q_2 does not operate because of the output $\overline{M}$ of the inverter **112** being at a low level voltage, and consequently, the n-scale counter **123** also remains in its inoperative state. In other words, the output level of a keyed tone signal is maintained at a fixed value as long as the make contact M is closed.

When the movable arm **111**s leaves the make contact M by the release of the hitherto depressed key, the make contact M is rendered to a low level voltage, and therefore, the AND gate Q_2 is enabled to begin delivering clock pulses produced by the pulse generator **117** to the n-scale counter to thereby be driven. In a similar

manner as described hereinabove in connection with the embodiment shown in FIG. 5, the decay effect producing functions are carried out by the combination of the *n*-scale counter **123** and the resistor voltage divider network **124.** Consequently, at the output terminal **126** of the keying circuit there may be obtained a keyed tone signal having a key touch-responsive level and desired sustain or decay amplitude characteristics without using RC timing circuits. Thus, the present keying circuit can produce tone signals having complex and delicate envelopes resembling those produced by a natural musical instrument.

I claim:

1. A keying system for use with an electronic musical instrument comprising:

a key-operated switch;

an input terminal to receive a tone signal to be keyed;

a sequentially changing-over voltage divider network including a circuit ground, a common input resistor having one end connected with said input terminal and another end defining an output line, a bank of resistor elements connected with the output line and respectively having values predetermined to represent the respective amplitudes as sampled values of an intended decaying envelope of the tone signal with time axis for individually constituting voltage dividers together with the common input resistor, and also including first switching elements respectively connected in series with said resistor elements individually to the ground and each having a control electrode, and a short-circuiting switching element connecting said output line to ground having a control electrode for grounding said output line when a given voltage is applied to said control electrode of said short-circuiting switching means, and a reference divider resistor being connected between the output line and the ground;

an output terminal connected to the output line for deriving a keyed tone signal;

an *n*-scale counter with successive n-output ends connected to the respective control electrodes of the switching elements for sequentially supplying a pulse to said first switching elements so as to render said switching elements conductive sequentially;

a counter drive circuit for producing clock pulses; and

gate means connected between said counter drive circuit and said *n*-scale counter and to said key-operated switch for controlling the flow of the clock pulses to said counter in response to the operation of said key-operated switch.

2. A keying system according to claim **1,** in which said gate means includes a flip-flop having a set input terminal responsive to the movement of the key-operated switch to detect the beginning of the depression of the corresponding key and to store a binary signal representing the condition of the key depression, a gate circuit responsive to said stored signal for allowing the flow of the clock pulses toward the *n*-scale counter, and a connection between the output of said flip-flop and said short-circuiting switching element which is rendered inoperative in the presence of said binary signal.

3. A keying system according to claim **2,** in which said gate circuit has first and second input terminals connected to said clock pulse producing circuit and the output of said flip-flop circuit, respectively, and a third input terminal connected to the set input terminal of said flip-flop, whereby said gate circuit is still kept closed even upon detecting the depression of the key and is enabled upon detecting the beginning of the release of the depressed key.

4. A keying system for an electronic musical instrument having a plurality of tone signal sources covering musical range of several octaves, a common output system, and a plurality of keyers individually connecting the sources to the output system, said keyers individually integrally comprising:

a bank of change-over controlled voltage divider circuits in series connected between each source and the output system, said voltage divider circuits including an input terminal, a common input resistor connected to said input terminal, a common output resistor having one end connected in series to the opposite end of said input resistor and the other end grounded, an output terminal connected at the junction between said input and output resistors, a bank of resistors and normally-nonconducting voltage-controlled switching elements individually in series thereto, which are in parallel connected across said output resistor, and a common normally conducting voltage-controlled switching element in parallel connected across said output resistor, said bank of the resistors successively being predetermined in value in correspondence to the decay amplitudes of a required pattern in the keyer;

an *n*-scale counter having a zero setting terminal and $n-1$ output setting terminals individually connected with said bank of the switching elements for successively supplying control pulses thereto, the number of which corresponds to that of said bank of switching elements;

a clock pulse generator for generating clock pulses to drive said *n*-scale counter;

gate means having an input and provided between said clock pulse generator and said *n*-scale counter to couple said clock pulses to said counter when an enabling signal is applied to said input; and

actuating means for applying a keying control voltage to said common switching element and an enabling signal to said gate means and including a playing key-operated switch, a DC potential source connected to said switch, so as to generate a keying control voltage when said switch is operated, and a binary memory connected to said key-operated switch and to said gate means for changeably storing the keying control voltage which is generated when said key-operated switch is operated, and providing an output as a function of the stored voltage, said output being supplied to said input of said gate means to enable said gate means.

5. The keying system according to claim **4,** in which said actuating means generates the keying control voltage when said playing key switch begins to be depressed, thereby providing percussive effects to the keyed tone signal.

6. The keying system according to claim **4,** in which said actuating means and said gate means are connected so that said enabling signal is supplied to said gate means only when the depressed key is released, whereby the keyed tone signal has a fixed amplitude waveform for the period during which the key is de-

pressed, while the keyed tone signal has a decay amplitude waveform once the depressed key is released.

7. The keying system according to claim **4**, in which said gate means is a two-input AND circuit receiving the clock pulses from the clock pulse generator and the output of said binary memory, respectively.

8. The keying system according to claim **6**, in which said gate means is a three-input AND circuit adapted to receive the clock pulses from the clock generator, the keying control voltage and the output of the memory, respectively.

9. The keying system according to claim **4**, in which said bank of voltage divider circuits includes a plurality of sets of resistors as said bank of resistors, each set of resistors being sequentially preset in values so as to have different amplitude pattern, and voltage-controlled switching elements in series to said sets of individual resistors between them and said bank of switching elements, and an amplitude pattern selector switch for selectively applying a DC voltage to the selected switching elements corresponding to the selected one of said sets of resistors.

10. The keying system according to claim **4**, in which a reset means is provided to reset the *n*-scale counter each time the keying control voltage is generated.

11. An integrable touch-responsive tone keyer circuit for an electronic musical instrument comprising a first and a second voltage divider network each having a bank of resistors and semi-conductor switching elements individually in series connected thereto, the values of the bank of resistors being successively preset in conformity with the characteristic amplitudes of a required pattern, said first divider network having a common input resistor for receiving a tone signal to be keyed, and connected in series with the bank of resistors thereof the junction of which is connected to the bank of resistors of said second divider network and constitutes an output end of the keyer;

a first and a second serial counters provided to said first and second divider networks respectively each for sequentially providing pulse outputs to the respective switching elements so as to successively constitute divider circuits by the bank of resistors;

a first and a second clock pulse generators provided individually for said first and a second counters for generating clock pulses thereby to drive said counters respectively;

a first and a second keying control circuit connected to a playing key-operated switch, means connecting said switch to an actuating potential, each of said control circuits including a memory connected to said key-operated switch, for shifting from a first to second output condition when said switch is operated to apply said actuating potential to said memory, gate circuits connected between the clock generators and the counters and to said memorys for coupling said clock generators to said counters so that said counters are driven by said pulses, and reset means for the memory and the counter being connected thereto, said first control circuit controlling the flow of the clock pulses produced from the first clock generator to said first counter in accordance with the depression speed of the key to thereby determine the level of the received tone signal by setting one of the first divider networks and said second control circuit controlling the flow of clock pulses from said second clock generator to said second counter once the depressed key is released to thereby determine the decay characteristics of the second divider network.

12. The touch-responsive tone keyer circuit according to claim **11**, in which each of said voltage divider networks includes a plurality of sets of resistors as said bank of resistors, each set of resistors being sequentially preset in value so as to have a different amplitude pattern, and voltage-controlled switching elements in series to said sets of individual resistors between them and said bank of switching elements, and an amplitude pattern selector switch for selectively applying a DC voltage to selected switching elements corresponding to a selected one of said sets of resistors.

13. The touch-responsive tone keyer circuit according to claim **11** in which said first and said second clock pulse generators are of the variable frequency type.

14. The keying system according to claim **4**, in which the frequency of the clock pulse generator is variable.

15. The keying system according to claim **4**, in which said switching elements are constituted by FET's.

16. The keying system according to claim **4**, in which said binary memory of the actuating means is constituted by a flip-flop circuit.

17. The touch-responsive tone keyer circuit according to claim **11**, in which said switching elements are constituted by FET's.

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