

[54] SWITCHING DEVICE

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[58] Field of Search 328/129, 130, 72, 73, 74, 328/75, 37; 331/111, 113

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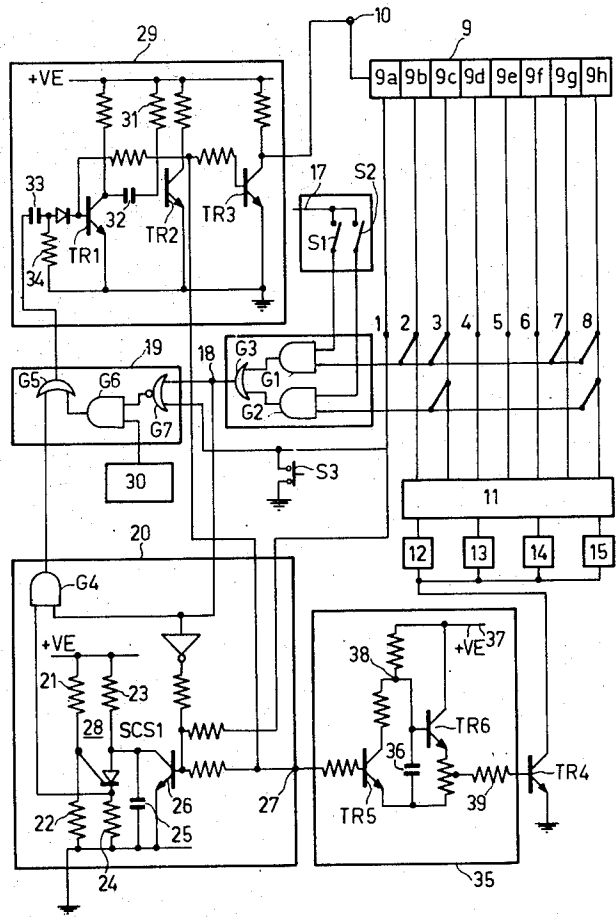
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[57] ABSTRACT

A switching and timing device comprising a series of control points each of which is associated with a combination of switching. Clock pulses cause actuation information to be advanced to control points in sequence, at either low rates for performance of functions, or at high rates to omit functions associated with selected control points. Operation of switching elements is inhibited for high pulse rates.

5 Claims, 10 Drawing Figures



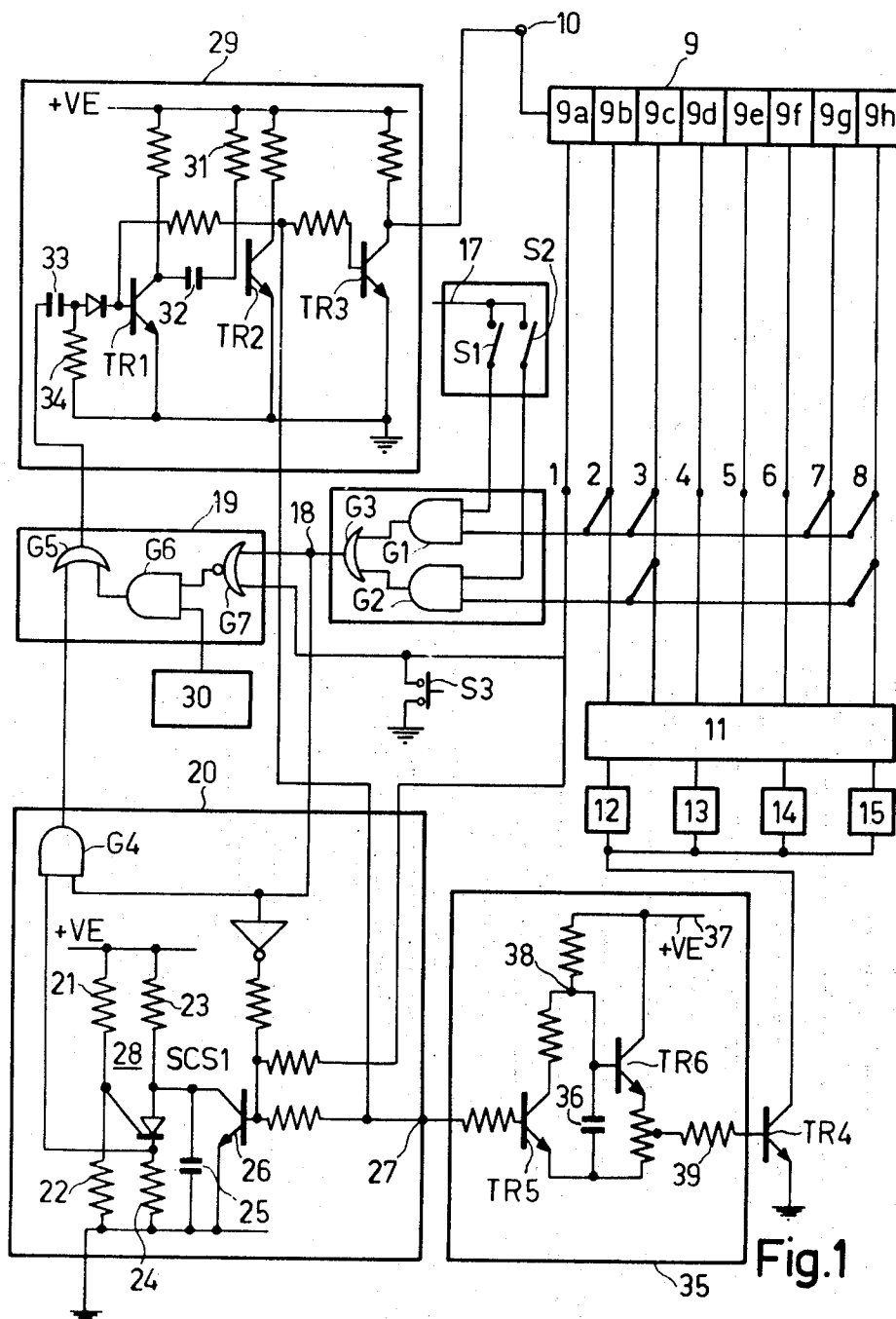


Fig.1



Fig. 2a

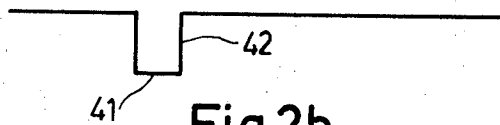
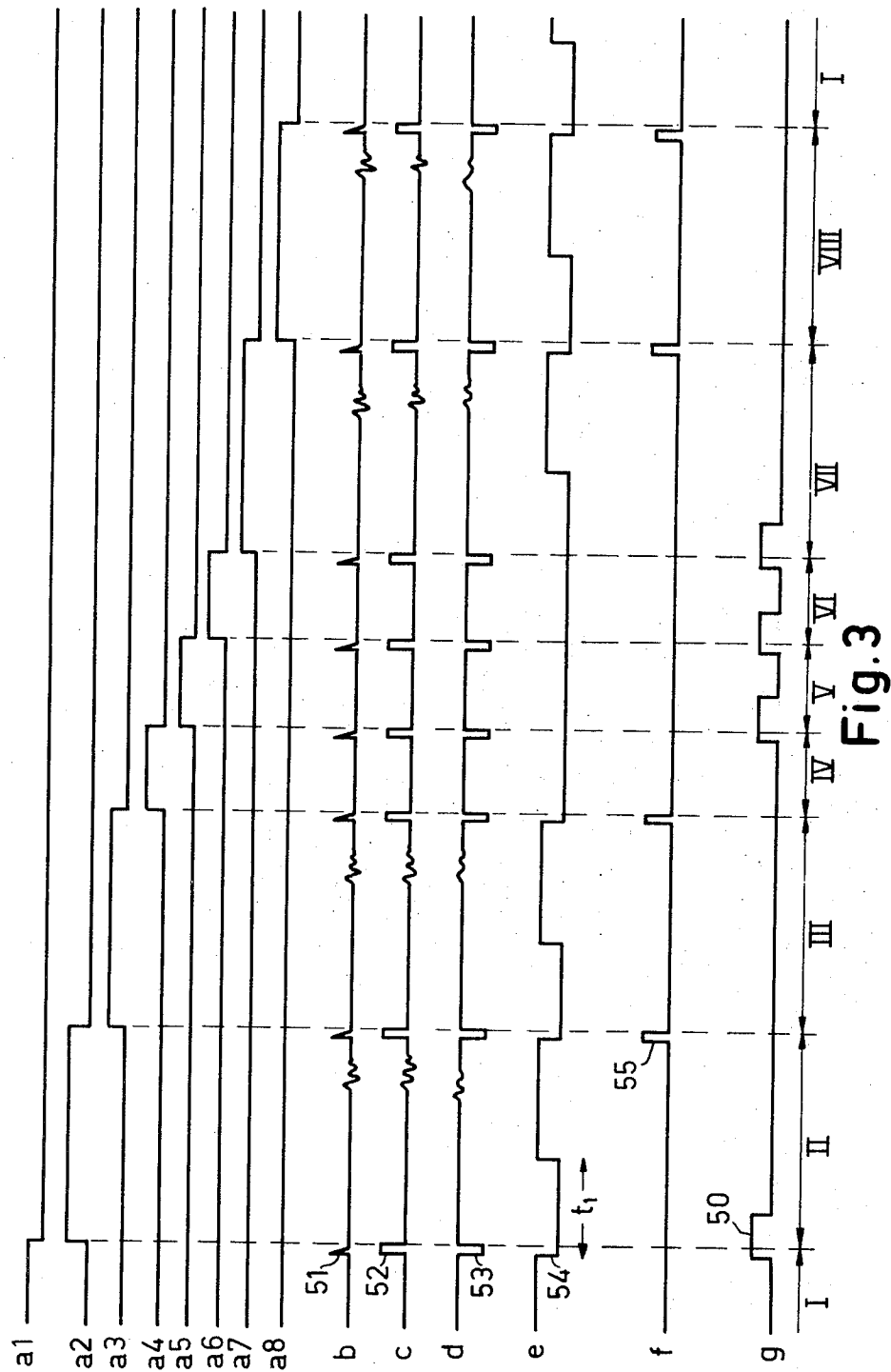


Fig. 2b



Fig. 2c



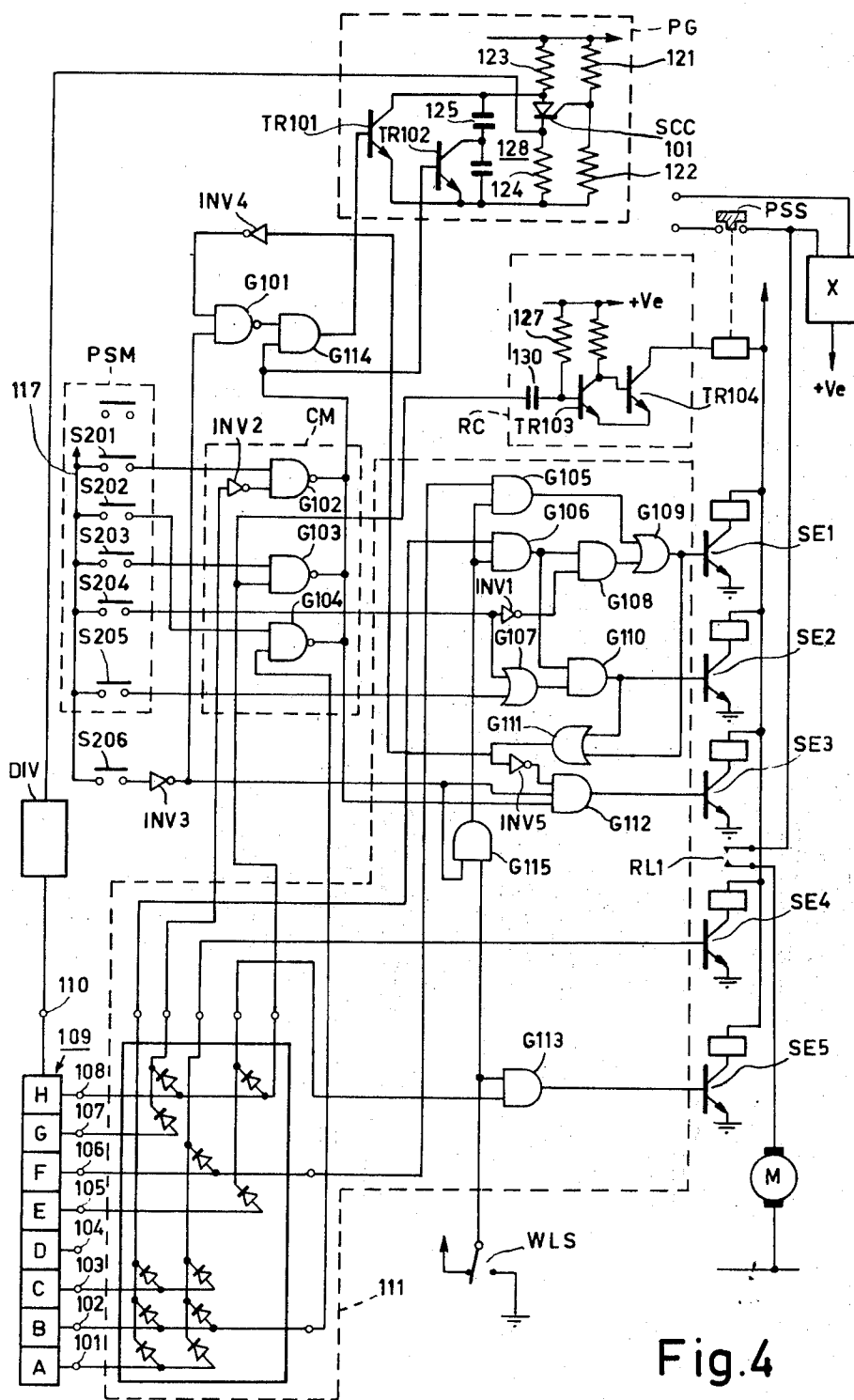


Fig.4

PROGRAMME SELECTED	1 FILL AGITATE 4 min	2 FILL AGITATE 4 min	3 FILL AGITATE 4 min	4 PUMP 4 min	5 SPIN 4 min	6 FILL AGITATE 4 min	7 PUMP 4 min	8 SPIN 4 min
SUPER WASH	*	*	*	*	*	*	*	*
	(warm fill)	(warm fill)	(warm fill)			(cold fill)		
NORMAL WASH	*		*	*	*	*	*	*
SPIN DRY							*	*

Fig.5

PROGRAMME SELECTED	1 FILL AGITATE 4 min	2 FILL AGITATE 4 min	3 FILL AGITATE 4 min	4 PUMP 4 min	5 SPIN 4 min	6 FILL AGITATE 4 min	7 PUMP 4 min	8 SPIN 4 min
SUPER WASH	*	*	*	*	*	*	*	*
	(cold fill)	(cold fill)	(cold fill)			(cold fill)		
SUPER WASH and HOT WASH	*	*	*	*	*	*	*	*
	(hot fill)	(hot fill)	(hot fill)			(cold fill)		
SUPER WASH and WARM WASH	*	*	*	*	*	*	*	*
	(warm fill)	(warm fill)	(warm fill)			(warm fill)		
SUPER WASH and DRIP DRY	*	*	*	*	*	*	*	*

Fig.6

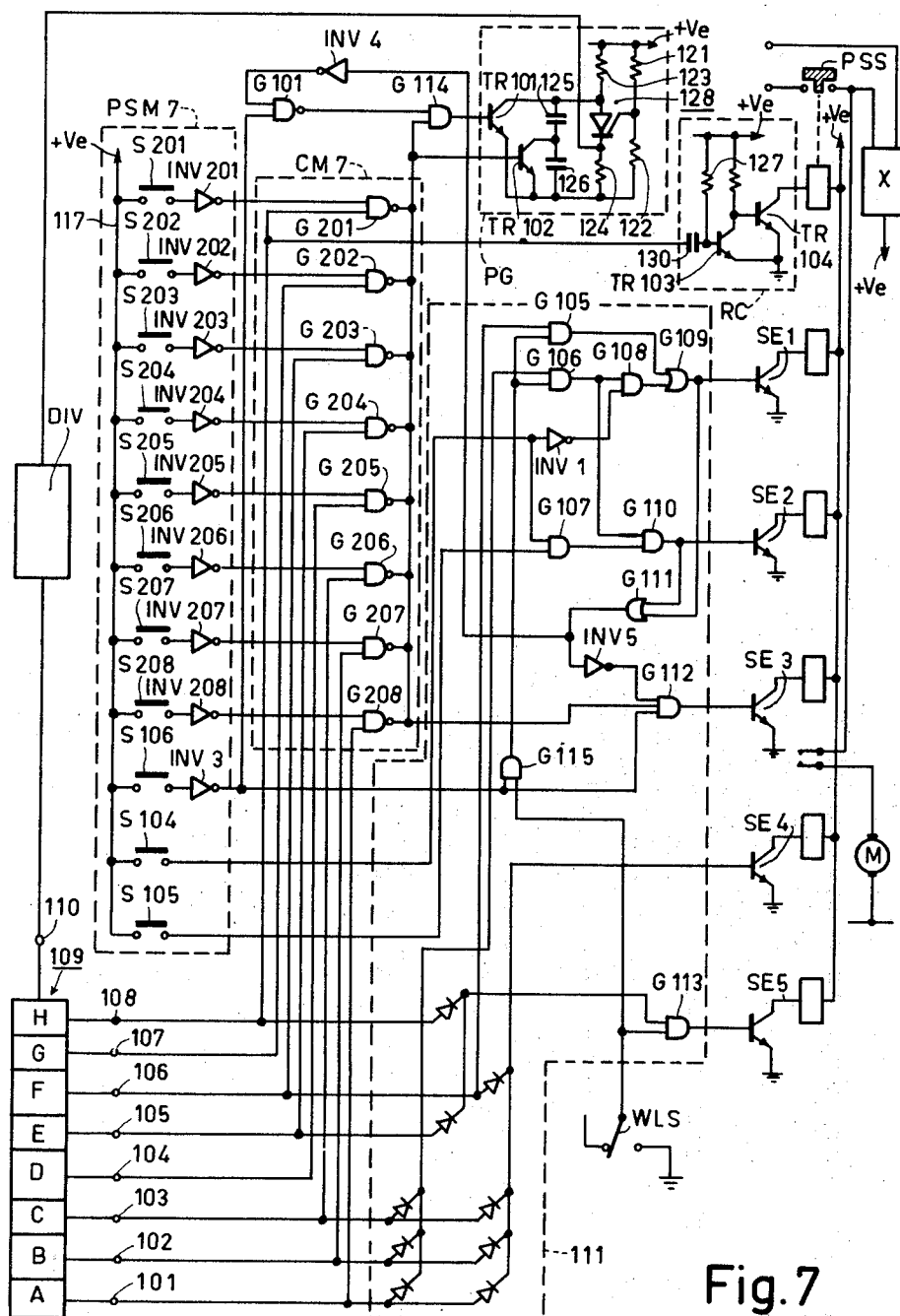


Fig. 7

SWITCHES ACTIVATED	FILL AGIT. 4 min	FILL AGIT. 4 min	FILL AGIT. 4 min	PUMP	SPIN	FILL AGIT. 4 min	PUMP	SPIN
S201 → S208	*	*	*	*	*	*	*	*
S201, S203 → S208	*		*	*	*	*	*	*
S207 & S205							*	*

Fig.8

SWITCHING DEVICE

The present invention relates to switching devices of the kind in which a series of switching functions are controlled by the stages of a shift register driven by timing pulses. Such switching devices are known and one such known switching device is driven by timing pulses produced in such a way that the time intervals between the pulses are determined by reference voltages present at the output of individual stages of the shift register during "on" states of the respective register stages.

With the known devices, there is the drawback that practical difficulties arise when attempting to provide variations of the series of switching functions. In this regard, different kinds of variation may be desired. One kind permits variation by the selective omission of one or more functions from the series. Another kind permits variation by the substitution of certain functions by different functions. The drawback is emphasized if it is desired to furnish a simply operated device which permits selection at will of any particular one or other of several variations.

The present invention seeks to improve upon the known devices.

The switching device in accordance with the invention comprises a plurality of control points, each control point of the plurality being associated with a combination of one or more switching elements whereby the switching elements for each combination are adapted to be actuated by the presence of actuation information at the control point associated therewith, a shift register having states related to the control points of the plurality for supplying actuation information to the control points of the plurality in a predetermined sequence under the control of timing pulses which advance the states of the register whereby a series of combinations of switching functions may be performed, the intervals between occurrence of consecutive timing pulses determining the period of time for which actuating information is present at the respective control points, pulse supply means capable of supplying to the shift register timing pulses either recurring at relatively long intervals or recurring at relatively short intervals, program selection means for providing selection information and comparison means for comparing selection information thus provided with actuation information present at the control points for determining, during the course of the selected program, whether the timing pulses supplied to the shift register recur at relatively long intervals or recur at relatively short intervals.

In one kind of switching device in accordance with the invention the said pulse supply means include a first pulse source for producing pulses recurring at relatively long intervals, a second pulse source for producing pulses recurring at relatively short intervals and a selection circuit arrangement permitting timing pulses for supply to the said shift register to be derived from either the first pulse source or the second pulse source.

In an alternative kind of switching device in accordance with the invention the said pulse supply means includes a pulse source from which timing pulses may be derived for supply to the shift register, the pulse source being adapted to operate in either a first mode of operation or a second mode of operation, the pulse source producing pulses recurring at relatively long intervals when operating in the first mode and producing

pulses recurring at relatively short intervals when operating in the second mode. With this kind of switching device the said pulse source may be in the form of a relaxation oscillator, the repetition frequency of which is determined by the series combination of two capacitors one of which is shunted by the collector-emitter path of a transistor adapted to be rendered either conductive so that the pulse source operates in the said first mode or non-conductive so that the pulse source operates in the said second mode.

With either kind of switching device the said pulse supply means may include a pulse source from whence timing pulses may be derived for supply to the shift register, the device being responsive to information representing the existence of a physical condition, such as the existence of a particular temperature or the existence of a particular level of liquid at a part of an apparatus in which the switching device is incorporated, the device being arranged to inhibit the operation of the pulse source to prevent advancement of the shift register into one or more predetermined states in the absence of the information representing existence of a physical condition.

If desired, in a switching device according to the invention the said program selection means may be adapted to alter one or more of said combinations of one or more switching elements upon alteration of program selection. In addition, or as an alternative thereto, a manually operable switching element combination alteration means may be incorporated in the device whereby alteration to one or more of said combinations of one or more switching elements may be accomplished independently of the program selection means.

The program selection means of the device may be relatively simple or may be complex depending upon the application for which the switching device is intended. It will be appreciated that the recurrence period of the timing pulses recurring at relatively short intervals is chosen to be only a few milliseconds for most application and since each timing pulse produced advances the state of the shift register, the provision of selection information by the program selection means such that during the course of a selected program a timing pulse occurs at a relatively short interval after a preceding timing pulse results in a corresponding state of the shift register being occupied for a few milliseconds only also or, in other words, the shift register being rapidly advanced. Under such conditions, actuation information supplied to the appropriate control points and the resultant actuation of switching elements related to the state of the shift register in question is of such short duration that for many applications of the device it may, for practical purposes be regarded as an omission of one of the combinations of switching functions from the series since the duration of the combination concerned is compressed. For other applications, according to another aspect of the invention, means may be provided for inhibiting the actuation of the switching elements for the total duration of a succession of timing pulses recurring at relatively short intervals whereby one or more combinations of switching functions may be omitted from the series by the supply to the shift register of timing pulses recurring at relatively short intervals.

As an alternative to providing such means for inhibiting the actuation of the switching elements for the total

duration of a succession of timing pulses recurring at relatively short intervals, suppression means may be provided, the suppression means being responsive to the said program selection information and/or to information representing the existence of a physical condition and/or to the actuation information present at the said control point and being arranged to either prevent actuation of one or more of the switching elements of a combination of a series related to the program in question or actuation and counteract the effect of such actuation.

It is advantageous in some applications for the said program selection means to comprise a plurality of program selection switching members each associated with a particular program, each member being adapted to occupy either a selected state or a non-selected state and each so related to the other members that only one of the plurality may occupy the selected state at a given time, the plurality of switching members collectively providing the said selection information, characterized in that when all members of the plurality occupy the non-selected state, the selection information so provided in combination with the said actuation information supplied to the control points determines the performance of a basic series of combinations of said switching functions, whereas when one of the members of the plurality occupies the selected state the selection information so provided in combination with the said actuation information supplied to the control points determines the performance of the basic series of combinations of said switching functions modified by the omission of one or more of the combinations from the basic series and/or by the compression of the duration of one or more of the combinations of the basic series and/or by the substitution of one or more of the combinations in the basic series by a different combination. However, for other applications of the invention it is advantageous for the said program selection means to comprise a plurality of switching members each associated with a portion of a basic series of combinations of switching functions, each adapted to occupy either a selected state or a non-selected state, the plurality of switching members collectively providing the said selection information, characterized in that when all members of the plurality occupy the selected state, the selection information so provided in combination with the said actuation information supplied to the control points determines the performance of a basic series of switching functions whereas when one of the members of the plurality occupies the non-selected state the said selection information so provided in combination with the said actuation information supplied to the control points determines the performance of the basic series of combinations of switching functions modified by the omission from the basic series of that portion associated with the member occupying the non-selected state or by the compression of the duration of that portion of the basic series associated with the member occupying the non-selected state.

In a switching device where means for inhibiting the actuation of the switching elements is provided, preferably the said timing pulses recurring at relatively short intervals are caused to recur periodically and for every timing pulse supplied to the shift register, the actuation of the switching elements is inhibited for a period of time commencing at or prior to the commencement of the timing pulse and terminating at or after elapse-

of a period equal to the recurrence period of the timing pulses recurring at relatively short intervals. Still preferably, every timing pulse applied to the shift register is derived from a reference pulse generator producing reference pulses of fixed duration, the leading edges of the reference pulses being employed to determine the commencement of the period of inhibiting of the actuation of the switching elements and the trailing edges of the reference pulses being employed to determine the instant of triggering the shift register. With such an arrangement, the reference pulse generator may be arranged to be triggered either from a source of trigger pulses recurring at relatively long intervals or from a source of periodically recurring trigger pulses recurring at relatively short intervals.

Several embodiments of the invention will now be described with reference to the accompanying drawings in which:

FIG. 1 is a schematic diagram of an embodiment of the invention.

FIGS. 2a-2c illustrate waveforms to assist in describing the operation of part of the circuit illustrated in FIG. 1.

FIG. 3 illustrates waveforms produced at various parts of the circuit of FIG. 1 in the course of operation of a particular program.

FIG. 4 is a schematic diagram of another embodiment of the invention.

FIG. 5 is a chart to assist in describing the operation of the circuit of FIG. 4.

FIG. 6 is another chart to assist in describing the operation of the circuit of FIG. 4.

FIG. 7 is a schematic diagram of a further embodiment of the invention.

FIG. 8 is a chart to assist in describing the operation of the circuit of FIG. 7.

Referring now to the switching device diagrammatically illustrated in FIG. 1.

In FIG. 1, the control points 1, 2, 3, 4, 5, 6, 7 and 8 are each connected to the output of a stage of the shift register 9 having stages 9a, 9b, 9c etc., control point 1 being connected to the output of stage 9a, control point 2 being connected to the output of stage 9b etc. The shift register 9 is driven by timing pulses supplied via the terminal 10. The shift register 9 is of known kind and operates in a known manner. In an initial state, the control point 1 is in the "high" state with the remaining control points all at the "low" state. The terms "high" and "low" indicate, in the present instance, a predetermined positive voltage level and a zero voltage level respectively.

At the occurrence of the first timing pulse supplied via the terminal 10, the shift register 9 is advanced so that the control point 2 goes to the "high" state, the control point 1 goes to the "low" state and control points 3 to 7 remain in the "low" state. This condition remains until the occurrence of the next timing pulse whereupon the control point 3 goes to the "high" state and control point 2 returns to the "low" state, control point 1 and control points 4 to 8 remain in the "low" state. The process is continued with the "high" state being transferred sequentially along the plurality of control points 1 to 8 at the occurrence of successive timing pulses. When the control point 8 is at the "high" state, the next succeeding timing pulses results in the shift register 9 being returned to its initial state.

The control points 1 to 8 are connected via the matrix 11 to the switching elements 12, 13, 14 and 15. The switching elements 12, 13, 14 and 15 are each in the form of a transistor provided with a load in its collector circuit. The load may be in the form of a relay, a lamp, a resistance etc. The connections from the control points 2 to 8 to the switching elements 12, 13, 14 and 15 are such that each of the control points 2 to 8 is associated with a combination of one or more of the switching elements 12 to 15, each control point being connected via the matrix 11 to the base electrodes of the transistors of the switching elements associated therewith.

Accordingly, if a particular control point is in the "high" state then the base electrodes of the transistors of the switching elements with which that particular control point is associated will also be in the "high" state, and if the particular terminal is in the "low" state, then the base electrodes of the transistors of the switching elements with which that terminal is associated will also be in the "low" state. The transistors of the switching elements are arranged so that each transistor is cut off when its base electrode is at the "low" state and is conducting when its base electrode is at the "high" state. Thus, the switching elements 12 to 15 may be regarded as being actuated when the base electrode of their respective transistor is in the "high" state, and the information provided by the control points 2 to 8 being in either the "high" or the "low" state may be regarded as actuating information.

The emitter electrodes of the transistors of the respective switching elements 12 to 15 are connected to earth via the collector emitter path of a single transistor TR4 to the base electrode of which is supplied a control potential in a manner to be discussed later. The foregoing description of the operation of the switching elements 12 to 15 assumes that the control potential at the base of the transistor 16 is such that the transistor TR4 is in the "on" state.

Two program selection switches S1 and S2 are provided. One side of each of the switches S1 and S2 is connected to the positive supply line 17. The other side of the switch S1 is connected to an input of the AND gate G1, whereas the other side of the switch S2 is connected to an input of the AND gate G2. Control points 2, 3, 7 and 8 are connected to the other input of the AND gate G1 whereas control points 3 and 8 are connected to the other input of the AND gate G2. The output of the AND gates G1 and G2 are connected to separate inputs of the OR gate G3. The output of the OR gate G3 is fed via the terminal 18 to both the gating network 19 and to the timing generator 20. The timing generator 20 consists of a simple relaxation oscillator denoted generally by the numeral 28 and comprising the silicon controlled switch SCS 1, the resistances 21, 22, 23, 24 and the capacitance 25. The values of the resistances 21, 22 and 23 and that of the capacitance 25 are so chosen that the period of the oscillator 28 is approximately 2 minutes, i.e., at 2 minute intervals after initiation of the oscillator 28, a pulse of short duration is produced at the cathode of the switch SCS1. The capacitance 25 is bridged by the collector/emitter path of the transistor 26 which is provided for disabling or resetting the oscillator 28. If the base electrode of the transistor 26 is "high", the collector/emitter path of the transistor 26 conducts short circuiting the capacitance 25. Accordingly, a positive pulse applied via the termi-

nal 27 resets the oscillator 28 by discharging the capacitance 25. Alternatively, if the control point 1 is "high" or the terminal 18 is "low," the oscillator 28 is disabled since capacitance 25 is short circuited.

The output of the oscillator 28 is fed to an input of the AND gate G4, the other input of which is connected to the terminal 18. Accordingly, if the terminal 18 is "high", then the oscillator 28 functions and the oscillator output is applied via the gate G4 and the OR gate G5 to the reference pulse oscillator 29 for triggering purposes.

The shaping network 30 is connected to a source of alternating voltage (not shown) having a frequency of 50 cycles per second which may, for example, be a source of alternating mains voltage and converts the alternating voltage into a square wave pulse train, having the same frequency. The output of the network 30 is continuously supplied to one of the inputs of the AND gate G6. The other input of the AND gate G6 is connected to the output of the NOR gate G7 which has 2 inputs. One of the inputs of the gate G7 is connected to the terminal 18 and the other input of the gate G7 is connected to the control point 1. The control point 1 may be connected to earth by operation of the starting switch S3. If both of the inputs of the NOR gate G7 are in the "low" state then the output of the gate G7 is "high" and the square wave output of the network 30 will be produced at the output of the AND gate G6 and will be fed to the input of the reference pulse generator 29 via the OR gate G5. However, if either or both of the inputs of the NOR gate G7 are in the "high" state then the output of the gate G7 will be "low" and the gate G6 will remain closed thus disconnecting the output of the shaping network 30 from the generator 29.

The reference pulse generator 29 comprises a monostable multivibrator constituted by the transistors TR 1 and TR2 which delivers a positive going fixed width output pulse at the collector electrode of the transistor TR2 each time the generator is triggered. In known manner, the width of the output pulse is determined by the value of the resistance 31 and that of the capacitance 32. The generator is triggered whenever a triggering pulse appears at the output of the gate G5, such a triggering pulse being conveyed to the base electrode of the transistor TR1 via the differentiating network constituted by the capacitance 33 and the resistance 34. The pulse 40 of FIG. 2a depicts a typical positive going reference pulse produced at the collector electrode of the transistor TR2. The pulse 40 has a duration of 5 milliseconds. Output pulses from the collector of the transistor TR2 are supplied to the terminal 27, to the inhibiting circuit 35 and to the base of the transistor TR3. The transistor TR3 functions as an inverter and for each reference pulse 40 applied to its base electrode, a negative going pulse 41, of FIG. 2b, also having a duration of 5 milliseconds is produced at the collector electrode of the transistor TR3.

The trailing edge 42 of each negative going pulse 41 is employed to advance the state of the shift register 9. As mentioned, the output pulse produced at the collector electrode of the transistor TR2 is also applied to the inhibiting circuit 35. The inhibiting circuit 35 comprises a re-triggable monostable multivibrator including the transistors TR5 and TR6. The operation of such a monostable multivibrator is well known and briefly is as follows. The capacitance 36 is connected to be charged from the positive supply line 37 via the resis-

tance 38 so that when the apparatus is switched on, the capacitance 36 becomes charged after approximately 30 milliseconds with the transistor TR6 conducting and the transistor TR5 cut off. The capacitance 36 is charged to a predetermined voltage determined by the value of the resistance 39 and the voltage drop across the base emitter path of the transistor TR6. At the occurrence of a positive going input pulse at the base of the transistor TR5, the transistor TR5 will conduct, thereby rapidly discharging the capacitance 36 and cutting off the transistor TR6. At cessation of the input pulse, the capacitance 36 commences to charge again. Whilst the transistor TR6 is conducting, a positive voltage is supplied to the base electrode of the transistor TR4 from the base resistance of the transistor TR6 causing the former to conduct but when the transistor TR6 is cut off, owing to the discharge of the capacitance 36, the voltage across the emitter resistance 39 falls, causing the transistor TR4 also to be cut off. The value of the resistance 38 and that of the capacitance 36 are chosen so that for every input pulse applied to the transistor TR5, the transistor TR6 will remain cut off for 30 milliseconds following each input pulse whilst the capacitance 36 is recharged to the predetermined value. Accordingly, if a further input pulse is applied before termination of the 30 milliseconds cut off period, i.e., before the capacitance 36 has sufficiently recharged for the transistor TR6 to recommence conduction, the capacitance 36 is discharged once more and the charging process is repeated.

Accordingly, each time a positive going pulse 40 is produced at the collector electrode of the transistor TR2, the transistor TR4 is cut off and the switching elements 12, 13, 14 and 15 are inhibited for a period commencing with the occurrence of the leading edge of the pulse 40 which lasts for a period of at least 30 milliseconds after the termination of the pulse 40. The pulse 43 of FIG. 2c shows the negative going pulse produced at the base electrode of the transistor TR4 for every generated reference pulse 40. Whereas the duration of the pulse 40 is 5 milliseconds, the duration of the pulse 43 is 35 milliseconds. Both pulses commence at the same instant. Of course, the pulse 43 denotes the period of time for which the transistor TR4 is in the cut-off state.

The operation of the circuit of FIG. 1 can be explained in association with FIG. 3 as follows. With the power supplies to the circuit switched on and assuming the switch S1 is closed to select the desired programme, the shift register 9 is in its initial state with the control point 1 in the "high" state and the remainder of the control points 2 to 8 in the "low" state. The "high" state of the control point 1 ensures that the transistor 26 is conducting and the oscillator 28 is disabled.

Under these conditions, the switch S1, being closed, has no effect at the initial state of the register 9; although the positive potential of supply line 17 is connected to an input of the gate G1, the output of the gate G1 remains "low" because the other input of the gate G1 (derived from the respective control points) is in the "low" state. Thus, the output of the OR gate G3 is "low" so that the input of the NOR gate G7 connected to the gate G3 is "low" and the input of G7 connected to the control point 1 is "high". Accordingly, the output of the gate G7 is also "low" ensuring that the AND gate G6 is closed and the output of the shaping network 30 cannot be supplied to the reference pulse generator

29. Since no triggering information is supplied to the reference pulse generator 29 from either the oscillator 28 or from the shaping network 30, no timing pulses are produced by the generator 29 and the shift register 9 remains in the initial state.

If now the start switch S3 is operated, the program associated with the switch S1 is commenced and, in this regard, the wave forms of FIG. 3 illustrate the wave forms produced at the various parts of the circuit of FIG. 1 as follows:

FIGS. 3a₁ to 3a₈ illustrate respectively the voltage wave forms present at the control points 1 to 8.

FIG. 3b illustrates the wave forms present at the base electrode of the transistor TR1.

FIG. 3c illustrates the wave forms present at the collector of the transistor TR2.

FIG. 3d illustrates the wave forms present at the collector of the transistor TR3.

FIG. 3e illustrates the wave forms present at the base of the transistor TR4.

Fig. 3f illustrates the wave forms present at the cathode of the silicon control rectifier SCS 1.

FIG. 3g illustrates the wave forms present at the output of the gate G6.

With the operation of the start switch S3, the control point 1 is momentarily shorted to earth and the output of the NOR gate G7 becomes "high," momentarily opening the gate G6 and allowing the single pulse 50 of FIG. 3g to be applied via the gate G6 and the gate G5 to the reference pulse generator 29, resulting in the differentiated pulse 51 of FIG. 3b being produced at the base of the transistor TR1. The fixed duration pulse 52 is thus generated at the collector electrode of the transistor TR2 so that the inhibiting circuit 35 is triggered and the switching elements 12 to 15 are inhibited from the instant coinciding with the leading edge of the pulse 52. The inhibition period is illustrated by the pulses 54 of FIG. 3e in which the time t_1 is approximately 35 milliseconds. Although the pulse 52 is also applied to the terminal 27, it has no effect since the transistor 26 is already in the ON state. The trailing edge of the negative going pulse 53 of FIG. 3d, generated simultaneously with the pulse 52, advances the shift register 9 to the second state. It will be appreciated that the trailing edge of the pulse 53 occurs 5 milliseconds later than the leading edge of the pulse 52 so that the switching elements 12 to 15 are in a state of inhibition during advancement of the state of the register 9.

Advancement of the shift register 9 to the second state results in the "high" state formerly present at the control point 1 to be transferred to the control point 2 and since the switch S1 is already closed, both inputs of the gate G1 are now "high," the output of gates G1 and G3 also become "high" and the output of the gate G7 becomes "low" immediately closing the gate G6 again to prevent any further pulses from the network 30 from reaching the generator 29. Simultaneously, since the terminal 18 is now "high," the transistor 26 is cut off and the oscillator 28 commences a cycle of oscillation. Since also the control point 2 is now in the "high" state, the base electrodes of the transistors of the respective switching elements 12 to 15 associated with the control point 2 are also placed in the "high" state so that the switching elements concerned will be actuated when the inhibition period terminates and the transistor TR4 is switched on again.

As mentioned, the period of oscillation of the oscillator 28 is approximately 2 minutes. Accordingly, the shift register 9 remains in the second state for an equivalent period. At the end of the 2 minute period, the oscillator 28 produces a positive going output pulse 55 of short duration at the cathode of the silicon control switch SCS 1. As the terminal 18 is "high," the gate G4 is open and the pulse 55 is conveyed via the gates G4 and G5 to the input of the reference pulse generator 29 whereupon another pulse 52 is generated again resulting in inhibition of the switching elements 12 to 15 and the triggering of the shift register 9 into the third state.

The process described in relation to the second state is thus repeated once more except that since the "high" state has been transferred to the control point 3, the switching elements associated with the control point 3 are actuated when the second period of inhibition is completed. At the completion of the third state of the shift register 9, another pulse 55 is produced by the oscillator 28, triggering the register 9 into its fourth state,

In the fourth state, the control point 4 becomes "high" and the gate G1 is closed so that the oscillator 28 is disabled and the gate G6 is opened so that the output of the network 30 is supplied to the generator 29.

The fourth state of the register 9 follows a similar pattern of operations to that of the first or initial state except that the gate G6 is not closed at the termination of the fourth state because, unlike the control point 2, the control point 5 is not connected to an input of the gate G1. Under these conditions, the oscillator 28 remains disabled and the gate G6 remains open whilst allowing further pulses recurring at relatively short intervals to be supplied from the network 30 to the generator 29 thereby advancing the state of the shift register rapidly to progress through the fifth state and the sixth state. In the seventh state, the control point 7 is, of course, "high" so that the gate G6 is closed and the oscillator 28 is enabled to commence a further cycle of oscillation. Thus, the seventh state and the eighth state of the register 9 follow a similar pattern of operations to the second and third states. At the conclusion of the eighth state, the register 9 is returned to its initial state completing the program associated with the switch S1.

It will be appreciated that the reference pulses 52 associated with the commencement of the fourth, fifth and sixth states of the register each initiates a period of inhibition of the switching elements 12 to 15 which is of greater duration than the interval between those pulses so that the switching elements 12 to 15 remain inhibited for the total duration of the succession of the relevant reference pulses and the shift register 9 is therefore "rapidly advanced" through the fourth, fifth and sixth states without the switching elements associated with the control points 4, 5 and 6 being actuated for the selected program under discussion i.e., the program associated with the switch S1. Of course, during the program there is no rapid advance of the shift register 9 in the case of the second, third, seventh and eighth states of the register 9. Each of these states has a duration of 2 minutes during which the combinations of the switching elements 12 to 15 associated with the respective control points 2, 3, 7 and 9 are actuated.

Now, in the program associated with the switch S2, the initial state of the register 9 would be similar to the

initial state in the case of the program associated with the switch S1. However, there would be a rapid advancement of the register through the second state, accompanied by inhibition of the switching elements 12 to 15, the third state would be for a duration of 2 minutes with the switching elements associated with the control point 3 actuated, there would be rapid advancement through the fourth, fifth, sixth and seventh states accompanied by inhibition of the switching elements 12 to 15 and the eighth state would be for a period of 2 minutes with the switching elements associated with the control point 8 actuated.

Referring now to the switching device diagrammatically illustrated in FIG. 4:

The switching device of FIG. 4 is intended to be employed for controlling switching operations required in an automatic clothes washing machine of the kind in which a washing container and an impeller having a common axis of rotation and capable of being independently driven by an electric motor are located within a wash tub to which hot or cold water may be supplied or removed. As is well known, clothes may be washed and partly dried in such washing machines by suitably arranging the sequence and/or repetition of operations including water supply, impeller agitation, water removal, container spinning, etc.

In FIG. 4, the control points 101, 102, 103, 104, 105, 106, 107 and 108 are each connected to the output of a stage of the shift register 109 having stages 109A, 109B, 109C etc. The shift register 109 is driven by timing pulses supplied via the terminal 110. The shift register 109 is of known kind and operates in a known manner. When the start switch PSS is closed, the mains voltage is supplied to the power supply circuit X and accordingly appropriate DC voltages are applied from the power supply circuit X to the respective DC supply lines (not shown). In addition, mains voltage is supplied to the mains supply line Y. When the shift register is in an initial state, with the switch PSS closed, the control point 101 is in the "high" state with the remaining control points all at the "low" state.

At the occurrence of the first timing pulse supplied via the terminal 110, the shift register 109 is advanced so that the control point 102 goes to the "high" state, the control point 101 goes to the "low" state and control points 103 to 108 remain in the "low" state. This condition remains until the occurrence of the next timing pulse whereupon the control point 103 goes to the "high" state and the control point 102 returns to the "low" state, the control point 101 and control points 104 to 108 remain in the "low" state. The process is continued with the "high" state being transferred sequentially along the plurality of control points 101 to 108 at the occurrence of successive timing pulses. When the control point 108 is at the "high" state, the next succeeding timing pulse results in the shift register 109 being returned to its initial state and simultaneously the start switch PSS is returned to the open condition owing to the energisation of the solenoid SOL by the operation of the reset circuit RC when the state at control point 108 changes from the "high" state to the "low" state.

The control points 101 to 108 are connected via the matrix 111 to one or more of the switching elements SE1, SE2, SE3 and SE4, SE5. The switching elements SE1, SE2, SE3 and SE4, SE5 are each in the form of a transistor provided with a load in its collector circuit.

The load of the individual switching elements may be in the form of a relay, a lamp, a resistance, a solenoid, etc. However, in the present instance, the load of the switching element SE1 is in the form of solenoid for actuating a cold water supply valve for supplying cold water to the washtub of the machine, the load of the switching element SE2 is a similar solenoid for actuating a hot water supply valve, the load of the switching element SE3 is the winding of a relay RL1, the load of the switching elements SE4 and SE5 are each in the form of a solenoid for respectively actuating a mechanism for causing the impeller of the machine to "agitate" or actuating a mechanism for causing the washing container to spin, provided that the motor M is running.

The connections from the control points 101 to 108 to the switching elements SE1 to SE5 are such that each of the control points is associated with a combination of one or more of the switching elements SE1 to SE5, each control point being connected either directly or indirectly to the base electrodes of the transistors of the switching elements associated therewith.

Accordingly, if a particular control point is in the "high" state then depending upon programme selection, the control electrodes of the transistors of the switching elements with which that particular control point is associated will also be in the "high" state and if the particular point is in the "low" state, then the electrodes of the transistors of the switching elements with which that control point is associated will also be in the "low" state. The transistors of the switching elements are arranged so that each transistor is cut off when its base electrode is at the "low" state and is conducting when its base electrode is at the "high" state. Thus, the switching elements SE1 to SE5 may be regarded as being actuated when their respective base electrodes are in the "high" state, and the information provided by the control points 101 - 108 being in either the "high" or the "low" state may be regarded as actuating information.

A program selection means PSM is provided which includes a switch assembly of the kind in which the two push-button operated switches, S201 and S202, are mechanically interlocked with each other so that only one switch of the assembly can remain in the closed condition at a given time. The switch assembly also incorporates a push-button, hereinafter preferred to as the blank push-button, which is not capable of closing any of the switches but is coupled with the mechanical interlocking mechanism in such a manner that, if operated, either switch of the assembly occupying the closed condition is opened.

The program selection means PSM also includes the auxiliary push-button operated switches S203, S204 and S205 which are mechanically independent of the pushbutton switch assembly of which the switches S201 and S202 form part. Switch S206 is a further auxiliary pushbutton operated switch which may, or may not, form part of the program selection means PSM depending upon the requirements. One side of each of the switches S201 to S206 is connected to the positive supply line 117. The other side of the switch S201 is connected to an input of the NAND gate G102, the other side of the switch S202 is connected to an input of the NAND gate G104, the other side of the switch S203 is connected to an input of the NAND gate G103, the other side of the switch S104 is connected to an input

of the OR gate G107 and also to an input of the AND gate G108 via the inverter INV1, the other side of the switch S205 is connected to the other input of the OR gate G107 whereas the other side of the HOLD switch S206 is connected via the inverter INV3 to an input of the NAND gate G101, to an input of the AND gate G112 and to an input of the AND gate G115.

The pulse supply means PG comprises a relaxation oscillator 128 constituted by the silicon controlled switch SCS101, the resistors 121, 122, 123 and 124, and the capacitance 125 and 126. The oscillator 128 is capable of being operated in any one of two alternative modes, the particular mode of operation depending upon the state of conductivity of the transistor TR102. When the transistor TR102 is non-conductive, the period of oscillation is determined by the values of the resistances 121, 122 and 123, and by the resultant values of the series combination of the capacitances 125 and 126. The selection of the values of the respective components is such that in this mode of operation the period of oscillation of the oscillator 128 is approximately 5 milliseconds. Alternatively, when the transistor TR102 is in the conductive state, the period of oscillation of the oscillator 128 is determined by the values of the resistances 121, 122 and 123, and by the value of the capacitance 125. The respective components are selected so that in this mode of operation the period of oscillation is approximately 30 seconds. Thus, the ratio of the period of oscillation in one mode to the period of oscillation to the other mode is of the order of 1:6000. In either mode of operation, a positive going output pulse of short duration is produced across the resistance 124 for every cycle of oscillation. The transistor TR102 is non-conductive when its base electrode is at zero potential, or in other words when the base potential is "low". The transistors TR102 is rendered conductive by application to the base electrode of a positive potential greater than approximately 0.6 volts, or in other words when the base potential is "high".

The series combination of the capacitances 125 and 126 are shunted by the collector-emitter path of the control transistor TR101. Application of a "high" voltage to the base of the transistor TR101 causes the transistor to conduct, short-circuiting the series combination of the capacitances 125 and 126 and thereby inhibiting operation of the oscillator 128 altogether. On the other hand, application of a "low" voltage to the base of the transistor TR101 ensures that the transistor is non-conductive and that the oscillator 128 operates in one mode of operation or the other depending upon the state of conductivity of the transistor TR102 and the presence of suitable operating potentials.

The output pulses of the pulse supply means PG are derived from across the resistance 124 and supplied to the divider DIV, the output pulses of which are fed to the terminal 110 and serve as timing pulses for triggering the shift register 109. The divider DIV is in the form of an eight-bit shift register which produces an output pulse for every eighth input pulse.

A comparison means CM includes the NAND gates G102, G103 and G104 the outputs of which are connected to the timing line TL. The state of the timing line TL determines the mode of operation of the oscillator 128.

The operation of the switching device of FIG. 4 will now be described in conjunction with the chart of FIG. 5 which sets out in tabular form a basic program and

modifications of that basic program for different settings of the program selection means.

The basic program is followed when the start button PSS is closed provided the "blank" push-button has previously been selected and none of the switches S203, S204, S205 and S206 are selected. The "blank" push-button may conveniently be marked "superwash" and the word "superwash" is employed in the chart of FIG. 5 to denote this basic program. In the chart of FIG. 5 there are eight columns, numbered accordingly, which coincide with the eight states of the shift register 109. As indicated in each column, certain events are carried out during each state of the basic program "superwash", the activities in question are each indicated in the column concerned and for the basic program "superwash" an asterisk appears in each column to show that every event is carried out in the course of the basic program. For other program or modifications indicated in the chart of FIG. 5, asterisks are omitted in certain columns alongside the indicated program or modification indicating that the particular event related to the column is omitted as the shift register 109 advances through the eight states.

In following the basic program "superwash", upon closure of the switch PSS under these conditions, the shift register 109 is in its initial state and accordingly the control point 101 is "high", the remaining control points 102 - 108 being "low".

Since neither of the switches S201 and S202 are closed, the timing line TL is in the "high" state ensuring that the transistor TR102 is conductive so that the oscillator 128 is set for that mode of operation for producing an output pulse every 30 seconds provided the transistor TR101 is simultaneously nonconductive. However, the state of conductivity of transistor TR101 depends, inter alia, upon the condition of the water level switch WLS. The water level switch WLS is associated with the wash tub of the machine and produces a "high" at one of the inputs of each of the AND gates G105, G106 and G113 whenever the level of the water in the wash tub is below a predetermined "full" level and produces a "low" at those inputs of the gates G105, G106 and G113 whenever the water in the wash tub has reached the predetermined "full" level. If the water level in the machine wash tub is below the "full" level when the shift register is in the initial state, the "high" produced by the switch WLS results in a "high" being produced at the output of the AND gate G114 provided the timing line TL is also "high" thereby preventing oscillation of the oscillator 128. Thus, the shift register must remain in the initial state so long as the water level of the machine is below the "full" level. During the initial state of the shift register 109 when performing the basic program with the water level of the machine washtub below the "full" level, since the control point 101 is in the "high" state the switching elements SE1 and SE4 are actuated but the switching elements SE2, SE3 and SE5 are not actuated. Switching elements SE1 is actuated via the AND gate G105 and the OR gate G109 and since the switching element SE1 is actuated, the solenoid forming the load is energised thereby opening the "cold water" supply valve for supplying cold water to the machine wash tub. Accordingly, the wash tub commences to fill. Even though the switching element SE4 is actuated, the actuation has no effect since the motor M is not energised, the contacts

of the relay RL 1 being open because the switching element SE3 is not actuated.

Once the water level in the machine wash tub has reached the "full" level, changeover of the switch WLS results in a "low" being applied to an input of each of the AND gates G105, G106 and G113. Accordingly, the AND gate G106 is closed so that actuating information from the control point 101 is no longer applied to the switching element SE1 and the cold water supply valve is closed. The closure of the gate G106 also results in the output of the OR gate G111 going "low" so that via the inverter INV4, the NAND gate G101 and the AND gate G114, the transistor TR101 is rendered non-conductive and via the inverter INV5 and the AND gate G112, the switching element SE3 is actuated so that the contacts of the relay RL1 are closed and the motor M is energised. As the switching element SE4 is already actuated, the impeller of the washing machine commences to agitate. Transistor TR101 being rendered conductive, permits the oscillator 128 to commence oscillation and produce an output pulse every 30 seconds and since the output of the oscillator 128 is connected to the shift register 109 via the divider DIV, a timing pulse is supplied to the shift register 109 4 minutes after the oscillator 128 has commenced to oscillate thereby triggering the shift register 109 into the second state whereupon the control point 101 goes "low" and the control point 102 goes "high".

In theory, similar switching operations are carried out for the second state of the shift register 109 as in the initial state whilst performing the basic program under discussion. However, in practice, as the water level in the machine wash tub has already reached the predetermined "full" level required for changeover of the switch WLS, the state of affairs existing during the latter portion of the initial state is continued, i.e., the output of the OR gate G111 is "low" so that the switching elements SE3 and SE4 are still actuated. Accordingly, throughout the second state, the impeller continues to agitate whereas the transistor TR101 remains non-conductive so that the oscillator 128 continues to oscillate and the divider DIV produces another timing pulse four minutes after the commencement of the second state which triggers the shift register 109 into the third state whereupon the control point 102 goes "low" and the control point 103 goes "high".

Again, in theory, similar switching operations are carried out for the third state of the shift register 109 as in the initial state during performance of the basic program under discussion. Again however, in practice, as the water level in the machine wash tub has already reached the predetermined level required for changeover of the switch WLS, the state of affairs existing during the latter portion of the initial state, and existing throughout the second state is continued, i.e., the output of the OR gate G111 is "low" so that the switching elements SE3 and SE4 are still actuated. Accordingly, during the third state the impeller continues to agitate whereas the oscillator 128 continues to oscillate and the divider DIV produces another timing pulse 4 minutes after the commencement of the third state which triggers the shift register 109 into the fourth state whereupon the control point 103 goes "low" and the control point 104 goes "high".

Before commencing a description of the operations associated with the fourth state of the shift register 109 during performance of the basic program, it should be

mentioned that the motor M is arranged to drive a water pump whenever the motor is running. Moreover, the mechanism for either causing the impeller of the machine to agitate or causing the washing container to "spin" provided that the motor is running is so arranged that when neither of the switching elements SE4 and SE5 are actuated, the water pump is connected to pump water out of the machine wash tub.

As there are no connections between the control point 104 and the matrix 111 then the change of state of the shift register 109 from the third state to the fourth state results in the switching element SE4 being no longer actuated. However, the timing line TL remains in the "high" state and the output of the OR gate G111 is still "low" so that other conditions of the third state continue in the fourth state in that the switching element SE3 remains actuated so that the motor M continues to be energised and in that the transistor TR101 remains non-conductive and the transistor TR102 remains conductive. Thus, the oscillator 128 continues to oscillate in the mode producing an output pulse every 30 seconds so that four minutes after the commencement of the fourth state the divider DIV produces a further timing pulse which triggers the shift register 109 into the fifth state whereupon the control point 104 goes "low" and the control point 105 goes "high". Of course, during the fourth state, since neither of the switching elements SE4 and SE5 are actuated, the water pump driven by the motor M is connected to pump water out of the machine wash tub whilst the impeller of the machine remains stationary. Owing to the removal of water from the machine wash tub, the switch WLS returns to the conduction under which it produces a "high" inter alia at one of the inputs of the gate G113.

In the fifth state, a "high" being produced at the control point 105 supplies a "high" to the base of the transistor incorporated in the switching element SE5 via the AND gate G113 which is open and the switching element SE5 is therefore actuated. Since the timing line TL is still "high" and since the output of the OR gate G111 is "low" the oscillator 128 continues to oscillate in the mode producing output pulses every 30 seconds and the switching element SE3 remains actuated so that the motor M continues to be energised. Actuation of the switching element SE5 thus results in the impeller of the washing machine being caused to spin but the water is no longer pumped from the wash tube. Again, 4 minutes after the commencement of the fifth state, the divider DIV produces a timing pulse triggering the shift register into its sixth state whereupon the control point 105 goes "low" and the control point 106 goes "high".

The operation of the device for the sixth state is similar to that of the first state during performance of the basic program although the information from the control point 106 reaches the related switching elements via a different series of gates. Again, since the switch WLS supplies a "high," switching element SE1 is actuated so that water is supplied to the machine wash tub until the predetermined "full" level is reached whilst simultaneously the transistor TR101 is rendered non-conductive thereby rendering the oscillator 128 inoperative. Again, when the water level in the machine wash tub has reached the "full" level, the switch WLS delivers a "low" so that the switching element SE1 ceases to be actuated and a "low" is produced at the output

of the OR gate G111 so that the switching element SE3 is actuated and the motor M is energised whereupon the switching element SE4 being actuated from the control point 106 causes the impeller of the machine to agitate. In addition, when the output of the OR gate G111 goes "low" the transistor TR101 is rendered non-conductive and the oscillator 128 commences to oscillate. Four minutes after the commencement of oscillation, the divider DIV produces a further timing pulse triggering the shift register 109 into the seventh state whereupon the control point 106 becomes "low" and the control point 107 becomes "high."

The operation of the device for the seventh state is similar to that of the fourth state during performance of the basic program, the switching element SE3 being actuated whilst the switching elements SE4 and SE5 are not actuated so that the water pump driven by the motor M removes water from the machine wash tub once more whilst the transistor TR101 remains non-conductive so that the oscillator continues to oscillate and four minutes after the commencement of the seventh state the divider DIV supplies a further timing pulse triggering the shift register into the eighth state whereupon the control point 107 goes "low" and the control point 108 goes "high."

The operation of the device during the eighth state is similar to that of the fourth state during performance of the basic program, the switching elements SE3 and SE5 being actuated so that the washing container is caused to spin whilst the transistor TR101 remains non-conductive so that the oscillator 128 continues to oscillate in the mode producing output pulses each 30 seconds and 4 minutes after the commencement of the eighth state, the divider DIV supplies a further timing pulse triggering the shift register 109 into the initial state once more whereupon the control point 108 goes "low" and the control point 101 goes "high." However, upon transition of the control point 108 from the "high" state to the "low" state, the differentiating network constituted by the resistance 127 and the capacitance 130 in the reset circuit RC causes the normally conducting transistor TR103 to be momentarily cut-off and the momentary increase of the collector voltage of the transistor TR103 causes the transistor TR104 to conduct heavily for a short period energising the solenoid SOL and releasing the switch PSS from the closed condition thus removing the mains power supply voltage from the mains line Y and from the power supply X.

Instead of selecting the basic program "Superwash," a secondary program may be selected such as "Normal wash" or "SpinDry." If either of these secondary programs are selected, then upon closure of the start switch PSS, the basic program is followed except that the basic program is modified by the shift register 109 being rapidly advanced through certain states during the performance of the program and the switching elements of the respective combinations associated with the states through which the shift register is rapidly advanced are still actuated. For some of the combinations of switching elements associated with the states through which the shift register 109 is rapidly advanced, one or more of the switching elements are rendered ineffective by the state of the relay RL1, the contacts of which thus act as a cancelling switch, producing cancellation of the function that would otherwise occur. Those switching elements not so rendered

ineffective control functions, the occurrence of which is such short duration that they may be disregarded for practical purposes.

From the chart of FIG. 5, it can be seen that in performance of the secondary program "Normal Wash," the basic program is followed except that the shift register 109 is rapidly advanced through the second state. The result of selecting "Normal Wash" instead of "Super Wash" is that after the filling of the machine was tub to the predetermined level, agitation of the impeller is for a total period of only 8 minutes instead of for a total period of 12 minutes.

Rapid advancement of the shift register 109 through the second state during performance of the secondary program "Normal Wash" occurs as follows:

Upon closure of the switch PSS, after previously selecting the "Normal Wash" push-button S102, without any of the switches S103 to S16 being selected, power supplies are supplied to the device as previously described, the shift register 109 being in the initial state with the control point 101 being "high." As mentioned, the initial state of the register 109 during performance of the secondary program "Normal Wash" coincides with the initial state of the register in the basic program "Super Wash" and at the end of the initial state, the control point 101 goes "low" and control point 102 goes "high" as the second state commences. The "high" present at the control point 102 is applied to one input of the "NAND" gate G104, the other input of which is also "high" since the switch S102 is closed. Accordingly, the output of the NAND gate G104 is "low" making the timing line TL also "low" thereby rendering the transistor TR102 non-conductive and ensuring that the transistor TR101 is also non-conductive. Thus, the oscillator 128 commences to oscillate in the mode in which an output pulse is produced every 5 milliseconds so that 40 milliseconds after the commencement of oscillation, the divider DIV produces a timing pulse which advances the shift register into the third state whereupon the control point 102 goes "low" and the control point 103 goes "high." During the second state, since the timing line TL is in the "low" state, the output of the AND G112 is also "low" and the switching element SE3 is not actuated and hence the contacts of the relay RL1 are open. Of course, since the contacts of the relay RL1 are open, the motor M is not energised and although the switching element SE4 is actuated, such actuation is rendered ineffective owing to the cancelling effect produced by non-actuation of the switching element SE3. In addition, the switching element SE1 is actuated but since actuation is for such a short period (40 milliseconds) its actuation may be ignored for practical purposes.

The 3th, 4th, 5th, 6th, 7th and 8th states of the register 109 in the performance of the secondary program "Normal Wash" coincide with the 3rd, 4th, 5th, 6th, 7th and 8th states respectively of the performance of the basic program "Super Wash."

From the chart of FIG. 5, it can be seen that in performance of the secondary program "SpinDry," the basic program is followed except that the shift register 109 is rapidly advanced through the first six states. The result of selecting "SpinDry" instead of "Super Wash" is that the function of filling and agitating associated with the 1st, 2nd and 3rd states, the pumping associated with the 4th state, the spinning associated with the 5th state and the filling and agitating associated

with the 6th state do not occur. The function of pumping associated with the 7th state and that of spinning associated with the 8th state are however carried out.

The selection of the secondary program "SpinDry" is accomplished by selection of the switch S201, without selection of any of the switches S203 to S206 and in the performance of this secondary program it will be appreciated that during the initial, 2nd, 3rd, 4th, 5th and 6th states of the shift register, the timing line TL is "low" since S204 is closed and that a "high" is present at both inputs of the NAND gate G102. As the timing line TL is "low", the oscillator 128 is operative and oscillates in that mode producing output pulses each 5 milliseconds so that the shift register is advanced by timing pulses supplied each 40 milliseconds to the terminal 110. Simultaneously, as the timing line TL is "low" the output of the AND gate G112 is also "low" and the switching element SE3 is not actuated and the motor M is not energised. Thus, the agitating function associated with the initial, 2nd 3rd and 6th states, the pumping function associated with the 4th state and the spinning function associated with the 5th state do not occur even though the switching element SE4 is actuated in the initial, 2nd, 3rd and 6th states and the switching element SE5 is actuated in the 5th state. Although actuation of the switching element SE1 occurs during the initial, 2nd, 3rd and 6th states, the energisation of the solenoid controlling the cold water supply valve is of such short duration that it can be neglected for practical purposes. Upon termination of the 6th state, the control point 106 goes "low" and the control point 107 goes "high." Thus, the 7th state commences and coincides with the 7th state of the basic program. Similarly, the 8th state of the register, identical with the 8th state of the basic program is carried out and the register is ultimately triggered into the initial state once more, whereupon the shift register is arrested by the release of the switch PSS upon transition from the 8th to the initial state.

Regardless of whether a basic program or a secondary program is selected, the program in question may be modified, as desired, by the additional selection of one or more of the auxiliary push-button operated switches S203 to S206. The effect of selecting any of the switches S203 to S205 is to alter the combination of switching elements associated with one or more states of the shift register 109 during performance of the selected basic or secondary program. The chart illustrated in FIG. 6, of the accompanying drawings illustrates the modifications to the basic program "Superwash" produced by selection of one or more of the switches S103 to S105.

The program illustrated in relation to "Superwash" in FIG. 6, of course, coincides with that illustrated in FIG. 5, since the conditions are those in which none of the auxiliary switches S203 to S205 are selected. The program illustrated in relation to "Superwash + Hot Wash" is produced by the combined selection of the "Superwash" push-button and the "Hot Wash" push-button (S204). In this event, the modified basic program followed is identical with the basic program "Superwash" except that in the initial, second and third states, the switching element SE1 is actuated in the basic program "Superwash" whereas the switching element SE2 is actuated in lieu thereof in the modified basic program. This change of combination of switch-

ing elements is brought about for the states in question by the AND gate G108 being disabled and by the AND gate G110 being enabled by the "high" produced by the switch S204 respectively supplied via the inverter INV1 to an input of the gate G108 and via the OR gate G107 to an input of the gate G110. It will be appreciated that actuation of the switching element SE2 in lieu of the switching element SE1 results in energization of the solenoid for opening the hot water supply valve instead of energization of the solenoid for opening the cold water supply valve. Similarly, the program illustrated in relation to "Superwash + Warm Wash" is produced by the simultaneous selection of the "Superwash" push-button and the "Warm Wash" push-button (S205). In this event, the modified basic program followed is identical with that for the basic program "Superwash" except that in the initial, second and third states of the basic program, the switching element SE1 alone is actuated for water filling whereas in the modified basic program the switching element SE2 as well as the switching element SE1 is actuated. This change of combination of switching elements is brought about for the states in question since the AND gate G110 is enabled by application of a "high" from the switch S205 via the OR gate G107.

The program illustrated in relation to "Superwash + Drip Dry" is produced by the simultaneous selection of the "Superwash" push-button and the "Drip Dry" push-button (S203). In this event, the modified basic program followed is identical with that for the basic program "Superwash" except that the "spin" function associated with the eighth state is omitted, the shift register 109 being rapidly advanced through the eighth state since the "high" produced at the control point 108 during the eighth state, in combination with the "high" produced by the switch S103 results in a "low" at the output of the NAND gate G103 during the state in question thereby making the timing line TL "low."

The consequences will be evident to persons skilled in the art if there is a simultaneous selection of "Superwash" and two of the auxiliary switches S203 to S205, for example, "Superwash + Hot Wash + Drip Dry."

The "Hold" switch S206 may be selected, if desired, at any part of a basic or secondary program, modified or otherwise. The selection of the "Hold" switch S206 results in a "low" being produced at the output of the inverter INV3, which disables the NAND gate G101 thus inhibiting the oscillator 128 altogether, disables the AND G112 so that the switching element SE3 cannot remain in the actuated condition and thus the motor M cannot remain energized, and disables the AND gate G115 thereby inhibiting any actuation of either of the switching elements SE1 and SE2.

Thus, selection of the "Hold" switch S206 arrests the performance of any function regardless of which state of the register is occupied at the time of selection. Return of the switch S206 to the "open" state restores the switching device to the condition existing at the time of selection thereby permitting the remainder of the program to be completed.

Referring now to the switching device diagrammatically illustrated in FIG. 7:

The switching device of FIG. 7 is described in the following as being intended for controlling switching operations required in an automatic clothes washing machine of the same kind which the switching device of FIG. 4 is intended to control. However, the switching

device of FIG. 7 is readily adaptable for other applications.

Many parts of the device of FIG. 7 are identical with corresponding parts in the device of FIG. 4 and accordingly like parts are denoted by like numerals or letters.

The chief differences between the switching device of FIG. 7 and that of FIG. 4 are that the program selection means PSM7 and the comparison means CM7 of FIG. 7 are considerably different from the program selection means PSM and the comparison means CM of FIG. 4. Because of these differences, there are consequential differences in the connection within the matrix 111. These differences will be readily detected and the reasons for them appreciated by persons skilled in the art studying the diagram of the figures in question.

The program selection means PSM7 of FIG. 7 includes eight push-button operated switches S201 to S208 which are mechanically independent of each other, each switch being associated with a state of the eight-state shift register 109. Each of the switches S201 to S208 is also associated with a NAND gate respectively G201 to G208. One side of each of the switches S201 to S208 is connected to the positive voltage line 117 and the other side of each of the switches S201 to S208 is connected via an inverter, respectively INV201 to INV208 to one input of the associated NAND gate, the other input of which is connected to the control point of the shift register 109 corresponding to the state concerned. Thus, to one input of the NAND gate G201, the switch S201 is connected via the inverter INV201 and to the other input of the NAND gate G201 is connected the control point 101 of the shift register 109. The other NAND gates G202 to G208 are similarly connected with the switches S202 to S208 via the respective inverters INV202 to INV208 and to the control points 102 to 108.

The device of FIG. 7 is capable of performing similar functions to the device of FIG. 4. However, the control of these functions is accomplished in a fundamentally different manner. When all of the switches S201 to S208 are selected, a basic program identical with the basic program of "Superwash" for the device of FIG. 4 is performed upon subsequent selection of the starting switch PSS. However, if all but one of the switches S201 to S208 are selected then upon subsequent selection of the start switch PSS, the basic program is not performed. Instead, a secondary program, identical with the basic program is performed except that the shift register 109 is rapidly advanced through that state associated with that switch which has not been selected so that the functions associated with the state in question of the shift register 109 are omitted during performance of the secondary program selected. Thus, the shift register 109 may be rapidly advanced through any or all of its states by suitable selection of any or all of the switches S201 to S208 and only the functions associated with the selected switch of the secondary program selected will be performed.

This is brought about by the comparison of the information supplied to the comparison means CM7 by the program selection means PSM7 and that supplied from the control points 101 to 108. The respective inputs of the NAND gates G201 to G208 coupled via their respective inverters INV201 to INV208 to the switches S201 to S208 are always "high" unless the appropriate switch is selected. Accordingly, if none of the switches

S201 to S208 are selected, the timing line TL will be "low" regardless of which state is occupied by the shift register 109. This is because one of the control points 101 - 108 is "high" and therefore both inputs of one of the NAND gates G201 to G208 must also be "high." Now, if any one of the switches S201 to S208 is selected, the timing line TL must go "high" when the shift register occupies that state associated with the selection switch concerned since the input of the related NAND gate derived from the selector switch in question is "low." As described in relation to FIG. 4, when the timing line TL is "low," the oscillator 128 oscillates in a mode producing an output pulse every 5 milliseconds thereby rapidly advancing the shift register 109 whereas when the timing line TL is "high," the oscillator 128 oscillates in a mode producing an output pulse every 30 seconds thereby advancing the shift register every four minutes.

Of course, in performing a secondary program, the actuation information produced at the control points 101 to 108 results in the actuation of similar combinations of the switching elements SE1 to SE5 for the respective states of the shift register 109 as in the performance of the basic program apart from those states through which the shift register 109 is rapidly advanced.

Similarly to FIG. 5, the chart of FIG. 8 respectively shows by way of example:

Firstly, the events carried out in performance of the basic program with the switches S201 to S208 all closed. The events carried out in this basic program coincide with the events of the basic program "Super Wash" described in relation to FIG. 4.

Secondly, the events carried out in performance of a secondary program with the switches S201 and S203 to S208 closed but switch S202 open. The events carried out in this secondary program coincide with the events of the basic program except that the shift register 109 is rapidly advanced through the second state.

Thirdly, the events carried out in the performance of another secondary program with the switches S207 and S208 closed but with the switches S201 to S206 open. The events carried out in this secondary program coincide with the events of the 7th and 8th states of the basic program, the shift register 109 being rapidly advanced through the first six states.

Again, regardless of whether the basic program or a secondary program is selected, the program in question may be modified, as desired, by the additional selection of one of the auxiliary push-button operated switches S104 and S105. Also, the "Hold" switch S106, may be selected, if desired, to arrest the performance of the selected program.

It will be understood that many variations of the embodiments of the invention described herein are possible. For instance, it will be obvious that, if desired, the register 9 of FIG. 1 may be extended to comprise many more stages than the eight stages indicated, thereby permitting a greater number of combinations of switching elements to be provided. Likewise, the shift register 109 of FIG. 4 or FIG. 7 may be extended.

It will also be obvious that the program selection means may be changed in any of the embodiments. In the embodiment of FIG. 1 a greater number of selection switches than the two switches indicated may be employed if associated with an appropriate gating system in place of the simple gating system provided by

the gates G1, G2 and G3 thus enabling selection, at will, if desired, of a considerable number of alternative programs. In fact, a program selection means somewhat similar to that of FIG. 4 or that of FIG. 7 may, with suitable modification be employed with the device of FIG. 1.

In one variation to the device described in relation to FIG. 7, the push-button switches S201 to S208 are replaced by other forms of switches. In this respect, the switches S201 to S208 may, for example, be replaced by an array of light dependent resistors each capable of functioning as a switch by falling in impedance upon irradiation with light from one of an array of light emitting diodes, provision being made for one of a variety of punched cards to be placed between the array of light emitting diodes and the array of light dependent resistors for blocking light from certain light dependent resistors and permitting light to fall upon others.

Of course, the period of the oscillator 28 of FIG. 1 need not be restricted to a period of 2 minutes. The oscillator 28 may be designed to operate for any desired specific period or means may be provided for adjusting the period of the oscillator. If desired, the oscillator 28 may be replaced by a pair or a series of oscillators having different periods of oscillation and the gating network 19 may be modified so that in association with the program selection arrangements and the actuation information present at the control points 1 to 8 either or any of the oscillators may be selected to determine the duration of the respective states of the register 9 in accordance with the selected program.

Similarly, the periods of oscillation of the oscillator 128 of either FIG. 4 or FIG. 7 may be different that described.

In still another variation, the inhibition system described in relation to FIG. 1 may, with suitable modification, be incorporated in either the device of FIG. 4 or that of FIG. 7 for the purpose of inhibiting either all the switching elements SE1 to SE5 or for the purpose of only inhibiting the switching element SE3 for the total duration of a succession of pulses recurring at relatively short intervals.

The invention is not restricted to the use of switching elements such as those described in relation to the switching elements 12 to 15 but any desired kind of switching element may be employed.

The switching elements described herein as incorporating transistors, may, if required, be replaced by switching elements incorporating a device in lieu of a transistor, such as a silicon controlled rectifier, a triac or other device provided with a control electrode and capable of carrying out a similar switching function. Instead of actuation of the switching elements occurring when a "high" is present at the respective control electrode, actuation may be arranged to occur, in known manner, when a "low" is present.

It will also be understood that the invention is not restricted to the use of reference pulses having a fixed duration of 5 milliseconds for inhibition purposes nor is it restricted to the use of the inhibition period specified in relation to the description given in relation to FIG. 1.

Many variations to the logic circuitry described herein will readily be apparent to persons skilled in the art and it will be appreciated that many portions of the logic circuitry described may be replaced by differently arranged logic circuitry, where appropriate such re-

placements being accompanied by inversion of the associated logic information to achieve a similar result to the logic circuitry being replaced. These and other variations are intended to be included within the scope of the present invention.

What is claimed is:

1. A switching device comprising:

a shift register comprising a plurality of stages having states which advance in response to timing pulses;

a plurality of control points;

means for supplying actuating information to respective control points in response to the states of said shift register, the intervals between occurrence of consecutive timing pulses determining the period of time for which actuating information is present at the respective control points;

a plurality of switching elements;

means for actuating a respective combination of switching elements in response to the presence of actuating information at a control point;

pulse means for supplying timing pulses to said shift register;

program selection means for providing selection information;

comparison means for comparing said selection information with actuating information present at the control points;

means for controlling a recurrence rate of said timing pulses to recur at either relatively long intervals or relatively short intervals; and

inhibition means for preventing the actuation of said switching elements during a time interval of a succession of timing pulses recurring at relatively short

intervals, whereby a number of said combinations of switching elements corresponding to a number of control points may be omitted by the supply to the shift register of timing pulses recurring at relatively short intervals.

2. A switching device as claimed in claim 1 wherein said inhibition means includes means for preventing actuation for a period of time greater than the time between timing pulses recurring at relatively short intervals, whereby inhibition is continuous during any time period in which more than two sequential pulses recur at relatively short intervals.

3. A switching device as claimed in claim 2, comprising in addition means for inhibiting in response to a timing pulse for a period of time commencing prior to advance of said shift register.

4. A switching device as claimed in claim 3 wherein said pulse means comprises a reference pulse generator producing reference pulses of fixed duration having a leading edge and a trailing edge and wherein said period of inhibition commences in response to the leading edge of a reference pulse and the shift register advances in response to the trailing edge.

5. A switching device as claimed in claim 1 wherein said pulse source comprises a relaxation oscillator, having a series combination of two capacitors for determining the repetition frequency, said source further comprising a transistor circuit having a transistor connected to one of said capacitors such that the collector-emitter path shunts said capacitor, so that pulses recur at relatively long intervals when said transistor is conductive.

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