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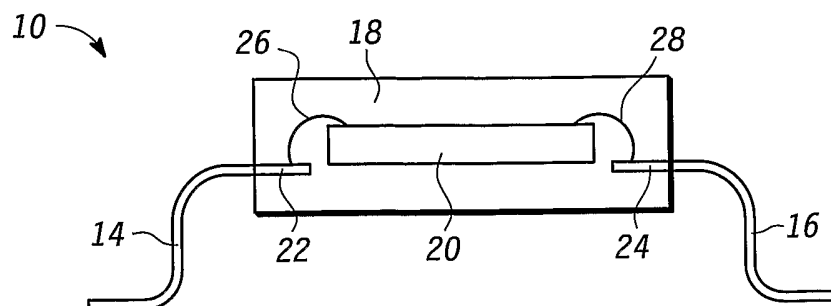
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(54) Title: SOLDERABLE METAL FINICH FOR INTEGRATED CIRCUIT PACKAGE LEADS AND METHOD FOR FORM-ING



(57) Abstract: A packaged integrated circuit (10) includes a die (20) surrounded by an encapsulant (18) in which leads (14) are used to electrically connect the die, which is internal to the encapsulant, externally. The leads have a primary metal that is used for electrical conduction and physical support. The external portion (30) of the lead is coated with another metal, typically tin, that is useful for soldering. This tin layer (32) is formed in a manner that ensures that it is porous. Although porous is generally thought to be a bad characteristic, it turns out to be very effective in absorbing stress and thus retarding whisker growth. Whisker growth, which can short adjacent leads together as well as cause other deleterious effects, has been a major source of failures in packaged integrated circuits. An additional layer (36) of very thin tin that is non-porous can be added before or after the porous tin layer has been deposited.

**SOLDERABLE METAL FINISH FOR INTEGRATED CIRCUIT PACKAGE LEADS
AND METHOD FOR FORMING**

Field of the Invention

5 [0001] This invention relates generally to integrated package leads, and more specifically, to solderable metal finishes for package leads.

Related Art

[0002] In semiconductor processing, an integrated circuit may be packaged to provide external connections via, for example, package leads. The package leads are used to provide
10 electrical connections from the integrated circuit which may then be used to electrically couple the integrated circuit to, for example, a printed circuit board (PCB). These package leads are typically finished to form a solderable surface so that the package leads may be soldered onto the PCB. The finish may also provide protection for the package leads from, for example, corrosion and oxidation. In one process used today, stress may be introduced
15 into the finish thus resulting in whiskers or filaments which extend from the package leads. The whiskers may grow to a length which causes shorts between the leads and/or to other sites on the PCB (once mounted onto the PCB). The whiskers may also result in other deleterious effects and has been a major source of failures in packaged integrated circuits. Therefore, a need exists for an improved solderable finish which reduces or prevents the
20 formation of such whiskers.

Brief Description of the Drawings

[0003] The present invention is illustrated by way of example and is not limited by the accompanying figures, in which like references indicate similar elements.

[0004] FIG. 1 illustrates a packaged integrated circuit in accordance with one
25 embodiment of the present invention; and

[0005] FIGs. 2-4 illustrates cross-sectional views of the integrated circuit package leads of FIG. 1 in accordance with various embodiments of the present invention.

[0006] Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of

some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

Detailed Description of the Drawings

[0007] Embodiments of the present invention relate to a porous solderable metal finish for integrated circuit package leads which reduces or prevents whiskering of the metal finish. In one embodiment, a porous metal finish including, for example, tin (Sn) is used to finish or coat the package metal leads. The parameters used for the formation of this finish results in a porous metal finish, where the porosity may be controlled and determined by controlling these parameters. Alternatively, the porous metal finish may include other metals or combination of metals in addition to or instead of tin. The porosity of the metal finish relieves stress in the metal finish and thus retards whisker growth, thereby resulting in an improved packaged IC.

[0008] FIG. 1 illustrates a packaged integrated circuit (IC) 10 in accordance with one embodiment of the present invention. Packaged IC 10 includes an integrated circuit die 20 surrounded by an encapsulant 18. IC die 20 is electrically coupled to package leads 14 and 16 via wire bonds 26 and 28, respectively, and wire bond posts 22 and 24, respectively. Therefore, for example, a bond pad of IC die 20 (not shown) may be provided as a connection external to encapsulant 18 via wire bond 26, wire bond post 22, and electrical lead 14. Thus package lead 14 may be soldered onto a PCB to provide electrical connections from IC die 20 to the PCB (not shown). Therefore, integrated circuit 10 may include any number of package leads as needed to provide external electrical connects for the bond pads of IC die 20. The formation of IC die 20, encapsulant 18, wire bonds 26 and 28, and wire bond posts 22 and 24 are known in the art and therefore will not be described in further detail herein. Package leads 14 and 16 are finished with a solderable metal to provide solderable package leads. The finish may also protect package leads 14 and 16 from corrosion and oxidation. In one embodiment, package leads 14 and 16 are finished with a porous solderable metal finish such that whiskering is reduced or prevented. The porous solderable metal finish will be described further below in reference to FIGs. 2-4. (Note that package leads 14 and 16 may also be referred to as external leads since they are external to encapsulant 18.)

[0009] Note that IC package 10 may include more or less elements, as needed, and may include any number of IC die such as IC die 20. Also, note that packaged IC 10 of FIG. 1 provides only one example of a packaged IC. That is, IC die 20 may be packaged in a variety

of other known ways which still use package leads such as package leads 14 and 16 for external electrical connections. For example, IC die 20 may be packaged as a quad flat package (QFP), quad flat no lead package (QFN), a plastic dual inline package (PDIP), small outline package (SOP, SOIC), plastic leaded chip carrier (PLCC), etc. Furthermore, the package leads such as package leads 14 and 16 may be trimmed and bent into a variety of different forms, such as the form illustrated in FIG. 1, or other forms, such as a "J" bend. Alternatively, the package leads may not be bent. Therefore, any of these types of packages includes package leads which may be finished using a porous metal finish, such as the porous metal finish that will be described in reference to package lead 14 in FIGs. 2-4.

[0010] FIG. 2 illustrates a cross section of a portion of package lead 14 having a conductive lead 30 (which, in the illustrated example, is an extension of wire bond post 22 external to encapsulant 18) and a porous solderable metal finish 32 which coats conductive lead 30, in accordance with one embodiment of the present invention. In one embodiment, conductive lead 30 includes copper; however, alternatively, conductive lead 30 may include another metal or metals. Conductive lead 30 may also be referred to as a metal lead, metal substrate, or primary metal and is used for electrical conduction and physical support. Therefore, note that each lead of packaged IC 10 has an external portion that is external to encapsulant 18 (such as, for example, conductive lead 30 which is coated with metal finish 32 to form package lead 14) and an internal portion that is internal to encapsulant 18 (such as, for example, wire bond post 22). Porous metal finish 32 (which may also be referred to as metal finish 32) includes a variety of pores, such as pore 34, which may have a variety of shapes and sizes. As used herein, a pore has a dimension across of at least approximately one micron, and the pores of porous metal finish 32 make up, on average, at least approximately 5 percent of the volume of metal finish 32 along the length of package lead 14, i.e. metal finish 32 has an average porosity of at least approximately 5 percent. Note that, as used herein, a material is considered porous if it has an average porosity of at least approximately 5 percent and non-porous if it has an average porosity of less than approximately 5 percent. In one embodiment, metal finish 32 has an average porosity of at least approximately 10 percent, or, more preferably, in a range of approximately 20 to 30 percent.

[0011] In one embodiment, metal finish 32 has a thickness sufficient to coat the outer surface of conductive lead portion 30. Note that after the package leads are singulated, as illustrated in FIG. 1, metal finish 32 may not coat the cut surfaces, such as, for example, at

the ends of the package leads. In one embodiment, metal finish 32 has a thickness of at least approximately 5 microns, or alternatively, at least approximately 9 microns. Alternatively, metal finish 32 may have a thickness in a range of approximately 5 to 25 microns, or more preferably, 5 to 15 microns. In one embodiment, the pores have a distance across at a largest diameter that is less than the thickness of metal finish 32. In one embodiment, the pores of metal finish 32 are not greater than approximately 5 microns across. In one embodiment, the pores may be substantially uniformly located throughout metal finish 32.

[0012] Note that the density and sizes of pores may be controlled by adjusting the parameters used in forming metal finish 32. In one embodiment, the density and size of the pores is controlled such that a number of adjacent pores do not create an opening in metal finish 32 which exposes portions of conductive lead portion 30. Alternatively, pores which expose portions of conductive lead portion 30 may be created. However, upon mounting the packaged IC to a PCB, the package leads are reflowed, where the reflowed metal finish may coat the previously exposed portions of conductive lead portion 30.

[0013] In one embodiment, metal finish 32 is a porous tin finish. Alternatively, metal finish 32 may be a tin alloy such as, for example, tin-silver, tin-bismuth, tin-copper, and tin-zinc. Alternatively, other metals or combination of metals may be used for metal finish 32, where metal finish 32 may include, for example, tin, aluminum, silver, cadmium, zinc, combinations thereof, or alloys of these metals. In one embodiment, metal finish 32 is formed by plating metal finish 32 onto conductive lead portion 30 prior to trimming and forming of package lead 14. For example, packaged IC 10 of FIG. 1 may be placed into a plating bath and brought through the plating bath to plate the metal leads of packaged IC 10 with porous metal finish 32. (Note that after the plating, the metal leads of packaged IC 10 may be trimmed and formed to form package leads 14 and 16 of FIG. 1.) The parameters or conditions of the plating process used to form metal finish 32, such as, for example, plating bath temperature, belt speed (i.e. speed through the plating bath), current density, and concentration of the majority metal intended for metal finish 32 within the plating bath, may be varied to control the porosity of metal finish 32. For example, in one embodiment, a plating bath temperature of approximately 40 degrees Celsius, a belt speed of approximately 60 mm/s, and a current density of approximately 13 amps/decimeter² may be used to plate metal finish 32. Alternatively, other combinations of parameter values may be used in which lower temperatures and/or higher belt speeds may be used. For example, in one embodiment,

the plating bath temperature is less than approximately 50 degrees Celsius and the belt speed is greater than approximately 50 mm/s, where at least one of the following criterion is met: the belt speed is at least approximately 60 mm/s and the temperature is not greater than approximately 40 degrees Celsius. Also, note that the current density used may not affect porosity of metal finish 32 as much as the combination of bath temperature and belt speed; therefore, other current density values may be used while still allowing for the desired porosity of metal finish 32.

[0014] As stated above, other values may be used for bath temperature and belt speed. For example, in one embodiment, the plating bath temperature may be at most approximately 60 degrees Celsius, or alternatively, at most approximately 43 degrees Celsius, or, more preferably, in a range of approximately 37 to 43 degrees Celsius. In one embodiment, the belt speed may be at least, approximately, 50 millimeters/second (mm/s), or, alternatively, at least approximately 55, or, more preferably, in a range of approximately 55 to 65 mm/s. Note that, in one embodiment, if a higher temperature is used, a faster belt speed may be needed to achieve the desired porosity of metal finish 32. Also, note that in different embodiments, the concentration of the majority metal intended for metal finish 32 within the plating bath may also be varied. For example, in the case of metal finish 32 being a porous tin or tin-alloy finish, the concentration of tin in the plating bath may be varied. Furthermore, note that the concentration of additives, in addition to the majority metal, may also be varied to possibly affect the porosity of metal finish 32.

[0015] Note that in alternate embodiments, metal finish 32 may be formed using other plating methods, such as, for example, electroless plating or fountain plating, where, for example, parameters of these methods may be varied to control the porosity of metal finish 32.

[0016] FIG. 3 illustrates a portion of package lead 14 in accordance with an alternate embodiment of the present invention. The embodiment of FIG. 3 is similar to that of FIG. 2 (in which like numbers indicate like elements); however, the embodiment of FIG. 3 includes an additional metal layer 36 between conductive lead 30 and metal finish 32. Metal layer 36 is less porous than metal finish 32. In one embodiment, metal layer 36 is non-porous, i.e. has an average porosity of less than 5 percent. In one embodiment, metal finish 32 is thicker than metal layer 36. For example, the thickness of metal finish 32 may be approximately four times thicker than metal layer 36, or alternatively, may be approximately nine times thicker

than metal layer 36. In one embodiment, metal layer 36 may include nickel, silver, or tin, etc, or an alloy of any of these metals. Metal layer 36 may be formed by plating metal (e.g. electroplating or electroless plating) onto conductive lead portion 30. In an alternate embodiment, a non-metal layer may be used in place of metal layer 36. For example, an organic coat or protectant may be used. In this example, metal finish 32 may be electroless plated onto the organic coat.

[0017] FIG. 4 illustrates a portion of package lead 14 in accordance with yet another alternate embodiment of the present invention. The embodiment of FIG. 4 is similar to the embodiment of FIG. 3; however, metal layer 36 is not present, and instead, a metal layer 38 is present over metal finish 32, such that metal finish 32 is between metal layer 38 and conductive lead portion 30. The descriptions provided above with respect to the composition and thickness of metal layer 36 also apply to metal layer 38. Metal layer 38 may also be formed by plating metal (e.g. electroplating or electroless plating) onto metal finish 32. Also, note that a non-metal layer may be used in place of metal layer 38, such as, for example, an organic coat or protectant.

[0018] In yet another alternate embodiment, package lead 14 may include two additional metal layers such as both metal layer 36 and metal layer 38. In this manner, metal finish 32 would be located between two metal layers. Alternatively, organic coats may be used in place of the metal layers, such that metal finish 32 is located between two organic coats.

[0019] By now it should be appreciated that there has been provided a porous metal finish for package leads which reduce or prevent the formation of whiskers while maintaining solderability of the package leads, where the porous metal finish includes an average porosity of at least 5 percent. The porosity of metal finish 32 may allow for stress relief of the metal finish, thus reducing or preventing the formation of whiskers. Therefore, although porous is generally thought to be a bad characteristic, it turns out to be very effective in absorbing stress and thus retarding whisker growth. Whisker growth, which can short adjacent leads together as well as cause other deleterious effects, has been a major source of failures in packaged integrated circuits. The porosity may be controlled by controlling the parameters or conditions of the plating process used to form metal finish 32. For example, different combinations of plating bath temperature and belt speed may be used to achieve different porosities.

[0020] Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

[0021] In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention.

[0022] Although the invention has been described with respect to specific conductivity types or polarity of potentials, skilled artisans appreciated that conductivity types and polarities of potentials may be reversed.

[0023] Moreover, the terms “front”, “back”, “top”, “bottom”, “over”, “under” and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. It is understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein.

[0024] Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms “comprises,” “comprising,” or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus. The terms “a” or “an”, as used herein, are defined as one or more than one.

[0025] The term “plurality”, as used herein, is defined as two or more than two. The term another, as used herein, is defined as at least a second or more.

CLAIMS

1. An external lead of a packaged integrated circuit comprising:
a metal substrate; and
a first layer of metal that coats the metal substrate, wherein the first layer of
5 metal is porous and comprises at least one of tin, cadmium, aluminum,
silver, and zinc.
2. The external lead of claim 1, further comprising a second layer of metal that coats the
metal substrate, wherein the second layer of metal is non-porous.
- 10 3. The external lead of claim 2 wherein the first layer of metal is between the second
layer of metal and the metal substrate.
4. The external lead of claim 2, wherein the second layer is between the first layer of
15 metal and the metal substrate.
5. The external lead of claim 2, wherein the first layer of metal is thicker than the second
layer of metal.
- 20 6. The external lead of claim 5, wherein the first layer of metal is at least approximately
four times thicker than the second layer of metal.
7. The external lead of claim 5, wherein the first layer of metal is at least approximately
nine times thicker than the second layer of metal.
- 25 8. The external lead of claim 1, wherein the first layer of metal has a thickness greater
than approximately five microns.
9. The external lead of claim 8, wherein the thickness of the first layer of metal is at least
30 approximately nine microns.
10. The external lead of claim 1, wherein the first layer of metal comprises pores that are
not greater than approximately 5 microns across.

11. The external lead of claim 1, wherein:

the first layer of metal has a thickness; and

the first layer of metal is characterized by having pores that have a distance

5 across at the largest dimension that is less than the thickness of the first layer of metal.

12. The external lead of claim 1, wherein the first layer of metal has an average porosity of between approximately twenty percent and thirty percent.

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13. The external lead of claim 1, wherein the first layer of metal comprises tin.

14. The external lead of claim 13, wherein the first layer of metal further comprises a metal selected from at least one of zinc, copper, bismuth, and silver.

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15. A packaged integrated circuit comprising:

an integrated circuit die surrounded by an encapsulant;

a plurality of leads, each lead having external portion that is external to the encapsulant and an internal portion that is internal to the encapsulant,

20

wherein:

the internal portion is electrically connected to the integrated circuit die; and

the external portion comprises a metal substrate and a first metal

layer that is porous and that coats the metal substrate, wherein

25

the first metal layer comprises at least one of tin, cadmium, aluminum, silver, and zinc.

16. The packaged integrated circuit of claim 15, wherein the first metal layer comprises tin.

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17. The packaged integrated circuit of claim 16, further comprising a second layer of metal that coats the metal substrate, wherein the second layer of metal is non-porous tin.

18. The packaged integrated circuit of claim 17 wherein the first layer of metal is between the second layer of metal and the metal substrate.

5 19. The packaged integrated circuit of claim 17, wherein the second layer is between the first layer of metal and the metal substrate.

20. The packaged integrated circuit of claim 17, wherein the first layer of metal is thicker than the second layer of metal.

10 21. The packaged integrated circuit of claim 17, wherein the first layer of metal is at least approximately four times thicker than the second layer of metal.

22. The packaged integrated circuit of claim 17, wherein the first layer of metal is at least approximately nine times thicker than the second layer of metal.

15

23. The packaged integrated circuit of claim 16, wherein the first layer of metal has a thickness greater than approximately five microns.

20 24. The packaged integrated circuit of claim 23, wherein the thickness of the first layer of metal is at least approximately nine microns.

25. The packaged integrated circuit of claim 16, wherein the first layer of metal comprises pores that are not greater than approximately 5 microns across.

25 26. The packaged integrated circuit of claim 16, wherein:
the first layer of metal has a thickness; and
the first layer of metal is characterized by having pores that have a distance
across at the largest dimension that is less than the thickness of the first
layer of metal.

30

27. The packaged integrated circuit of claim 16, wherein the first layer of metal has an average porosity of between approximately twenty percent and thirty percent.

28. The packaged integrated circuit of claim 16, wherein the first layer of metal further comprises a metal selected from at least one of zinc, copper, bismuth, and silver.

29. A method of plating a metal lead of a packaged integrated circuit, comprising:
5 placing the packaged integrated circuit in a plating bath; and
bringing the packaged integrated circuit through the plating bath under conditions that result in plating the lead with a first layer of metal, wherein the first layer of metal is porous and comprises at least one of tin, cadmium, aluminum, silver, and zinc.

10 30. The method of claim 29, wherein the first layer of metal comprises tin.

31. The method of claim 30, wherein the bringing the packaged integrated circuit through the plating bath is further characterized by:

15 the plating bath being at a temperature of less than approximately 50 degrees Celsius; and
a speed of bringing the packaged integrated circuit through the bath being greater than approximately fifty millimeters per second;
wherein at least one of the following criterion is met:
20 the speed is at least approximately sixty millimeters per second; and
the temperature is not greater than approximately 40 degrees Celsius.

32. The method of claim 29, further comprising
bringing the packaged integrated circuit through the plating bath under conditions
25 that result in plating the lead with a second layer of metal, wherein the second metal layer is non-porous.

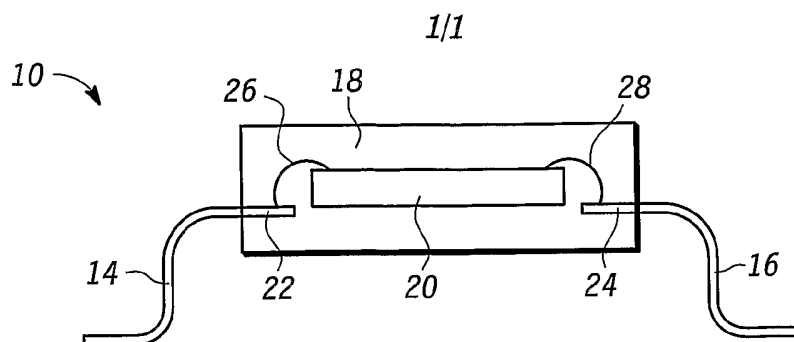


FIG. 1

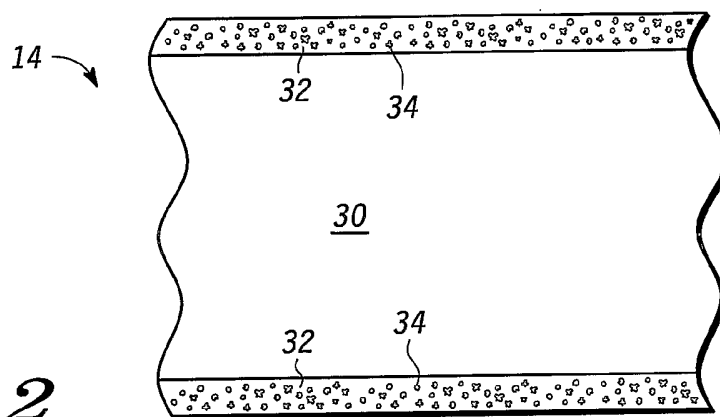


FIG. 2

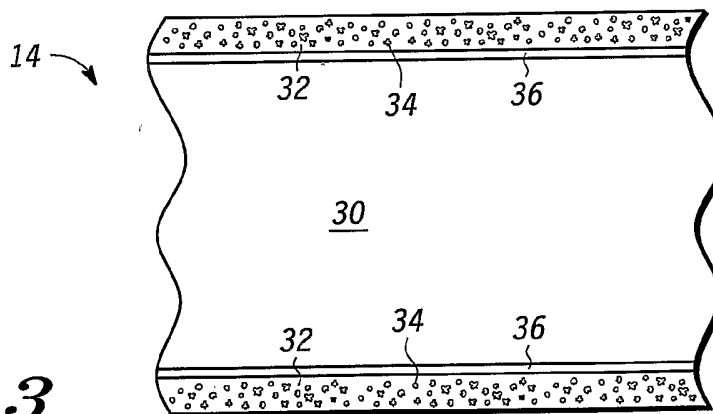


FIG. 3

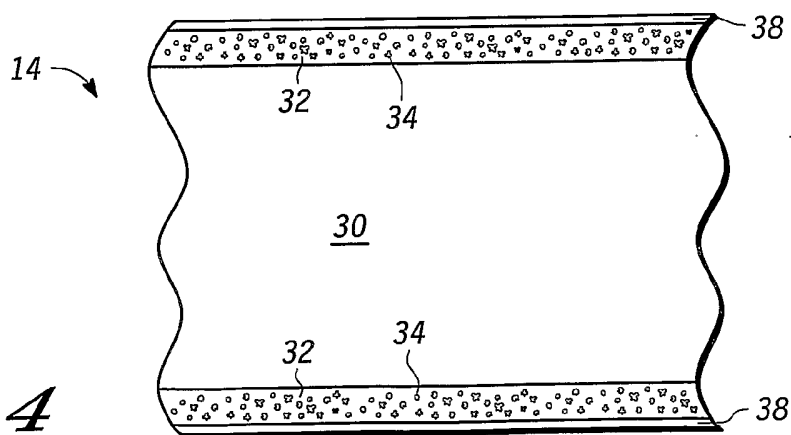


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US05/21499

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 23/495, 21/44
US CL : 257/666, 677, 750; 438/123

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/666, 677, 750; 438/123

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST (USPGPUB, USPAT, EPO, JPO, DWPI, IBM_TDB)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,646,330 B2 (KUBARA et al) 11 November 2003 (11.11.2003), figures 2-3 and columns 4-9.	1-32
Y	US 4,529,667 A (SHIGA et al) 16 July 1985 (16.07.1985), column 1, lines 11-20 and column 1, line 64 to column 2, line 2.	1-32
Y	US 5,741,544 A (MAHULIKAR et al) 21 April 1998 (21.04.1998), column 2, lines 23-28	1-32
Y, P	US 6,849,574 B1 (HEIDEMANN et al) 01 February 2005 (01.02.2005), column 2, lines 18-20.	2,3,5-7,17,18,20-22
Y	US 3,459,642 A (SCHAFLER et al) 05 August 1969 (05.08.1969), column 8, lines 48-50.	2,4,17,19
Y, P	US 2004/0237282 A1 (HINES et al) 02 December 2004 (02.12.2004), see sections 0038, 0039 and 0043.	10,12,25,27



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

29 September 2005 (29.09.2005)

Date of mailing of the international search report

18 OCT 2005

Name and mailing address of the ISA/US

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