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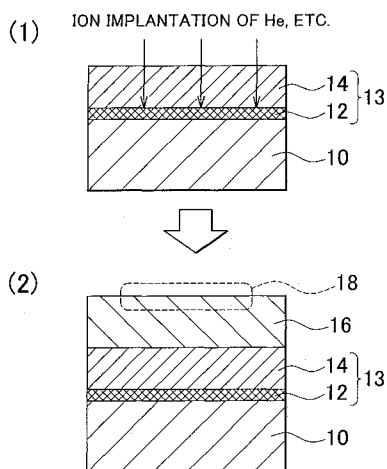
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(54) Title: PROCESS FOR PRODUCING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

FIG. 1



(57) Abstract: A process for producing a semiconductor device includes: forming an SiC epitaxial layer on an SiC substrate; implanting the epitaxial layer with ions; forming a gettering layer having a higher defect density than a defect density of the SiC substrate; and carrying out a heat treatment on the epitaxial layer. The semiconductor device includes an SiC substrate, an SiC epitaxial layer formed on the SiC substrate, and a gettering layer having a higher defect density than a defect density of the SiC substrate.



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PROCESS FOR PRODUCING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

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1. Field of the Invention

[0001] The invention relates to a process for producing a semiconductor device and the semiconductor device, and more specifically, relates to the gettering of impurities in an SiC substrate for forming a semiconductor device.

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2. Description of Related Art

[0002] To prevent degradation of semiconductor characteristics by metallic impurities in a semiconductor crystal of Si, etc., a strain region is created by ion implantation, laser irradiation, forming a film of a different material, and the like, to provide a gettering center for the impurities.

15

[0003] As a problem unique to SiC monocrystals, the inventors have discovered that when a heat treatment is carried out thereon at a high temperature, particularly a temperature of 1500°C or higher, impurities such as metals that are either contained in the crystal or lie adjacent thereto diffuse through the crystal.

20

[0004] Impurities are always present in SiC semiconductor monocrystals that are used as practical materials. More specifically, when SiC monocrystals are grown by the solution method, metal elements are often added to the SiC solution to increase the growth rate, improve crystallinity, and the like. For example, Japanese Patent Application Publication No. 2007-261844 (JP-2007-261844 A) discloses the addition of Cr, and Japanese Patent Application Publication No. 2009-126770 (JP-2009-126770 A) discloses the addition of Ni to the SiC growth solution, and in some cases these metals remain as impurities in the grown SiC monocrystal. When an epitaxial layer for the device region is formed on such an SiC substrate produced by the solution method, the

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diffusion of the metal impurities from the SiC substrate into the epitaxial layer will degrade the properties of the device.

[0005] Therefore, the amounts of impurity elements adversely affecting conductive and device properties that are incorporated into the crystal must be reduced and those impurity elements that do become incorporated must be contained outside the device region. In the case of a Si crystal, alkali metal elements such as Na, K, Li, etc., and heavy metal elements such as Fe, Cu, Au, Cr, etc., are taken into account. It is known that alkali metal elements affect adversely metal-oxide-semiconductor (MOS) characteristics, and heavy metal elements cause shortening carrier life and oxidation stacking fault (OSF) defects. Therefore, the gettering (capture and immobilization) of these residual impurity elements by the use of a strained layer that is intentionally formed in a specific part of the crystal (outside the device region) is already available in the case of Si crystals.

[0006] In the case of an SiC crystal, on the other hand, thermal diffusion is not considered to occur substantially at the kind of heat treatment temperature (maximum of about 1200°C) that is normally used for a Si crystal because the diffusion coefficient of the impurities is extremely small (Yu. A. Vodakov and E. N. Mokhov, "Silicon Carbide" 1973 (Univ. South Carolina Press, Columbia, 1974, p. 508)). Therefore, almost no reports concerning gettering technology in SiC crystals can be found.

[0007] With this new knowledge, however, the inventors have ascertained that when a high temperature heat treatment (1500°C or higher) specific to SiC is carried out, even heavy metal elements such as Cr and Ni will diffuse through the SiC crystal even though the diffusion coefficients of the impurities are low compared with Si. Therefore, these elements must be taken into account, and it has become necessary carry out a gettering treatment on SiC crystals.

[0008] Japanese Patent Application Publication No. 2007-251172 (JP-2007-251172 A) discloses using He and H ion beams to form an ion-enriched layer of a given depth on an SiC substrate or a Si substrate, and then conducting gettering to trap contaminants such as heavy metal ions by carrying out a heat treatment at a temperature

that does not exceed a critical temperature whereat destruction of the substrate occurs. Unlike Si, however, in SiC, the diffusion of contaminants does not easily occur and it is difficult to achieve recovery of the substrate after gettering. Therefore, as an issue specific to SiC, it is necessary to focus on the sites on the substrate and the manufacturing processes that require gettering, and to eliminate unnecessary process steps. However, JP-2007-251172 A does not disclose an example wherein gettering is carried out on SiC, and it contains no statements or implications relevant to this issue.

[0009] Japanese Patent Application Publication No. 2010-098107 (JP-2010-098107 A) discloses that in a semiconductor apparatus used as an imaging device, a gettering layer of a desired depth was fabricated by irradiation with a laser beam from the side opposite the epitaxial layer, which is the structural element for forming the circuit layer, etc.

[0010] Japanese Patent Application Publication No. 2006-231430 (JP-2006-231430 A) discloses setting the temperature for forming a gettering layer at 1100°C to 1300°C when carrying out gettering of heavy metals.

[0011] Japanese Patent Application Publication No. 58-147126 (JP-58-147126 A) discloses forming a gettering layer on the underside of a semiconductor substrate by carrying out a heat treatment at a temperature of 1050°C or higher to diffuse supersaturated interstitial oxygen therethrough.

[0012] Japanese Patent Application Publication No. 07-201971 (JP-07-201971 A) discloses fabricating a plurality of semiconductor device sections on a substrate and forming a gettering site on the sides opposite the divided sections of the semiconductor devices that also serve as the device formation regions of the semiconductor substrate.

[0013] However, none of this related art assumes the diffusion of contaminating metallic elements that are either present in the substrate crystal or infiltrate from outside the substrate crystal in a SiC semiconductor substrate, and they have not noticed the need of a gettering layer therefor, particularly when a heat treatment at 1500°C or higher is carried out.

SUMMARY OF THE INVENTION

[0014] The invention provides a process for producing a semiconductor device that includes forming a gettering layer to capture and immobilize impurity elements in an SiC semiconductor substrate. The invention also provides a semiconductor device that includes a gettering layer to capture and immobilize impurity elements in an SiC semiconductor substrate.

[0015] A first aspect of the invention relates to a process for producing a semiconductor device. This production process includes: forming an SiC epitaxial layer on an SiC substrate; implanting the epitaxial layer with ions; forming a gettering layer having a higher defect density than a defect density of the SiC substrate; and carrying out a heat treatment on the epitaxial layer.

[0016] According to the first aspect of the invention, because a gettering layer with a higher defect density than the SiC substrate is formed, the impurity elements are captured and immobilized preferentially in the gettering layer.

[0017] In this production process, the heat treatment may include a treatment at 1500°C or higher, and the gettering layer may be formed prior to the treatment at 1500°C or higher.

[0018] In this production process, the gettering layer may be formed by ion implantation to the epitaxial layer, and an amount of an implantation dose may be controlled such that the defect density of the gettering layer is higher than the density of impurities to be captured, and a compensated defect density is equal to or lower than a carrier density of the semiconductor device.

[0019] In this production process, the gettering layer may be formed deeper than a depth of material removed by etching that is carried out prior to growing the epitaxial layer.

[0020] In this production process, the gettering layer may be formed in a region, on the SiC substrate, other than a device formation region where the semiconductor device is to be formed on the SiC substrate.

[0021] In this production process, the defect density of the gettering layer may be determined on the basis of electrical current on the SiC substrate when the semiconductor device is operated.

5 [0022] In this production process, the gettering layer may be formed in a region, on the SiC substrate, other than a device formation region when the gettering layer is formed in the epitaxial layer after the epitaxial layer has grown.

[0023] In this production process, the gettering layer may be formed by irradiation with an electron beam or neutron beam from a side opposite to an epitaxial layer side of the SiC substrate.

10 [0024] A second aspect of the invention relates to a semiconductor device. This semiconductor device includes an SiC substrate, an SiC epitaxial layer formed on the SiC substrate, and a gettering layer having a higher defect density than a defect density of the SiC substrate.

15 BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Features, advantages, and technical and industrial significance of exemplary embodiments of the invention will be described below with reference to the accompanying drawings, in which like numerals denote like elements, and wherein:

20 FIG. 1 shows the formation of the gettering layer according to one aspect of the invention;

FIG. 2A shows the formation of the gettering layer according to another aspect of the invention;

FIG. 2B shows the formation of the gettering layer according to another aspect of the invention;

25 FIG. 3 shows the formation of the gettering layer according to yet another aspect of the invention;

FIG 4A shows an example wherein the formation of the gettering layer of the invention has been applied;

FIG 4B shows an example wherein the formation of the gettering layer of the invention has been applied;

FIG 4C shows an example wherein the formation of the gettering layer of the invention has been applied;

5 FIG 4D shows an example wherein the formation of the gettering layer of the invention has been applied;

FIG 4E shows an example wherein the formation of the gettering layer of the invention has been applied;

10 FIG 4F shows an example wherein the formation of the gettering layer of the invention has been applied;

FIG 4G shows an example wherein the formation of the gettering layer of the invention has been applied;

FIG. 5 shows a profile of the Cr concentration in Comparative Example 1;

FIG. 6 shows a profile of the Cr concentration in Comparative Example 2;

15 FIG. 7 shows a profile of the Cr concentration in Comparative Example 3;

FIG. 8 shows a profile of the Cr concentration in Example 1 of the invention;

FIG. 9 shows a profile of the Cr concentration in Example 2 of the invention;

FIG. 10 shows a profile of the Cr concentration in Example 3 of the invention;

FIG. 11 shows a profile of the Fe concentration in Example 4 of the invention;

20 FIG. 12 shows a profile of the Zn concentration in Example 5 of the invention; and

FIG. 13 shows a profile of the Ti concentration in Example 6 of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS

[0026] The production process of the semiconductor device of the invention
25 includes the steps of forming an SiC epitaxial layer on an SiC substrate, and when a semiconductor device is fabricated by conducting various types of ion implantation and heat treatments on the epitaxial layer, forming a gettering layer with a higher defect density than the SiC substrate.

[0027] More specifically, before a high-temperature heat treatment of 1500°C or higher (including oxidation and crystal growth) is carried out, by ion implantation of an element, such as a noble gas, in a SiC monocrystal substrate at high density, impurity elements such as heavy metals that will be incorporated into the crystal during the high-temperature heat treatment are captured and immobilized in the gettering layer, thereby blocking the diffusion thereof.

[0028] In one aspect of the invention, a gettering layer is formed on the SiC substrate to prevent the impurities contained in the SiC substrate from diffusing to the epitaxial layer that contains the device formation region that has been formed on the substrate. This primarily counteracts diffusion in the direction of substrate thickness.

[0029] More specifically, when a low N (nitrogen) density epitaxial growth layer, i.e., a device formation region, is stacked on top of the substrate, ions of a rare gas element are implanted into the surface of the substrate before epitaxial growth, and a gettering layer is formed wherein the implanted ion density assumes a Gaussian distribution, a box profile distribution (constant within a given range of depth), etc.

[0030] Before epitaxial growth is carried out, part of the surface of the substrate is removed by H₂ etching to expose a clean fresh surface. Therefore, ion implantation to form the gettering layer, which is carried out before the above step (H₂ etching), must be continued until it is deeper than the amount of material to be removed by the H₂ etching.

[0031] In addition, the implantation dose must be controlled such that the density of defects forming the gettering layer that is generated by the ion implantation will be greater than the density of the impurities to be captured, and such that the compensation defect density (gettering sites + non-gettering sites) does not exceed the concentration of the semiconductor device carrier (e.g., the N density (in the case of an n-type semiconductor)). By so doing, it becomes easier to guarantee conductivity in the SiC substrate because the movement of electrons is assured even after the introduction of the defects for gettering. The defect density of the gettering layer is determined on the basis of the electrical current on the SiC substrate when the semiconductor device is operated.

[0032] As shown at the top of FIG. 1, point defects, dislocations, stacking faults, etc., are formed at the ion implantation region 12 or the region that the implanted ions have passed through 14 on the substrate 10 by a rare gas such as He. These defects act as gettering sites and as a whole form a gettering layer 13. As shown at the bottom of FIG.

5 1, when a low N concentration epitaxial layer 16 is formed at 1500°C to 1800°C, for example, impurities such as heavy metals that diffuse from the substrate 10 are captured and immobilized in the gettering layer 13. As a result, diffusion and infiltration of impurity elements from the substrate 10 into the epitaxial layer 16 is prevented.

[0033] Preferably a rare gas such as He or Ar is used as the implantation ion. H, 10 or group 4 elements such as Si, C, or Ge can also be used. In the case of an n-type semiconductor substrate, a group 5 element such as N can also be used. Group 3 elements are undesirable because they have the effect of reducing conductivity.

[0034] As a method of forming the gettering layer 13 other than ion implantation, any method that can form defects from the outermost surface of the 15 substrate such as electron beam irradiation, neutron beam irradiation, etc., can also be used.

[0035] The gettering layer formed by the method of the invention can capture and immobilize (getter) a variety of heavy metal elements. This layer is particularly effective for gettering Cr, Ni, Fe, Zn, etc.

20 [0036] In another aspect of the invention, a gettering layer is formed at a site other than a region whereon a semiconductor device will be formed (also referred to herein as the "device formation region") in the epitaxial layer on the SiC substrate (i.e., other than the breakdown voltage holding member) and, rather than the impurities within the SiC substrate, impurities infiltrating from areas surrounding the substrate are 25 prevented from diffusing into the epitaxial layer that contains the device formation region. In one case, as shown in FIG. 2A, a gettering layer 13 is formed at a position shallower than the device formation region 18 of the epitaxial layer 16 to counteract diffusion in the direction of substrate thickness, and in another case, as shown in FIG. 2B, a gettering layer 13 is formed at a site that surrounds the device formation region 18 of the epitaxial

layer 16 horizontally to counteract diffusion in the parallel direction to the surface of the substrate. As described below, metals such as Cr diffuse through the epitaxial layer very easily, so if gettering is impossible within a device region such as a p-n junction device resulting from an epitaxial junction, a gettering layer can be formed within the contact
5 layer or at another member (e.g., a device isolation layer, etc.) near the surface as shown in FIGS. 2A and 2B.

[0037] Typically, the impurities diffuse when a heat treatment is carried out at a high temperature exceeding 1500°C. At this time, there is concern that the device properties will change if gettering should occur within the device formation region, so
10 gettering is carried out at a site outside the device formation region. In particular, it is necessary to make sure that the implanted ions, electrons, etc., do not pass through any region to which the depletion layer extends when the device is operated. Regardless of whether the site formed gettering layer is a region where current flows or does not flow, the amount of the dose is controlled such that it does not dramatically inhibit current flow.

15 [0038] Unlike Si, SiC is a compound semiconductor, and therefore the crystal defects that are produced when the implanted ions, electrons, etc., pass through the crystal (particularly, intrinsic defects such as atomic vacancies) are thermally stable, and in some cases recovery is impossible even if a heat treatment is carried out at a temperature exceeding 1700°C. In the case of Si, the number of divacancies decreases
20 with a heat treatment at about 400°C. Therefore, if implantation species pass through the device formation region of SiC, the device may not operate as designed.

[0039] In still another aspect of the invention, a gettering layer 13 can be formed without introducing defects into the device formation region by carrying out irradiation or implantation of the epitaxial layer 16 with an electron beam, neutron beam, or
25 lightweight ions from the back side rather than from the upper side of the substrate 10 as shown in FIG. 3. FIG. 3 illustrates a case wherein an electrode 20 is formed on the device formation region 18.

[0040] FIGS. 4A to 4G illustrate examples wherein the method of the invention has been applied to various types of semiconductor devices. The invention can also be

applied to various types of devices such as transistors other than those illustrated in the drawings.

[0041] The invention is described in greater detail below through examples.

[Comparative Example 1] An SiC substrate with a particularly high Cr concentration (10^{17} cm^{-3}) was fabricated by the solution method to verify the effect of the invention. An epitaxial layer was formed on this substrate by chemical vapor deposition (CVD). As shown in FIG. 5, the profile of Cr concentration in the resulting material revealed that Cr had diffused from the substrate into the epitaxial layer, and part of the Cr had even penetrated to the surface of the test sample.

[0042] **[Comparative Example 2]** To observe the phenomenon of Comparative Example 1 more easily, Cr was implanted into the surface of the epitaxial layer by ion implantation. As illustrated in FIG. 6, a box profile distribution with a depth of 400 nm and a concentration of $1 \times 10^{17} \text{ cm}^{-3}$ was formed. When this test sample was heat treated for 240 min at 1780°C , the profile of the Cr concentration changed as shown in FIG. 7.

This difference means that the implanted Cr had diffused.

[0043] Table 1 shows a summary of the relationship between heat treatment temperature and the presence or absence of diffusion. It is clear that Cr diffuses with a heat treatment of 1500°C or higher.

[0044] Table 1

Heat treatment temperature	Diffusion (Yes/No)
1300°C	Almost none
1500°C	Yes
1780°C	Yes
1850°C	Yes

[0045] **[Comparative Example 3]** The same test as in Comparative Example 2 was carried out using a commercially available SiC wafer, and the results revealed no Cr diffusion. Therefore, it is clear that gettering of Cr is caused by defects that are few in an epitaxial layer and that are many in a commercially available wafer.

[0046] **[Example 1]** Additional defects were introduced by also implanting Ar ions into a test sample that had undergone Cr ion implantation on the surface of the epitaxial layer in the same manner as in Comparative Example 2. The Ar was introduced

in a Gaussian distribution to a depth of 200 nm at a concentration of $1 \times 10^{21} \text{ cm}^{-3}$ (monoenergetic implantation at an energy of 270 keV). This test sample was heat treated for 30 min at 1780°C. As shown in FIG. 8, the results reveal that the Cr concentration profile was almost unchanged in the ion implantation region (Ar penetration region), i.e.,
5 gettering had occurred.

[0047] [Example 2] Additional defects were introduced by also implanting He ions into a test sample that had undergone Cr ion implantation on the surface of the epitaxial layer in the same manner as in Comparative Example 2. The He was introduced in a Gaussian distribution to a depth of 1 μm at a concentration of $1 \times 10^{21} \text{ cm}^{-3}$
10 (monoenergetic implantation at an energy of 360 keV). This test sample was heat treated for 30 min at 1780°C. As shown in FIG. 9, the results revealed that the Cr concentration profile was almost unchanged in the ion implantation region (He penetration region), i.e., gettering had occurred.

[0048] [Example 3] Additional defects were introduced by also implanting H
15 ions into a test sample that had undergone Cr ion implantation on the surface of the epitaxial layer in the same manner as in Comparative Example 2. The H was introduced in a Gaussian distribution to a depth of 2.2 μm at a concentration of $1 \times 10^{20} \text{ cm}^{-3}$ (monoenergetic implantation at an energy of 350 keV). This test sample was heat treated for 30 min at 1780°C. As shown in FIG. 10, the results reveal that although the Cr
20 concentration profile changed in the ion implantation region (H penetration region), Cr remained at a concentration of about $1 \times 10^{16} \text{ cm}^{-3}$ in the H implantation region, and it appears that gettering occurred. In this example it appears that Cr, which had not been completely captured, diffused because the H implantation dose was insufficient. It is clear, however, that gettering is possible even with H. Theoretically, a similar gettering
25 effect as with H implantation can be expected with an electron beam or neutron beam (but the implantation dose must be made sufficiently large).

[0049] [Example 4] Fe ions were implanted into the epitaxial layer, and a box profile distribution with a depth of 400 nm and a concentration of $1 \times 10^{17} \text{ cm}^{-3}$ was formed. Then He ions were implanted into this test sample in the same manner as in

Example 2, and after a heat treatment for 30 min at 1780°C, the Fe concentration profile was investigated. As shown in FIG. 11 ("with He implantation"), the results clearly reveal that a box profile was retained and that gettering occurred (diffusion was blocked).

[0050] [Comparative Example 4] Fe ions were implanted in the same manner as in Example 4, but He ions were not implanted. In this case, as shown in FIG. 11 ("without He implantation"), the box profile becomes disarrayed, and the Fe clearly has diffused (gettering did not occur).

[0051] [Example 5] Zn ions were implanted into the epitaxial layer, and a box profile distribution with a depth of 400 nm and a concentration of $1 \times 10^{17} \text{ cm}^{-3}$ was formed. Then He ions were implanted into this test sample in the same manner as in Example 2, and after a heat treatment for 30 min at 1780°C, the Zn concentration profile was investigated. As shown in FIG. 12, the results clearly reveal that a box profile was retained and that gettering occurred (diffusion was blocked).

[0052] [Example 6] Ti ions were implanted into the epitaxial layer, and a box profile distribution with a depth of 400 nm and a concentration of $1 \times 10^{17} \text{ cm}^{-3}$ was formed. Then Ar ions were implanted into this test sample in the same manner as in Example 1, and after a heat treatment for 30 min at 1780°C, the Ti concentration profile was investigated. As shown in FIG. 13, the results clearly reveal that a box profile was retained and that gettering occurred (diffusion was blocked).

[0053] According to the invention, a process for producing a semiconductor device is provided that includes the formation of a gettering layer to capture and immobilize impurity elements in an SiC semiconductor substrate.

CLAIMS:

1. A process for producing a semiconductor device,
the process comprising:
forming an SiC epitaxial layer on an SiC substrate;
implanting the epitaxial layer with ions;
forming a gettering layer having a higher defect density than a defect density of the SiC substrate; and
carrying out a heat treatment on the epitaxial layer.
2. The process according to claim 1, wherein
the heat treatment includes a treatment at 1500°C or higher; and
the gettering layer is formed prior to the treatment at 1500°C or higher.
3. The process according to claim 1 or 2, wherein
the gettering layer is formed by ion implantation to the epitaxial layer, and
an amount of an implantation dose is controlled such that a defect density of the gettering layer is higher than a density of impurities to be captured, and a compensated defect density is equal to or lower than a carrier density of the semiconductor device.
4. The process according to any one of claims 1 to 3, wherein the gettering layer is formed deeper than a depth of material removed by etching that is carried out prior to growing the epitaxial layer.
5. The process according to any one of claims 1 to 4, wherein the gettering layer is formed in a region, on the SiC substrate, other than a device formation region where the semiconductor device is to be formed on the SiC substrate.

6. The process according to any one of claims 1 to 4, wherein the defect density of the gettering layer is determined on the basis of electrical current on the SiC substrate when the semiconductor device is operated.
7. The process according to any one of claims 1 to 6, wherein the gettering layer is formed in a region, on the SiC substrate, other than a device formation region when the gettering layer is formed in the epitaxial layer after the epitaxial layer has grown.
8. The process according to any one of claims 1 to 7, wherein the gettering layer is formed by irradiation with an electron beam or neutron beam from a side opposite to an epitaxial layer side of the SiC substrate.
9. A semiconductor device comprising:
 - an SiC substrate;
 - an SiC epitaxial layer formed on the SiC substrate; and
 - a gettering layer having a higher defect density than a defect density of the SiC substrate.

FIG. 1

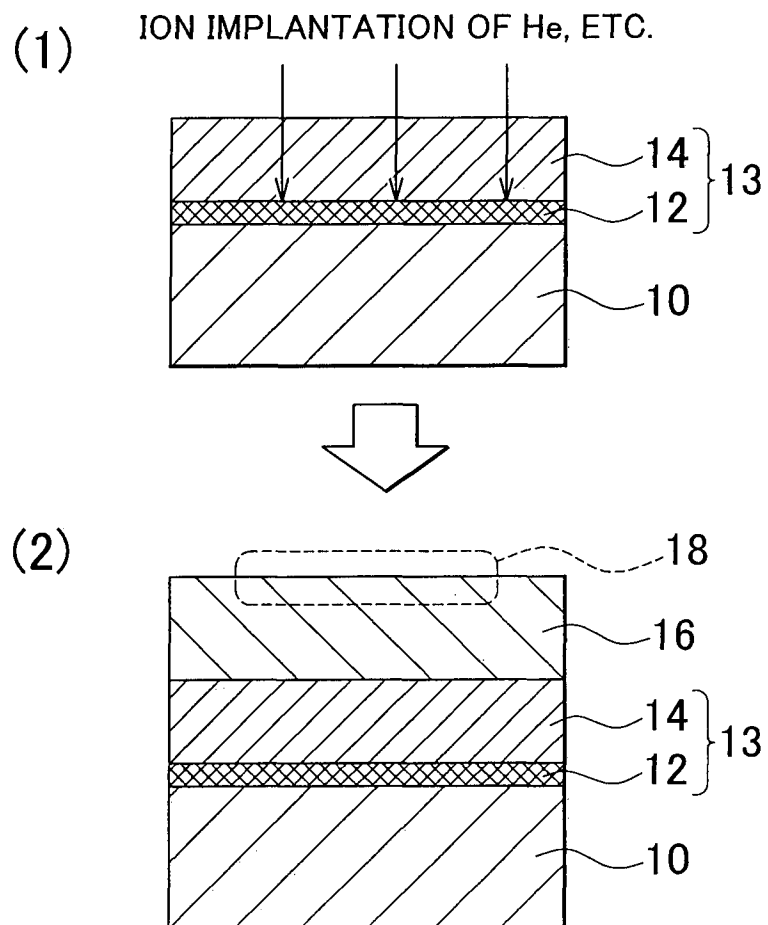


FIG. 2

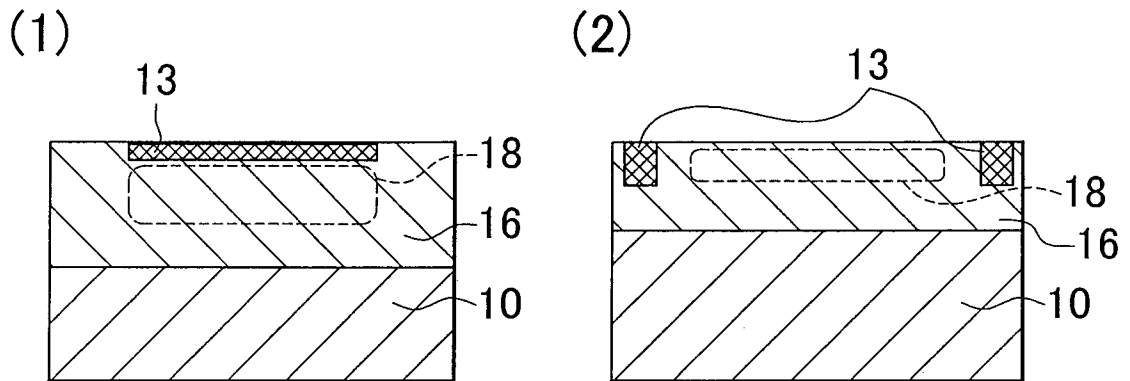


FIG. 3

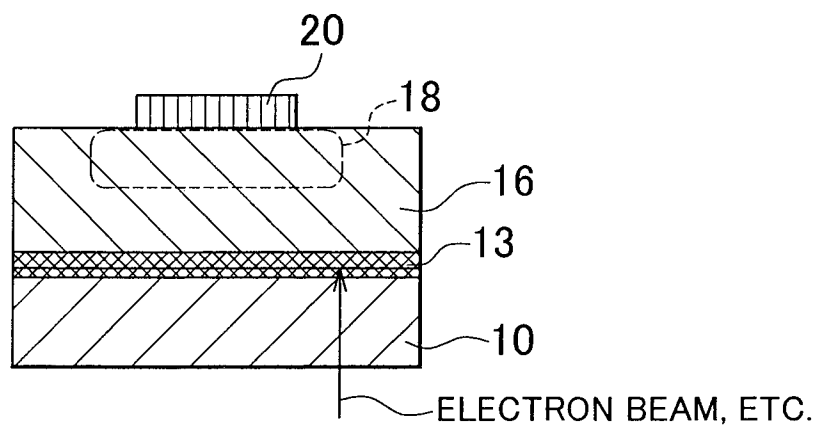
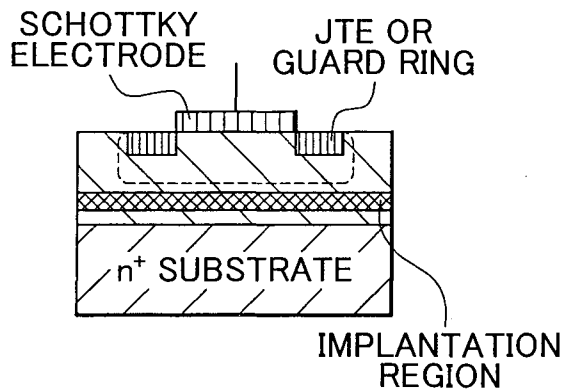
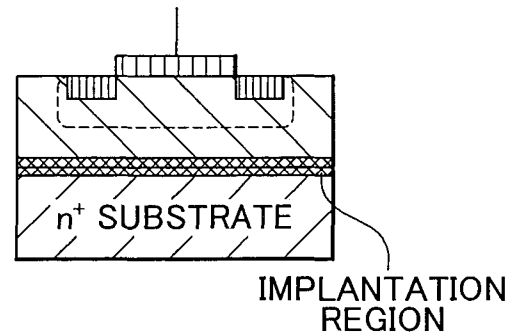


FIG. 4

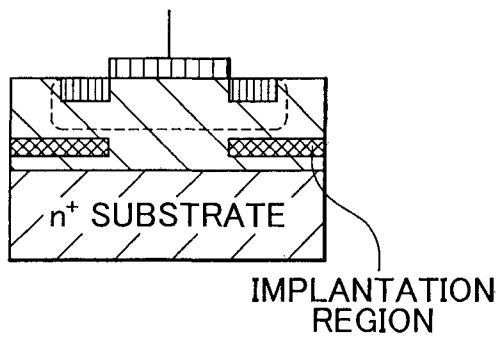
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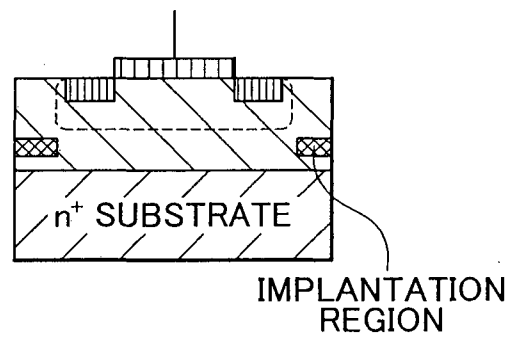
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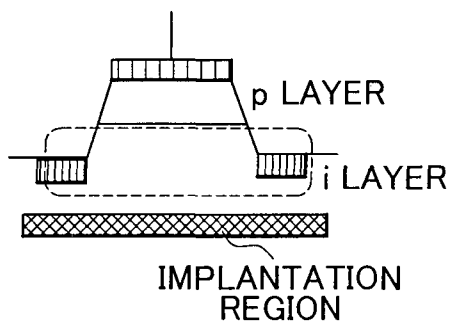
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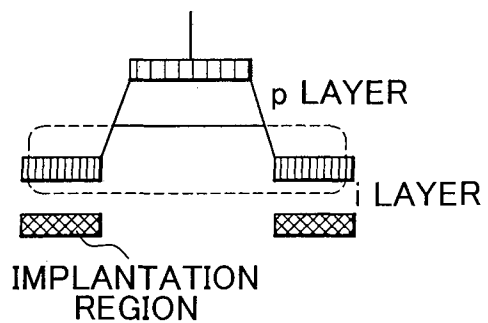
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(5) MESA PIN DIODE (EPITAXIAL JUNCTION)



(6) MESA PIN DIODE (EPITAXIAL JUNCTION)



(7)

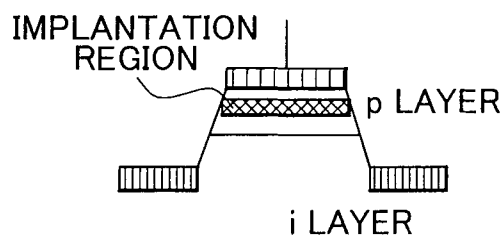


FIG. 5

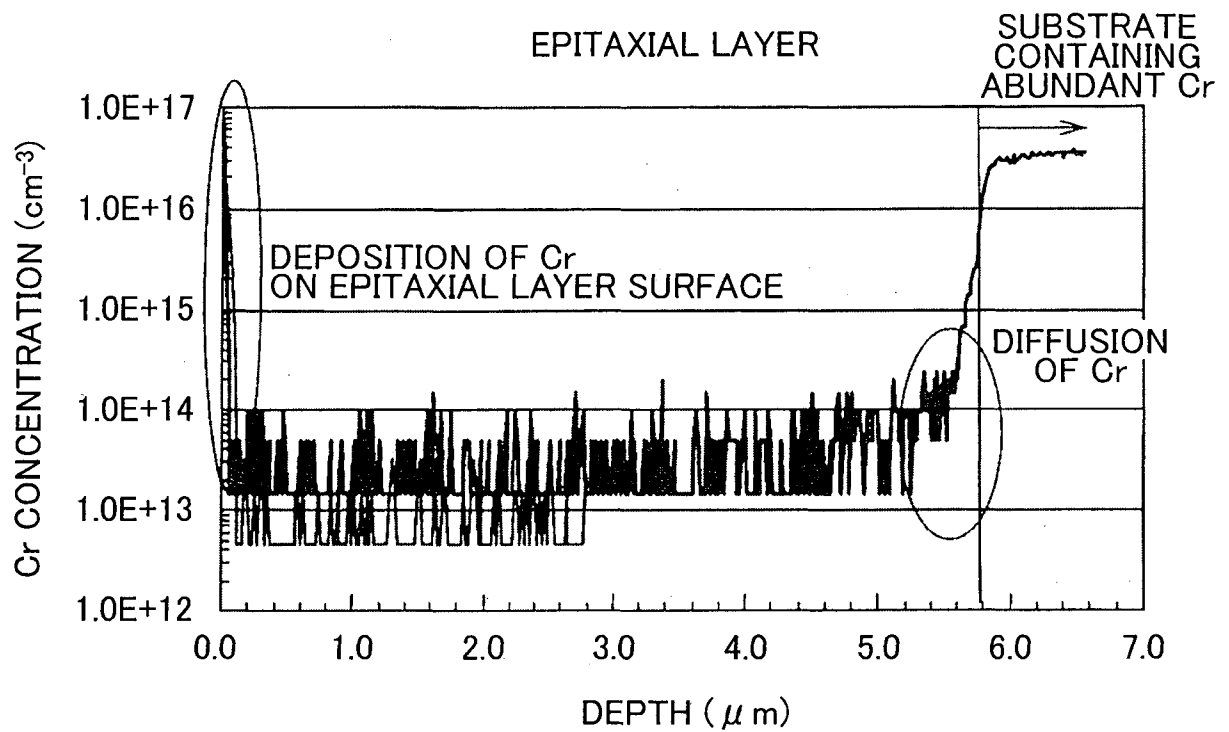


FIG. 6

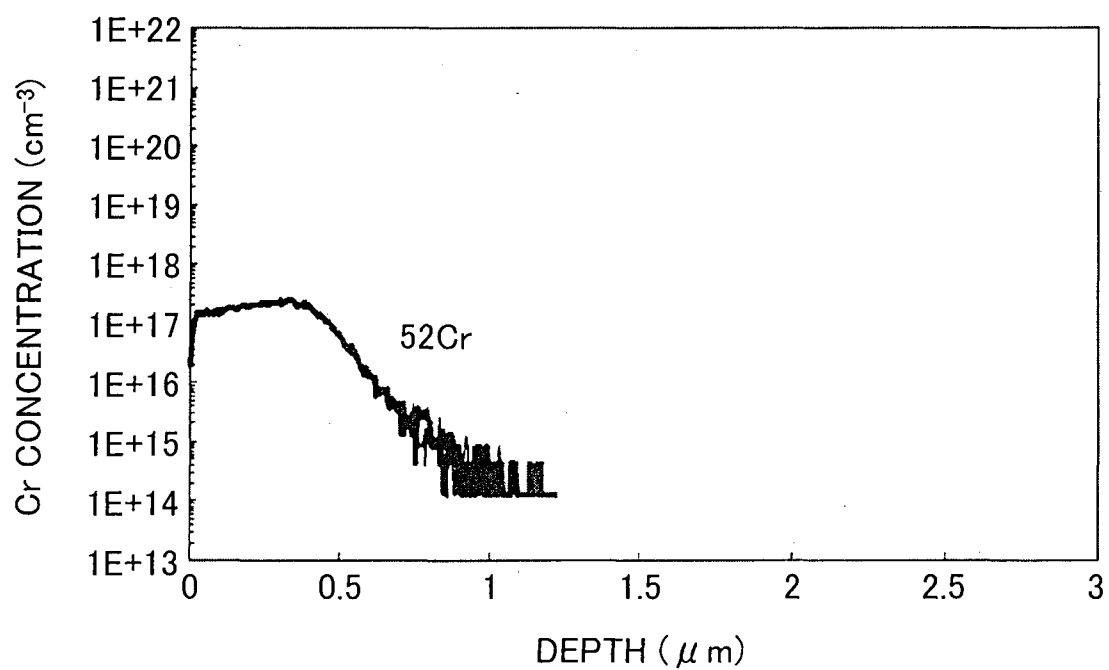


FIG. 7

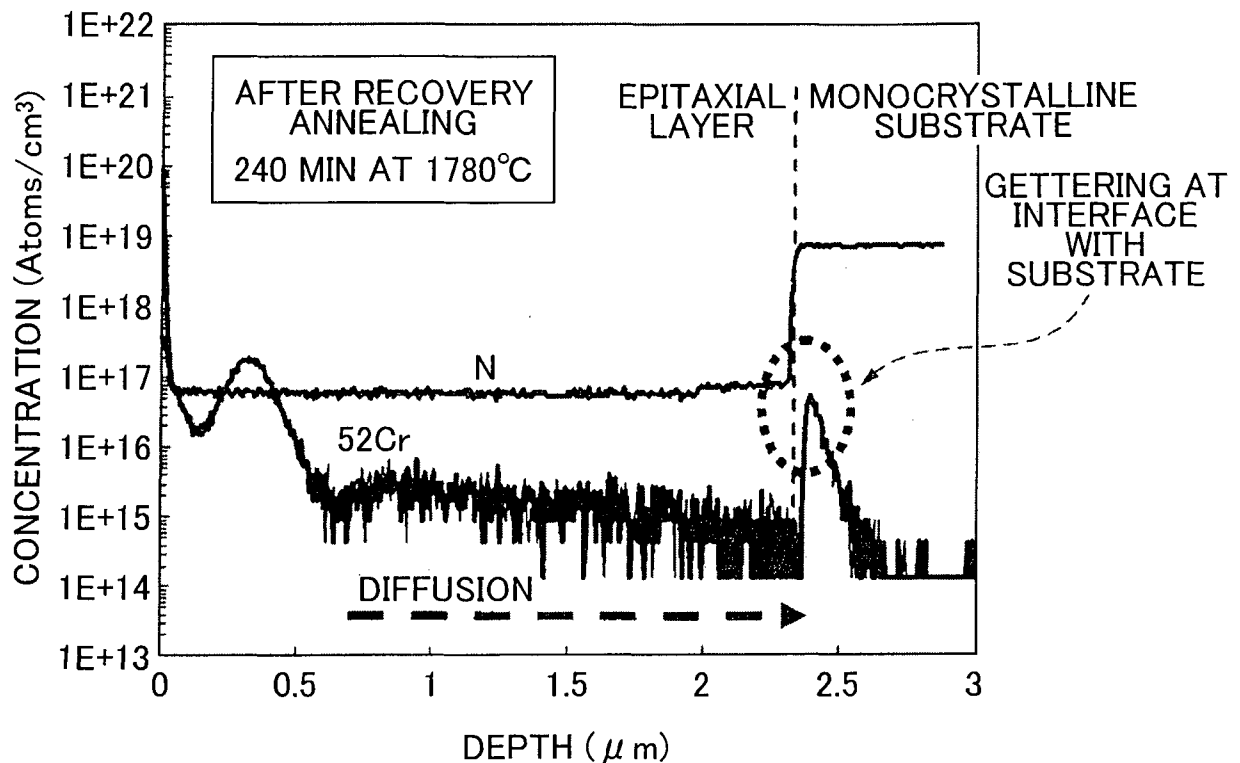


FIG. 8

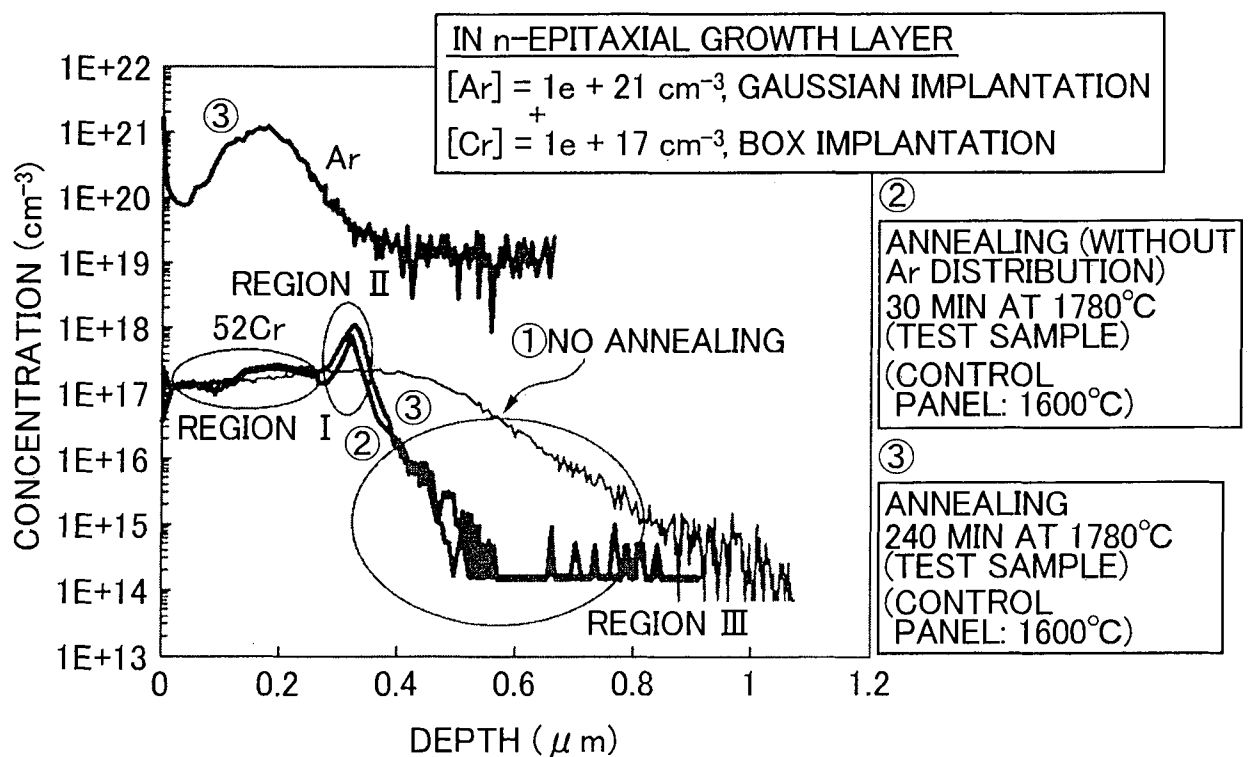


FIG. 9

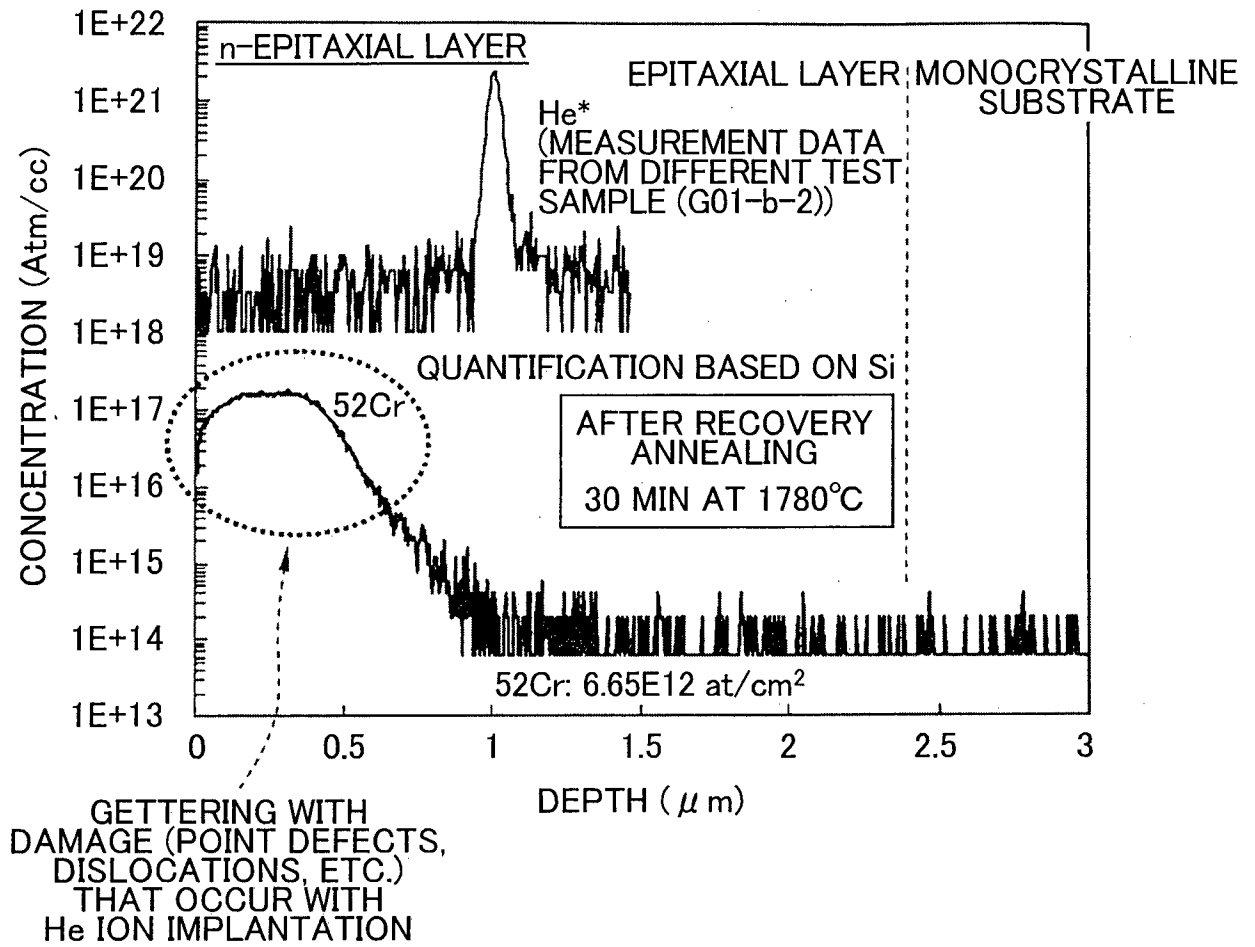


FIG. 10

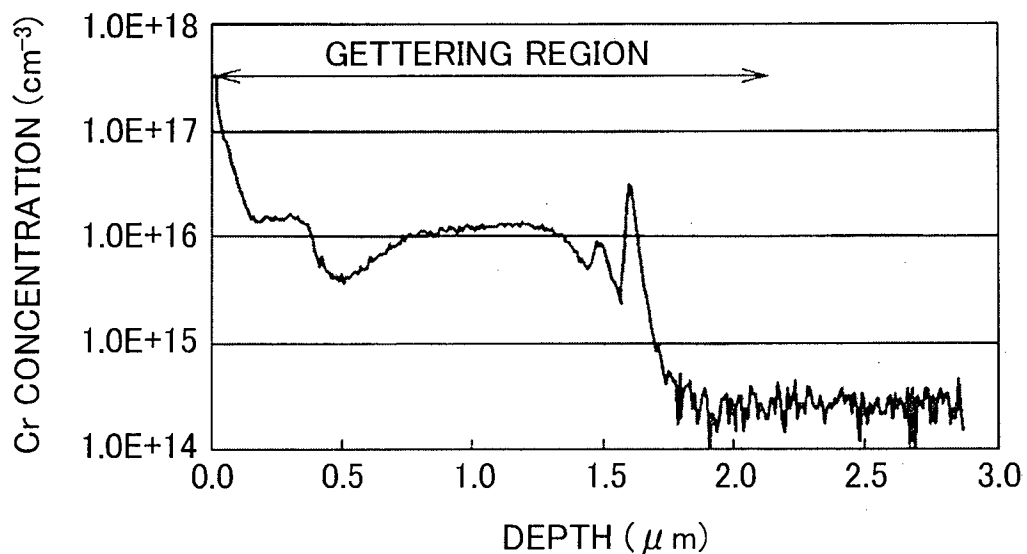


FIG. 11

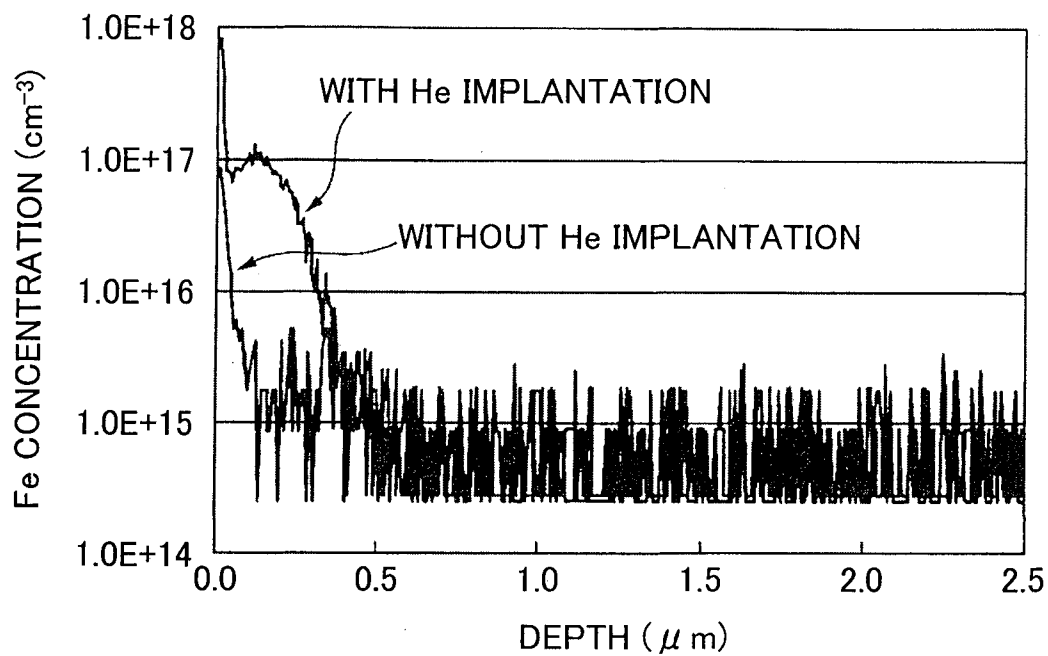


FIG. 12

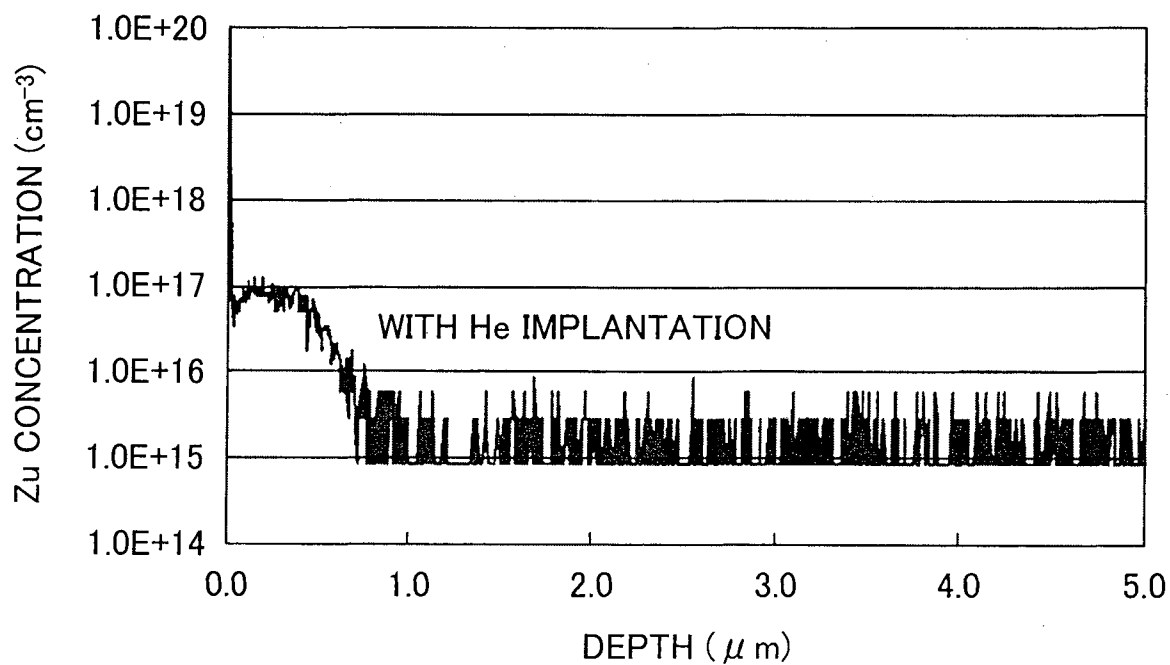
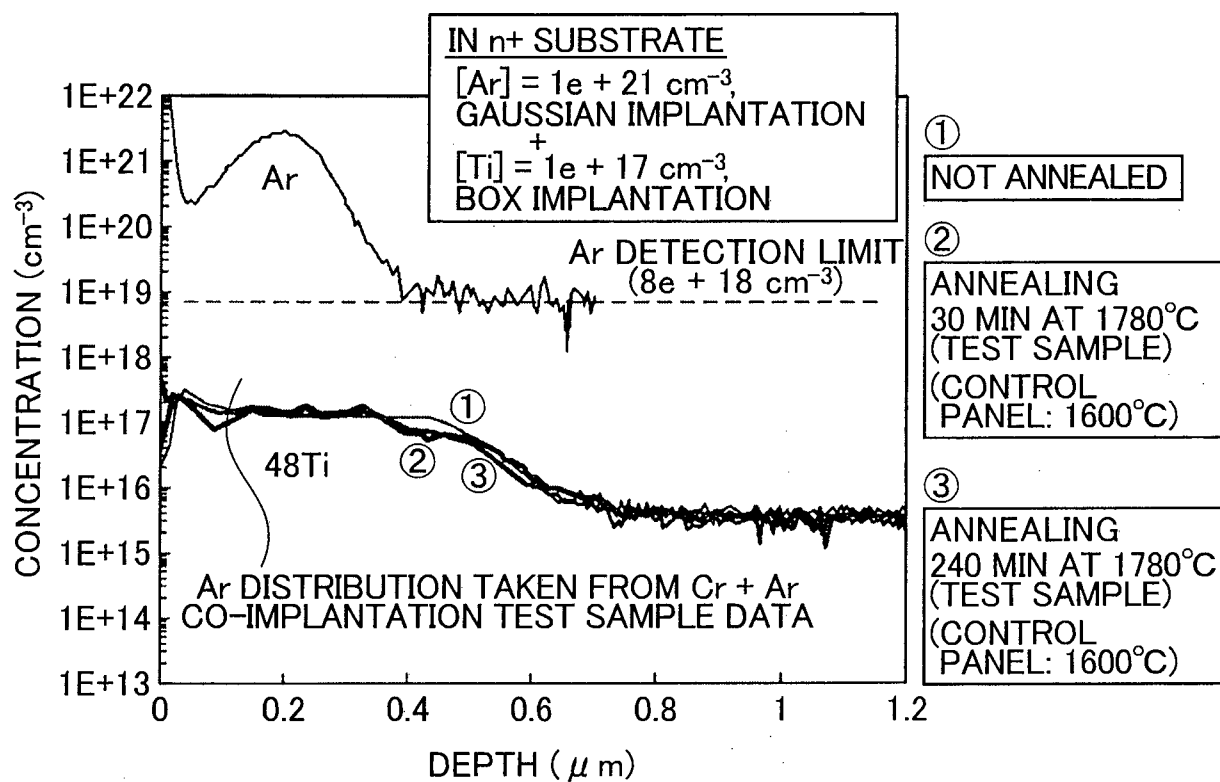


FIG. 13



INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/000875

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L21/322 H01L29/872 H01L29/868 ADD. H01L21/263 H01L21/265 H01L29/16		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, INSPEC, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	OTTAVIANI L ET AL: "Improvement of the thermal conductivity in 4H-SiC epitaxial layer by introducing gettering sites", MATERIALS SCIENCE FORUM TRANS TECH PUBLICATIONS LTD. SWITZERLAND, vol. 600-603, 2009, pages 525-528, XP002681559, ISSN: 0255-5476	1-7,9
Y	page 525 ----- -/--	8
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search	Date of mailing of the international search report	
9 August 2012	22/08/2012	
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Gélébart, Jacques	

INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	----- LIU CAICHI ET AL: "Gettering of metal impurities in silicon by fast neutron irradiation", 1998 5TH INTERNATIONAL CONFERENCE ON SOLID-STATE AND INTEGRATED CIRCUIT TECHNOLOGY. PROCEEDINGS (CAT. NO.98EX105) IEEE PISCATAWAY, NJ, USA, 1998, pages 341-343, XP002681562, ISBN: 0-7803-4306-9 abstract	8
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A	----- LACQUET B M ET AL: "ARGON ION IMPLANTATION GETTERING OF LARGE AREA P-N JUNCTIONS AND SCHOTTKY DIODES", NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - B: BEAM INTERACTIONS WITH MATERIALS AND ATOMS, ELSEVIER, AMSTERDAM, NL, vol. B06, no. 1/02, 1 January 1985 (1985-01-01), pages 372-375, XP000836602, ISSN: 0168-583X, DOI: 10.1016/0168-583X(85)90659-7 abstract	9
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International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JAN VOBECKÝVOBECKY ET AL: "High-Power P-i-N Diode With the Local Lifetime Control Based on the Proximity Gettering of Platinum", IEEE ELECTRON DEVICE LETTERS, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 23, no. 7, 1 July 2002 (2002-07-01), XP011066640, ISSN: 0741-3106 page 392 -----	9
A	EP 0 840 367 A2 (MOTOROLA INC [US]) 6 May 1998 (1998-05-06) abstract -----	9
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Information on patent family members

International application No

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