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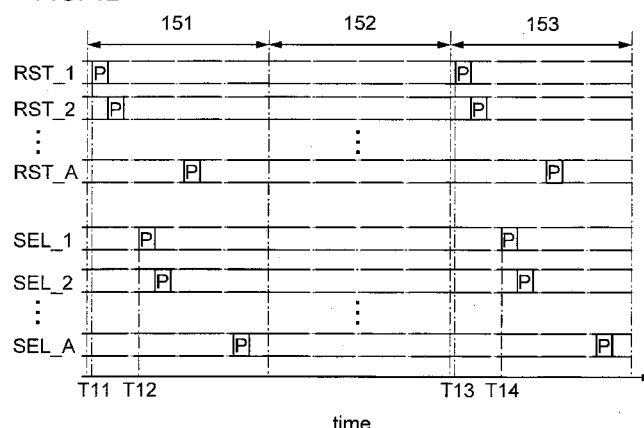
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FIG. 1B



(57) Abstract: To reduce power consumption, included are a selection signal output circuit, a reset signal output circuit, and a photodetector circuit. The selection signal output circuit is for outputting a selection signal. The reset signal output circuit is for outputting a reset signal. The photodetector circuit is supplied with the reset signal and the selection signal, is brought into a reset state in accordance with the input reset signal, generates a voltage corresponding to the illuminance of incident light when light enters the photodetector circuit, and outputs the generated voltage as a data signal in accordance with the input selection signal. In a first period, the reset signal output circuit and the selection signal output circuit output the reset signal and the selection signal, respectively. In a second period, stopped are output of the reset signal from the reset signal output circuit and output of the selection signal from the selection signal output circuit.

DESCRIPTION

**METHOD FOR DRIVING INPUT CIRCUIT AND METHOD FOR DRIVING
INPUT-OUTPUT DEVICE**

5

TECHNICAL FIELD

[0001]

An embodiment of the present invention relates to a method for driving an input circuit. Another embodiment of the present invention relates to a method for driving an
10 input-output device.

BACKGROUND ART

[0002]

In recent years, technological development of the following has been advanced:
15 input circuits capable of inputting data when light is incident thereon, input-output devices capable of inputting data when light is incident thereon and performing output in accordance with the input data, and the like.

[0003]

Examples of the input circuits include touch panels incorporating image sensors
20 or photosensors. The image sensors generally include CCD sensors and CMOS sensors. The CCD sensors are image sensors that perform charge transmission by vertical CCD and parallel CCD. The CMOS sensors are image sensors manufactured through a CMOS process. The CMOS sensors can control charge reading for each pixel with the use of switches of MOS transistors (for example, Patent Document 1).

25 [0004]

Examples of the input-output devices include input-output devices incorporating photosensors (for example, Patent Document 2). The input-output devices incorporating photosensors can function as touch panels when pixel portions are provided with display circuits and photodetector circuits (also referred to as
30 photosensors) and the photodetector circuits detect the illuminance of light incident on the pixel portions. Further, the input-output devices incorporating photosensors can

also change display states in accordance with detection results obtained by the photodetector circuits and display input text data, for example.

[Reference]

[0005]

5 [Patent Document 1] Japanese Published Patent Application No. 2009-049740

[Patent Document 2] Japanese Published Patent Application No. 2007-018458

DISCLOSURE OF INVENTION

[0006]

10 Conventional input circuits and input-output devices consume a large amount of power because data of the illuminance of light is read with photodetector circuits repeatedly every several milliseconds to several tens of milliseconds. Moreover, in the conventional input circuits and input-output devices, reading operations are performed in the photodetector circuits even in the case where there is no change in illuminance of
15 light incident on the photodetector circuits, and excessive power is consumed accordingly.

[0007]

 An object of one embodiment of the present invention is to reduce power consumption.

20 [0008]

 One embodiment of the present invention includes a selection signal output circuit, a reset signal output circuit, and a photodetector circuit. The selection signal output circuit is for outputting a selection signal. The reset signal output circuit is for outputting a reset signal. The photodetector circuit is supplied with the reset signal and
25 the selection signal, is brought into a reset state in accordance with the input reset signal, generates a voltage corresponding to the illuminance of incident light when light enters the photodetector circuit, and outputs the generated voltage as a data signal in accordance with the input selection signal. In a first period, the reset signal output circuit and the selection signal output circuit output the reset signal and the selection
30 signal, respectively. In a second period, stopped are output of the reset signal from the reset signal output circuit and output of the selection signal from the selection signal

output circuit.

[0009]

One embodiment of the present invention is a method for driving an input circuit. The input circuit includes a selection signal output circuit, a reset signal output
5 circuit, and a photodetector circuit. The selection signal output circuit is for outputting a selection signal. The reset signal output circuit is for outputting a reset signal. The photodetector circuit is supplied with the reset signal and the selection signal, is brought into a reset state in accordance with the input reset signal, generates a voltage corresponding to the illuminance of incident light when light enters the photodetector
10 circuit, and outputs the generated voltage as a data signal in accordance with the input selection signal. The method for driving the input circuit is as follows. In a first period, the reset signal output circuit and the selection signal output circuit output the reset signal and the selection signal, respectively, whereby the photodetector circuit outputs the data signal. In a second period, stopped are output of the reset signal from
15 the reset signal output circuit and output of the selection signal from the selection signal output circuit.

[0010]

One embodiment of the present invention is a method for driving an input circuit. The input circuit includes a selection signal output circuit, a reset signal output
20 circuit, and a photodetector circuit. The selection signal output circuit includes a first shift register to which a first start signal, a first clock signal, and a power supply voltage are input and outputs a selection signal when the first shift register outputs a signal. The reset signal output circuit includes a second shift register to which a second start signal, a second clock signal, and a power supply voltage are input and outputs a reset
25 signal when the second shift register outputs a signal. The photodetector circuit is supplied with the reset signal and the selection signal, is brought into a reset state in accordance with the input reset signal, generates a voltage corresponding to the illuminance of incident light when light enters the photodetector circuit, and outputs the generated voltage as a data signal in accordance with the input selection signal. The
30 method for driving the input circuit is as follows. In a first period, the second start signal and the second clock signal are output to the second shift register, and the first

start signal and the first clock signal are output to the first shift register. In a second period, stopped are output of the second start signal and the second clock signal to the second shift register and output of the first start signal and the first clock signal to the first shift register.

5 [0011]

One embodiment of the present invention is a method for driving an input circuit. The input circuit includes a selection signal output circuit, a reset signal output circuit, and a photodetector circuit. The selection signal output circuit includes a first shift register to which a first start signal, a first clock signal, and a power supply voltage
10 are input and outputs a selection signal when the first shift register outputs a signal. The reset signal output circuit includes a second shift register to which a second start signal, a second clock signal, and a power supply voltage are input and outputs a reset signal when the second shift register outputs a signal. The photodetector circuit is supplied with the reset signal and the selection signal, is brought into a reset state in
15 accordance with the input reset signal, generates a voltage corresponding to the illuminance of incident light when light enters the photodetector circuit, and outputs the generated voltage as a data signal in accordance with the input selection signal. The method for driving the input circuit is as follows. In a first period, the second start signal, the second clock signal, and the power supply voltage are output to the second
20 shift register, and the first start signal, the first clock signal, and the power supply voltage are output to the first shift register. In a second period, stopped are output of the second start signal, the second clock signal, and the power supply voltage to the second shift register and output of the first start signal, the first clock signal, and the power supply voltage to the first shift register.

25 [0012]

One embodiment of the present invention is a method for driving an input-output device. The input-output device includes a display circuit, a selection signal output circuit, a reset signal output circuit, and a photodetector circuit. The display circuit is supplied with a scan signal and supplied with an image signal in
30 accordance with the scan signal to be in a display state depending on the image signal. The selection signal output circuit includes a first shift register to which a first start

signal, a first clock signal, and a power supply voltage are input and outputs a selection signal when the first shift register outputs a signal. The reset signal output circuit includes a second shift register to which a second start signal, a second clock signal, and a power supply voltage are input and outputs a reset signal when the second shift register
5 outputs a signal. The photodetector circuit is supplied with the reset signal and the selection signal, is brought into a reset state in accordance with the input reset signal, generates a voltage corresponding to the illuminance of incident light when light enters the photodetector circuit, and outputs the generated voltage as a data signal in accordance with the input selection signal. In the input-output device, the display
10 circuit performs a displaying operation, and the photodetector circuit performs a reading operation. The method for driving the input-output device is as follows. In the reading operation, in a first period, the second start signal and the second clock signal are output to the second shift register, and the first start signal and the first clock signal are output to the first shift register. In a second period, stopped are output of the second
15 start signal and the second clock signal to the second shift register and output of the first start signal and the first clock signal to the first shift register.

[0013]

One embodiment of the present invention is a method for driving an input-output device. The input-output device includes a display circuit, a selection
20 signal output circuit, a reset signal output circuit, and a photodetector circuit. The display circuit is supplied with a scan signal and supplied with an image signal in accordance with the scan signal to be in a display state depending on the image signal. The selection signal output circuit includes a first shift register to which a first start signal, a first clock signal, and a power supply voltage are input and outputs a selection
25 signal when the first shift register outputs a signal. The reset signal output circuit includes a second shift register to which a second start signal, a second clock signal, and a power supply voltage are input and outputs a reset signal when the second shift register outputs a signal. The photodetector circuit is supplied with the reset signal and the selection signal, is brought into a reset state in accordance with the input reset signal,
30 generates a voltage corresponding to the illuminance of incident light when light enters the photodetector circuit, and outputs the generated voltage as a data signal in

accordance with the input selection signal. In the input-output device, the display circuit performs a displaying operation, and the photodetector circuit performs a reading operation. The method for driving the input-output device is as follows. In the reading operation, in a first period, the second start signal, the second clock signal, and the power supply voltage are output to the second shift register, and the first start signal, the first clock signal, and the power supply voltage are output to the first shift register. In a second period, stopped are output of the second start signal, the second clock signal, and the power supply voltage to the second shift register and output of the first start signal, the first clock signal, and the power supply voltage to the first shift register.

10 [0014]

Note that in this specification, terms with ordinal numbers, such as “first” and “second”, are used in order to avoid confusion among components, and the terms do not limit the components numerically.

[0015]

15 According to one embodiment of the present invention, an operation of outputting a signal to the photodetector circuit can be selectively stopped; thus, power consumption can be reduced.

BRIEF DESCRIPTION OF DRAWINGS

20 [0016]

FIGS. 1A and 1B illustrate an example of an input circuit in Embodiment 1.

FIGS. 2A and 2B illustrate a configuration example of a shift register.

FIGS. 3A and 3B show an example of a method for driving the shift register in FIG. 2A.

25 FIGS. 4A to 4C illustrate a configuration example of a shift register.

FIG. 5 shows an example of a method for driving the shift register in FIG. 4A.

FIGS. 6A to 6F illustrate photodetector circuits and timing charts thereof.

FIGS. 7A and 7B illustrate an example of an input-output device in Embodiment 5.

30 FIG. 8 illustrates an example of circuit configuration of a display circuit.

FIGS. 9A to 9D are cross-sectional schematic views each illustrating a structural

example of a transistor.

FIGS. 10A to 10C are cross-sectional schematic views illustrating a method for manufacturing the transistor in FIG. 9A.

FIGS. 11A and 11B are cross-sectional schematic views illustrating a method
5 for manufacturing the transistor in FIG. 9A.

FIGS. 12A to 12F illustrate structural examples of electronic devices in Embodiment 8.

BEST MODE FOR CARRYING OUT THE INVENTION

10 [0017]

Hereinafter, embodiments of the present invention will be described with reference to the drawings. Note that the present invention is not limited to the following description, and it will be easily understood by those skilled in the art that various changes and modifications can be made without departing from the spirit and
15 scope of the present invention. Thus, the present invention should not be interpreted as being limited to the following description of the embodiments.

[0018]

Note that contents described in the following embodiments can be combined with or replaced with each other as appropriate.

20 [0019]

[Embodiment 1]

In this embodiment, described is an input circuit which can input data when light enters the input circuit.

[0020]

25 An example of the input circuit in this embodiment is described with reference to FIGS. 1A and 1B. FIGS. 1A and 1B are diagrams for describing the example of the input circuit in this embodiment.

[0021]

First, an example of the configuration of the input circuit in this embodiment is
30 described with reference to FIG. 1A. FIG. 1A is a block diagram illustrating the example of the configuration of the input circuit in this embodiment.

[0022]

The input circuit in FIG. 1A includes a selection signal output circuit (also referred to as SELOUT) 101, a reset signal output circuit (also referred to as RSTOUT) 102, a photodetector circuit (also referred to as PS) 103p, and a reading circuit (also referred to as READ) 104.

[0023]

The selection signal output circuit 101 includes a shift register, and a start signal, a clock signal, and a power supply voltage are input to the shift register. When the shift register outputs a signal, the selection signal output circuit 101 outputs a selection signal SEL. The selection signal SEL is for controlling whether the photodetector circuit 103p outputs a signal. For example, the signal output from the shift register may be output as the selection signal SEL. Alternatively, the signal may be output from the shift register to a logic circuit and an output signal of the logic circuit may be output as the selection signal SEL.

[0024]

Note that a voltage generally refers to a difference between potentials at two points (also referred to as a potential difference). However, values of both a voltage and a potential are represented using volt (V) in a circuit diagram or the like in some cases, so that it is difficult to discriminate between them. This is why in this specification, a potential difference between a potential at one point and a potential to be the reference (also referred to as the reference potential) is used as a voltage at the point in some cases except for a case particularly specified.

[0025]

The reset signal output circuit 102 includes a shift register, and a start signal, a clock signal, and a power supply voltage are input to the shift register. When the shift register outputs a signal, the reset signal output circuit 102 outputs a reset signal RST. When the reset signal output circuit 102 is provided, the photodetector circuit 103p can be brought into a reset state. The reset signal RST is for controlling whether the photodetector circuit 103p is reset. For example, the signal output from the shift register may be output as the reset signal RST. Alternatively, the signal may be output from the shift register to a logic circuit and an output signal of the logic circuit may be

the reset signal RST.

[0026]

Note that the number of the signals output from the shift register of the selection signal output circuit 101 may be either the same as or different from that of the signals output from the shift register of the reset signal output circuit 102. Further, the number of the selection signals SEL output from the selection signal output circuit 101 may be either the same as or different from that of the reset signals RST output from the reset signal output circuit 102.

[0027]

10 The photodetector circuit 103p generates a voltage corresponding to the illuminance of incident light when light enters the photodetector circuit 103p. Note that a voltage corresponding to the illuminance of incident light is also referred to as an optical data voltage. The photodetector circuit 103p is provided in the photodetection portion 103 to which data is input externally when light is detected.

15 [0028]

Supplied with the reset signal RST, the photodetector circuit 103p is brought into a reset state in accordance with the supplied reset signal RST. Note that when the photodetector circuit 103p is in a reset state, an optical data voltage is a reference value.

[0029]

20 Further, supplied with the selection signal SEL, the photodetector circuit 103p outputs an optical data voltage as a data signal in accordance with the supplied selection signal SEL.

[0030]

For example, the photodetector circuit 103p may include an amplifying transistor and a photoelectric conversion element (also referred to as PCE).

[0031]

When light enters the photoelectric conversion element, a current (also referred to as a photocurrent) corresponding to the illuminance of incident light flows through the photoelectric conversion element.

30 [0032]

The amplifying transistor has two terminals and a control terminal for

controlling a conduction state between the two terminals. The voltage of the control terminal changes in accordance with a photocurrent corresponding to the illuminance of incident light, whereby the amplifying transistor sets the voltage of an output signal of the photodetector circuit 103p. Thus, an optical data voltage output from the photodetector circuit 103p depends on the illuminance of light incident on the photodetector circuit 103p.

[0033]

The photodetector circuit 103p may be further provided with an output selecting transistor so that an optical data voltage is output as a data signal from the photodetector circuit 103p when the transistor is turned on in accordance with the selection signal SEL.

[0034]

The reading circuit 104 has a function of reading an optical data voltage output from the selected photodetector circuit 103p as a data signal.

[0035]

For example, a selection circuit may be used for the reading circuit 104. Supplied with a reading selection signal, the selection circuit used for the reading circuit 104 selects the photodetector circuit 103p from which an optical data voltage is read, in accordance with the input reading selection signal. Note that the selection circuit may select a plurality of the photodetector circuits 103p, from which optical data voltages are read, at one time. The selection circuit may include, for example, a plurality of transistors so that the photodetector circuit 103p from which an optical data voltage is read can be selected when the plurality of transistors are turned on or off.

[0036]

Note that by using a control circuit, for example, operations of the selection signal output circuit 101, the reset signal output circuit 102, and the reading circuit 104 can be controlled.

[0037]

The control circuit has a function of outputting a control signal that is a pulse signal. The control signal is output to the selection signal output circuit 101, the reset signal output circuit 102, and the reading circuit 104, whereby operations of the selection signal output circuit 101, the reset signal output circuit 102, and the reading circuit 104

can be controlled in accordance with a pulse of the control signal. For example, output of a start signal, a clock signal, or a power supply voltage to the shift registers of the selection signal output circuit 101 and the reset signal output circuit 102 can be started or stopped in accordance with a pulse of the control signal. The control circuit may be
5 controlled using a CPU, for example. For example, an interval between pulses of control signals generated by the control circuit may be set using a CPU.

[0038]

Operations of the selection signal output circuit 101, the reset signal output circuit 102, and the reading circuit 104 may be controlled in accordance with not only
10 the control circuit but an operation signal. The operation signal is a signal indicating whether a user has performed an input operation of the input circuit. As the input operation, a user's operation of touching the photodetection portion 103, or the like can be given. For example, when an operation signal is input to the control circuit through an interface, the control circuit generates a control signal whose interval between pulses
15 of control signals is set in accordance with the input operation signal, and the generated control signal is output to the selection signal output circuit 101 or the reset signal output circuit 102.

[0039]

Next, an example of a method for driving the input circuit in FIG. 1A is
20 described as an example of a method for driving the input circuit in this embodiment.

[0040]

In the example of a method for driving the input circuit in FIG. 1A, there are a period in which at least an operation of the selection signal output circuit is stopped to stop output of the selection signal to the photodetector circuit. The example of a
25 method for driving the input circuit in FIG. 1A is described with reference to FIG. 1B. FIG. 1B illustrates the example of a method for driving the input circuit in FIG. 1A. Here, for example, the number of the selection signals SEL and the number of the reset signals RST are each A (A is a natural number larger than or equal to 3).

[0041]

30 First, in a period 151, the reset signal output circuit 102 outputs the reset signals RST. At a time T11, the reset signal output circuit 102 outputs a pulse of the first reset

signal RST_1 and then sequentially outputs pulses of the second to the A-th reset signals RST_2 to RST_A. In addition, in the period 151, the selection signal output circuit 101 outputs the selection signals SEL. At a time T12, the selection signal output circuit 101 outputs a pulse of the first selection signal SEL_1 and then sequentially outputs pulses of the second to the A-th selection signals SEL_2 to SEL_A. Note that the timing when the pulse of the first selection signal SEL_1 is output is not limited to the time T12 and it is acceptable as long as the timing is after output of the pulse of the first reset signal RST_1.

[0042]

10 The photodetector circuit 103p is brought into a reset state in accordance with the input reset signal RST and then generates an optical data voltage. Supplied with a pulse of the selection signal SEL, the photodetector circuit 103p outputs the generated optical data voltage as a data signal.

[0043]

15 Then, the reading circuit 104 sequentially reads optical data voltages output from the photodetector circuit 103p. When all the optical data voltages are read, the reading operation is completed. The read optical data voltages are used as data signals for executing predetermined processing. That is the operation in the period 151.

[0044]

20 Next, in a period 152, output of the reset signals RST from the reset signal output circuit 102 and output of the selection signals SEL from the selection signal output circuit 101 are stopped. At that time, the pulses of the first to the A-th reset signals RST_1 to RST_A are not output, and the pulses of the first to the A-th selection signals SEL_1 to SEL_A are not output. Note that a stop of a signal means, for example, a stop of a pulse of the signal or inputting a voltage which does not function as a signal to a wiring for outputting a signal. A pulse generated due to a noise or the like is not necessarily stopped.

[0045]

Further, an optical data voltage is not output from the photodetector circuit 103p to which the pulse of the selection signal SEL is not input. That is an operation in the period 152.

[0046]

When output of the reset signals RST from the reset signal output circuit 102 is resumed, as shown in a period 153, the reset signal output circuit 102 outputs the reset signals RST. At a time T13, the reset signal output circuit 102 outputs the pulse of the first reset signal RST_1 and then sequentially outputs the pulses of the second to the A-th reset signals RST_2 to RST_A. When output of the selection signals SEL from the selection signal output circuit 101 is resumed, as shown in the period 153, the selection signal output circuit 101 outputs the selection signals SEL. At a time T14, the selection signal output circuit 101 outputs the pulse of the first selection signal SEL_1 and then sequentially outputs the pulses of the second to the A-th selection signals SEL_2 to SEL_A. Note that the timing when the pulse of the first selection signal SEL_1 is output is not limited to the time T14 and it is acceptable as long as the timing is after output of the pulse of the first reset signal RST_1. That is the example of a method for driving the input circuit in FIG. 1A.

15 [0047]

The operations in the period 151, the period 152, and the period 153 may be performed a plurality of times.

[0048]

The timing when the period shifts from the period 151 to the period 152 may be set with a pulse of the control signal generated in accordance with the operation signal. For example, the operation of the input circuit may be switched from the operation in the period 151 to the operation in the period 152 when the pulse of the control signal is input to the input circuit. After a certain period of time passes, the operation may be switched from the operation in the period 152 to the operation in the period 153. At that time, switching from the operation in the period 152 to the operation in the period 153 may be performed in accordance with the pulse of the control signal.

[0049]

As described with reference to FIGS. 1A and 1B, in the input circuit of this embodiment, the selection signal output circuit outputs the selection signals in a first period, and at least output of the selection signals is stopped in a second period. Thus, the operation of the photodetector circuit can be stopped in part of the periods, resulting

in reduction in power consumption.

[0050]

Further, in the case of the input circuit of this embodiment, the period can be shifted from the first period to the second period; therefore, power consumption can be reduced without disturbing an actual operation. For example, when a user does not perform an input operation of the input circuit, output of a signal from the photodetector circuit is stopped, and only when a user performs the input operation of the input circuit, output of the selection signal from the selection signal output circuit and output of the reset signal from the reset signal output circuit are started. Consequently, power consumption can be reduced.

[0051]

Moreover, in the input circuit of this embodiment, not only output of the selection signals but output of the reset signals can be stopped. Thus, power consumption can be further reduced as compared to the case where only output of the pulses of the selection signals is stopped.

[0052]

[Embodiment 2]

In this embodiment, further described is the shift register of the selection signal output circuit and the reset signal output circuit in the input circuit of the above embodiment.

[0053]

The shift register of the selection signal output circuit and the reset signal output circuit in the input circuit of the above embodiment is described with reference to FIGS. 2A and 2B. FIGS. 2A and 2B are diagrams for describing the shift register.

[0054]

First, an example of the configuration of the shift register of the selection signal output circuit and the reset signal output circuit in the input circuit of the above embodiment is described with reference to FIG. 2A. FIG. 2A is a diagram illustrating the configuration example of the shift register.

[0055]

The shift register in FIG. 2A includes P-stage (P is a natural number larger than

or equal to 3) sequential circuits (also referred to as FFs).

[0056]

To the shift register in FIG. 2A, a start signal SP is input as a start signal and a clock signal CLK1, a clock signal CLK2, a clock signal CLK3, and a clock signal CLK4
5 are input as clock signals. By using the plurality of clock signals, the speed of a signal output operation of the shift register can be increased.

[0057]

The sequential circuits are described below.

[0058]

10 Each of the sequential circuits 10_1 to 10_P is supplied with a set signal ST, a reset signal RE, a clock signal CK1, a clock signal CK2, and a clock signal CK3 and outputs a signal OUT1 and a signal OUT2. The clock signal CK1, the clock signal CK2, and the clock signal CK3 are delayed by a 1/4 cycle sequentially. Note that any three of the clock signals CLK1 to CLK4 may be used as the clock signal CK1, the clock
15 signal CK2, and the clock signal CK3. The clock signals of the same combination are not input to the sequential circuits adjacent to each other.

[0059]

In addition, the circuit configuration of the sequential circuit in FIG. 2A is described with reference to FIG. 2B. FIG. 2B is a circuit diagram illustrating the circuit
20 configuration of the sequential circuit in FIG. 2A.

[0060]

The sequential circuit in FIG. 2B includes a transistor 31, a transistor 32, a transistor 33, a transistor 34, a transistor 35, a transistor 36, a transistor 37, a transistor 38, a transistor 39, a transistor 40, and a transistor 41.

25 [0061]

The transistors of the shift register in FIG. 2B are field-effect transistors each having at least a source, a drain, and a gate unless otherwise specified.

[0062]

The source refers to all or part of a source region, a source electrode, and a
30 source wiring. A conductive layer having a function of both a source electrode and a source wiring is referred to as a source in some cases without distinction between a

source electrode and a source wiring.

[0063]

The drain refers to all or part of a drain region, a drain electrode, and a drain wiring. A conductive layer having a function of both a drain electrode and a drain wiring is referred to as a drain in some cases without distinction between a drain electrode and a drain wiring.

[0064]

The gate refers to all or part of a gate electrode or all or part of a gate wiring. A conductive layer having a function of both a gate electrode and a gate wiring is referred to as a gate in some cases without distinction between a gate electrode and a gate wiring.

[0065]

Further, the source and the drain of the transistor may be interchanged in some cases, depending on the structure, the operating condition, or the like of the transistor.

15 [0066]

A voltage V_a is input to one of the source and the drain of the transistor 31, and the set signal ST is input to the gate of the transistor 31.

[0067]

One of the source and the drain of the transistor 32 is electrically connected to the other of the source and the drain of the transistor 31, and a voltage V_b is input to the other of the source and the drain of the transistor 32.

[0068]

One of the source and the drain of the transistor 33 is electrically connected to the other of the source and the drain of the transistor 31, and the voltage V_a is input to the gate of the transistor 33.

[0069]

The voltage V_a is input to one of the source and the drain of the transistor 34, and the clock signal CK3 is input to the gate of the transistor 34.

[0070]

30 One of the source and the drain of the transistor 35 is electrically connected to the other of the source and the drain of the transistor 34, the other of the source and the

drain of the transistor 35 is electrically connected to the gate of the transistor 32, and the clock signal CK2 is input to the gate of the transistor 35.

[0071]

The voltage Va is input to one of the source and the drain of the transistor 36,
5 and the reset signal RE is input to the gate of the transistor 36.

[0072]

One of the source and the drain of the transistor 37 is electrically connected to the gate of the transistor 32 and the other of the source and the drain of the transistor 36, the voltage Vb is input to the other of the source and the drain of the transistor 37, and
10 the set signal ST is input to the gate of the transistor 37.

[0073]

The clock signal CK1 is input to one of the source and the drain of the transistor 38, and the gate of the transistor 38 is electrically connected to the other of the source and the drain of the transistor 33.

15 [0074]

One of the source and the drain of the transistor 39 is electrically connected to the other of the source and the drain of the transistor 38, the voltage Vb is input to the other of the source and the drain of the transistor 39, and the gate of the transistor 39 is electrically connected to the gate of the transistor 32.

20 [0075]

The clock signal CK1 is input to one of the source and the drain of the transistor 40, and the gate of the transistor 40 is electrically connected to the other of the source and the drain of the transistor 33.

[0076]

25 One of the source and the drain of the transistor 41 is electrically connected to the other of the source and the drain of the transistor 40, the voltage Vb is input to the other of the source and the drain of the transistor 41, and the gate of the transistor 41 is electrically connected to the gate of the transistor 32.

[0077]

30 Note that one of the voltage Va and the voltage Vb is a high power supply voltage Vdd, and the other is a low power supply voltage Vss. The high power supply

voltage Vdd is a voltage relatively higher than the low power supply voltage Vss. The low power supply voltage Vss is a voltage relatively lower than the high power supply voltage Vdd. The values of the voltage Va and the voltage Vb are interchanged in some cases, depending on the polarity of the transistor, or the like. The difference
5 between the voltage Va and the voltage Vb is a power supply voltage.

[0078]

In FIG. 2B, a portion where the other of the source and the drain of the transistor 33, the gate of the transistor 38, and the gate of the transistor 40 are electrically connected to one another is referred to as a node NA. A portion where the gate of the
10 transistor 32, the other of the source and the drain of the transistor 35, the other of the source and the drain of the transistor 36, the one of the source and the drain of the transistor 37, the gate of the transistor 39, and the gate of the transistor 41 are electrically connected to one another is referred to as a node NB. A portion where the other of the source and the drain of the transistor 38 and the one of the source and the drain of the
15 transistor 39 are electrically connected to each other is referred to as a node NC. A portion where the other of the source and the drain of the transistor 40 and the one of the source and the drain of the transistor 41 are electrically connected to each other is referred to as a node ND.

[0079]

20 The sequential circuit in FIG. 2B outputs a voltage of the node NC and a voltage of the node ND as the signal OUT1 and the signal OUT2, respectively.

[0080]

Further, the start signal SP is input as the set signal ST to the gate of the transistor 31 and the gate of the transistor 37 in the first sequential circuit 10_1.

25 [0081]

The gate of the transistor 31 and the gate of the transistor 37 in the (Q+2)-th (Q is a natural number larger than or equal to 1 and smaller than or equal to (P-2)) sequential circuit 10_Q+2 are electrically connected to the other of the source and the drain of the transistor 38 in the (Q+1)-th sequential circuit 10_Q+1. At that time, the
30 signal OUT1 in the sequential circuit 10_Q+1 is the set signal ST in the sequential circuit 10_Q+2.

[0082]

The other of the source and the drain of the transistor 38 in the U-th (U is a natural number larger than or equal to 3 and smaller than or equal to P) sequential circuit 10_U is electrically connected to the gate of the transistor 36 in the (U-2)-th sequential circuit 10_U-2. At that time, the signal OUT1 in the sequential circuit 10_U is the reset signal RE in the sequential circuit 10_U-2.

[0083]

Further, a signal RP1 is input as the reset signal to the gate of the transistor 36 in the (P-1)-th sequential circuit 10_P-1. The signal OUT2 output from the (P-1)-th sequential circuit 10_P-1 is not necessarily used to operate the other circuits.

[0084]

A signal RP2 is input as the reset signal to the gate of the transistor 36 in the P-th sequential circuit 10_P. The signal OUT2 output from the P-th sequential circuit 10_P is not necessarily used to operate the other circuits.

15 [0085]

The transistors 31 to 41 may have the same conductivity type.

[0086]

In the shift register of this embodiment, a protective circuit may be provided so as to be electrically connected to a terminal to be supplied with the high power supply voltage Vdd in each of the first to the (P-2)-th sequential circuits 10_1 to 10_P-2. By providing the protective circuit, even when the value of the high power supply voltage Vdd is large enough to break an element due to noise or the like, breakdown of the element in the shift register can be suppressed.

[0087]

25 In the shift register of this embodiment, a protective circuit may be provided so as to be electrically connected to the other of the source and the drain of the transistor 38 in each of the first to the (P-2)-th sequential circuits 10_1 to 10_P-2. By providing the protective circuit, even when the value of the voltage of the signal OUT1 is large enough to break an element due to noise or the like, breakdown of the element in the circuit to which the signal OUT1 is input can be suppressed.

[0088]

In addition, an example of the operation of the sequential circuit in FIG. 2B is described with reference to FIG. 3A. FIG. 3A is a timing chart for describing the example of the operation of the sequential circuit in FIG. 2B. For example, the transistors 31 to 41 in the sequential circuit in FIG. 2B are all n-channel transistors, and the high power supply voltage Vdd and the low power supply voltage Vss are input as the voltage Va and the voltage Vb, respectively.

[0089]

First, at a time T61, the clock signal CK1 is at a low level, the clock signal CK2 is changed to a low level, the clock signal CK3 is at a high level, the set signal ST is changed to a high level, and the reset signal RE is at a low level.

[0090]

At that time, the sequential circuit is set to a set state. The transistor 31 and the transistor 33 are turned on, so that a voltage of the node NA (also referred to as V_{NA}) starts to change. When the voltage of the node NA is raised to be higher than the threshold voltage of the transistor 38, the transistor 38 is turned on, and when the voltage of the node NA is raised to be higher than the threshold voltage of the transistor 40, the transistor 40 is turned on. Further, the voltage of the node NA changes to be equivalent to the voltage Va. When the voltage of the node NA changes to be equivalent to the voltage Va, the transistor 33 is turned off. Since the transistor 34 is in an on state, the transistor 35 is in an off state, the transistor 36 is in an off state, and the transistor 37 is in an on state, a voltage of the node NB (also referred to as V_{NB}) changes to be equivalent to the voltage Vb. When the voltage of the node NB changes, the transistor 32, the transistor 39, and the transistor 41 are turned off. At that time, the signal OUT1 and the signal OUT2 are at a low level.

[0091]

Next, at a time T62, the clock signal CK1 is changed to a high level, the clock signal CK2 remains at a low level, the clock signal CK3 is changed to a low level, the set signal ST remains at a high level, and the reset signal RE remains at a low level.

[0092]

At that time, the transistor 31 is turned off and the transistor 33 remains in an off state, so that the node NA is brought into a floating state. At that time, the transistor

38 and the transistor 40 remain in an on state; thus, voltages of the other of the source and the drain of the transistor 38 and the other of the source and the drain of the transistor 40 are raised. Then, the voltage of the node NA is raised because of capacitive coupling due to parasitic capacitance caused between the gate and the other of the source and the drain of each of the transistor 38 and the transistor 40, which is a so-called bootstrap operation. The voltage of the node NA is raised to a value still larger than the sum of the voltage V_a and the threshold voltage of the transistor 38 (also referred to as V_{th38}) or the threshold voltage of the transistor 40 (V_{th40}), that is, raised to $(V_a + V_{th38} + V_x)$ or $(V_a + V_{th40} + V_x)$. At that time, the transistor 38 and the transistor 40 remain in an on state. Since the transistor 34 is turned off, the transistor 35 remains in an off state, the transistor 36 remains in an off state, and the transistor 37 remains in an on state, the transistor 32, the transistor 39, and the transistor 41 remain in an off state. Further, at that time, the signal OUT1 and the signal OUT2 are set to a high level.

15 [0093]

Next, at a time T63, the clock signal CK1 remains at a high level, the clock signal CK2 is changed to a high level, the clock signal CK3 remains at a low level, the set signal ST is changed to a low level, and the reset signal RE remains at a low level.

[0094]

20 At that time, the transistor 31 is turned off, so that the voltage of the node NA is kept to be much larger than the sum of the voltage V_a and the threshold voltage of the transistor 38 or the threshold voltage of the transistor 40. Since the transistor 33 remains in an off state, the transistor 38 and the transistor 40 remain in an on state. Further, the transistor 34 remains in an off state, the transistor 35 remains in an off state, the transistor 36 remains in an off state, and the transistor 37 is turned off, so that the voltage of the node NB is kept to be equivalent to the voltage V_b . Thus, the transistor 32, the transistor 39, and the transistor 41 remain in an off state. Further, at that time, the signal OUT1 and the signal OUT2 remain at a high level.

[0095]

30 Next, at a time T64, the clock signal CK1 is changed to a low level, the clock signal CK2 remains at a high level, the clock signal CK3 is changed to a high level, the

set signal ST remains at a low level, and the reset signal RE is changed to a high level.

[0096]

At that time, the sequential circuit is set to a reset state. The transistor 34, the transistor 35, and the transistor 36 are turned on and the transistor 37 remains in an off state; thus, the voltage of the node NB starts to change. When the voltage of the node NB is raised to be higher than the threshold voltage of the transistor 32, the transistor 32 is turned on. When the voltage of the node NB is raised to be higher than the threshold voltage of the transistor 39, the transistor 39 is turned on. When the voltage of the node NB is raised to be higher than the threshold voltage of the transistor 41, the transistor 41 is turned on. At that time, the voltage of the node NB changes to be equivalent to the voltage Vb. Further, the voltage of the one of the source and the drain of the transistor 33 changes to be equivalent to the voltage Vb, so that the transistor 33 is turned on and the voltage of the node NA starts to change. When the voltage of the node NA changes to be lower than the threshold voltage of the transistor 38, the transistor 38 is turned off, and when the voltage of the node NA changes to be lower than the threshold voltage of the transistor 40, the transistor 40 is turned off. The voltage of the node NA changes to be equivalent to the voltage Vb. At that time, the signal OUT1 and the signal OUT2 are at a low level.

[0097]

Next, at a time T65, the clock signal CK1 remains at a low level, the clock signal CK2 is changed to a low level, the clock signal CK3 remains at a high level, the set signal ST remains at a low level, and the reset signal RE remains at a high level.

[0098]

At that time, the transistor 34 remains in an on state, the transistor 35 is turned off, the transistor 36 remains in an on state, and the transistor 37 remains in an off state; thus, the voltage of the node NB is kept to be equivalent to the voltage Va and the transistor 32, the transistor 39, and the transistor 41 remain in an on state. At that time, the transistor 31 remains in an off state, the transistor 33 remains in an on state, and the voltage of the node NA is kept to be equivalent to the voltage Vb; thus, the transistor 38 and the transistor 40 remain in an off state. Further, at that time, the signal OUT1 and the signal OUT2 remain at a low level.

[0099]

As described above, the sequential circuit can output the signal OUT1 and the signal OUT2. That is an example of the operation of the sequential circuit in FIG. 2B.

[0100]

5 Subsequently, an example of the operation of the shift register in FIG. 2A is described.

[0101]

In the case of the shift register in FIG. 2A, there is a period in which signal output is stopped. An example of a method for driving the shift register in FIG. 2A for
10 which the period when signal output is stopped is set is described with reference to FIG. 3B. FIG. 3B is a timing chart showing the example of a method for driving the shift register in FIG. 2A.

[0102]

First, described is an operation in a period in which the shift register in FIG. 2A
15 performs signal output. As shown in a period 311 in FIG. 3B, the start signal SP, a power supply voltage Vp, and the clock signals CLK1 to CLK4 are input. When a pulse of the start signal SP is input to the first sequential circuit 10_1, pulses of the signals OUT1 and the signals OUT2 are output sequentially from the first to the P-th sequential circuits 10_1 to 10_P in accordance with the clock signals CLK1 to CLK4.
20 That is the operation in the period in which the shift register in FIG. 2A performs signal output.

[0103]

Next, described is an operation in a period in which signal output of the shift register in FIG. 2A is stopped. As shown in a period 312 in FIG. 3B, stopped is output
25 of the power supply voltage Vp, the clock signals CLK1 to CLK4, and the start signal SP to the shift register.

[0104]

At that time, output of the start signal SP to the shift register is stopped first. Then, output of the clock signal CLK1 to the shift register is stopped, output of the clock
30 signal CLK2 to the shift register is stopped, output of the clock signal CLK3 to the shift register is stopped, output of the clock signal CLK4 to the shift register is stopped, and

output of the power supply voltage V_p to the shift register is stopped. Thus, malfunctions of the shift register in stopping signal output of the shift register can be suppressed.

[0105]

- 5 When output of the power supply voltage V_p , the clock signals CLK1 to CLK4, and the start signal SP to the shift register is stopped, output of the pulses of the signals OUT1 and the signals OUT2 from the first to the P-th sequential circuits 10_1 to 10_P is stopped. That is the operation in the period in which signal output of the shift register in FIG. 2A is stopped.

10 [0106]

Further, described is an operation in the case where signal output of the shift register in FIG. 2A is resumed. As shown in a period 313 in FIG. 3B, resumed is output of the start signal SP, the clock signals CLK1 to CLK4, and the power supply voltage V_p to the shift register.

15 [0107]

- At that time, output of the power supply voltage V_p to the shift register is resumed first. Then, output of the clock signal CLK1 to the shift register is resumed, output of the clock signal CLK2 to the shift register is resumed, output of the clock signal CLK3 to the shift register is resumed, output of the clock signal CLK4 to the shift register is resumed, and output of the start signal SP to the shift register is resumed. Note that at that time, it is preferable to output the clock signals CLK1 to CLK4 after application of the high power supply voltage V_{dd} to a wiring through which the clock signals CLK1 to CLK4 are output.

20 [0108]

- 25 In the case where output of the start signal SP, the clock signals CLK1 to CLK4, and the power supply voltage V_p is resumed, when a pulse of the start signal SP is input to the first sequential circuit 10_1, pulses of the signals OUT1 and the signals OUT2 are output sequentially from the first to the P-th sequential circuits 10_1 to 10_P in accordance with the clock signals CLK1 to CLK4. That is the operation in the period in which signal output of the shift register in FIG. 2A is resumed.

30 [0109]

As described with reference to FIGS. 2A and 2B and FIGS. 3A and 3B, the shift register of this embodiment includes the sequential circuits of the plurality of stages. Each of the plurality of sequential circuits includes a first transistor, a second transistor, and a third transistor. The first transistor has a gate to which a set signal is input and controls whether to turn on the second transistor in accordance with the set signal. The second transistor has a source and a drain one of which is supplied with a clock signal and controls whether to set the voltage of an output signal from the sequential circuit to a value corresponding to the voltage of the clock signal. The third transistor has a gate to which a reset signal is input and controls whether to turn off the second transistor in accordance with the reset signal. With such a structure, signal output of the shift register can be stopped easily.

[0110]

For example, the shift register of this embodiment can be used for the reset signal output circuit of the above embodiment. Thus, a period in which reset signal output is stopped can be provided. Further, with the structure, when output of the start signal, the clock signals, and the power supply voltage to the shift register is stopped, the period in which signal output of the shift register is stopped can be provided.

[0111]

Moreover, the shift register of this embodiment can be used for the selection signal output circuit of the above embodiment. Thus, a period in which selection signal output is stopped can be provided. Further, with the structure, when output of the start signal, the clock signals, and the power supply voltage to the shift register is stopped, the period in which signal output of the shift register is stopped can be provided.

[0112]

[Embodiment 3]

In this embodiment, further described is the shift register of the selection signal output circuit and the reset signal output circuit in the input circuit of the above embodiment.

[0113]

The shift register of the selection signal output circuit and the reset signal output circuit in the input circuit of the above embodiment may have a structure different from

that in Embodiment 2. A configuration example of the shift register of the selection signal output circuit and the reset signal output circuit in the input circuit of the above embodiment is described with reference to FIGS. 4A to 4C. FIGS. 4A to 4C are diagrams for describing a configuration example of the shift register.

5 [0114]

First, the configuration example of the shift register of the selection signal output circuit and the reset signal output circuit in the input circuit of the above embodiment are described with reference to FIG. 4A. FIG. 4A is a diagram illustrating the configuration example of the shift register.

10 [0115]

The shift register in FIG. 4A includes O (O is a natural number) sequential circuits of O stages.

[0116]

To the shift register in FIG. 4A, the start signal SP is input as a start signal and a
15 clock signal CLK11 and a clock signal CLK12 are input as clock signals.

[0117]

Each of the sequential circuits 20_1 to 20_O is supplied with the set signal ST, the clock signal CK1, and the clock signal CK2, and outputs a signal OUT11. As the clock signal CK1, one of the clock signal CLK11 and the clock signal CLK12 can be
20 used. As the clock signal CK2, the other of the clock signal CLK11 and the clock signal CLK12 can be used. As the clock signal CLK12, for example, an inverted clock signal of the clock signal CLK11 can be used. The clock signals serving as the clock signal CK1 and the clock signal CK2 are alternately input to the sequential circuits adjacent to each other.

25 [0118]

In addition, the circuit configuration of the sequential circuit in FIG. 4A is described with reference to FIG. 4B. FIG. 4B is a circuit diagram illustrating the circuit configuration of the sequential circuit in FIG. 4A.

[0119]

30 The sequential circuit in FIG. 4B includes a clocked inverter 51, an inverter 52, and a clocked inverter 53.

[0120]

The clocked inverter 51 has a data signal input terminal and a data signal output terminal. The clocked inverter 51 is supplied with the set signal ST through the data signal input terminal and then supplied with the clock signal CK1 and the clock signal
5 CK2 through the data signal input terminal.

[0121]

The inverter 52 has a data signal input terminal and a data signal output terminal. The data signal input terminal of the inverter 52 is electrically connected to the data signal output terminal of the clocked inverter 51. The inverter 52 outputs as the signal
10 OUT11 a voltage depending on a voltage input through the data signal input terminal, through the data signal output terminal.

[0122]

The clocked inverter 53 has a data signal input terminal and a data signal output terminal. The data signal input terminal of the clocked inverter 53 is electrically
15 connected to the data signal output terminal of the inverter 52. The data signal output terminal of the clocked inverter 53 is electrically connected to the data signal output terminal of the clocked inverter 51.

[0123]

In addition, an example of the circuit configuration of the clocked inverter of
20 the sequential circuit in FIG. 4B is described with reference to FIG. 4C. FIG. 4C is a circuit diagram illustrating the example of the circuit configuration of the clocked inverter.

[0124]

The clocked inverter in FIG. 4C includes a transistor 54a, a transistor 54b, a
25 transistor 54c, and a transistor 54d.

[0125]

The transistors of the clocked inverter in FIG. 4C are field-effect transistors each having at least a source, a drain, and a gate unless otherwise specified.

[0126]

30 The clock signal CK1 is input to the gate of the transistor 54a, and the voltage Va is input to one of the source and the drain of the transistor 54a. The transistor 54a is

a p-channel transistor.

[0127]

One of the source and the drain of the transistor 54b is electrically connected to the other of the source and the drain of the transistor 54a. The transistor 54b is a
5 p-channel transistor.

[0128]

One of the source and the drain of the transistor 54c is electrically connected to the other of the source and the drain of the transistor 54b. The transistor 54c is an n-channel transistor.

10 [0129]

The clock signal CK2 is input to the gate of the transistor 54d. One of the source and the drain of the transistor 54d is electrically connected to the other of the source and the drain of the transistor 54c. The voltage Vb is input to the other of the source and the drain of the transistor 54d. The transistor 54d is an n-channel transistor.

15 [0130]

In the clocked inverter in FIG. 4C, the gate of the transistor 54b and the gate of the transistor 54c function as the data signal input terminals, and the other of the source and the drain of the transistor 54b and the one of the source and the drain of the transistor 54c function as the data signal output terminals.

20 [0131]

Further, an example of the operation of the shift register in FIG. 4A is described. It is assumed here that the high power supply voltage Vdd and the low power supply voltage Vss are input as the voltage Va and the voltage Vb, respectively.

[0132]

25 In the case of the shift register in FIG. 4A, there is a period in which signal output is stopped. An example of a method for driving the shift register in FIG. 4A for which the period is set is described below.

[0133]

First, described is an operation in a period in which the shift register in FIG. 4A
30 performs signal output. As shown in a period 321 in FIG. 5, the start signal SP and the clock signals CLK11 and CLK12 are input to the shift register. When a pulse of the

start signal SP is input to the first sequential circuit 20_1, pulses of the signals OUT11 are output sequentially from the first to the O-th sequential circuits 20_1 to 20_O in accordance with the clock signals CLK11 and CLK12. That is the operation in the period in which the shift register in FIG. 4A performs signal output.

5 [0134]

Next, described is an operation in a period in which signal output of the shift register in FIG. 4A is stopped. As shown in a period 322 in FIG. 5, stopped is output of the clock signals CLK11 and CLK12 and the start signal SP to the shift register.

[0135]

10 At that time, output of the start signal SP to the shift register is stopped first. Then, after output of the pulses of the signals OUT11 from all the sequential circuits, output of the clock signals CLK11 and CLK12 to the shift register is stopped. Thus, malfunctions of the shift register in stopping signal output of the shift register can be suppressed. Moreover, after output of the clock signals CLK11 and CLK12 to the shift
15 register is stopped, output of the power supply voltage Vp to the shift register may be stopped to further reduce power consumption.

[0136]

When output of the clock signals CLK11 and CLK12 and the start signal SP to the shift register is stopped, output of the pulses of the signals OUT11 from the first to
20 the O-th sequential circuits 20_1 to 20_O is stopped. That is the operation in the period in which signal output of the shift register in FIG. 4A is stopped.

[0137]

Further, described is an operation in a period in which signal output of the shift register, which has been stopped, is resumed. As shown in a period 323 in FIG. 5,
25 resumed is output of the start signal SP and the clock signals CLK11 and CLK12 to the shift register.

[0138]

At that time, output of the clock signals CLK11 and CLK12 to the shift register is resumed, and output of the start signal SP to the shift register is resumed. Note that
30 at that time, it is preferable to output the clock signals CLK11 and CLK12 after application of the high power supply voltage Vdd to a wiring through which the clock

signals CLK11 and CLK12 are output. In the case where output of the power supply voltage Vp to the shift register is stopped in the period 322, output of the power supply voltage Vp to the shift register is resumed before resumption of output of the clock signals CLK11 and CLK12.

5 [0139]

In the case where output of the start signal SP and the clock signals CLK11 and CLK12 is resumed, when a pulse of the start signal SP is input to the first sequential circuit 20_1, pulses of the signals OUT11 are output sequentially from the first to the O-th sequential circuits 20_1 to 20_O in accordance with the clock signals CLK11 and
10 CLK12. That is the operation in the period in which signal output of the shift register in FIG. 4A is resumed.

[0140]

As described with reference to FIGS. 4A to 4C and FIG. 5, the shift register of this embodiment includes the clocked inverters. With such a structure, output of the
15 power supply voltage and the clock signal to the sequential circuit can be stopped easily to stop output of an output signal.

[0141]

For example, the shift register of this embodiment can be used for the reset signal output circuit of the above embodiment. Thus, a period in which reset signal
20 output is stopped can be provided. Further, with the structure, when output of the start signal, the clock signals, and the power supply voltage to the shift register is stopped, the period in which signal output of the shift register is stopped can be provided.

[0142]

Moreover, the shift register of this embodiment can be used for the selection
25 signal output circuit of the above embodiment. Thus, a period in which selection signal output is stopped can be provided. Further, with the structure, when output of the start signal, the clock signals, and the power supply voltage to the shift register is stopped, the period in which signal output of the shift register is stopped can be provided.

[0143]

30 [Embodiment 4]

In this embodiment, the photodetector circuit in the input circuit of the above

embodiment is further described.

[0144]

The photodetector circuit in the input circuit of the above embodiment is described with reference to FIGS. 6A to 6F. FIGS. 6A to 6F are diagrams for
5 describing the photodetector circuit.

[0145]

First, configuration examples of the photodetector circuit of this embodiment are described with reference to FIGS. 6A to 6C. FIGS. 6A to 6C are diagrams each illustrating the configuration example of the photodetector circuit of this embodiment.

10 [0146]

The photodetector circuit in FIG. 6A includes a photoelectric conversion element 121a, a transistor 122a, and a transistor 123a.

[0147]

The transistors of the photodetector circuit in FIG. 6A are field-effect transistors
15 each having at least a source, a drain, and a gate unless otherwise specified.

[0148]

The photoelectric conversion element 121a has a first terminal and a second terminal. The reset signal RST is input to the first terminal of the photoelectric conversion element 121a.

20 [0149]

The gate of the transistor 122a is electrically connected to the second terminal of the photoelectric conversion element 121a.

[0150]

One of the source and the drain of the transistor 123a is electrically connected to
25 one of the source and the drain of the transistor 122a. The selection signal SEL is input to the gate of the transistor 123a.

[0151]

The voltage V_a is input to one of the other of the source and the drain of the transistor 122a and the other of the source and the drain of the transistor 123a.

30 [0152]

In addition, the photodetector circuit in FIG. 6A outputs the voltage of the other

of the other of the source and the drain of the transistor 122a and the other of the source and the drain of the transistor 123a, as a data signal. The voltage of the other of the other of the source and the drain of the transistor 122a and the other of the source and the drain of the transistor 123a at that time is an optical data voltage.

5 [0153]

The photodetector circuit in FIG. 6B includes a photoelectric conversion element 121b, a transistor 122b, a transistor 123b, a transistor 124, and a transistor 125.

[0154]

The transistors of the photodetector circuit in FIG. 6B are field-effect transistors
10 each having at least a source, a drain, and a gate unless otherwise specified.

[0155]

The photoelectric conversion element 121b has a first terminal and a second terminal. The voltage V_b is input to the first terminal of the photoelectric conversion element 121b.

15 [0156]

A charge accumulation control signal TX is input to the gate of the transistor 124. One of the source and the drain of the transistor 124 is electrically connected to the second terminal of the photoelectric conversion element 121b.

[0157]

20 The gate of the transistor 122b is electrically connected to the other of the source and the drain of the transistor 124.

[0158]

The reset signal RST is input to the gate of the transistor 125. The voltage V_a is input to one of a source and a drain of the transistor 125. The other of the source and
25 the drain of the transistor 125 is electrically connected to the other of the source and the drain of the transistor 124.

[0159]

The selection signal SEL is input to the gate of the transistor 123b. One of the source and the drain of the transistor 123b is electrically connected to one of the source
30 and the drain of the transistor 122b.

[0160]

The voltage V_a is input to one of the other of the source and the drain of the transistor 122b and the other of the source and the drain of the transistor 123b.

[0161]

In addition, the photodetector circuit in FIG. 6B outputs the voltage of the other
5 of the other of the source and the drain of the transistor 122b and the other of the source and the drain of the transistor 123b, as a data signal. The voltage of the other of the other of the source and the drain of the transistor 122b and the other of the source and the drain of the transistor 123b at that time is an optical data voltage.

[0162]

10 The photodetector circuit in FIG. 6C includes a photoelectric conversion element 121c, a transistor 122c, and a capacitor 126.

[0163]

The transistor of the photodetector circuit in FIG. 6C is a field-effect transistor having at least a source, a drain, and a gate unless otherwise specified.

15 [0164]

The photoelectric conversion element 121c has a first terminal and a second terminal. The reset signal RST is input to the first terminal of the photoelectric conversion element 121c.

[0165]

20 The capacitor 126 has a first terminal and a second terminal. The selection signal SEL is input to the first terminal of the capacitor 126. The second terminal of the capacitor 126 is electrically connected to the second terminal of the photoelectric conversion element 121c.

[0166]

25 The gate of the transistor 122c is electrically connected to the second terminal of the photoelectric conversion element 121c. The voltage V_a is input to one of a source and a drain of the transistor 122c.

[0167]

The photodetector circuit in FIG. 6C outputs the voltage of the other of the
30 source and the drain of the transistor 122c, as a data signal. The voltage of the other of the source and the drain of the transistor 122c at that time is an optical data voltage.

[0168]

The photoelectric conversion elements 121a to 121c each have a function of generating a current corresponding to the illuminance of incident light when light enters the photoelectric conversion element. As the photoelectric conversion elements 121a to 121c, photodiodes, phototransistors, or the like can be used. When the photoelectric conversion elements 121a to 121c are photodiodes, one of an anode and a cathode of the photodiode corresponds to the first terminal of the photoelectric conversion element, and the other of the anode and the cathode of the photodiode corresponds to the second terminal of the photoelectric conversion element. When the photoelectric conversion elements 121a to 121c are phototransistors, one of a source and a drain of the phototransistor corresponds to the first terminal of the photoelectric conversion element, and the other of the source and the drain of the phototransistor corresponds to the second terminal of the photoelectric conversion element. Note that in the photodiode, a conducting state (also referred to as the state C) is a state where a forward voltage is applied and a current flows between the first terminal and the second terminal, while a nonconducting state (also referred to as the state NC) is a state where a reverse voltage is applied, so that a forward current does not flow. In addition, when the photodiode is in a nonconducting state, light incident thereon may cause a current to flow between the first terminal and the second terminal. In the phototransistor, a conducting state refers to an on state (also referred to as the state ON), while a nonconducting state refers to an off state (also referred to as the state OFF). In addition, when the phototransistor is in a nonconducting state, light incident thereon may cause a current to flow between the first terminal and the second terminal.

[0169]

The transistors 122a to 122c each have a function of an amplifying transistor for setting an output signal (optical data voltage) of the photodetector circuit. As the transistors 122a to 122c, it is possible to use transistors each including as a channel formation layer, for example, a semiconductor layer belonging to Group 14 of the periodic table (e.g., silicon) or an oxide semiconductor layer. The oxide semiconductor layer of the transistor, which has a function of the channel formation layer, is a semiconductor layer highly purified to be intrinsic (also referred to as I-type) or

substantially intrinsic. Note that the high purification means at least one of the following concepts: removal of hydrogen from an oxide semiconductor layer as much as possible; and reduction of defects, which are caused by oxygen deficiency in an oxide semiconductor layer, by supply of oxygen to the oxide semiconductor layer.

5 [0170]

The transistor 124 controls whether to set the voltage of the gate of the transistor 122b to a voltage corresponding to a photocurrent generated by the photoelectric conversion element 121b by being turned on or off in accordance with the charge accumulation control signal TX. The charge accumulation control signal TX
10 can be generated by a shift register, for example. Note that in the photodetector circuit of this embodiment, the transistor 124 is not necessarily provided; however, in the case of providing the transistor 124, the voltage of the gate of the transistor 122b can be held for a certain period of time when the gate of the transistor 122b is in a floating state.

[0171]

15 The transistor 125 controls whether to reset the voltage of the gate of the transistor 122b to the voltage V_a by being turned on or off in accordance with the reset signal RST. Note that in the photodetector circuit of this embodiment, the transistor 125 is not necessarily provided; however, in the case of providing the transistor 125, the voltage of the gate of the transistor 122b can be reset to the desired voltage.

20 [0172]

The off-state current of the transistor 124 and the transistor 125 is preferably low and for example, the off-state current per micrometer in channel width is preferably 10 aA (1×10^{-17} A) or less, more preferably 1 aA (1×10^{-18} A) or less, still more preferably 10 zA (1×10^{-20} A) or less, further preferably 1 zA (1×10^{-21} A) or less. The
25 use of a transistor with low off-state current as each of the transistor 124 and the transistor 125 can suppress variation in voltage of the gate of the transistor 122b due to leakage current of the transistor 124 and the transistor 125. As the transistor with low off-state current, a transistor including an oxide semiconductor layer as a channel formation layer can be used, for example. The oxide semiconductor layer of the
30 transistor, which has a function of the channel formation layer, is a semiconductor layer highly purified to be intrinsic (also referred to as I-type) or substantially intrinsic.

[0173]

The transistors 123a and 123b each controls whether to output the optical data voltage as a data signal from the photodetector circuit by being turned on or off in accordance with the selection signal SEL. As the transistors 123a and 123b, it is possible to use transistors each including as a channel formation layer, for example, a semiconductor layer or an oxide semiconductor layer including a semiconductor belonging to Group 14 of the periodic table (e.g., silicon or germanium). The oxide semiconductor layer of the transistor, which has a function of the channel formation layer, is a semiconductor layer highly purified to be intrinsic (also referred to as I-type) or substantially intrinsic.

[0174]

Subsequently, described are examples of methods for driving the photodetector circuits in FIGS. 6A to 6C.

[0175]

First, the example of the method for driving the photodetector circuit in FIG. 6A is described with reference to FIG. 6D. FIG. 6D is a diagram for describing the example of the method for driving the photodetector circuit in FIG. 6A and shows states of the reset signal RST, the selection signal SEL, the photoelectric conversion element 121a, and the transistor 123a.

[0176]

In the example of the method for driving the photodetector circuit in FIG. 6A, first, in a period T31, a pulse of the reset signal RST is input.

[0177]

At that time, the photoelectric conversion element 121a is brought into a conducting state and the transistor 123a is turned off.

[0178]

At that time, the voltage of the gate of the transistor 122a is reset to a certain value.

[0179]

Then, in a period T32 after input of the pulse of the reset signal RST, the photoelectric conversion element 121a is brought into a nonconducting state and the

transistor 123a remains in an off state.

[0180]

At that time, a photocurrent flows between the first terminal and the second terminal of the photoelectric conversion element 121a in accordance with the illuminance of light incident on the photoelectric conversion element 121a. Further, the voltage value of the gate of the transistor 122a varies depending on the photocurrent.

[0181]

Then, in the period T33, a pulse of the selection signal SEL is input.

[0182]

At that time, the photoelectric conversion element 121a remains in a nonconducting state, the transistor 123a is turned on, a current flows through the source and the drain of the transistor 122a and the source and the drain of the transistor 123a, and the photodetector circuit in FIG. 6A outputs as a data signal the voltage of the other of the other of the source and the drain of the transistor 122a and the other of the source and the drain of the transistor 123a. That is the example of the method for driving the photodetector circuit in FIG. 6A.

[0183]

Next, the example of the method for driving the photodetector circuit in FIG. 6B is described with reference to FIG. 6E. FIG. 6E is a diagram for describing the example of the method for driving the photodetector circuit in FIG. 6B.

[0184]

In the example of the method for driving the photodetector circuit in FIG. 6B, first, in a period T41, a pulse of the reset signal RST is input. In addition, in the period T41 and a period T42, a pulse of the charge accumulation control signal TX is input. Note that in the period T41, the timing for starting input of the pulse of the reset signal may be earlier than the timing for starting input of the pulse of the charge accumulation control signal TX.

[0185]

At that time, first, in the period T41, the photoelectric conversion element 121b is brought into a conducting state so that the transistor 124 is turned on, whereby the voltage of the gate of the transistor 122b is reset to a value equivalent to the voltage V_a .

[0186]

Then, in the period T42 after input of the pulse of the reset signal RST, the photoelectric conversion element 121b is brought into a nonconducting state, the transistor 124 remains in an on state, and the transistor 125 is turned off.

5 [0187]

At that time, a photocurrent flows between the first terminal and the second terminal of the photoelectric conversion element 121b in accordance with the illuminance of light incident on the photoelectric conversion element 121b. Further, the voltage value of the gate of the transistor 122b varies depending on the photocurrent.

10 [0188]

Then, in a period T43 after input of the pulse of the charge accumulation control signal TX, the transistor 124 is turned off.

[0189]

At that time, the voltage of the gate of the transistor 122b is kept to be a value
15 corresponding to a photocurrent of the photoelectric conversion element 121b in the period T42. Note that the period T43 is not necessary; however, in the case where there is the period T43, the timing for the photodetector circuit to output an optical data voltage as a data signal can be set appropriately.

[0190]

20 Then, in a period T44, a pulse of the selection signal SEL is input.

[0191]

At that time, the photoelectric conversion element 121b remains in a nonconducting state and the transistor 123b is turned on.

[0192]

25 Further, at that time, a current flows through the source and the drain of the transistor 122b and the source and the drain of the transistor 123b, and the photodetector circuit in FIG. 6B outputs as a data signal the voltage of the other of the other of the source and the drain of the transistor 122b and the other of the source and the drain of the transistor 123b. That is the example of the method for driving the photodetector
30 circuit in FIG. 6B.

[0193]

Next, the example of the method for driving the photodetector circuit in FIG. 6C is described with reference to FIG. 6F. FIG. 6F is a diagram for describing the example of the method for driving the photodetector circuit in FIG. 6C.

[0194]

5 In the example of the method for driving the photodetector circuit in FIG. 6C, first, in a period T51, a pulse of the reset signal RST is input.

[0195]

At that time, the photoelectric conversion element 121c is brought into a conducting state and the voltage of the gate of the transistor 122c is reset to a certain
10 value.

[0196]

Then, in a period T52 after input of the pulse of the reset signal RST, the photoelectric conversion element 121c is brought into a nonconducting state.

[0197]

15 At that time, a photocurrent flows between the first terminal and the second terminal of the photoelectric conversion element 121c in accordance with the illuminance of light incident on the photoelectric conversion element 121c. Further, the voltage of the gate of the transistor 122c varies depending on the photocurrent.

[0198]

20 Then, in a period T53, a pulse of the selection signal SEL is input.

[0199]

At that time, the photoelectric conversion element 121c remains in a nonconducting state, a current flows between the source and the drain of the transistor 122c, and the photodetector circuit in FIG. 6C outputs as a data signal the voltage of the
25 other of the source and the drain of the transistor 122c. That is the example of the method for driving the photodetector circuit in FIG. 6C.

[0200]

As described with reference to FIGS. 6A to 6F, the photodetector circuit of the above embodiment includes the photoelectric conversion element and the transistor.
30 The photodetector circuit outputs an optical data voltage as a data signal in accordance with the selection signal. With such a structure, for example, input of the selection

signal can be stopped to stop output of the optical data voltage from the photodetector circuit; therefore, a period in which output of the optical data voltage of the photodetector circuit is stopped can be provided.

[0201]

5 [Embodiment 5]

In this embodiment, described is an input-output device that can output data and can input data when light enters the input-output device.

[0202]

An example of the input-output device in this embodiment is described with
10 reference to FIGS. 7A and 7B. FIGS. 7A and 7B are diagrams for describing the example of the input-output device in this embodiment.

[0203]

First, an example of the configuration of the input-output device in this embodiment is described with reference to FIG. 7A. FIG. 7A is a block diagram
15 illustrating the configuration example of the input-output device in this embodiment.

[0204]

The input-output device in FIG. 7A includes a scan signal output circuit (also referred to as SCNOUT) 201, an image signal output circuit (also referred to as IMGOUT) 202, a selection signal output circuit 203, a reset signal output circuit 204, a
20 plurality of display circuits (also referred to as DISP) 205k, a photodetector circuit 205p, and a reading circuit 206.

[0205]

The scan signal output circuit 201 has a function of outputting a scan signal SCN. The scan signal output circuit 201 selects the display circuit 205k to which an
25 image signal IMG is to be input, in accordance with the scan signal SCN. The scan signal output circuit 201 includes, for example, a shift register. A start signal, a clock signal, and a power supply voltage are input to the shift register and the shift register outputs a signal, whereby the scan signal output circuit 201 can output the scan signal SCN. As the shift register, a shift register applicable to the selection signal output
30 circuit or the reset signal output circuit in the above embodiment can be used, for example.

[0206]

The image signal output circuit 202 has a function of outputting the image signal IMG. The image signal output circuit 202 outputs the image signal IMG to the display circuit 205k selected by the scan signal output circuit 201. The image signal
5 output circuit 202 includes, for example, a shift register and an analog switch. A start signal, a clock signal, and a power supply voltage are input to the shift register, and the shift register outputs a signal to the analog switch. When the analog switch is turned on in accordance with the output signal of the shift register, the image signal output circuit 202 can output the image signal IMG. As the shift register, a shift register applicable to
10 the selection signal output circuit or the reset signal output circuit in the above embodiment can be used, for example.

[0207]

The selection signal output circuit 203 includes a shift register, and a start signal, a clock signal, and a power supply voltage are input to the shift register. When the shift
15 register outputs a signal, the selection signal output circuit 203 outputs the selection signal SEL. The selection signal SEL is for controlling whether the photodetector circuit 205p outputs a signal. For example, a plurality of signals output from the shift register may be output as the selection signals SEL. Alternatively, a plurality of signals may be output from the shift register to a logic circuit and output signals of the logic
20 circuit may be the selection signals SEL.

[0208]

The reset signal output circuit 204 includes a shift register, and a start signal, a clock signal, and a power supply voltage are input to the shift register. When the shift register outputs a signal, the reset signal output circuit 204 outputs the reset signal RST.
25 The reset signal output circuit 204 is not necessarily provided; however, when the reset signal output circuit 204 is provided, the photodetector circuit 205p can be brought into a reset state. The reset signal RST is for controlling whether the photodetector circuit 205p is reset. For example, a plurality of signals output from the shift register may be output as the reset signals RST. Alternatively, a plurality of signals may be output from
30 the shift register to a logic circuit and output signals of the logic circuit may be the reset signals RST.

[0209]

The scan signal SCN is input to the display circuit 205k and then the image signal IMG is input to the display circuit 205k in accordance with the input scan signal SCN. The display circuit 205k changes the display state in accordance with the input
5 image signal IMG.

[0210]

The display circuit includes, for example, a selecting transistor and a display element. The selecting transistor controls whether to output the image signal IMG to the display element by being turned on or off in accordance with the scan signal SCN.
10 The display element changes the display state in accordance with the input image signal IMG.

[0211]

As the display element of the display circuit, a liquid crystal element, a light-emitting element, or the like can be used. A liquid crystal element is an element
15 whose light transmittance is changed by voltage application, and a light-emitting element is an element whose luminance is controlled with a current or a voltage. As the light-emitting element, an electroluminescent element (also referred to as an EL element) or the like may be used.

[0212]

20 The photodetector circuit 205p generates a voltage corresponding to the illuminance of incident light when light enters the photodetector circuit 205p.

[0213]

Supplied with one of the reset signal RST, the photodetector circuit 205p is brought into a reset state in accordance with the supplied reset signal RST.

25 [0214]

Further, supplied with one of the selection signals SEL, the photodetector circuit 205p outputs an optical data voltage as a data signal in accordance with the supplied selection signal SEL.

[0215]

30 As the photodetector circuit 205p, for example, a photodetector circuit applicable to the input circuit of the above embodiment can be used.

[0216]

Note that a pixel portion 205 is a region from which data is output and to which data is externally input by detection of light. For example, the pixel portion 205 may be formed in such a manner that pixels each including one or more display circuits 205k and one or more photodetector circuits 205p are arranged in matrix. Alternatively, a display circuit portion including the plurality of display circuits 205k arranged in matrix and a photodetection portion including the plurality of photodetector circuits 205p arranged in matrix may be separately provided in the pixel portion.

[0217]

10 The reading circuit 206 has a function of reading an optical data voltage output from the selected photodetector circuit 205p as a data signal.

[0218]

For example, a selection circuit may be used for the reading circuit 206. Supplied with a reading selection signal, the selection circuit selects the photodetector circuit 205p from which an optical data signal is to be read, in accordance with the input reading selection signal. Note that the selection circuit may select a plurality of the photodetector circuits 205p, from which optical data voltages are read, at one time. The selection circuit may include, for example, a plurality of transistors so that the photodetector circuit 205p from which an optical data voltage is to be read can be selected when the plurality of transistors are turned on or off.

[0219]

Note that for example, a control circuit enables control of operations of the scan signal output circuit 201, the image signal output circuit 202, the selection signal output circuit 203, the reset signal output circuit 204, and the reading circuit 206.

25 [0220]

The control circuit has a function of outputting a control signal that is a pulse signal. The control signal is output to the scan signal output circuit 201, the image signal output circuit 202, the selection signal output circuit 203, and the reset signal output circuit 204, whereby the operations of the scan signal output circuit 201, the image signal output circuit 202, the selection signal output circuit 203, and the reset signal output circuit 204 can be controlled in accordance with a pulse of the control

signal. For example, output of a start signal, a clock signal, or a power supply voltage to the shift register of the selection signal output circuit 203 or the reset signal output circuit 204 can be started or stopped in accordance with the pulse of the control signal. The control circuit may be controlled using a CPU, for example. For example, the
5 interval between pulses of control signals generated by the control circuit may be set using a CPU. Further, the reading circuit 206 may be controlled in accordance with the pulse of the control signal.

[0221]

The scan signal output circuit 201, the image signal output circuit 202, the
10 selection signal output circuit 203, and the reset signal output circuit 204 may be controlled in accordance with not only the control circuit but an operation signal. For example, when an operation signal is input to the control circuit through an interface, the control circuit generates a control signal whose interval between pulses of control signals is set in accordance with the input operation signal, and the generated control signal is
15 output to the scan signal output circuit 201, the image signal output circuit 202, the selection signal output circuit 203, and the reset signal output circuit 204. Further, the reading circuit 206 may be controlled in accordance with a pulse of the operation signal.

[0222]

Next, an example of a method for driving the input-output device in FIG. 7A is
20 described as an example of a method for driving the input-output device in this embodiment.

[0223]

In the example of a method for driving the input-output device in FIG. 7A, a displaying operation and a reading operation are performed.

25 [0224]

In the example of a method for driving the input-output device in FIG. 7A, there are a period in which at least an operation of the selection signal output circuit is stopped to stop output of the selection signal to the photodetector circuit. The example of a method for driving the input-output device in FIG. 7A, for which the period is set, is
30 described with reference to FIG. 7B. FIG. 7B illustrates the example of a method for driving the input-output device in FIG. 7A. Here, for example, the number of the

selection signals SEL and the number of the reset signals RST are each A (A is a natural number larger than or equal to 3).

[0225]

First, in a period 211, the scan signal output circuit 201 outputs the scan signals
5 SCN, and the reset signal output circuit 204 outputs the reset signals RST. At a time T21, the scan signal output circuit 201 outputs a pulse of the first scan signal SCN_1 and then sequentially outputs pulses of the second to the A-th scan signal SCN_2 to SCN_A, and the reset signal output circuit 204 outputs a pulse of the first reset signal RST_1 and then sequentially outputs pulses of the second to the A-th reset signals RST_2 to RST_A.
10 In addition, in a period 211, the selection signal output circuit 203 outputs the selection signals SEL. At a time T22, the selection signal output circuit 203 outputs a pulse of the first selection signal SEL_1 and then sequentially outputs pulses of the second to the A-th selection signals SEL_2 to SEL_A. Note that the timing when the pulse of the first selection signal SEL_1 is output is not limited to the time T22 and it is acceptable as
15 long as the timing is after output of the pulse of the first reset signal RST_1. Note that the timing when the pulse of the first reset signal RST_1 is output may be different from the timing when the pulse of the first scan signal SCN_1 is output.

[0226]

Further, supplied with the pulse of the scan signal SCN, the display circuit 205k
20 is supplied with the image signal IMG.

[0227]

The display element of the display circuit 205k to which the image signal IMG has been input is brought into a display state depending on a voltage of the image signal IMG.

25 [0228]

The photodetector circuit 205p is brought into a reset state when the pulse of the reset signal RST is input thereto and then generates an optical data voltage. Supplied with a pulse of the selection signal SEL, the photodetector circuit 205p outputs the generated optical data voltage as a data signal.

30 [0229]

Then, the reading circuit 206 sequentially reads optical data voltages output

from the photodetector circuits 205p. When all the optical data voltages are read, the reading operation is completed. The read optical data voltages are used as data signals for executing predetermined processing. That is the operation in the period 211.

[0230]

5 Next, in a period 212, the scan signal output circuit 201 outputs the scan signals SCN, and output of the reset signals RST from the reset signal output circuit 204 and output of the selection signals SEL from the selection signal output circuit 203 are stopped. At that time, the pulses of the first to the A-th reset signals RST_1 to RST_A are not output, and the pulses of the first to the A-th selection signals SEL_1 to SEL_A
10 are not output. Note that a stop of a signal means, for example, a stop of a pulse of the signal or inputting a voltage which does not function as a signal to a wiring through which a signal is output. A pulse generated due to a noise or the like is not necessarily stopped.

[0231]

15 Supplied with the pulse of the scan signal SCN, the display circuit 205k is supplied with the image signal IMG.

[0232]

 The display element of the display circuit 205k to which the image signal IMG has been input is brought into a display state depending on a voltage of the image signal
20 IMG.

[0233]

 Note that at that time, output of the scan signals SCN from the scan signal output circuit 201 may be stopped.

[0234]

25 Further, an optical data voltage is not output from the photodetector circuit 205p to which the pulse of the selection signal SEL is not input. That is an operation in the period 212.

[0235]

 When output of the reset signals RST from the reset signal output circuit 204 is
30 resumed, as shown in a period 213, the reset signal output circuit 204 outputs the reset signals RST again. At a time T23, the reset signal output circuit 204 outputs the pulse

of the first reset signal RST_1 and then sequentially outputs the pulses of the second to the A-th reset signals RST_2 to RST_A. When output of the selection signals SEL from the selection signal output circuit 203 is resumed, as shown in the period 213, the selection signal output circuit 203 outputs the selection signals SEL again. At a time
5 T24, the selection signal output circuit 203 outputs the pulse of the first selection signal SEL_1 and then sequentially outputs the pulses of the second to the A-th selection signals SEL_2 to SEL_A. Note that the timing when the pulse of the first selection signal SEL_1 is output is not limited to the time T24 and it is acceptable as long as the timing is after output of the pulse of the first reset signal RST_1.

10 [0236]

Note that in the case where output of the scan signals SCN from the scan signal output circuit 201 is stopped, output of the scan signals SCN from the scan signal output circuit 201 can be resumed after that. That is the example of a method for driving the input-output device in FIG. 7A.

15 [0237]

The operations in the period 211, the period 212, and the period 213 may be performed a plurality of times.

[0238]

The timing when the period shifts from the period 211 to the period 212 may be
20 set by a pulse of the control signal generated in accordance with the operation signal. For example, the operation of the input-output device may be switched from the operation in the period 211 to the operation in the period 212 when the pulse of the control signal is input to the input-output device. After a certain period of time passes, the operation may be switched from the operation in the period 212 to the operation in
25 the period 213. At that time, switching from the operation in the period 212 to the operation in the period 213 may be performed when the pulse of the control signal is input to the input-output device.

[0239]

As described with reference to FIGS. 7A and 7B, in the input-output device of
30 this embodiment, the selection signal output circuit outputs the selection signals in a first period, and then output of the selection signals is stopped in a second period. Thus, the

operation of the photodetector circuit can be stopped in part of the periods, resulting in reduction in power consumption. For example, the reading operation is performed in the case where a user inputs data with the use of the pixel portion (for example, in the case where a keyboard is displayed in the pixel portion and data is input with the
5 keyboard), and the operation of the photodetector circuit is stopped in the case where a user does not input data (for example, in the case where the user sees the pixel portion). Consequently, power consumption can be reduced.

[0240]

Moreover, in the input-output device of this embodiment, not only output of the
10 selection signals but output of the reset signals can be stopped. Thus, power consumption can be further reduced as compared to the case where only output of the pulses of the selection signals is stopped.

[0241]

[Embodiment 6]

15 In this embodiment, further described is the display circuit in the input-output device of the above embodiment.

[0242]

An example of the circuit configuration of the display circuit in the input-output device of the above embodiment is described with reference to FIG. 8. FIG. 8 is a
20 circuit diagram for describing the circuit configuration of the display circuit.

[0243]

The display circuit in FIG. 8 includes a transistor 241, a liquid crystal element 242, and a capacitor 243.

[0244]

25 The transistor is a field-effect transistor having at least a source, a drain, and a gate unless otherwise specified.

[0245]

The scan signal SCN is input to the gate of the transistor 241. The image signal IMG is input to one of the source and the drain of the transistor 241.

30 [0246]

The off-state current of the transistor 241 is preferably low and for example, the

off-state current per micrometer in channel width is preferably 10 aA (1×10^{-17} A) or less, more preferably 1 aA (1×10^{-18} A) or less, still more preferably 10 zA (1×10^{-20} A) or less, further preferably 1 zA (1×10^{-21} A) or less. The use of a transistor with low off-state current as the transistor 241 can suppress variation in voltage applied to the liquid crystal element 242 due to leakage current between the source and the drain of the transistor 241. As the transistor with low off-state current, a transistor including an oxide semiconductor layer as a channel formation layer can be used, for example. The oxide semiconductor layer of the transistor, which has a function of the channel formation layer, is a semiconductor layer highly purified to be intrinsic (also referred to as I-type) or substantially intrinsic.

[0247]

The liquid crystal element 242 has a first terminal and a second terminal. The first terminal of the liquid crystal element 242 is electrically connected to the other of the source and the drain of the transistor 241. A constant voltage is selectively input to the second terminal of the liquid crystal element 242.

[0248]

The liquid crystal element 242 may include a pixel electrode which functions as part or the whole of the first terminal, a common electrode which functions as part or the whole of the second terminal, and a liquid crystal layer whose light transmittance varies depending on a voltage applied between the pixel electrode and the common electrode.

[0249]

Note that the pixel electrode may include a region transmitting visible light and a region reflecting visible light. The region transmitting visible light in the pixel electrode transmits light from a backlight, and the region reflecting visible light in the pixel electrode reflects light incident through the liquid crystal layer.

[0250]

Examples of a liquid crystal that can be used for the liquid crystal layer are a nematic liquid crystal, a cholesteric liquid crystal, a smectic liquid crystal, a discotic liquid crystal, a thermotropic liquid crystal, a lyotropic liquid crystal, a low-molecular liquid crystal, a polymer dispersed liquid crystal (PDLC), a ferroelectric liquid crystal, an anti-ferroelectric liquid crystal, a main-chain liquid crystal, a side-chain

high-molecular liquid crystal, a banana-shaped liquid crystal, and the like.

[0251]

The resistivity of a liquid crystal material used for the liquid crystal layer is $1 \times 10^{12} \Omega \cdot \text{cm}$ or more, preferably $1 \times 10^{13} \Omega \cdot \text{cm}$ or more, more preferably $1 \times 10^{14} \Omega \cdot \text{cm}$ or more. Note that the resistivity in this specification is measured at 20 °C. In the case where a liquid crystal element is formed using the liquid crystal material, the resistivity of the liquid crystal element may be $1 \times 10^{11} \Omega \cdot \text{cm}$ or more, furthermore $1 \times 10^{12} \Omega \cdot \text{cm}$ or more in some cases because of an impurity mixed into a liquid crystal layer from an alignment film, a sealant, or the like.

10 [0252]

As the resistivity of the liquid crystal material is higher, the leakage current of the liquid crystal layer can be reduced and the decrease over time of the voltage applied to the liquid crystal element in the display period can be suppressed. As a result, the display period of the display circuit, in which one writing of the image data is reflected, can be extended, so that the frequency of writing the image data into the display circuit can be decreased, which leads to reduction in power consumption of the input-output device.

[0253]

The following modes are examples of a method for driving the liquid crystal element: a TN (twisted nematic) mode, an STN (super twisted nematic) mode, an OCB (optically compensated birefringence) mode, an ECB (electrically controlled birefringence) mode, an FLC (ferroelectric liquid crystal) mode, an AFLC (anti-ferroelectric liquid crystal) mode, a PDLC (polymer dispersed liquid crystal) mode, a PNLC (polymer network liquid crystal) mode, a guest-host mode, and the like.

25 [0254]

The capacitor 243 has a first terminal and a second terminal. The first terminal of the capacitor 243 is electrically connected to the other of the source and the drain of the transistor 241. A constant voltage is selectively input to the second terminal of the capacitor 243.

30 [0255]

The capacitor 243 has a function of a storage capacitor, and can include a first

electrode which functions as part of or the whole of the first terminal, a second electrode which functions as part of or the whole of the second terminal, and a dielectric layer. The capacitance of the capacitor 243 may be set in consideration of the off-state current of the transistor 241. In this embodiment, it is only necessary to provide a storage
5 capacitor having capacitance which is $1/3$ or less, preferably $1/5$ or less of the capacitance of the liquid crystal element in each display circuit (also referred to as liquid crystal capacitance). The capacitor 243 is not necessarily provided. When the capacitor 243 is not provided in the display circuit, the aperture ratio of a pixel portion can be increased.

10 [0256]

Next, described is an example of a method for driving the display circuit in FIG. 8.

[0257]

First, the transistor 241 is turned on in accordance with a pulse of the scan
15 signal SCN, a voltage of the first terminal of the liquid crystal element 242 is set to a value equivalent to a voltage of the image signal IMG, and a voltage depending on the image signal IMG is applied between the first terminal and the second terminal of the liquid crystal element 242. The liquid crystal element 242 has a light transmittance set in accordance with a voltage applied between the first terminal and the second terminal
20 and is brought into a predetermined display state in accordance with the voltage. At that time, the display state of the display circuit is held for a certain period of time. The above operations are also performed on the other display circuits, whereby display states of all the display circuits are set. Accordingly, a voltage of the image signal IMG is written to each of the display circuits as a data signal. Thus, an image based on data of
25 the image signal IMG is displayed in the pixel portion. That is the example of the method for driving the display circuit in FIG. 8.

[0258]

As described with reference to FIG. 8, the display circuit of the input-output circuit in the above embodiment may include the transistor and the liquid crystal element.
30 Since the liquid crystal element can transmit light depending on an applied voltage, when the display circuit and a photodetector circuit are provided in the pixel portion, a

displaying operation and a reading operation can be performed.

[0259]

[Embodiment 7]

In this embodiment, described is a transistor including an oxide semiconductor layer, which is applicable to the input circuit and the input-output device described in the above embodiment.

[0260]

The transistor including an oxide semiconductor layer, which is applicable to the input circuit and the input-output device described in the above embodiment, is a transistor including a semiconductor layer highly purified to be intrinsic (also referred to as I-type) or substantially intrinsic.

[0261]

As an oxide semiconductor used for the oxide semiconductor layer, a four-component metal oxide, a three-component metal oxide, or a two-component metal oxide can be used, for example. As the four-component metal oxide, an In-Sn-Ga-Zn-O-based metal oxide or the like can be used. As the three-component metal oxide, an In-Ga-Zn-O-based metal oxide, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, a Sn-Ga-Zn-O-based metal oxide, an Al-Ga-Zn-O-based metal oxide, a Sn-Al-Zn-O-based metal oxide, or the like can be used. As the two-component metal oxide, an In-Zn-O-based metal oxide, a Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, a Zn-Mg-O-based metal oxide, a Sn-Mg-O-based metal oxide, an In-Mg-O-based metal oxide, an In-Sn-O-based metal oxide, or the like can be used. Alternatively, as the oxide semiconductor, an In-O-based metal oxide, a Sn-O-based metal oxide, a Zn-O-based metal oxide, or the like may be used. The metal oxide that can be used as the oxide semiconductor may contain SiO_2 .

[0262]

As the oxide semiconductor, a material represented by $\text{InMO}_3(\text{ZnO})_m$ (m is larger than 0) can be used. Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, Ga, Ga and Al, Ga and Mn, Ga and Co, and the like can be given as M .

[0263]

The band gap of the oxide semiconductor layer is 2 eV or more, preferably 2.5 eV or more, more preferably 3 eV or more. Thus, the number of carriers generated by thermal excitation is negligible. Further, the amount of impurity such as hydrogen which may serve as a donor is reduced to a certain amount or less so that the carrier concentration is less than $1 \times 10^{14}/\text{cm}^3$, preferably $1 \times 10^{12}/\text{cm}^3$ or less. That is, the carrier concentration of the oxide semiconductor layer is reduced to zero or substantially zero.

[0264]

In the oxide semiconductor layer, the avalanche breakdown is not likely to occur and the withstand voltage is high. For example, the band gap of silicon is as narrow as 1.12 eV; therefore, electrons are likely to be generated owing to the avalanche breakdown, and electrons that are accelerated to be so rapid as to go over a barrier to the gate insulating layer are increased in number. In contrast, since the oxide semiconductor used for the aforementioned oxide semiconductor layer has a band gap of 2 eV or more which is wider than that of silicon, the avalanche breakdown is not likely to occur and resistance to hot-carrier degradation is higher than that of silicon, and the withstand voltage is thus high.

[0265]

The hot-carrier degradation means, for example, deterioration of transistor characteristics caused by fixed charge which is generated when highly-accelerated electrons are injected into a gate insulating layer from a channel in the vicinity of a drain; or deterioration of transistor characteristics caused by a trap level which is formed at the interface of a gate insulating layer by highly-accelerated electrons. The deterioration of transistor characteristics is, for example, gate leakage or the variation in threshold voltage. The factors of the hot-carrier degradation are channel-hot-electron injection (also referred to as CHE injection) and drain-avalanche-hot-carrier injection (also referred to as DAHC injection).

[0266]

Note that the band gap of silicon carbide, which is one of materials having high withstand voltage, is substantially equal to that of an oxide semiconductor used for the oxide semiconductor layer, but electrons are less likely to be accelerated in an oxide

semiconductor because the mobility of the oxide semiconductor is lower than that of silicon carbide by approximately two orders of magnitude. Further, since a barrier between an oxide semiconductor and a gate insulating layer is larger than a barrier between silicon carbide, gallium nitride, or silicon and a gate insulating layer, the number of electrons injected into the gate insulating layer is extremely small, whereby hot-carrier degradation is less likely to be caused and withstand voltage is high as compared to the case of silicon carbide, gallium nitride, or silicon. The oxide semiconductor has a high withstand voltage even in an amorphous state.

[0267]

10 In a transistor including the oxide semiconductor layer, the off-state current per micrometer in channel width can be 10 aA (1×10^{-17} A) or less, preferably 1 aA (1×10^{-18} A) or less, more preferably 10 zA (1×10^{-20} A) or less, still more preferably 1 zA (1×10^{-21} A) or less.

[0268]

15 In the transistor including the oxide semiconductor layer, degradation due to light (e.g., the variation in threshold voltage) is less likely to be caused.

[0269]

Structural examples of the transistor including an oxide semiconductor layer, which is applicable to the input circuit and the input-output device described in the above embodiment, are described with reference to FIGS. 9A to 9D. FIGS. 9A to 9D are cross-sectional schematic views illustrating the structural examples of the transistor.

[0270]

The transistor illustrated in FIG. 9A is one of bottom-gate transistors and is also an inverted staggered transistor.

25 [0271]

The transistor illustrated in FIG. 9A includes a conductive layer 401a serving as a gate electrode, an insulating layer 402a serving as a gate insulating layer, an oxide semiconductor layer 403a serving as a channel formation layer, and a conductive layer 405a and a conductive layer 406a serving as source and drain electrodes.

30 [0272]

The conductive layer 401a is provided over a substrate 400a, the insulating layer

402a is provided over the conductive layer 401a, the oxide semiconductor layer 403a is provided over the conductive layer 401a with the insulating layer 402a therebetween, and the conductive layer 405a and the conductive layer 406a are each provided over part of the oxide semiconductor layer 403a.

5 [0273]

In the transistor illustrated in FIG. 9A, an oxide insulating layer 407a is provided in contact with part of a top surface of the oxide semiconductor layer 403a (part of the top surface over which the conductive layer 405a or the conductive layer 406a is not provided). In addition, a protective insulating layer 409a is provided over the oxide
10 insulating layer 407a.

[0274]

The transistor illustrated in FIG. 9B is one of bottom-gate transistors called a channel-protective (channel-stop) transistor and is also an inverted staggered transistor.

[0275]

15 The transistor illustrated in FIG. 9B includes a conductive layer 401b serving as a gate electrode, an insulating layer 402b serving as a gate insulating layer, an oxide semiconductor layer 403b serving as a channel formation layer, an insulating layer 427 serving as a channel protective layer, and a conductive layer 405b and a conductive layer 406b serving as source and drain electrodes.

20 [0276]

The conductive layer 401b is provided over a substrate 400b, the insulating layer 402b is provided over the conductive layer 401b, the oxide semiconductor layer 403b is provided over the conductive layer 401b with the insulating layer 402b therebetween, the insulating layer 427 is provided over the conductive layer 401b with
25 the insulating layer 402b and the oxide semiconductor layer 403b therebetween, and the conductive layer 405b and the conductive layer 406b are provided over part of the oxide semiconductor layer 403b with the insulating layer 427 therebetween. The conductive layer 401b may overlap with the whole oxide semiconductor layer 403b. When the conductive layer 401b overlaps with the whole oxide semiconductor layer 403b,
30 incidence of light on the oxide semiconductor layer 403b can be suppressed. It is not always necessary to employ that structure, and the conductive layer 401b may overlap

with part of the oxide semiconductor layer 403b.

[0277]

Further, a protective insulating layer 409b is in contact with an upper portion of the transistor in FIG. 9B.

5 [0278]

The transistor illustrated in FIG. 9C is one of bottom-gate transistors.

[0279]

The transistor illustrated in FIG. 9C includes a conductive layer 401c serving as a gate electrode, an insulating layer 402c serving as a gate insulating layer, an oxide semiconductor layer 403c serving as a channel formation layer, and a conductive layer 405c and a conductive layer 406c serving as source and drain electrodes.

[0280]

The conductive layer 401c is provided over a substrate 400c, the insulating layer 402c is provided over the conductive layer 401c, the conductive layer 405c and the conductive layer 406c are provided over part of the insulating layer 402c, and the oxide semiconductor layer 403c is provided over the conductive layer 401c with the insulating layer 402c, the conductive layer 405c, and the conductive layer 406c therebetween. The conductive layer 401c may overlap with the whole oxide semiconductor layer 403c. When the conductive layer 401c overlaps with the whole oxide semiconductor layer 403c, incidence of light on the oxide semiconductor layer 403c can be suppressed. It is not always necessary to employ that structure, and the conductive layer 401c may overlap with part of the oxide semiconductor layer 403c.

[0281]

Further, in the transistor illustrated in FIG. 9C, an oxide insulating layer 407c is in contact with a top surface and a side surface of the oxide semiconductor layer 403c. In addition, a protective insulating layer 409c is provided over the oxide insulating layer 407c.

[0282]

The transistor illustrated in FIG. 9D is one of top-gate transistors.

30 [0283]

The transistor illustrated in FIG. 9D includes a conductive layer 401d serving as

a gate electrode, an insulating layer 402d serving as a gate insulating layer, an oxide semiconductor layer 403d serving as a channel formation layer, and a conductive layer 405d and a conductive layer 406d serving as source and drain electrodes.

[0284]

5 The oxide semiconductor layer 403d is provided over a substrate 400d with an insulating layer 447 therebetween, the conductive layer 405d and the conductive layer 406d are each provided over part of the oxide semiconductor layer 403d, the insulating layer 402d is provided over the oxide semiconductor layer 403d, the conductive layer 405d, and the conductive layer 406d, and the conductive layer 401d is provided over the
10 oxide semiconductor layer 403d with the insulating layer 402d therebetween.

[0285]

Moreover, components of the transistors illustrated in FIGS. 9A to 9D are described below.

[0286]

15 As the substrates 400a to 400d, a glass substrate of barium borosilicate glass, aluminoborosilicate glass, or the like can be used, for example.

[0287]

Alternatively, a substrate formed of an insulator, such as a ceramic substrate, a quartz substrate, or a sapphire substrate, may be used as the substrates 400a to 400d.

20 Still alternatively, a crystallized glass substrate, a plastic substrate, or a semiconductor substrate of silicon or the like may be used as the substrates 400a to 400d.

[0288]

 The insulating layer 447 serves as a base layer preventing diffusion of an impurity element from the substrate 400d. As the insulating layer 447, a silicon nitride
25 layer, a silicon oxide layer, a silicon nitride oxide layer, a silicon oxynitride layer, an aluminum oxide layer, or an aluminum oxynitride layer can be used, for example. The insulating layer 447 may be formed by stacking layers of materials which can be applied to the insulating layer 447. Alternatively, the insulating layer 447 can be a stack of a layer including a light-blocking material and a layer including any of the above materials
30 applicable to the insulating layer 447. When the insulating layer 447 is formed using a layer including a light-blocking material, light can be prevented from entering the oxide

semiconductor layer 403d.

[0289]

Note that in the transistors illustrated in FIGS. 9A to 9C, an insulating layer may be provided between the substrate and the conductive layer serving as a gate electrode,
5 as in the transistor illustrated in FIG. 9D.

[0290]

As the conductive layers 401a to 401d, a layer of a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium or an alloy material containing any of these materials as a main component
10 can be used, for example. The conductive layers 401a to 401d may be formed by stacking layers of materials which can be applied to the conductive layers 401a to 401d.

[0291]

As the insulating layers 402a to 402d, a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, an aluminum oxide layer, an
15 aluminum nitride layer, an aluminum oxynitride layer, an aluminum nitride oxide layer, or a hafnium oxide layer can be used, for example. The insulating layers 402a to 402d may be formed by stacking layers of materials which can be applied to the insulating layers 402a to 402d. The layers of materials which can be applied to the insulating layers 402a to 402d can be formed by a plasma CVD method, a sputtering method, or the
20 like. For example, the insulating layers 402a to 402d can be formed in such a manner that a silicon nitride layer is formed by a plasma CVD method and a silicon oxide layer is formed over the silicon nitride layer by a plasma CVD method.

[0292]

As an oxide semiconductor which can be used in the oxide semiconductor
25 layers 403a to 403d, a four-component metal oxide, a three-component metal oxide, and a two-component metal oxide can be given, for example. As the four-component metal oxide, an In-Sn-Ga-Zn-O-based metal oxide and the like can be given. As the three-component metal oxide, an In-Ga-Zn-O-based metal oxide, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, a Sn-Ga-Zn-O-based metal oxide, an
30 Al-Ga-Zn-O-based metal oxide, a Sn-Al-Zn-O-based metal oxide, and the like can be given. As the two-component metal oxide, an In-Zn-O-based metal oxide, a

Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, a Zn-Mg-O-based metal oxide, a Sn-Mg-O-based metal oxide, an In-Mg-O-based metal oxide, an In-Sn-O-based metal oxide, and the like can be given. Alternatively, as the oxide semiconductor, an In-O-based metal oxide, a Sn-O-based metal oxide, a Zn-O-based metal oxide, or the like may be used. The metal oxide that can be used as the oxide semiconductor may contain SiO₂. Here, for example, the In-Ga-Zn-O-based metal oxide means an oxide containing at least In, Ga, and Zn, and the composition ratio of the elements is not particularly limited. The In-Ga-Zn-O-based metal oxide may contain an element other than the In, Ga, and Zn.

10 [0293]

Further, as an oxide semiconductor which can be used in the oxide semiconductor layers 403a to 403d, a metal oxide represented by InMO₃(ZnO)_m (m is larger than 0) can be given. Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, Ga, Ga and Al, Ga and Mn, Ga and Co, and the like can be given as M.

[0294]

As the conductive layers 405a to 405d and the conductive layers 406a to 406d, a layer of a metal material such as aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten or an alloy material containing any of the metal materials as a main component may be used, for example. The conductive layers 405a to 405d and the conductive layers 406a to 406d may be formed by stacking layers of materials which can be applied to the conductive layers 405a to 405d and the conductive layers 406a to 406d.

[0295]

25 For example, the conductive layers 405a to 405d and the conductive layers 406a to 406d may be formed by stacking a metal layer of aluminum or copper and a high-melting-point metal layer of titanium, molybdenum, tungsten, or the like. The conductive layers 405a to 405d and the conductive layers 406a to 406d may have a structure in which a metal layer of aluminum or copper is provided between a plurality of high-melting-point metal layers. Further, when the conductive layers 405a to 405d and the conductive layers 406a to 406d are formed using an aluminum layer to which an

element that prevents generation of hillocks or whiskers (e.g., Si, Nd, or Sc) is added, heat resistance can be increased.

[0296]

Alternatively, the conductive layers 405a to 405d and the conductive layers
5 406a to 406d may be formed using a layer containing a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an alloy of indium oxide and tin oxide ($\text{In}_2\text{O}_3\text{-SnO}_2$, abbreviated as ITO), an alloy of indium oxide and zinc oxide ($\text{In}_2\text{O}_3\text{-ZnO}$), or such a metal oxide material containing silicon oxide may be used, for example.

10 [0297]

Furthermore, another wiring may be formed using the material used to form the conductive layers 405a to 405d and the conductive layers 406a to 406d.

[0298]

As the insulating layer 427, a layer which can be applied to the base layer 447
15 can be used, for example. The insulating layer 427 may be formed by stacking layers of materials which can be applied to the insulating layer 427.

[0299]

As the oxide insulating layer 407a and the oxide insulating layer 407c, an oxide insulating layer may be used and, for example, a silicon oxide layer or the like may be
20 used. The oxide insulating layer 407a and the oxide insulating layer 407c may be formed by stacking layers of materials which can be applied to the oxide insulating layer 407a and the oxide insulating layer 407c.

[0300]

As the protective insulating layers 409a to 409c, an inorganic insulating layer
25 may be used and, for example, a silicon nitride layer, an aluminum nitride layer, a silicon nitride oxide layer, an aluminum nitride oxide layer, or the like may be used. The protective insulating layers 409a to 409c may be formed by stacking layers of materials which can be applied to the protective insulating layers 409a to 409c.

[0301]

30 In order to reduce surface unevenness due to the transistor of this embodiment, a planarization insulating layer may be provided over the transistor (in the case where

the transistor includes an oxide insulating layer or a protective insulating layer, over the transistor with the oxide insulating layer or the protective insulating layer therebetween). As the planarization insulating layer, a layer of an organic material such as polyimide, acrylic, or benzocyclobutene may be used. Alternatively, a layer of a low-dielectric
5 constant material (also referred to as a low-k material) may be used as the planarization insulating layer. The planarization insulating layer may be formed by stacking layers of materials which can be applied to the planarization insulating layer.

[0302]

An example of the fabrication method of the transistor in FIG. 9A is described
10 with reference to FIGS. 10A to 10C and FIGS. 11A and 11B as an example of the fabrication method of the transistor including an oxide semiconductor layer, which is applicable to the input circuit or the input-output circuit in the above embodiment. FIGS. 10A to 10C and FIGS. 11A and 11B are cross-sectional schematic views illustrating the example of the fabrication method of the transistor in FIG. 9A.

15 [0303]

First, the substrate 400a is prepared, and a first conductive film is formed over the substrate 400a.

[0304]

A glass substrate is used as the substrate 400a, for example.

20 [0305]

As the first conductive film, a film of a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material which contains any of the metal materials as a main component may be used. The first conductive film may be formed by stacking layers of materials which
25 can be applied to the first conductive film.

[0306]

Next, a first photolithography process is carried out: a first resist mask is formed over the first conductive film, the first conductive film is selectively etched with the use of the first resist mask to form the conductive layer 401a, and the first resist mask is
30 removed.

[0307]

In this embodiment, the resist mask may be formed by an ink-jet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced.

[0308]

5 In order to reduce the number of photomasks and steps in the photolithography process, the etching may be performed using a resist mask formed with the use of a multi-tone mask. A multi-tone mask is a mask through which light is transmitted to have a plurality of intensities. A resist mask formed with the use of a multi-tone mask has a plurality of thicknesses and further can be changed in shape by etching; therefore,
10 the resist mask can be used in a plurality of etching steps for processing into different patterns. Therefore, a resist mask corresponding to at least two or more kinds of different patterns can be formed with one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography processes can be also reduced, whereby a manufacturing process can be simplified.

15 [0309]

Next, the insulating layer 402a is formed over the conductive layer 401a.

[0310]

For example, the insulating layer 402a may be formed by a high-density plasma CVD method. For example, a high-density plasma CVD method using microwaves
20 (e.g., microwaves with a frequency of 2.45 GHz) is preferable because a high-quality insulating layer which is dense and has a high withstand voltage can be formed. When the oxide semiconductor layer is in contact with the high-quality insulating layer formed by a high-density plasma CVD method, the interface states can be reduced and interface characteristics can be favorable.

25 [0311]

Any other method such as a sputtering method or a plasma CVD method may be employed to form the insulating layer 402a. Further, heat treatment may be performed after formation of the insulating layer 402a. The heat treatment can improve film quality of the insulating layer 402a and the interface characteristics between the
30 insulating layer 402a and the oxide semiconductor.

[0312]

Next, an oxide semiconductor film 530 having a thickness of 2 nm to 200 nm inclusive, preferably 5 nm to 30 nm inclusive is formed over the insulating layer 402a. For example, the oxide semiconductor film 530 may be formed by a sputtering method.

[0313]

5 Note that before the oxide semiconductor film 530 is formed, powder substances (also referred to as particles or dust) attached on a surface of the insulating layer 402a are preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. The reverse sputtering refers to a method in which, without application of a voltage to a target side, an RF power source is used for
10 application of a voltage to a substrate side in an argon atmosphere to generate plasma in the vicinity of the substrate to modify a surface. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used.

[0314]

15 For example, the oxide semiconductor film 530 may be formed using an oxide semiconductor material which can be applied to the oxide semiconductor layer 403a. In this embodiment, the oxide semiconductor film 530 is formed by a sputtering method with the use of an In-Ga-Zn-O-based oxide target, for example. FIG. 10A is a cross-sectional schematic view of this stage. The oxide semiconductor film 530 may be
20 formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas and oxygen.

[0315]

As a target for forming the oxide semiconductor film 530 by a sputtering method, for example, an oxide target having the following composition ratio can be
25 used: the composition ratio of $\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3:\text{ZnO}$ is 1:1:1 [molar ratio]. Without limitation to the above target, for example, an oxide target having the following composition ratio may be used: the composition ratio of $\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3:\text{ZnO}$ is 1:1:2 [molar ratio]. The proportion of the volume of a portion except for an area occupied by a space and the like with respect to the total volume of the oxide target formed (also
30 referred to as the fill rate) is 90% to 100% inclusive, preferably, 95% to 99.9% inclusive. With the use of a metal oxide target with high fill rate, a dense oxide semiconductor film

is formed.

[0316]

It is preferable that a high-purity gas in which impurities such as hydrogen, water, a hydroxyl group, and hydride are removed be used for example, as the sputtering
5 gas for the formation of the oxide semiconductor film 530.

[0317]

Before formation of the oxide semiconductor film 530, it is preferable that the substrate 400a over which the conductive layer 401a is formed or the substrate 400a over which the conductive layer 401a and the insulating layer 402a are formed be heated in a
10 preheating chamber of the sputtering apparatus so that impurities such as hydrogen and moisture adsorbed onto the substrate 400a are eliminated. The preheating in the preheating chamber can prevent hydrogen, a hydroxyl group, and moisture from entering the insulating layer 402a and the oxide semiconductor film 530. Note that a cryopump is preferable as an evacuation unit provided in the preheating chamber. The preheat
15 treatment may be omitted. The preheat treatment in the preheating chamber may be similarly performed on the substrate 400a over which layers up to and including the conductive layer 405a and the conductive layer 406a are formed before formation of the oxide insulating layer 407a.

[0318]

20 When the oxide semiconductor film 530 is formed by a sputtering method, the substrate 400a is placed in a deposition chamber kept under reduced pressure, and the temperature of the substrate 400a is set to 100 °C to 600 °C inclusive, preferably 200 °C to 400 °C inclusive. By heating the substrate 400a, the concentration of an impurity contained in the oxide semiconductor film 530 can be reduced. Moreover, damage of
25 the oxide semiconductor film 530 due to sputtering is reduced. Then, a sputtering gas from which hydrogen and moisture are removed is introduced into the deposition chamber from which remaining moisture is being removed, and the oxide semiconductor film 530 is formed over the insulating layer 402a with the use of the target.

[0319]

30 Note that in this embodiment, for example, an entrapment vacuum pump may be used as a means for removing moisture remaining in the deposition chamber in which

sputtering is performed. As the entrapment vacuum pump, a cryopump, an ion pump, or a titanium sublimation pump is preferably used, for example. When a cryopump is used as an example, a compound including either or both a hydrogen atom or/and a carbon atom, or the like can be eliminated, and thus the concentration of an impurity included in a film formed in the deposition chamber can be reduced. Further, in this embodiment, a turbo pump provided with a cold trap may be used as a means for removing moisture remaining in the deposition chamber in which sputtering is performed.

[0320]

10 An example of the deposition condition is as follows: the distance between the substrate and the target is 100 mm, the pressure is 0.6 Pa, the direct-current (DC) power is 0.5 kW, and the atmosphere is an oxygen atmosphere (the flow rate of the oxygen is 100%). Note that when a pulse direct current power source is used, powder substances generated in deposition can be reduced and the film thickness can be uniform.

15 [0321]

Next, a second photolithography process is carried out: a second resist mask is formed over the oxide semiconductor film 530, the oxide semiconductor film 530 is selectively etched with the use of the second resist mask to process the oxide semiconductor film 530 into an island-shaped oxide semiconductor layer, and the second resist mask is removed.

[0322]

In the case of forming a contact hole in the insulating layer 402a, the contact hole may be formed at the time of processing the oxide semiconductor film 530 into the island-shaped oxide semiconductor layer.

25 [0323]

For example, dry etching, wet etching, or both dry etching and wet etching may be employed for etching the oxide semiconductor film 530. As an etchant used for wet etching, for example, a mixed solution of phosphoric acid, acetic acid, and nitric acid can be used. In addition, ITO07N (produced by Kanto Chemical Co., Inc.) may be used.

30 [0324]

Next, heat treatment is performed on the oxide semiconductor layer. The

oxide semiconductor layer can be dehydrated or dehydrogenated through the heat treatment. The temperature of the heat treatment is 400 °C to 750 °C inclusive or higher than or equal to 400 °C and lower than the strain point of the substrate. Here, the substrate is put in an electric furnace which is a kind of heat treatment apparatus and
5 heat treatment is performed on the oxide semiconductor layer at 450 °C for one hour in a nitrogen atmosphere, and then, the oxide semiconductor layer is not exposed to the air so that entry of water and hydrogen into the oxide semiconductor layer is prevented; thus, an oxide semiconductor layer 403a is obtained (see FIG. 10B).

[0325]

10 Note that a heat treatment apparatus is not limited to an electric furnace, and may include a device for heating an object to be processed by heat conduction or heat radiation from a heating element such as a resistance heating element. For example, a rapid thermal anneal (RTA) apparatus such as a gas rapid thermal anneal (GRTA) apparatus or a lamp rapid thermal anneal (LRTA) apparatus may be used. An LRTA
15 apparatus is an apparatus for heating an object to be processed by radiation of light (electromagnetic waves) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high temperature gas. As the high temperature gas, an inert gas which does not react
20 with an object to be processed in heat treatment, such as nitrogen or a rare gas like argon, is used.

[0326]

For example, as the heat treatment, GRTA in which the substrate is moved into an inert gas heated to a high temperature as high as 650 °C to 700 °C, heated for several
25 minutes, and moved out of the heated inert gas may be performed.

[0327]

Note that in the heat treatment in the heat treatment apparatus, it is preferable that water, hydrogen, and the like be not contained in the atmosphere of nitrogen or a rare gas such as helium, neon, or argon. It is preferable that the purity of nitrogen or
30 the rare gas such as helium, neon, or argon which is introduced into the heat treatment apparatus be set to 6N (99.9999%) or higher, preferably 7N (99.99999%) or higher.

That is, it is preferable to set the impurity concentration to 1 ppm or lower, preferably 0.1 ppm or lower.

[0328]

Further, after the oxide semiconductor layer is heated through the heat treatment
5 in the heat treatment apparatus, a high-purity oxygen gas, a high-purity N₂O gas, or
ultra-dry air (having a dew point -40 °C or lower, preferably -60 °C or lower) may be
introduced in the furnace where the heat treatment has been performed. It is preferable
that water, hydrogen, and the like be not contained in an oxygen gas or an N₂O gas.
The purity of the oxygen gas or the N₂O gas which is introduced into the heat treatment
10 apparatus is preferably 6N or higher, more preferably 7N or higher. That is, it is
preferable to set the concentration of impurities in the oxygen gas or the N₂O gas to 1
ppm or lower, more preferably 0.1 ppm or lower. By the action of the oxygen gas or
the N₂O gas, oxygen which has been reduced at the same time as the step of removing
impurities by dehydration or dehydrogenation is supplied, so that the oxide
15 semiconductor layer 403a can be highly purified.

[0329]

The heat treatment in the heat treatment apparatus may be performed on the
oxide semiconductor film 530 which has not yet been processed into the island-shaped
oxide semiconductor layer. In that case, the substrate 400a is taken out of the heat
20 treatment apparatus after the heat treatment in the heat treatment apparatus, and then the
oxide semiconductor film 530 is processing into the island-shaped oxide semiconductor
layer.

[0330]

Note that the heat treatment in the heat treatment apparatus may be performed at
25 any of the following timings instead of the above timing as long as it is after formation
of the oxide semiconductor layer: after the conductive layer 405a and the conductive
layer 406a are formed over the oxide semiconductor layer 403a; and after the oxide
insulating layer 407a is formed over the conductive layer 405a and the conductive layer
406a.

30 [0331]

In the case of forming a contact hole in the insulating layer 402a, the contact

hole may be formed before the heat treatment in the heat treatment apparatus is performed on the oxide semiconductor film 530.

[0332]

Further, the oxide semiconductor layer may be formed using an oxide semiconductor film formed to have a crystal region (single crystal region) with a large thickness, namely, a crystal region whose c-axes are aligned perpendicularly to a surface of the film, regardless of a material of a base component used, such as oxide, nitride, or metal, by performing deposition twice and performing heat treatment twice. For example, a first oxide semiconductor film with a thickness of 3 nm to 15 nm inclusive is formed, and heat treatment is performed in nitrogen, oxygen, a rare gas, or a dry air atmosphere at a temperature of 450 °C to 850 °C inclusive, preferably 550 °C to 750 °C inclusive, so that a first oxide semiconductor film having a crystal region (including a plate-like crystal) in a region including a surface is formed. Then, a second oxide semiconductor film which has a larger thickness than the first oxide semiconductor film is formed, and heat treatment is performed at a temperature of 450 °C to 850 °C inclusive, preferably 600 °C to 700 °C inclusive, so that crystal growth proceeds upward from the first oxide semiconductor film to the second oxide semiconductor film with the use of the first oxide semiconductor film as a seed of the crystal growth and thus the whole second oxide semiconductor film is crystallized. In such a manner, the oxide semiconductor layer 403a may be formed using the oxide semiconductor film having a crystal region with a large thickness.

[0333]

Next, a second conductive film is formed over the insulating layer 402a and the oxide semiconductor layer 403a.

[0334]

As the second conductive film, a film of a metal material such as aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten, or an alloy material which contains any of the metal materials as a main component may be used, for example. The second conductive film may be formed by stacking films of materials which can be applied to the second conductive film.

[0335]

Next, a third photolithography process is carried out: a third resist mask is formed over the second conductive film, the second conductive film is selectively etched with the use of the third resist mask to form the conductive layer 405a and the conductive layer 406a, and the third resist mask is removed (see FIG. 10C).

5 [0336]

Furthermore, another wiring may be formed using the second conductive film at the time of forming the conductive layer 405a and the conductive layer 406a.

[0337]

When light exposure is performed in the formation of the third resist mask,
10 ultraviolet light, a KrF laser beam, or an ArF laser beam is preferably used. The channel length L of a transistor that is completed later is determined by a distance between bottom edges of the conductive layer 405a and the conductive layer 406a, which are adjacent to each other over the oxide semiconductor layer 403a. In the formation of the third resist mask, in the case where light exposure is performed for a
15 channel length L of less than 25 nm, the light exposure may be performed using extreme ultraviolet light having an extremely short wavelength of several nanometers to several tens of nanometers. Light exposure with extreme ultraviolet light leads to a high resolution and a large depth of focus. Thus, the channel length L of the transistor that is completed later can be 10 nm to 1000 nm inclusive and the use of such a transistor
20 formed through the light exposure enables higher speed operation of a circuit. Moreover, the off-state current of the transistor is significantly low; thus, power consumption can be reduced.

[0338]

In the case of etching the second conductive film, etching conditions are
25 preferably optimized in order to prevent the oxide semiconductor layer 403a from being divided by the etching. However, it is difficult to set conditions under which only the second conductive film can be etched and the oxide semiconductor layer 403a is not etched. In some cases, only part of the oxide semiconductor layer 403a is etched to be the oxide semiconductor layer 403a having a groove portion (a recessed portion) when
30 the second conductive film is etched.

[0339]

In this embodiment, since a titanium film is used as the second conductive film and an In-Ga-Zn-O-based oxide semiconductor is used as the oxide semiconductor layer 403a, an ammonium hydroxide-hydrogen peroxide mixture (a mixture of ammonia, water, and a hydrogen peroxide solution) is used as an etchant.

5 [0340]

Next, the oxide insulating layer 407a is formed over the oxide semiconductor layer 403a, the conductive layer 405a, and the conductive layer 406a. At that time, the oxide insulating layer 407a is in contact with part of the top surface of the oxide semiconductor layer 403a.

10 [0341]

The oxide insulating layer 407a may be formed to a thickness of at least 1 nm using a method by which impurities such as water and hydrogen do not enter the oxide insulating layer 407a, such as a sputtering method, as appropriate. When hydrogen is contained in the insulating layer 407a, entry of the hydrogen into the oxide semiconductor layer, or extraction of oxygen in the oxide semiconductor layer by the hydrogen may occur, thereby causing the backchannel of the oxide semiconductor layer to have lower resistance (to be n-type), so that a parasitic channel may be formed. Therefore, it is important that a method in which hydrogen is not used is employed in order to form the insulating layer 407a containing as little hydrogen as possible.

20 [0342]

In this embodiment, a silicon oxide film is formed to a thickness of 200 nm as the oxide insulating layer 407a by a sputtering method. The substrate temperature in deposition may be higher than or equal to room temperature and lower than or equal to 300 °C and is 100 °C in this embodiment. The silicon oxide film can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere containing a rare gas and oxygen.

[0343]

As a target, a silicon oxide target or a silicon target may be used. Further, a silicon oxide target, a silicon target, or the like may be used as a target for forming the oxide insulating layer 407a. For example, the silicon oxide film may be formed using a silicon target by a sputtering method in an atmosphere containing oxygen.

[0344]

It is preferable that a high-purity gas in which impurities such as hydrogen, water, a hydroxyl group, and hydride are removed be used as the sputtering gas for the formation of the oxide insulating layer 407a.

5 [0345]

Before formation of the oxide insulating layer 407a, plasma treatment with the use of a gas such as N_2O , N_2 , or Ar may be performed to remove water or the like adsorbed onto an exposed surface of the oxide semiconductor layer 403a. In the case where the plasma treatment is performed, the oxide insulating layer 407a is preferably
10 formed without exposure to the air in contact with part of the top surface of the oxide semiconductor layer 403a.

[0346]

Further, second heat treatment may be performed in an inert gas atmosphere or an oxygen gas atmosphere (preferably at a temperature of 200 °C to 400 °C inclusive, for
15 example, 250 °C to 350 °C inclusive). For example, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. The second heat treatment is performed while part of the top surface of the oxide semiconductor layer 403a is in contact with the oxide insulating layer 407a.

[0347]

20 Through the above steps, impurities such as hydrogen, moisture, a hydroxyl group, and hydride (also referred to as a hydrogen compound) are intentionally removed from the oxide semiconductor layer. Additionally, oxygen can be supplied. Accordingly, the oxide semiconductor layer is highly purified.

[0348]

25 Through the above steps, the transistor is formed (see FIG. 11A).

[0349]

When a silicon oxide layer having a lot of defects is used as the oxide insulating layer 407a, heat treatment performed after formation of the silicon oxide layer has an effect in diffusing an impurity such as hydrogen, moisture, a hydroxyl group, or hydride
30 contained in the oxide semiconductor layer 403a to the oxide insulating layer 407a so that the impurity contained in the oxide semiconductor layer 403a can be further

reduced.

[0350]

A protective insulating layer 409a may be formed over the oxide insulating layer 407a. For example, a silicon nitride film is formed by an RF sputtering method.

- 5 Since high productivity can be achieved with an RF sputtering method, an RF sputtering method is preferably employed as a formation method of the protective insulating layer 409a. In this embodiment, a silicon nitride film is formed as the protective insulating layer 409a (see FIG. 11B).

[0351]

- 10 In this embodiment, as the protective insulating layer 409a, a silicon nitride film is formed with the use of a target of a silicon semiconductor by heating the substrate 400a over which layers up to and including the oxide insulating layer 407a are formed, to a temperature of 100 °C to 400 °C, introducing a sputtering gas containing high-purity nitrogen in which hydrogen and moisture are removed. In that case, the protective
15 insulating layer 409a is preferably formed while moisture remaining in the treatment chamber is removed, similarly to the oxide insulating layer 407a.

[0352]

- After the formation of the protective insulating layer 409a, heat treatment may be further performed at a temperature of 100 °C to 200 °C inclusive in the air for an hour
20 to 30 hours inclusive. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from a room temperature to a temperature of 100 °C to 200 °C inclusive and then decreased to a room temperature. That is an example of a method for manufacturing the transistor in FIG.
25 9A.

[0353]

- Although the example of the fabrication method of the transistor in FIG. 9A is described, the present invention is not limited to this example. For example, as for the components of FIGS. 9B to 9D which have the same designations as the components of
30 FIG. 9A and whose function is at least partly the same as that of the components of FIG. 9A, description of the example of the fabrication method of the transistor in FIG. 9A can

be referred to as appropriate.

[0354]

As described above, the transistor including an oxide semiconductor layer, which is applicable to the input circuit or the input-output circuit in the above
5 embodiment, is a transistor including an oxide semiconductor layer as a channel formation layer. The oxide semiconductor layer used in the transistor is highly purified by heat treatment to be i-type or substantially i-type.

[0355]

The highly purified oxide semiconductor layer includes extremely few carriers
10 (close to 0). The carrier concentration of the oxide semiconductor layer is less than $1 \times 10^{14} / \text{cm}^3$, preferably less than $1 \times 10^{12} / \text{cm}^3$, still preferably less than $1 \times 10^{11} / \text{cm}^3$. Therefore, the off-state current per micrometer in channel width can be 10 aA (1×10^{-17} A) or less, preferably 1 aA (1×10^{-18} A) or less, more preferably 10 zA (1×10^{-20} A) or less, still more preferably 1 zA (1×10^{-21} A) or less.

15 [0356]

For example, when the transistor is used in the display circuit in the input-output device of the above embodiment, a period in which an image based on image data at the time of displaying a still image is held can be made longer, so that power consumption of the input-output device can be reduced.

20 [0357]

Further, for example, by using the transistor, a selection signal output circuit, a reset signal output circuit, and a photodetector circuit can be formed in the same process; thus, manufacturing cost of the input-output device can be reduced.

[0358]

25 Furthermore, for example, by using the transistor, a scan signal output circuit, an image signal output circuit, a selection signal output circuit, a reset signal output circuit, a display circuit, and a photodetector circuit can be formed in the same process; thus, manufacturing cost of the input-output device can be reduced.

[0359]

30 [Embodiment 8]

In this embodiment, described are electronic devices each provided with the

input-output device of the above embodiment.

[0360]

Structural examples of the electronic devices in this embodiment are described with reference to FIGS. 12A to 12F. FIGS. 12A to 12F illustrate the structural
5 examples of the electronic devices of this embodiment.

[0361]

The electronic device in FIG. 12A is a personal digital assistant. The personal digital assistant in FIG. 12A has at least an input-output portion 1001. The personal digital assistant in FIG. 12A can be used as a cell phone, for example, when the
10 input-output portion 1001 is provided with an operation portion 1002. The input-output portion 1001 is not necessarily provided with the operation portion 1002, and the personal digital assistant in FIG. 12A may be additionally provided with an operation button. Further, the personal digital assistant in FIG. 12A may be utilized as a scratch pad or a handy scanner.

15 [0362]

The electronic device in FIG. 12B is an information guide terminal such as an automotive navigation system. The information guide terminal in FIG. 12B has at least an input-output portion 1101, and may also have operation buttons 1102, an external input terminal 1103, and the like. When the input-output device of the above
20 embodiment is provided for the input-output portion 1101, data can be input to the input-output portion 1101 with the use of light. For example, a shadow cast by a finger or the like on the input-output portion 1101 changes the illuminance of light incident on the shadow area of the input-output portion 1101. By detecting the change, data can be input to the input-output device.

25 [0363]

The electronic device in FIG. 12C is a laptop personal computer. The laptop personal computer in FIG. 12C has a housing 1201, an input-output portion 1202, a speaker 1203, an LED lamp 1204, a pointing device 1205, a connection terminal 1206, and a keyboard 1207. The laptop personal computer in FIG. 12C has a housing 1201, a
30 display portion 1202, a speaker 1203, an LED lamp 1204, a pointing device 1205, a connection terminal 1206, and a keyboard 1207. The input-output device of the above

embodiment is provided for the input-output portion 1202. When the input-output device of the above embodiment is provided for the input-output portion 1202, an input operation can be performed in such a manner that text is written directly on the input-output portion 1202. Further, when the input-output device of the above
5 embodiment is provided for the input-output portion 1202, an input portion which is substitute for the keyboard 1207 can be provided in the input-output portion 1202.

[0364]

The electronic device illustrated in FIG. 12D is a portable game machine. The portable game machine in FIG. 12D has an input-output portion 1301, an input-output
10 portion 1302, a speaker 1303, a connection terminal 1304, an LED lamp 1305, a microphone 1306, a recording medium reading portion 1307, operation buttons 1308, and a sensor 1309. The input-output device of the above embodiment is provided for both or either the input-output portion 1301 and/or the input-output portion 1302. When the input-output device of the above embodiment is provided for the input-output
15 portion 1301, data can be input to the input-output portion 1301 with the use of light.

[0365]

The electronic device in FIG. 12E is an e-book reader. The e-book reader in FIG. 12E has at least a housing 1401, a housing 1403, an input-output portion 1405, an input-output portion 1407, and a hinge 1411.

20 [0366]

The housings 1401 and 1403 are connected by the hinge 1411 so that the e-book reader in FIG. 12E can be opened and closed along the hinge 1411. With such a structure, the e-book reader can be handled like a paper book. The input-output portion 1405 and the input-output portion 1407 are incorporated in the housing 1401 and the
25 housing 1403, respectively. The input-output portion 1405 and the input-output portion 1407 may display different images. For example, one image can be displayed across both the input-output portions. In the case where different images are displayed on the input-output portion 1405 and the input-output portion 1407, for example, text may be displayed on the input-output portion on the right side (the input-output portion 1405 in
30 FIG. 12E) and graphics may be displayed on the input-output portion on the left side (the input-output portion 1407 in FIG. 12E).

[0367]

In the e-book reader in FIG. 12E, the housing 1401 or the housing 1403 may be provided with an operation portion or the like. For example, the e-book reader in FIG. 12E may have a power switch 1421, operation keys 1423, and a speaker 1425. In the case of the e-book reader in FIG. 12E, pages of an image with a plurality of pages can be turned with the operation keys 1423. Furthermore, in the e-book reader in FIG. 12E, a keyboard, a pointing device, or the like may be provided in either or both the input-output portion 1405 or/and the input-output portion 1407. In addition, an external connection terminal (an earphone terminal, a USB terminal, a terminal connectable to a variety of cables such as an AC adapter and a USB cable, or the like), a recording medium insertion portion, or the like may be provided on the back surface or the side surface of the housing 1401 and the housing 1403 in FIG. 12E. Furthermore, the e-book reader in FIG. 12E may have a function of an electronic dictionary.

[0368]

Further, the input-output device of the above embodiment may be provided for both or either the input-output portion 1405 and/or the input-output portion 1407. When the input-output device of the above embodiment is provided for both or either the input-output portion 1405 and/or the input-output portion 1407, data can be input to both or either the input-output portion 1405 and/or the input-output portion 1407 with the use of light.

[0369]

The e-book reader in FIG. 12E may transmit and receive data wirelessly. With such a structure, desired book data or the like can be purchased and downloaded from an electronic book server.

[0370]

The electronic device in FIG. 12F is a display. The display in FIG. 12F has a housing 1501, an input-output portion 1502, a speaker 1503, an LED lamp 1504, operation buttons 1505, a connection terminal 1506, a sensor 1507, a microphone 1508, and a supporting base 1509. The input-output device of the above embodiment may be provided for the input-output portion 1502. When the input-output device of the above embodiment is provided for the input-output portion 1502, data can be input to the

input-output portion 1502 with the use of light.

[0371]

The electronic device of this embodiment may have a power supply circuit including a solar battery cell, a power storage device for charging a voltage output from the solar battery cell, and a DC converter circuit for converting a voltage charged in the power storage device into voltages needed for circuits. With such a structure, an external power source is not needed because power consumption of the input-output device of the above embodiment is low, and thus the electronic device can be used for a long period of time even at a place without an external power source.

10 [0372]

By applying the input-output device described in the above embodiment to an input-output portion of an electronic device, a low-power-consumption electronic device can be provided.

15 This application is based on Japanese Patent Application serial No. 2010-056728 filed with the Japan Patent Office on March 12, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A method for driving an input circuit including a selection signal output circuit outputting a selection signal; a reset signal output circuit outputting a reset signal;
5 and a photodetector circuit supplied with the selection signal and the reset signal,
the method comprising:

outputting a data signal from the photodetector circuit when the reset signal output circuit and the selection signal output circuit output the reset signal and the selection signal, respectively, in a first period; and
10 stopping an output of the reset signal from the reset signal output circuit, and an output of the selection signal from the selection signal output circuit in a second period.

2. A method for driving an input circuit including a selection signal output circuit, a reset signal output circuit, and a photodetector circuit,
15 wherein the selection signal output circuit includes a first shift register to which a first start signal, a first clock signal, and a power supply voltage are input and outputs a selection signal when the first shift register outputs a signal,

wherein the reset signal output circuit includes a second shift register to which a second start signal, a second clock signal, and a power supply voltage are input and
20 outputs a reset signal when the second shift register outputs a signal, and

wherein the photodetector circuit is supplied with the reset signal and the selection signal,

the method comprising:
outputting the second start signal and the second clock signal to the second shift
25 register and outputting the first start signal and the first clock signal to the first shift register, in a first period; and

stopping an output of the second start signal and the second clock signal to the second shift register, and an output of the first start signal and the first clock signal to the first shift register, in a second period.

30

3. A method for driving an input circuit including a selection signal output

circuit, a reset signal output circuit, and a photodetector circuit,

wherein the selection signal output circuit includes a first shift register to which a first start signal, a first clock signal, and a power supply voltage are input and outputs a selection signal when the first shift register outputs a signal,

5 wherein the reset signal output circuit includes a second shift register to which a second start signal, a second clock signal, and a power supply voltage are input and outputs a reset signal when the second shift register outputs a signal, and

wherein the photodetector circuit is supplied with the reset signal and the selection signal,

10 the method comprising:

outputting the second start signal, the second clock signal, and the power supply voltage to the second shift register and outputting the first start signal, the first clock signal, and the power supply voltage to the first shift register, in a first period; and

15 stopping an output of the second start signal, the second clock signal, and the power supply voltage to the second shift register, and an output of the first start signal, the first clock signal, and the power supply voltage to the first shift register, in a second period.

4. The method for driving an input circuit according to claim 3,

20 wherein an output of the first clock signal to the first shift register is stopped after stopping output of the power supply voltage to the first shift register, and

wherein an output of the second clock signal to the second shift register is stopped after stopping an output of the power supply voltage to the second shift register.

25 5. A method for driving an input-output device including a display circuit, a selection signal output circuit, a reset signal output circuit, and a photodetector circuit,

wherein the display circuit is supplied with a scan signal and supplied with an image signal in accordance with the scan signal to be in a display state depending on the image signal,

30 wherein the selection signal output circuit includes a first shift register to which a first start signal, a first clock signal, and a power supply voltage are input and outputs a

selection signal when the first shift register outputs a signal,

wherein the reset signal output circuit includes a second shift register to which a second start signal, a second clock signal, and a power supply voltage are input and outputs a reset signal when the second shift register outputs a signal,

5 wherein the photodetector circuit is supplied with the reset signal and the selection signal, and performs a reading operation,

wherein, in the reading operation, the method comprises:

outputting the second start signal and the second clock signal to the second shift register and outputting the first start signal and the first clock signal to the first shift register, in a first period; and

10 stopping an output of the second start signal and the second clock signal to the second shift register, and an output of the first start signal and the first clock signal to the first shift register, in a second period.

15 6. A method for driving an input-output device including a display circuit, a selection signal output circuit, a reset signal output circuit, and a photodetector circuit,

wherein the display circuit is supplied with a scan signal and supplied with an image signal in accordance with the scan signal to be in a display state depending on the image signal,

20 wherein the selection signal output circuit includes a first shift register to which a first start signal, a first clock signal, and a power supply voltage are input and outputs a selection signal when the first shift register outputs a signal,

wherein the reset signal output circuit includes a second shift register to which a second start signal, a second clock signal, and a power supply voltage are input and outputs a reset signal when the second shift register outputs a signal,

25 wherein the photodetector circuit is supplied with the reset signal and the selection signal, and performs a reading operation,

wherein, in the reading operation, the method comprises:

outputting the second start signal, the second clock signal, and the power supply voltage to the second shift register and outputting the first start signal, the first clock signal, and the power supply voltage to the first shift register, in a first period; and

30

stopping an output of the second start signal, the second clock signal, and the power supply voltage to the second shift register, and an output of the first start signal, the first clock signal and the power supply voltage to the first shift register, in a second period.

5

7. The method for driving an input-output device according to claim 6,
wherein an output of the first clock signal to the first shift register is stopped
after stopping an output of the power supply voltage to the first shift register, and
wherein an output of the second clock signal to the second shift register is
10 stopped after stopping an output of the power supply voltage to the second shift register.

FIG. 1A

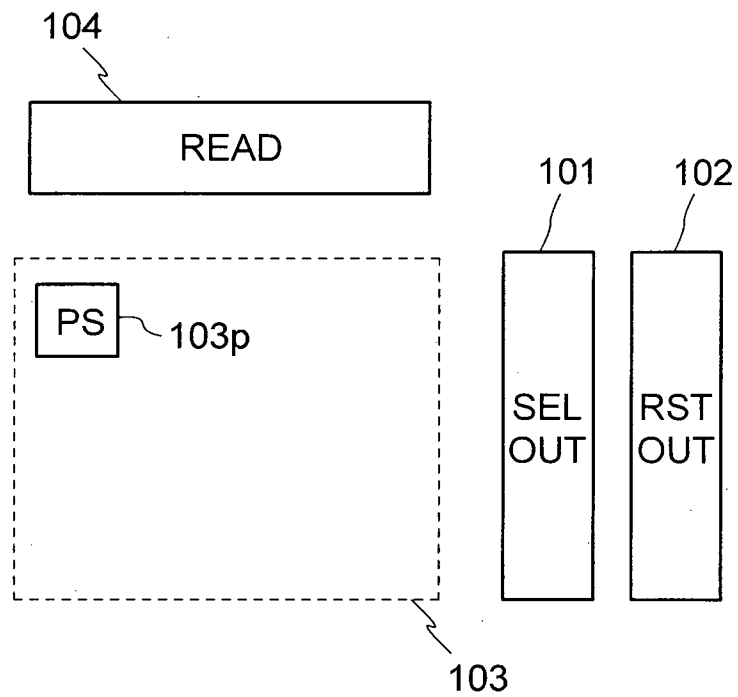
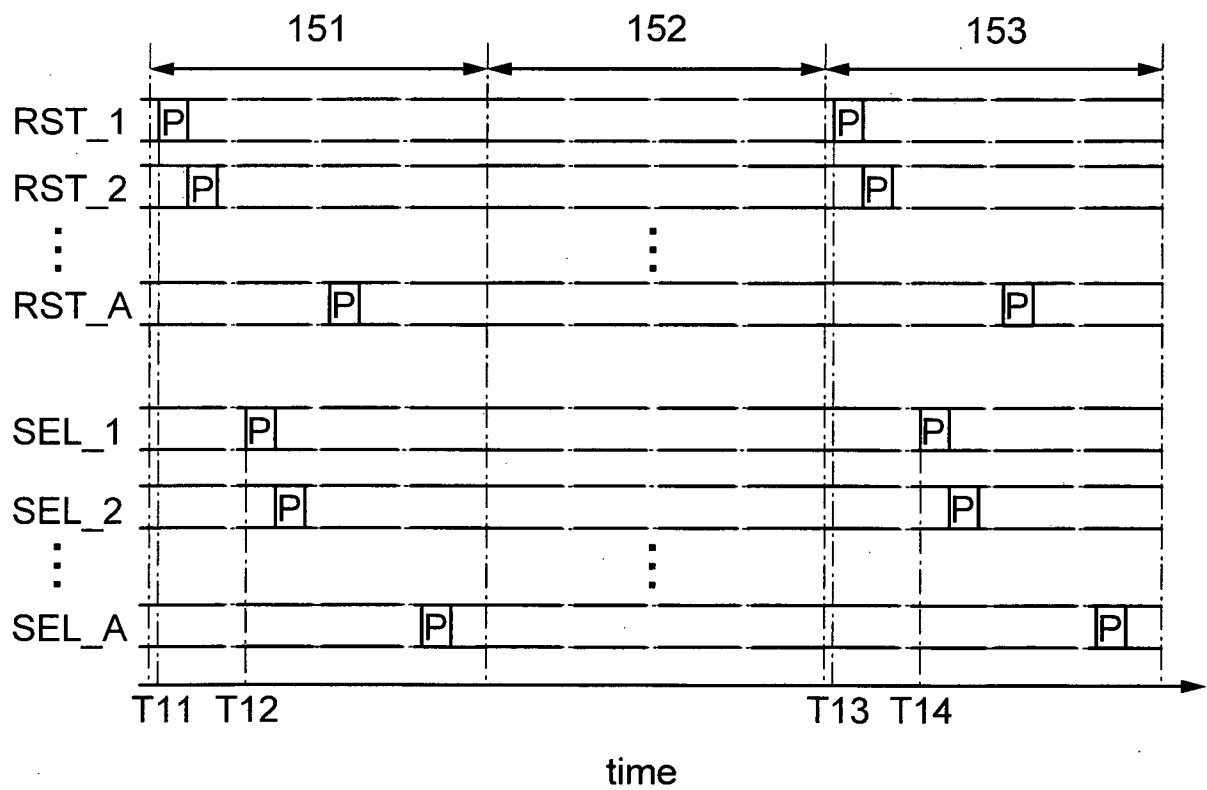


FIG. 1B



3/13

FIG. 3A

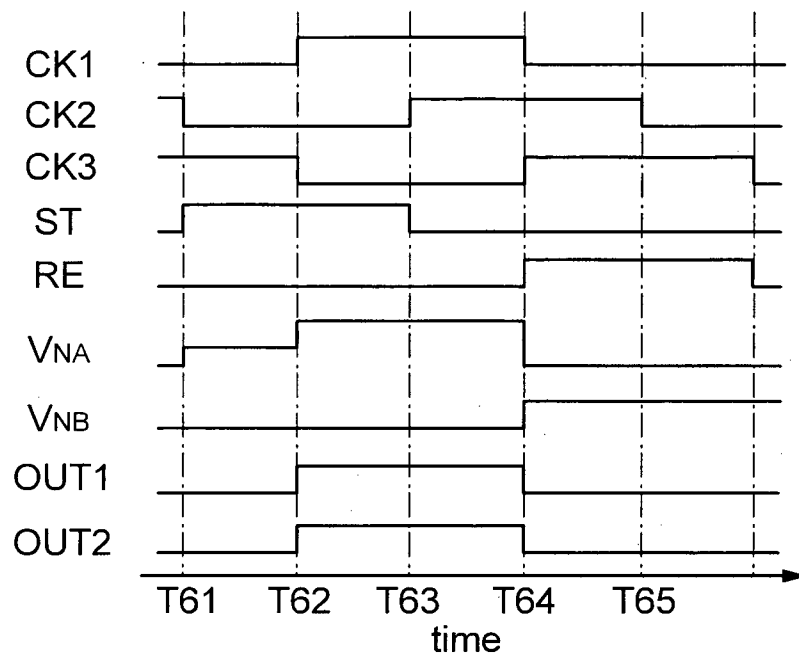


FIG. 3B

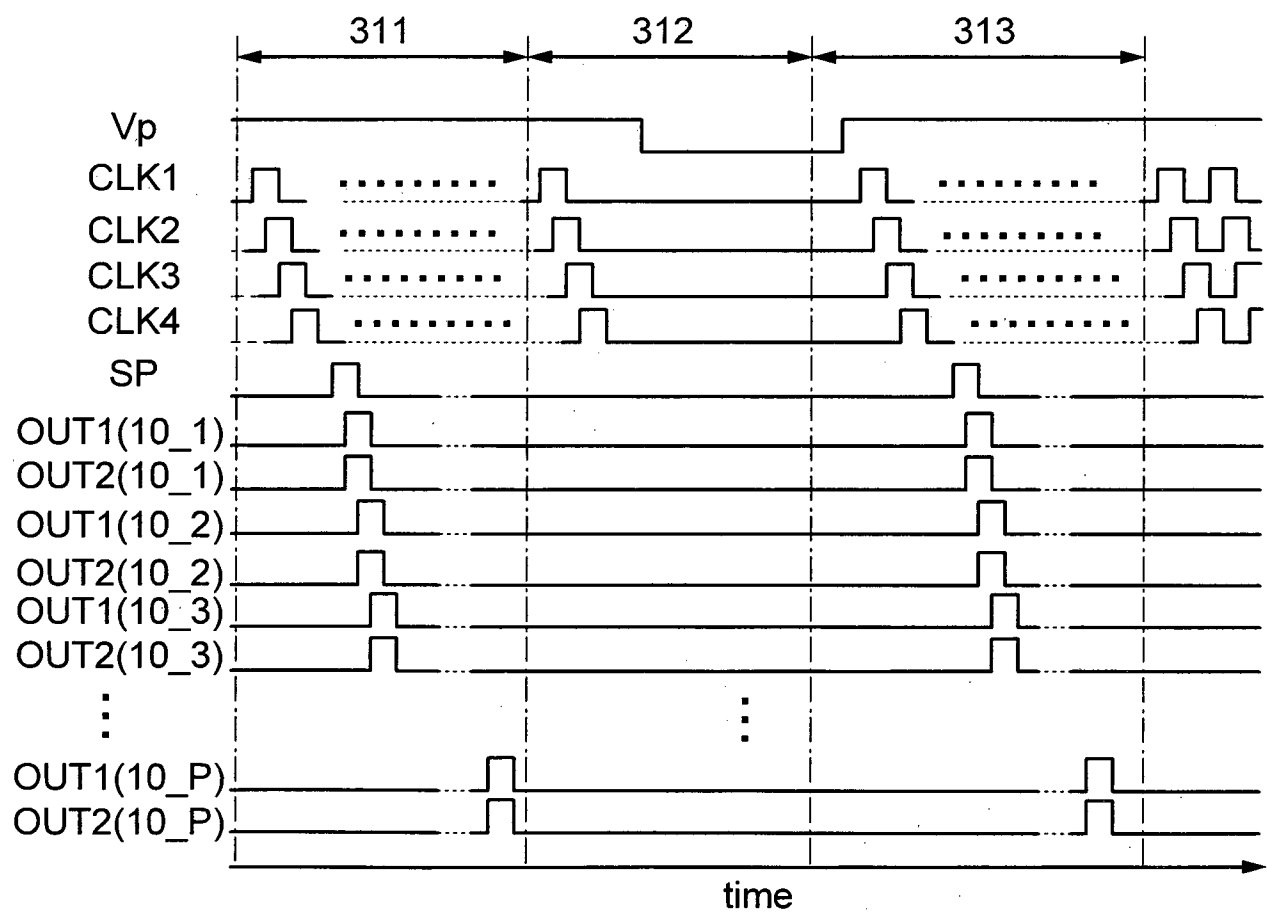


FIG. 4A

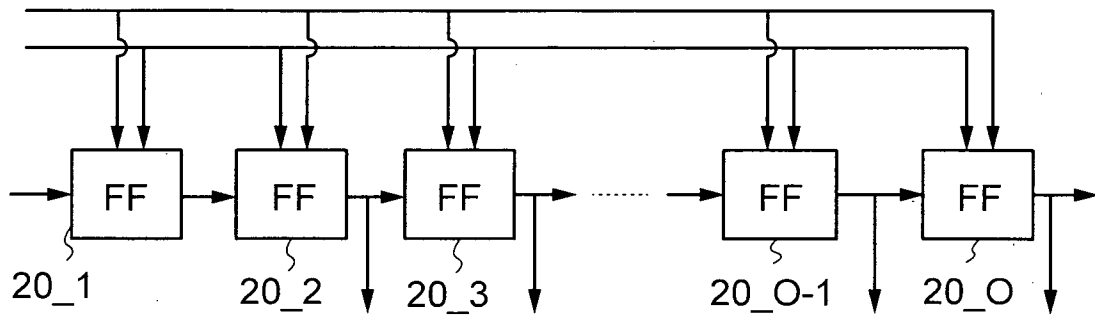


FIG. 4B

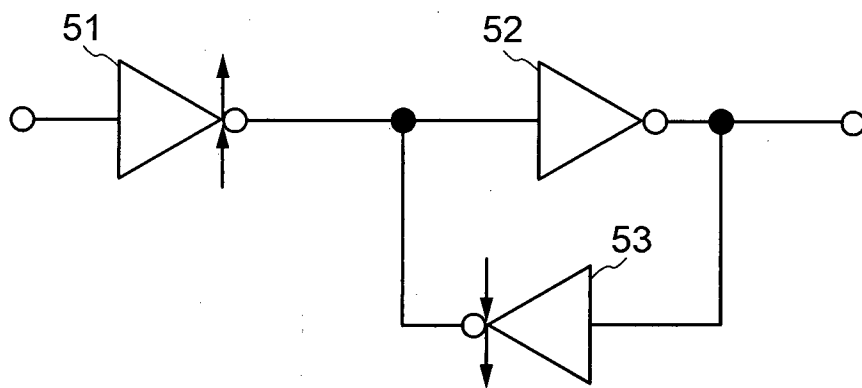
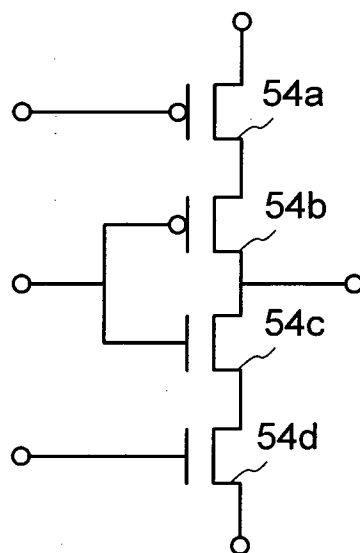


FIG. 4C



5/13

FIG. 5

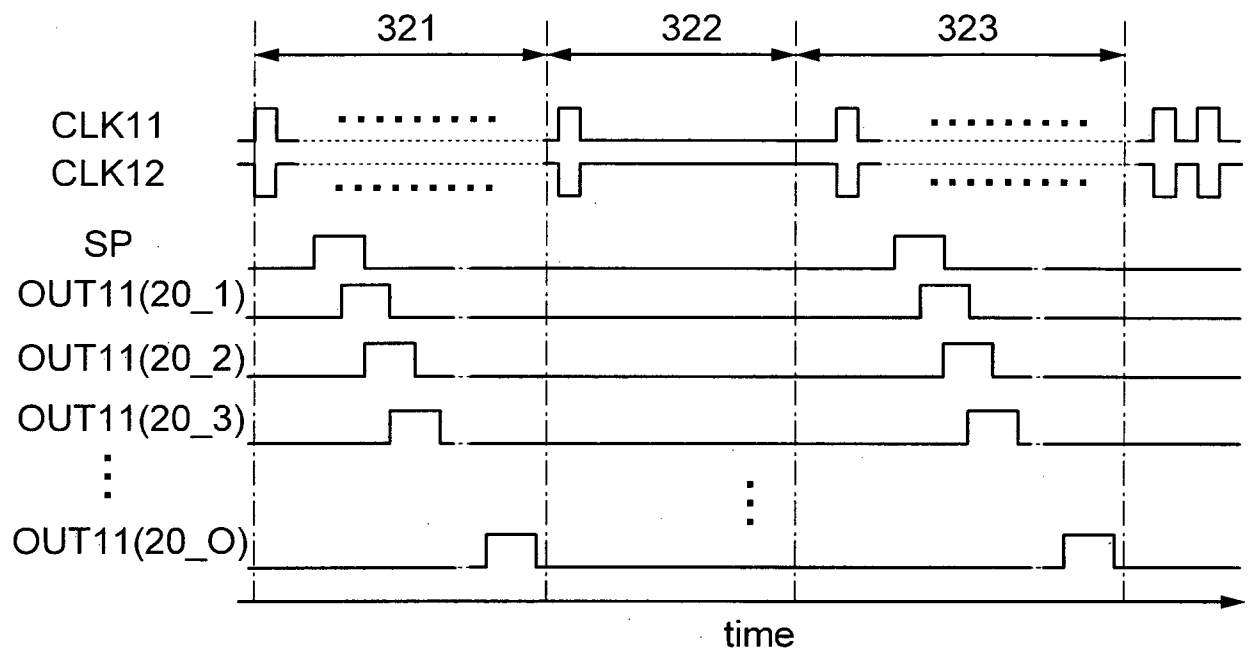


FIG. 6A

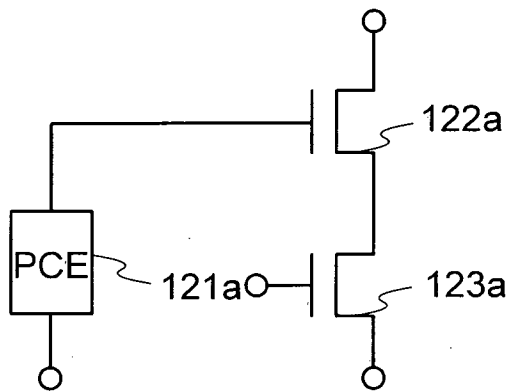


FIG. 6D

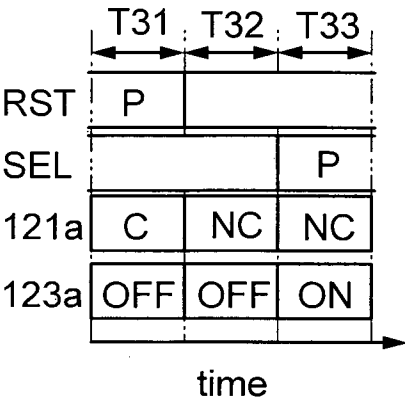


FIG. 6B

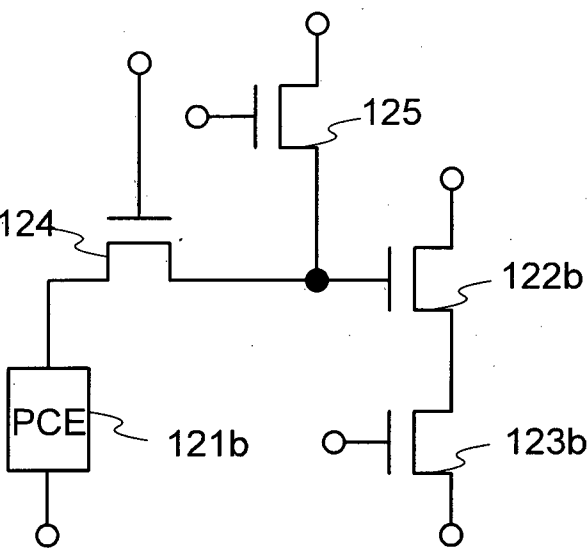


FIG. 6E

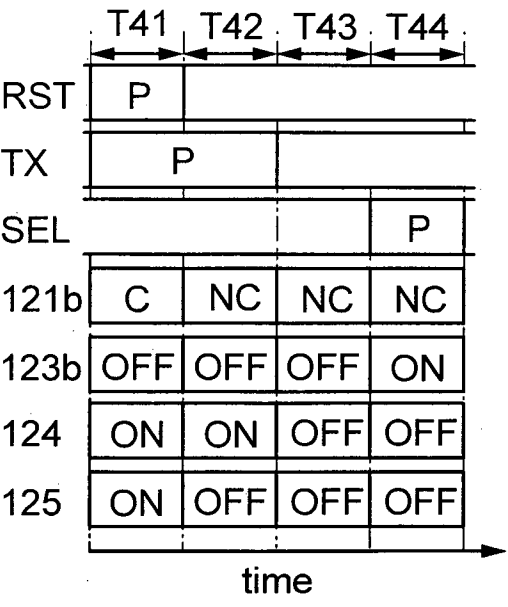


FIG. 6C

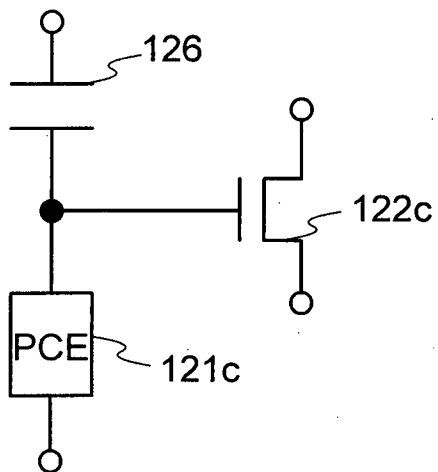


FIG. 6F

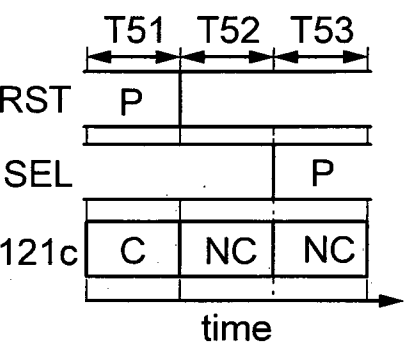


FIG. 7A

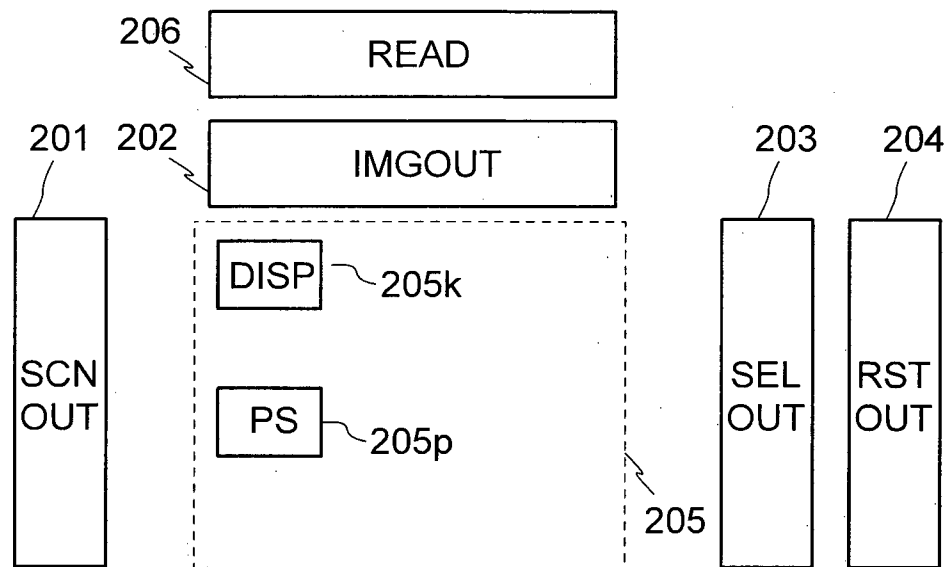


FIG. 7B

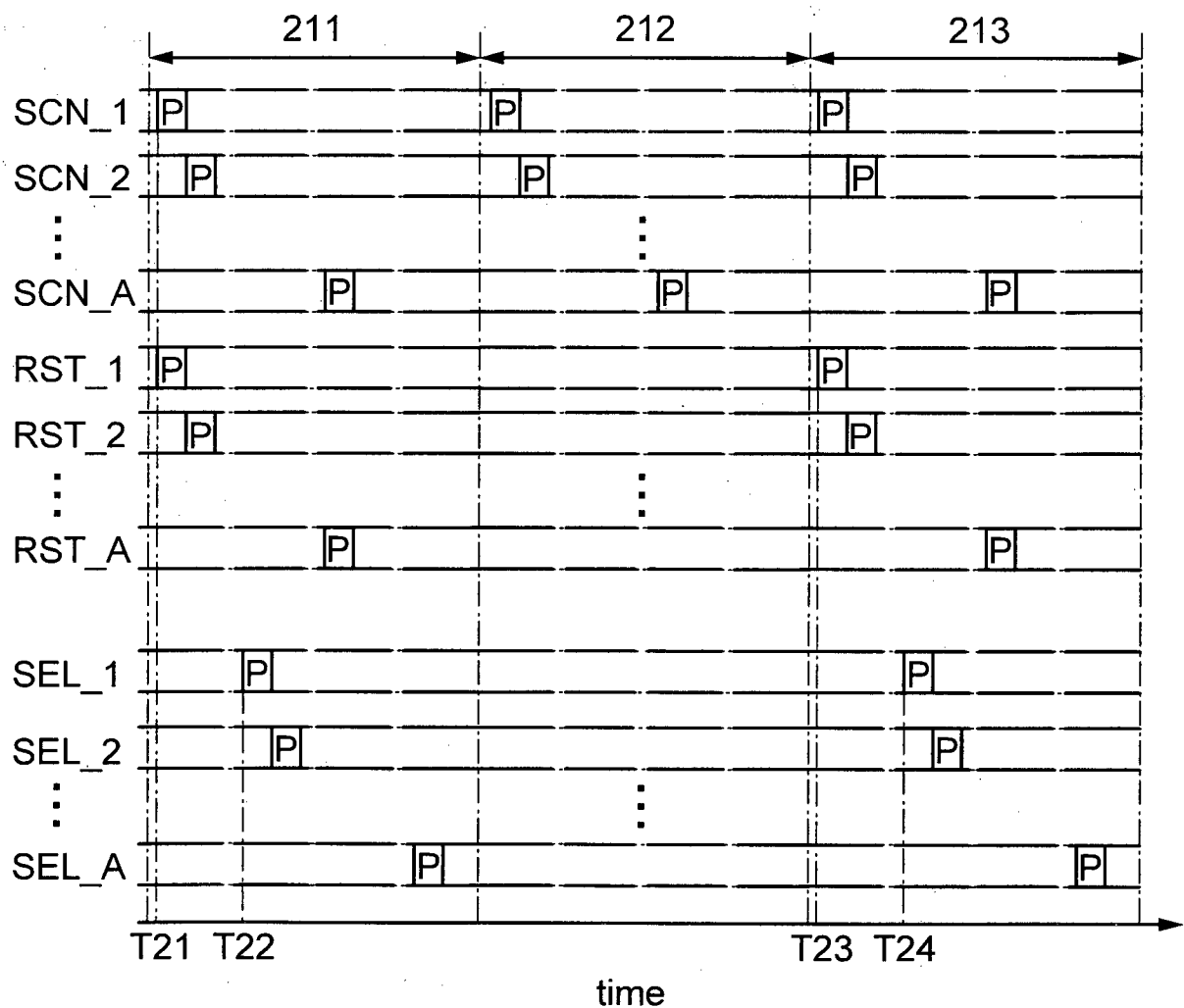


FIG. 8

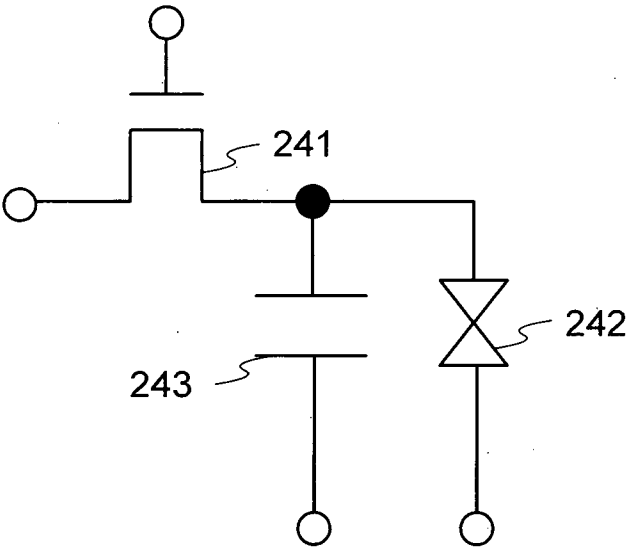


FIG. 9A

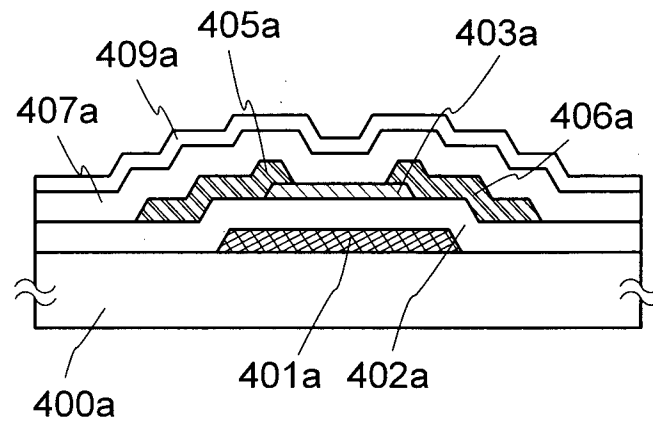


FIG. 9B

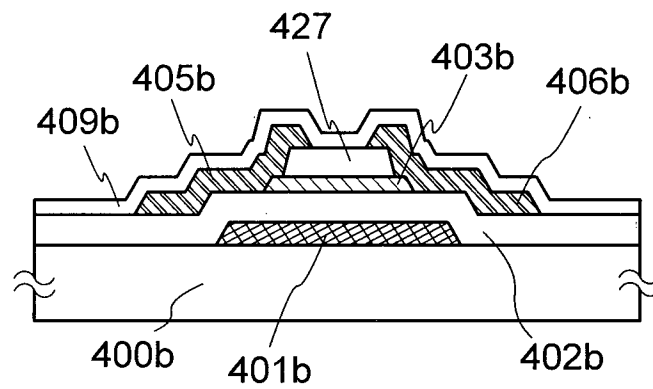


FIG. 9C

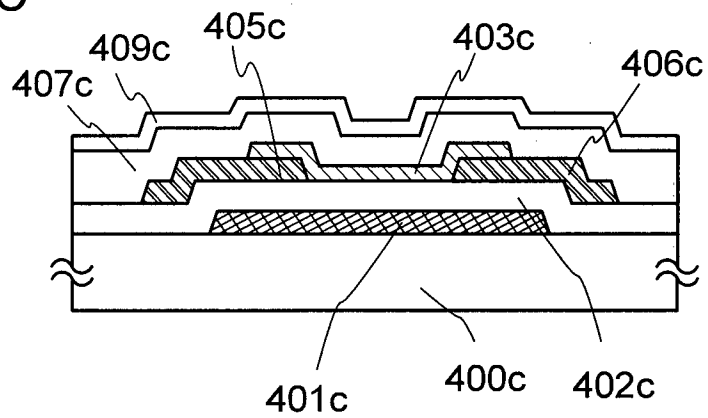


FIG. 9D

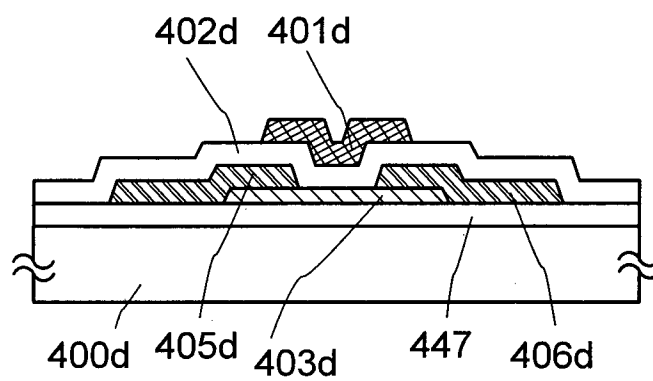


FIG. 10A

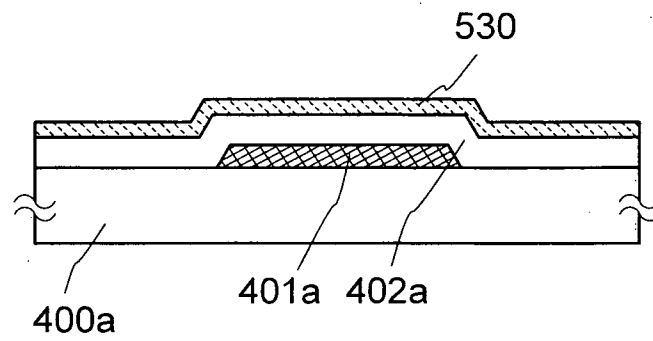


FIG. 10B

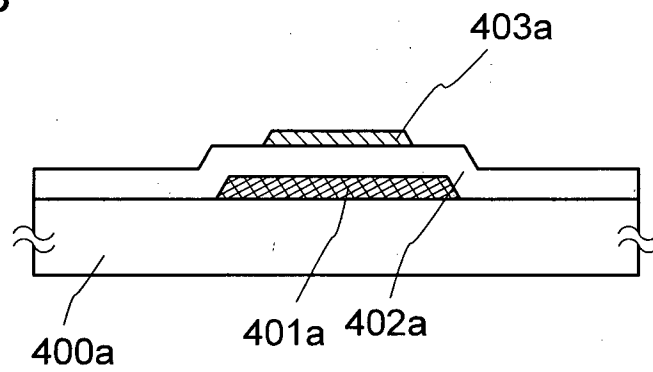


FIG. 10C

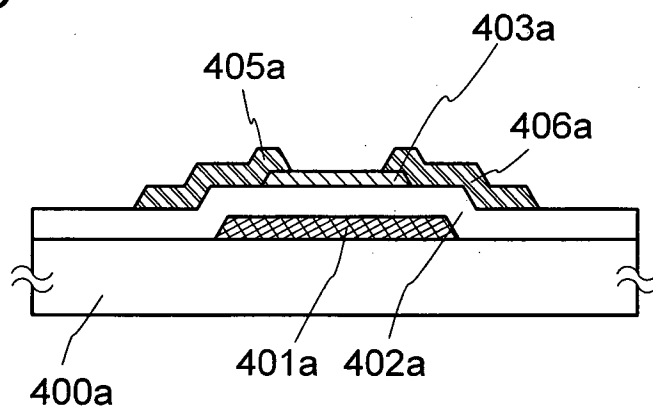


FIG. 11A

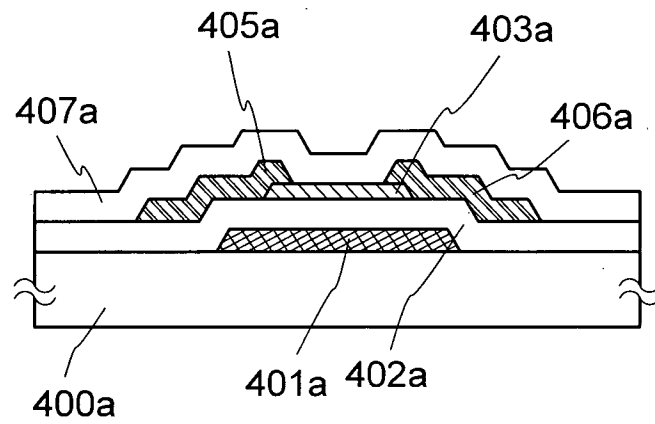


FIG. 11B

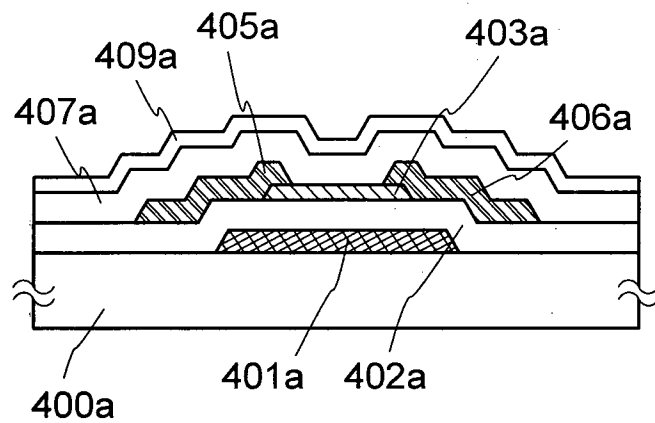


FIG. 12A

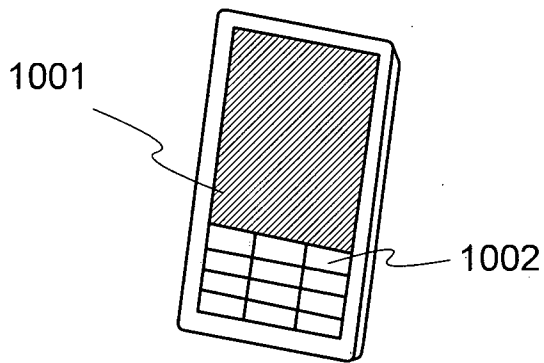


FIG. 12D

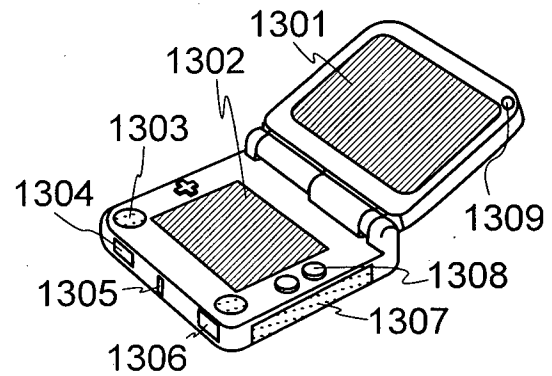


FIG. 12B

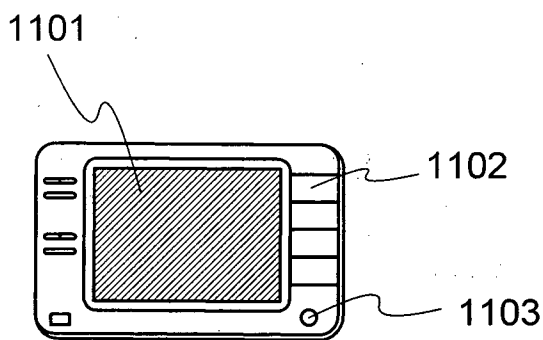


FIG. 12E

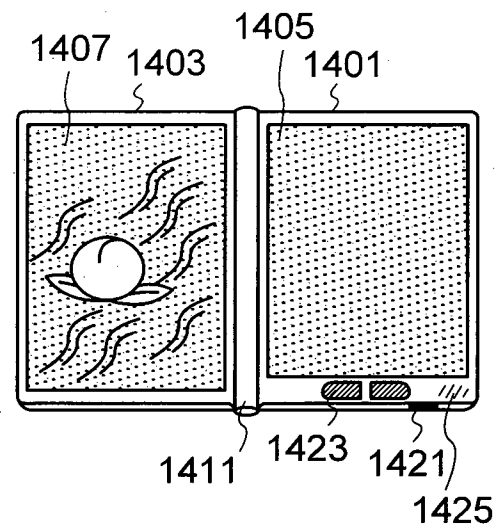


FIG. 12C

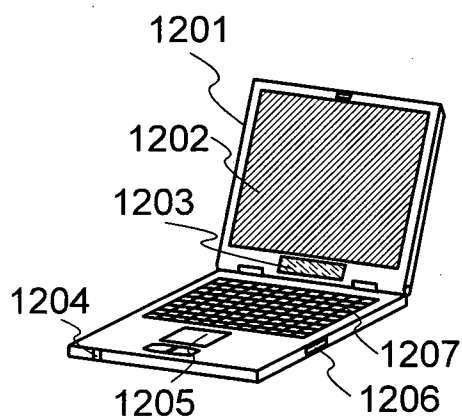
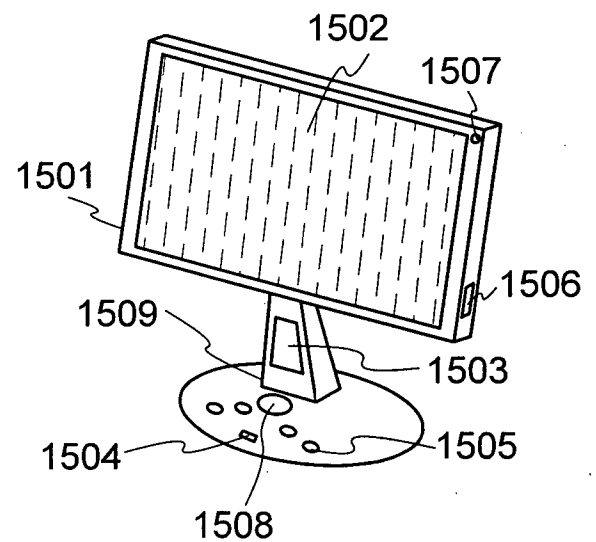


FIG. 12F



[EXPLANATION OF REFERENCES]

10: sequential circuit, 20: sequential circuit, 31: transistor, 32: transistor, 33: transistor, 34: transistor, 35: transistor, 36: transistor, 37: transistor, 38: transistor, 39: transistor, 40: transistor, 41: transistor, 51: clocked inverter, 52: inverter, 53: clocked inverter, 54a: transistor, 54b: transistor, 54c: transistor, 54d: transistor, 101: selection signal output circuit, 102: reset signal output circuit, 103: photodetection portion, 103p: photodetector circuit, 104: reading circuit, 121: photoelectric conversion element, 121a: photoelectric conversion element, 121b: photoelectric conversion element, 121c: photoelectric conversion element, 122a: transistor, 122b: transistor, 122c: transistor, 123a: transistor, 123b: transistor, 123c: transistor, 124: transistor, 125: transistor, 126: capacitor, 201: scan signal output circuit, 202: image signal output circuit, 203: selection signal output circuit, 204: reset signal output circuit, 205: pixel portion, 205k: display circuit, 205p: photodetector circuit, 206: reading circuit, 241: transistor, 242: liquid crystal element, 243: capacitor, 400a: substrate, 400b: substrate, 400c: substrate, 400d: substrate, 401a: conductive layer, 401b: conductive layer, 401c: conductive layer, 401d: conductive layer, 402a: insulating layer, 402b: insulating layer, 402c: insulating layer, 402d: insulating layer, 403a: oxide semiconductor layer, 403b: oxide semiconductor layer, 403c: oxide semiconductor layer, 403d: oxide semiconductor layer, 405a: conductive layer, 405b: conductive layer, 405c: conductive layer, 405d: conductive layer, 406a: conductive layer, 406b: conductive layer, 406c: conductive layer, 406d: conductive layer, 407a: oxide insulating layer, 407c: oxide insulating layer, 409a: protective insulating layer, 409b: protective insulating layer, 409c: protective insulating layer, 427: insulating layer, 447: insulating layer, 530: oxide semiconductor film, 1001: input-output portion, 1002: operation portion, 1101: input-output portion, 1102: operation button, 1103: external input terminal, 1201: housing, 1202: input-output portion, 1203: speaker, 1204: LED lamp, 1205: pointing device, 1206: connection terminal, 1207: keyboard, 1301: input-output portion, 1302: input-output portion, 1303: speaker, 1304: connection terminal, 1305: LED lamp, 1306: microphone, 1307: recording medium reading portion, 1308: operation button, 1309: sensor, 1401: housing, 1403: housing, 1405: input-output portion, 1407: input-output portion, 1411: hinge, 1421: power switch, 1423: operation key, 1425: speaker, 1501: housing, 1502: input-output portion, 1503: speaker, 1504: LED lamp, 1505: operation button, 1506: connection terminal, 1507: sensor, 1508: microphone, and 1509: supporting base.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/053620

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H04N5/374 (2011.01) i, G06F3/041 (2006.01) i, G06F3/042 (2006.01) i,
H04N5/376 (2011.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H04N5/374, G06F3/041, G06F3/042, H04N5/376

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 9-163232 A (OLYMPUS OPTICAL CO.,LTD.) 1997.06.20, Paragraphs 【0007】 - 【0008】 , 【0016】 (No Family)	1-7
Y	JP 2001-285723 A (FUJITSU LIMITED) 2001.10.12, Paragraphs 【 0010 】 , 【 0038 】 , Figs.1-2 & US 2001/0028392 A1 & US 2006/0250513 A1 & EP 1143706 A2 & KR 10-2001-0093686 A	1-7
Y	JP 2003-163346 A (SEMICONDUCTOR ENERGY LABORATORY CO.,LTD.) 2003.06.06, Paragraphs 【0056】 - 【0057】 , Fig.7 & JP 2003-158678 A & US 2003/0052324 A1	1-7



Further documents are listed in the continuation of Box C.



See patent family annex.

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“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Date of the actual completion of the international search

11.03.2011

Date of mailing of the international search report

22.03.2011

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5P 9847

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/053620

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2008-176159 A (HITACHI DISPLAYS LTD) 2008.07.31, Paragraph 【0011】 & US 2008/0186267 A1 & CN 101231808 A & CN 101872585 A	1-7
A	JP 2009-181360 A (FUJI XEROX CO., LTD.) 2009.08.13, Paragraph 【0064】 (No Family)	1-7