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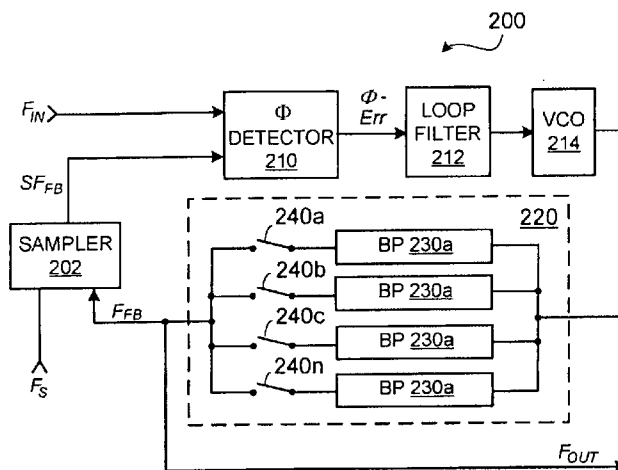


FIG. 2

(57) Abstract: A phase-locked loop (200) includes a sampler (202), a phase detector (210), a loop filter (212), and a VCO (214). The loop achieves frequency multiplication without the need for a divider in the loop's feedback path. The VCO (214) is operated above the Nyquist rate of the sampler, causing the loop to lock on an aliased signal. Any variations in the VCO output frequency (i.e., jitter or phase noise) are fed back to the phase detector (210) 1-for-1, without attenuation normally associated with frequency dividers. Loop gain can therefore be kept high, even in loops that provide high closed loop frequency multiplication. According to one variation, a harmonic generator (540) is placed between the VCO and the sampler, thus causing the loop to lock on harmonics of the VCO frequency. Open loop gain and precision are thus further improved.

TITLE

PHASE LOCKING ON ALIASED FREQUENCIES

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BACKGROUND

FIELD OF THE INVENTION

10 This invention relates generally to automatic test equipment for electronics, and, more particularly, to techniques for generating periodic signals for testing electronic devices.

DESCRIPTION OF RELATED ART

15 Electronics manufacturers commonly use automatic test equipment (ATE) for testing semiconductor components and electronic assemblies. ATE reduces costs to manufacturers by allowing products to be tested early in the manufacturing process. Early testing allows defective units to be identified and discarded before substantial additional costs are incurred. In addition, ATE allows manufacturers to grade different
20 units according to their tested levels of performance. Better performing units can generally be sold at higher prices.

One of the basic functions of ATE is to generate signals of predetermined frequency. These signals may include, for example, digital clocks, analog waveforms, and RF waveforms. Often, particular testing scenarios require a test system to produce
25 multiple signals of different frequency. Commonly, frequency and phase differences between different signals must be precisely controlled. Phase-locked loops are commonly used in ATE systems to produce signals with precisely controlled frequency and phase.

Fig. 1 shows a block diagram of a conventional phase-locked loop (PLL) 100.
30 The PLL 100 receives an input signal, F_{IN} , and generates an output signal, F_{OUT} . The PLL 100 includes a phase detector 110, a loop filter 112, and a voltage-controlled oscillator (VCO) 114. It also includes an output frequency divider 118 and a feedback

frequency divider 116. The input signal, F_{IN} , may be supplied by any suitable source, such as a crystal oscillator.

The conventional PLL 100 is a closed loop feedback system that operates essentially as follows. The phase detector 110 compares the input signal F_{IN} to the feedback signal F_{FB} to generate an error signal, which varies in relation to the difference in phase between F_{IN} and F_{FB} . The loop filter 112 smoothes the error signal and generally helps to stabilize the feedback loop. The VCO 114 converts the filter's output signal into an oscillatory signal, F_{VCO} , which has a frequency that varies in relation to the filter's output signal. The feedback divider 116 (generally a counter) divides the frequency of F_{VCO} by an integer, M , to produce the feedback signal, F_{FB} . Outside the loop, the output divider 118 divides the frequency of F_{VCO} by an integer, N , to produce F_{OUT} . As the feedback tends to drive the difference between F_{IN} and F_{FB} to zero, it consequently drives the frequency of F_{VCO} to a value equal to the frequency of $F_{IN} * M$, and therefore tends to drive the frequency of the output signal F_{OUT} to a value equal to the frequency of $F_{IN} * M/N$.

The conventional PLL 100 provides many benefits. For example, output frequency F_{OUT} can be varied, through appropriate selection of N and M , over a wide range of values. In addition, phase noise in the PLL can generally be reduced by setting the bandwidth of the loop filter 112 to arbitrarily low values.

Nevertheless, we have recognized certain shortcomings in the PLL 100, which limits its usefulness in many ATE applications. High frequency applications, such as RF signal generation, require high frequency VCOs. The speed of the VCOs in these applications often greatly exceeds the speed of the phase detectors. This problem is conventionally addressed by making the value of M in the feedback divider 116 very large.

Making the value of M large involves certain drawbacks, however. For instance, the larger the value of M , the greater the reduction in the open-loop gain of the PLL 100. As is known, reducing open-loop gain increases loop tracking errors. It also impairs the ability of the loop to reject noise. To illustrate this effect, consider that the feedback divider 116 not only divides the frequency of F_{VCO} by M , but it also divides any variations (i.e., phase noise or, equivalently, timing jitter) by the same value of M . Sensitivity is therefore reduced.

The frequency divider 116 also adds noise directly. Frequency dividers are commonly implemented as counters, which are known to create spurious noise at their

outputs. Although this noise can be attenuated by the loop filter 112, attenuation cannot generally be achieved without setting the bandwidth of the loop filter to a much lower frequency than the offending noise components of the divider 116. Reducing bandwidth to this degree, however, has the effect of reducing programming speed of the PLL 100,
5 which can negatively impact ATE system performance and throughput.

What is desired is a phase-locking circuit that can produce high frequency signals with low phase noise, without sacrificing programming speed.

SUMMARY

10 In accordance with the present invention, a phase-locking circuit employs a sampler for producing aliased feedback signals, upon which a circuit is caused to lock.

BRIEF DESCRIPTION OF THE DRAWINGS

The ensuing description will be better understood by reference to the
15 accompanying drawings, in which—

Fig. 1 is a block diagram of a conventional phase-locked loop that is operable to produce a wide range of frequencies;

Fig. 2 is a block diagram of phase-locking circuitry according to an illustrative embodiment of the invention;

20 Fig. 3 is a frequency plot showing how frequencies higher than the Nyquist rate can alias to frequencies lower than the Nyquist rate in the circuit of Fig. 2;

Fig. 4 is a frequency plot showing how a band of frequencies higher than the Nyquist rate can alias to a band of frequencies lower than the Nyquist rate in the circuit of Fig. 2;

25 Fig. 5 is a simplified schematic of an illustrative embodiment of phase-locking circuitry, wherein harmonics of the VCO output signal are employed to improve precision;

Fig. 6 is a frequency plot showing how various bands of harmonics are created in the circuit of Fig. 5, wherein one or more of the harmonic bands are aliased to
30 frequencies lower than the Nyquist rate;

Fig. 7 is a block diagram showing an illustrative embodiment of phase-locking circuitry that employs a digital phase detector and a digital loop filter;

Fig. 8 is a simplified block diagram of automatic test equipment that includes phase locking circuitry according to one or more embodiments of the invention;

5 Fig. 9 is a block diagram of a digital phase detector that is suitable for use with the phase-locking circuitry of Fig. 7; and

Fig. 10 is a block diagram of another digital phase detector that is suitable for use with the phase-locking circuitry of Fig. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 2 shows an illustrative embodiment of a phase-locking circuit 200. The phase-locking circuit 200 receives an input signal, F_{IN} , and produces an output signal, F_{OUT} . The circuit 200 includes a sampler 202, a phase detector 210, a loop filter 212, and
 5 a controllable oscillator, such as a VCO (voltage-controlled oscillator) 214. The sampler 202 receives a feedback signal, F_{FB} , at its input and provides a sampled feedback signal, SF_{FB} , at its output. The phase detector 210 has 2 inputs and an output. The first input receives the input signal F_{IN} , and the second input receives the sampled feedback signal, SF_{FB} . The loop filter 212 and the VCO 214 each have an input and an output.

10 The circuit 200 also includes a circuit path 220, coupled from the output of the VCO 214 to the input of the sampler 202, for providing the feedback signal, F_{FB} . Bandpass filters 230a – 230n are preferably provided in the circuit path 220. These bandpass filters are preferably individually selectable via switches 240a – 240n. Each filter preferably has a different center frequency.

15 During operation, the sampler 202 is made to sample the feedback signal, F_{FB} , at a sampling rate F_S . The phase detector 210 receives the sampled feedback signal, SF_{FB} , and outputs an error signal, Φ -Err. The error signal varies in response to the difference between SF_{FB} and F_{IN} . The loop filter 212 filters the error signal and helps to stabilize the loop. The VCO 214 converts the filtered error signal into an oscillatory waveform,
 20 F_{VCO} . The frequency of F_{VCO} varies in response to the level of the filtered error signal.

One of the bandpass filters 230a – 230n is selected for filtering noise from F_{VCO} . The selected filter is preferably the one having the center frequency that is closest to the expected frequency of the F_{VCO} . The desired filter is selected by closing its associated switch (one of 240a – 240n) and opening the remaining switches.

25 The circuit 200 behaves in an essentially normal manner when the frequency of F_{VCO} is less than the Nyquist rate ($F_S/2$) of the sampler. However, significant differences arise when the frequency of F_{VCO} is greater than the Nyquist rate.

As is known, a phenomenon called “aliasing” arises in discrete-time systems when a signal being sampled at a rate F_S contains frequency components greater than
 30 $F_S/2$. Aliasing causes out-of-band frequencies, e.g., those above the Nyquist rate, to appear as images within the system’s bandwidth. These images are normally regarded as errors. However, we have recognized that these aliased images can be used to improve performance.

Fig. 3 shows a frequency plot of a discrete-time system that is sampled at a rate F_s . The horizontal line represents frequency, with zero frequency (DC) appearing at the left and increasing frequencies extending to the right. Frequencies are represented in multiples of the Nyquist rate, $F_s/2$. As shown, frequencies above the Nyquist rate
 5 produce aliased images within the system bandwidth (i.e., below the Nyquist rate). In particular, any component that is an increment δ greater than any multiple of the Nyquist rate produces an aliased image at a frequency δ within the system bandwidth.

The creation of aliased images has significant consequences in the phase-locking circuit of Fig. 2. When the frequency of F_{VCO} exceeds $F_s/2$, an aliased image of that
 10 frequency appears within the sampler's bandwidth and the circuit is made to lock on that image. This means that the phase-locking circuit 200 can be operated with substantial gain without requiring a frequency divider in its feedback path. The circuit 200 can be made to produce arbitrarily high frequencies, limited only by its analog characteristics.

Output frequency ambiguity can arise if the VCO 214 operates over too large a
 15 frequency range. For instance, if the output range (maximum frequency minus minimum frequency) exceeds $F_s/2$, then the phase-locking circuit may be able to satisfy its feedback conditions at two or more different VCO frequencies. Preferably, this condition is avoided by limiting the bandwidth of each of the bandpass filters 230a – 230n to less than $F_s/2$. Alternatively, it may be avoided by selecting a VCO 214 that has an output
 20 range less than $F_s/2$.

Significant performance benefits arise from the use of aliased images in the phase-locking circuit 200. These are best understood with reference to Fig. 4.

Fig. 4 is a frequency plot that shows the effect of aliasing on a band of frequencies. As shown, a band or range of frequencies 410 above the Nyquist rate is
 25 aliased to create a mirror image 412 within the system bandwidth. Significantly, the width of the bands 410 and 412 are identical. If the band 410 is 1 kHz wide, the band 412 will be 1 kHz wide. If it is assumed that the band 410 represents the frequencies produced by the VCO 214, then the width of the band 410 can be regarded as the phase noise (or equivalently, timing jitter) in F_{VCO} . In the conventional phase-locked loop of
 30 Fig. 1, the feedback divider would reduce the width of the band 410, effectively reducing loop gain and sensitivity. In the phase-locking circuit of Fig. 2, however, loop gain and sensitivity are preserved. The phase noise around F_{VCO} is aliased back into the system's bandwidth without compression or attenuation.

The use of aliased signals therefore allows the phase-locking circuit 200 to be operated at high gain (where F_{OUT} is much greater than F_{IN}) without the need for feedback dividers. It allows open loop gain and therefore precision to be kept high. Since feedback dividers are not required, the noise spurs normally introduced by these devices are avoided. Therefore, the need to slow down the loop filter and suffer the consequent reduction in programming speed is also avoided.

Fig. 5 shows another illustrative embodiment of phase-locking circuitry. A phase-locking circuit 500 includes a sampler 502, a phase detector 510, a loop filter 512, a controllable oscillator, such as a VCO 514, and a bank of bandpass filters 530. These are similar to the sampler 202, phase detector 210, loop filter 212, VCO 214, and bandpass bank of Fig. 2. However, the circuit 500 also includes a harmonic generator 540.

The harmonic generator 540 receives a filtered version of F_{VCO} and generates one or more harmonics of that signal. These harmonics, or overtones, have frequencies that are integer multiples of the frequency of F_{VCO} , i.e., the fundamental frequency.

A second bandpass bank 550 is optionally coupled to the output of the harmonic generator 540. The second bandpass bank 550 may be used to select one or more specific harmonics to be presented to the sampler 502. Selection of particular harmonics is not required, however.

The harmonic generator 540 effectively multiplies the width of noise bands fed back to the sampler 502. It therefore further increases open loop gain and sensitivity of the phase-locking circuit 500.

Fig. 6 is a frequency plot that shows the mechanism by which phase noise is multiplied. As shown, F_{VCO} and its harmonics create aliased images within the system's bandwidth. Significantly, a width of a band of phase noise around each harmonic of F_{VCO} can be seen to vary in proportion to the order of the harmonic. For example, the band of noise around the $3F_{VCO}$ is three times as wide as the band around F_{VCO} . Each of these bands is aliased back into the bandwidth of the system. Absent a bandpass bank 550, all of these aliased bands appear simultaneously at the input of the sampler 502.

The elements of the phase-locking circuits 200/500 can be implemented in a wide variety of ways. The phase detector 210/510 can be either an analog phase detector or a digital phase detector. Similarly, the loop filter 212/512 can be either an analog loop filter or a digital loop filter. Analog and digital phase detectors and loop filters are well-known in the art.

If an analog phase detector is used, the sampler 202/502 is implemented as an analog sampling circuit, such as a sample-and-hold circuit or a track-and-hold circuit. These devices are well-known and readily available off the shelf. In this arrangement, the input signal F_{IN} is preferably an analog signal, such as the output of a crystal oscillator.

If a digital phase detector is used, the sampler 202/502 preferably includes an analog sampling circuit (described above) coupled to an analog-to-digital converter (ADC). The analog sampling circuit and ADC are both clocked at F_S . Preferably, a sampling ADC is used, i.e., one which includes both an analog sampling circuit and an ADC in a single device package. Digital values are thus provided to the phase detector at a rate F_S . In this arrangement, F_{IN} is preferably a digital signal.

The VCO 214/514 is preferably a conventional type. VCOs are well-known and are commercially available off the shelf.

The harmonic generator 540 is preferably implemented as a non-linear analog circuit, such as a clipping circuit or a commercially available RF comb generator. As is known, clipping circuits flatten the positive and negative peaks of a sinusoid, thus introducing harmonics of the sinusoid's fundamental frequency. Optionally, the harmonic generator 540 may be equipped with an amplifier for boosting low amplitude harmonics.

Fig. 7 shows a largely digital embodiment of a phase-locking circuit 700 with a particular arrangement of elements. The circuit includes a digital phase detector 710 and a sampling ADC 712.

The digital phase detector 710 receives input data, F_{REF} , Φ_{REF} , which is indicative of a reference frequency and a reference phase. The digital phase detector 710 compares this reference frequency and phase with a sampled feedback signal from the sampling ADC 712 to produce a digital phase error. A digital loop filter 714 filters the digital phase error, and a digital-to-analog converter (DAC) converts the filtered phase error into an analog signal. An analog filter smoothes the output of the DAC 716, and a VCO 720 converts the smoothed DAC output into an oscillatory signal. A first bandpass filter bank 722, a harmonic generator 730, and an optional second bandpass bank 740 operate essentially as described above in connection with the first bandpass bank 530, the harmonic generator 540, and the optional second bandpass bank 550 of Fig. 5.

The digital loop filter 714 offers a particular advantage in the circuit 700. If any of the circuit elements, such as the ADC 712 or DAC 716, are found to repeatably

generate noise at known frequencies, or if noise at certain known frequencies is injected into circuit from its environment, the digital loop filter 714 can be programmed to have low gain, or a "zero," at each offending noise frequency. Designing the loop filter 714 in this fashion reduces noise in the output signal, F_{OUT} , and contributes to the overall

5 precision of the circuit.

Fig. 9 shows an example of a digital phase detector that is particularly suitable for the phase-locking circuit 700. As shown in Fig. 9, the first input of the digital phase detector is coupled to a digital oscillator 914, and the second input of the digital phase detector is coupled to a down-converter 910. Based upon the input data (F_{REF} , ϕ_{REF}), the digital oscillator 914 synthesizes a digital reference signal having frequency a F_{OSC} and a
10 phase ϕ_{OSC} . F_{OSC} is preferably equal to F_{REF} , and ϕ_{OSC} is preferably equal to ϕ_{REF} .

The digital reference signal is preferably a quadrature reference signal, i.e., it is provided in two parts that represent two sinusoids separated by a phase difference of 90-degrees. Conventionally, a first part of the quadrature reference signal is designated as a cosine and a second part is designated as a sine. Therefore, the first part of the
15 quadrature reference signal has the form $\cos(2\pi F_{OSC}t + \phi_{OSC})$ and the second part has the form $\sin(2\pi F_{OSC}t + \phi_{OSC})$.

The quadrature reference signal is provided to the down-converter 910, whereupon it is mixed with the feedback signal. Taking the digital phase detector out of
20 the context of the phase-locking circuit 700, the feedback signal can be regarded more generally as a sampled periodic signal having the form $\cos(2\pi F_{IN}t + \phi_{IN})$.

The down-converter 910 produces a difference signal in response to the sampled periodic signal and quadrature reference signal. The difference signal is preferably a quadrature signal having two parts: one part having substantially the form $\cos[2\pi (F_{IN} - F_{OSC})t + \phi_{IN} - \phi_{OSC}]$, and the other part having substantially the form $\sin[2\pi (F_{IN} - F_{OSC})t + \phi_{IN} - \phi_{OSC}]$. Therefore, the frequency of the quadrature difference signal equals the
25 difference between the input and oscillator frequencies, $F_{IN} - F_{OSC}$, and the phase of the quadrature difference signal equals the difference between the input and oscillator phases, $\phi_{IN} - \phi_{OSC}$.

30 The quadrature difference signal is provided to a phase extractor 916. The phase extractor 916 generates a cumulative phase difference represented by the quadrature difference signal. In the preferred embodiment, the phase extractor 916 performs an ATAN2 function. As is known, ATAN2 generates a 4-quadrant inverse tangent of a quotient of two inputs. Where the two inputs to ATAN2 are a sine and a cosine of the

same angle, θ , $\text{ATAN2}[\sin(\theta), \cos(\theta)]$ is simply the angle, θ . Therefore, ATAN2 of the two parts of the quadrature difference signal evaluates to $[2\pi (F_{\text{IN}} - F_{\text{OSC}})t + \varphi_{\text{IN}} - \varphi_{\text{OSC}}]$. This value corresponds to the cumulative phase difference between the output of the digital oscillator 914 and the sampled periodic signal. If F_{IN} , F_{OSC} , φ_{IN} and φ_{OSC} are constant, the values described by the cumulative phase difference take the form of a straight line over time.

In the context of the phase-locking circuit 700, the cumulative phase difference produced by the phase extractor 916 provides a digital phase error. Optionally, a phase φ_{ADJ} may be added to or subtracted from the cumulative phase difference, via a summer 920, to adjust the phase error passed to other components of the phase-locking circuit 700. Adding or subtracting phase via the summer 920 has the effect of shifting the phase of the synthesizer's output signal, F_{OUT} .

For the digital phase detector of Fig. 9 to perform properly, the digital oscillator 914 should be able to generate the quadrature reference signal with precision. For example, F_{OSC} should substantially equal the frequency specified by F_{REF} (nominally, F_{OSC} and F_{REF} are equal) and φ_{OSC} must substantially equal the phase specified by φ_{REF} (nominally, φ_{OSC} and φ_{REF} are equal). This requirement places significant demands on the digital oscillator 914, as it is required to produce precise values of the quadrature reference signal on the fly and at the requisite sampling rate.

This requirement can be achieved with relative ease if F_{OSC} and F_{S} are related, such that $K/F_{\text{OSC}} = L/F_{\text{S}}$, where K and L are both integers. In this case, the digital oscillator 914 can employ a look-up table for generating the quadrature reference signal. The look-up table associates pre-stored values of the quadrature reference signal with successive cycles of the sample clock. The digital oscillator can thus generate the quadrature reference signal simply by cycling through values stored its look-up table.

The situation becomes more complex, however, if K/F_{OSC} does not equal L/F_{S} . Under this circumstance, a simple look-up table cannot be used because the values that are proper for one iteration through the look-up table become improper for other iterations. A different solution is required. One solution is to provide the digital oscillator 914 with a computing engine for calculating values of the quadrature reference signal on the fly and at speed. However, this solution is complex.

Another solution is shown in Fig. 10, which shows another example of a suitable digital phase detector 710. The down-converter 1010, phase extractor 1016, and summer 1020 of Fig. 10 are substantially the same as the down-converter 910, phase extractor

916, and summer 920 of Fig. 9. However, Fig. 10 also includes a calculation unit 1012, an accumulator 1018, and a second summer 1022.

The calculation unit 1012 divides the input data (F_{REF} , ϕ_{REF}) into two parts, a primary part and a secondary part. The primary part (F_{OSC} , ϕ_{OSC}) represents an approximation of the reference signal (F_{REF} , ϕ_{REF}) that the digital oscillator 1014 can readily generate, such as by using a look-up table. The secondary part (ϕ_{RES}) represents a residual phase value, i.e., the error in the above approximation. The primary part preferably meets the requirement that $K/F_{OSC} = L/F_S$. If F_{OSC} does not equal F_{REF} , then as a matter of convention K and L are preferably selected such that F_{OSC} is slightly greater than F_{REF} . Therefore, the secondary part, ϕ_{RES} , represents the phase difference between F_{OSC} and F_{REF} that accrues over each cycle of F_S .

The accumulator 1018 accumulates (i.e., adds to its own contents) values of ϕ_{RES} on each cycle of F_S . The values held by the accumulator 1018, when viewed over time, thus take the form of a straight line.

The output of the phase extractor 1016 does not account for the secondary part of the input data. The summer 1022 corrects this output by subtracting the output of the accumulator 1018 from the output of the phase extractor 1016. The output of the summer 1022 thus accounts for both the primary and secondary parts of the input data, and produces an accurate representation of phase error between the sampled periodic signal and the reference (i.e., F_{REF} , ϕ_{REF}).

Certain elements of the digital phase detectors of Figs. 9 and 10, such as the ATAN2 function and the accumulator 1020, have logic definitions that are commercially available. These definitions may be purchased, downloaded, and embodied in an FPGA or ASIC with little original design work.

The reference data (F_{REF} , ϕ_{REF}) is preferably variable. When the digital phase detector of Figs. 9 or 10 is used in a synthesizer, the reference data is preferably programmable for establishing different output frequencies. The values of the integers K and L are preferably updated each time a new value of reference data is programmed. To minimize the size of the residue, K is preferably made as large as practicable. K and L may be computed manually, or may be generated by software, firmware, or hardware based upon the desired output frequency and the sampling rate.

Although they are not required, the digital phase detectors of Figs. 9 and 10 provide many benefits in the phase-locking circuit 700. For example, phase error is updated at a high frequency, such as once per cycle of the sample clock. In addition,

phase error is provided with exceedingly high resolution. Because the phase residue, ϕ_{RES} , is managed independently of the primary part of the reference frequency, a large number of bits of numerical precision can be applied to ϕ_{RES} . Also, the contribution of ϕ_{RES} to the overall phase error can be made exceedingly small by increasing the number of cycles of F_{OSC} (i.e., the value of K) that are stored in the look-up table used to implement the digital oscillator 1014.

Fig. 8 shows an application of phase-locking circuits of the types shown in Figs. 2, 5, and 7. As shown in Fig. 8, an automatic test system 812 is controlled by a host computer 810 for testing a UUT (unit under test) 840. The UUT may be any type of device or assembly to be tested. The automatic test system 812 includes instruments, such as an analog instrument 820, a digitizer 822, and an arbitrary waveform generator (AWG) 824. The automatic test system 812 also includes a plurality of digital electronic channels, shown generally as digital pins 826, 828, and 830. The digital electronic channels are arranged for sourcing and sensing digital signals.

Notably, the automatic test system 812 includes a plurality of phase-locking circuits 816a-g. These phase-locking circuits are of the same general type shown in any of Figs. 2, 5, and 7. The phase-locking circuits 816a-g each receive a clock signal, F_s , from a system clock 814. They each also receive respective input signals (or data) from the host computer 810 for specifying desired output frequencies and phases. In response to the clock and respective input, the phase-locking circuits 816a-g each generate a respective periodic output signal. The output signals are provided to the instruments 820, 822, and 824, which can use frequency references or clocks for their normal operation. The output signals also provide clocks for controlling the digital pins 826, 828, and 830. They may further be used to provide a frequency reference for a pattern generator 818. The pattern generator 818 operates in conjunction with the phase-locking circuits for causing the digital pins to source and/or sense digital signals with specified formatting and at precisely controlled instants of time.

Having described certain embodiments of the invention hereof, numerous alternative embodiments or variations can be made. For example, although phase-locking circuits shown and described preferably include a bank of bandpass filters (230, 530, and 722) coupled to the output of the VCO, these filters are not strictly required. In addition, although the bandpass filters are preferably implemented as analog filters that precede the sampler (202, 502) or the sampling ADC (712), they can alternatively be implemented as digital filters provided at the output of the sampler or sampling ADC.

A particular advantage of the phase-locking circuits disclosed is that they provide closed loop frequency gain without requiring frequency dividers (such as counters) in their feedback paths. This should not be taken to mean, however, that feedback dividers are prohibited. Certain instances may arise wherein feedback dividers are deemed
5 desirable in the context of the circuits disclosed. Aliasing will occur, even with feedback dividers, provided that the overall frequency gain (output frequency divided by input frequency) of the circuit path between the VCO and the sampler is greater than $F_s/2F_{\text{MIN}}$, where F_{MIN} represents the lowest frequency provided by the VCO.

The sampling rate F_s , with which the sampler (202, 502) or sampling ADC (712)
10 is operated, is preferably fixed. However, this is not required. It may also be variable. According to one variant, F_s may be derived from the output of the VCO.

As shown and described, the VCO is made to operate at frequencies higher than the Nyquist rate ($F_s/2$); however, this is not required, either. Aliasing can occur with VCO frequencies below the Nyquist rate if a harmonic generator (540, 730) produces
15 harmonics above the Nyquist rate.

Those skilled in the art will therefore understand that various changes in form and detail may be made to the embodiments disclosed herein without departing from the scope of the invention.

20 What is claimed is:

1. Phase-locking circuitry, comprising:
 - a sampler, having an input and an output, constructed and arranged for operating at a sampling rate F_S ;
 - a phase detector, having an input and an output, the input being coupled to the output of the sampler;
 - a controllable oscillator having an input and an output, the input being coupled to the output of the phase detector; and
 - a circuit path coupled from the output of the controllable oscillator to the input of the sampler, the circuit path being constructed and arranged to deliver a feedback signal to the sampler having a frequency greater than $F_S/2$.
2. Phase-locking circuitry as recited in claim 1, wherein the controllable oscillator is operable to generate an output signal having a frequency greater than $F_S/2$.
3. Phase-locking circuitry as recited in claim 1, wherein the circuit path comprises a bank of band-pass filters.
4. Phase-locking circuitry as recited in claim 3, wherein the bank of band-pass filters comprises a plurality of band-pass filters each having a different center frequency and each having a bandwidth less than $F_S/2$.
5. Phase-locking circuitry as recited in claim 1, wherein the input of the phase detector is a first input, and the phase detector further has a second input arranged for receiving an oscillatory analog signal.
6. Phase-locking circuitry as recited in claim 1, wherein the input of the phase detector is a first input, and the phase detector further has a second input arranged for receiving a digital value indicative of a desired output frequency.

7. Phase-locking circuitry as recited in claim 1, wherein the circuit path comprises a non-linear element constructed and arranged for generating at least one harmonic of a signal generated by the controllable oscillator.
8. Phase-locking circuitry as recited in claim 7, wherein the non-linear element is one of a clipping circuit and a frequency comb generator.
9. Phase-locking circuitry as recited in claim 7, wherein the circuit path further comprises a bank of selectable band-pass filters coupled between the output of the controllable oscillator and the non-linear element.
10. Phase-locking circuitry as recited in claim 1, further comprising a loop filter coupled between the output of the phase detector and the input of the controllable oscillator.
11. Phase-locking circuitry as recited in claim 10, wherein the loop filter comprises a digital loop filter.
12. A phase-locking circuit, comprising:
 - a sampler, having an input and an output;
 - a phase detector, having an input and an output, the input being coupled to the output of the sampler;
 - a controllable oscillator having an input and an output, the input being coupled to the output of the phase detector; and
 - a harmonic generator coupled between the output of the controllable oscillator and the input of the sampler.
13. A phase-locking circuit as recited in claim 12, further comprising a bank of band-pass filters coupled between the controllable oscillator and the harmonic generator.

14. A phase-locking circuit as recited in claim 13, wherein the bank of band-pass filters comprises a plurality of band-pass filters each having a different center frequency.
15. A phase-locking circuit as recited in claim 13, further comprising a bank of selectable band-pass filters coupled between the non-linear element and the sampler.
16. A phase-locking circuit as recited in claim 12, further comprising a bank of selectable band-pass filters coupled between the non-linear element and the sampler.
17. A phase-locking circuit as recited in claim 12, wherein the harmonic generator comprises a non-linear element.
18. A phase-locking circuit as recited in claim 12, wherein the sampler is operable at a sampling rate F_S , and the harmonic generator is constructed and arranged for generating at least one harmonic having a frequency greater than $F_S/2$.
19. Phase-locking circuitry, comprising:
- a sampler, having an input and an output, constructed and arranged for operating at a sampling rate F_S ;
 - a phase detector, having an input and an output, the input being coupled to the output of the sampler;
 - a controllable oscillator having an input and an output, the input being coupled to the output of the phase detector, the controllable oscillator being constructed and arranged for generating a range of operating frequencies greater than a minimum frequency F_{MIN} ; and
 - a circuit path coupled from the output of the controllable oscillator to the input of the phase detector and having a frequency gain greater than $F_S/2F_{MIN}$.
20. A method of phase-locking, comprising:

generating an oscillatory signal having a fundamental frequency, the oscillatory signal having at least one component with a frequency greater than $F_S/2$;

sampling the oscillatory signal at a sampling rate F_S to produce a sampled signal having at least one aliased component;

generating a phase error responsive to a difference between the sampled signal and a reference signal; and

varying the fundamental frequency of the oscillatory signal in response to the phase error.

21. A method as recited in claim 20, wherein the step of generating the oscillatory signal comprises:

generating a precursor of the oscillatory signal; and
band-pass filtering the precursor of the oscillatory signal.

22. A method as recited in claim 21, wherein the step of generating the oscillatory signal further comprises generating at least one harmonic of the band-pass filtered precursor of the oscillatory signal.

23. A method as recited in claim 20, wherein the step of generating the oscillatory signal comprises:

generating a precursor of the oscillatory signal; and
generating at least one harmonic of the precursor of the oscillatory signal.

24. A method as recited in claim 23, further comprising band-pass filtering the at least one harmonic of the precursor of the oscillatory signal.

25. A method as recited in claim 20, wherein the step of generating a phase error comprises:

generating a precursor of the phase error; and

filtering the precursor of the phase error.

26. A method as recited in claim 25, wherein the step of filtering the precursor of the phase error comprises digitally filtering the precursor of the phase error.

27. An automatic test system, comprising:

a host computer adapted for running a test program;

a plurality of phase-locking circuits, operative in response to data from the host computer, for producing a plurality of reference frequencies; and

a plurality of instruments, coupled to the plurality of phase-locking circuits and adapted for generating a stimulus signal and/or receiving a response signal responsive to the plurality of reference frequencies,

wherein each of the plurality of phase-locking circuits includes—

a sampler, having an input and an output, constructed and arranged for operating at a sampling rate F_s ;

a phase detector, having an input and an output, the input being coupled to the output of the sampler;

a controllable oscillator having an input and an output, the input being coupled to the output of the phase detector; and

a circuit path coupled from the output of the controllable oscillator to the input of the sampler, the circuit path being constructed and arranged to deliver a feedback signal to the sampler having a frequency greater than $F_s/2$.

28. An automatic test system as recited in claim 27, wherein the input of the phase detector is a first input, and the phase detector further has a second input for receiving data indicative of a desired output frequency.

29. An automatic test system as recited in claim 27, wherein the plurality of instruments comprises a digital drive circuit.

30. An automatic test system as recited in claim 27, wherein the plurality of instruments comprises an analog source.

31. An automatic test system as recited in claim 27, wherein the plurality of instruments comprise an RF source.

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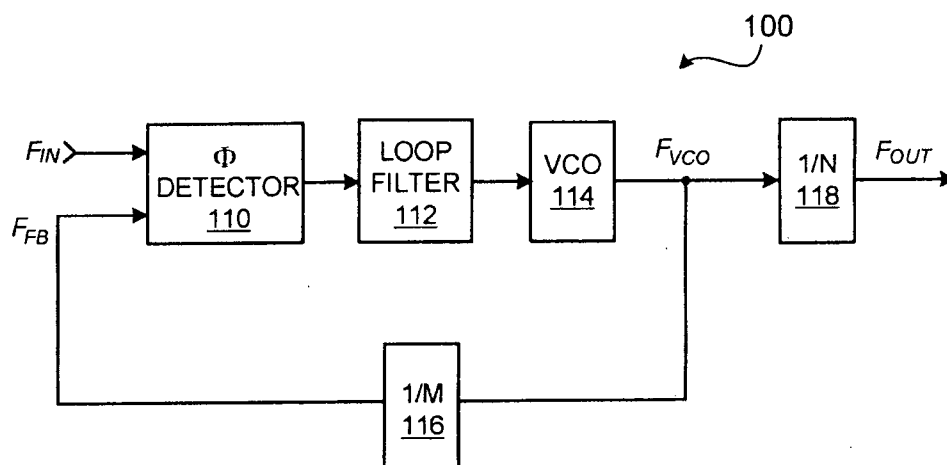
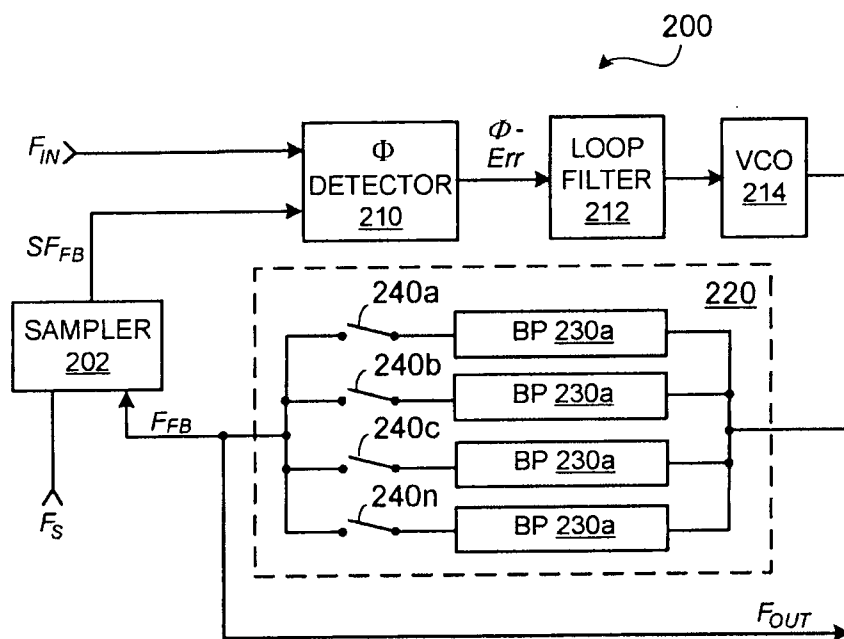
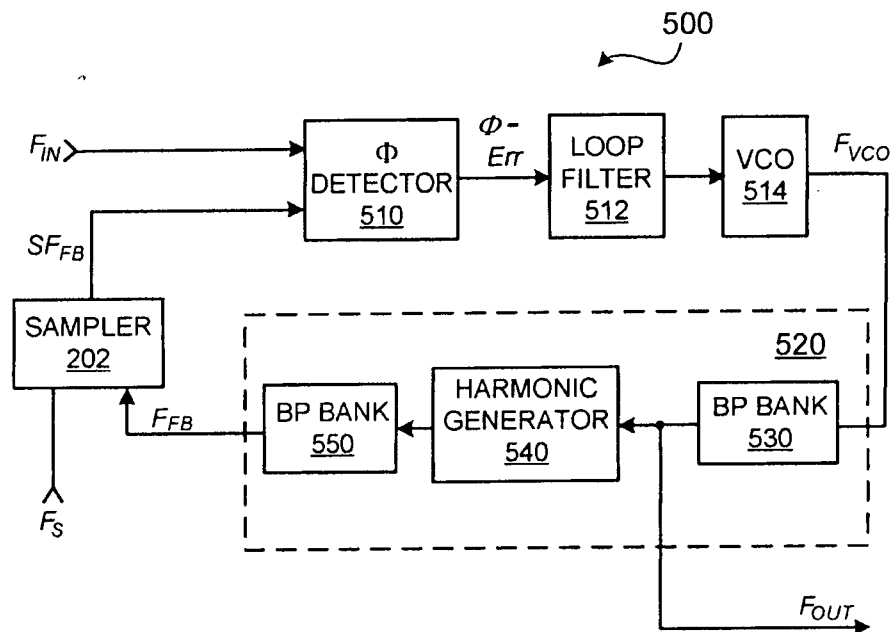
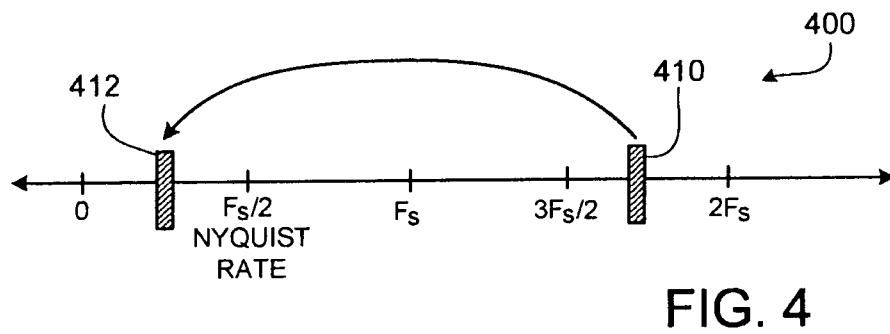
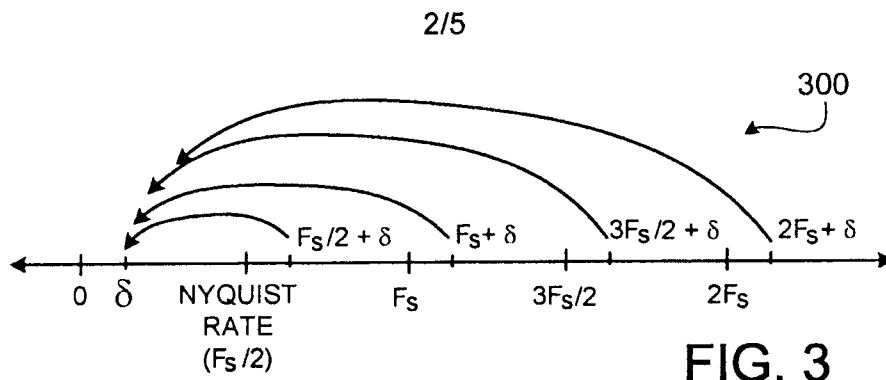
PRIOR ART
FIG. 1

FIG. 2



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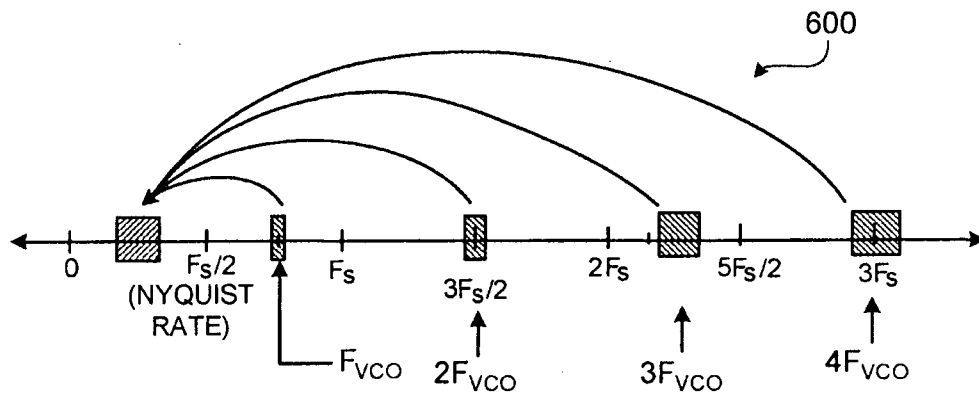


FIG. 6

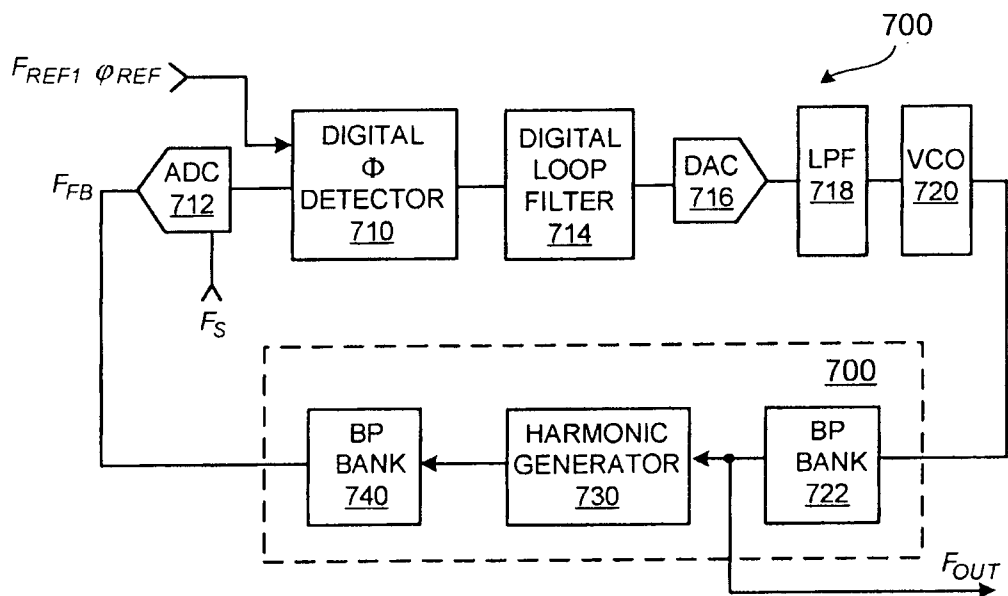


FIG. 7

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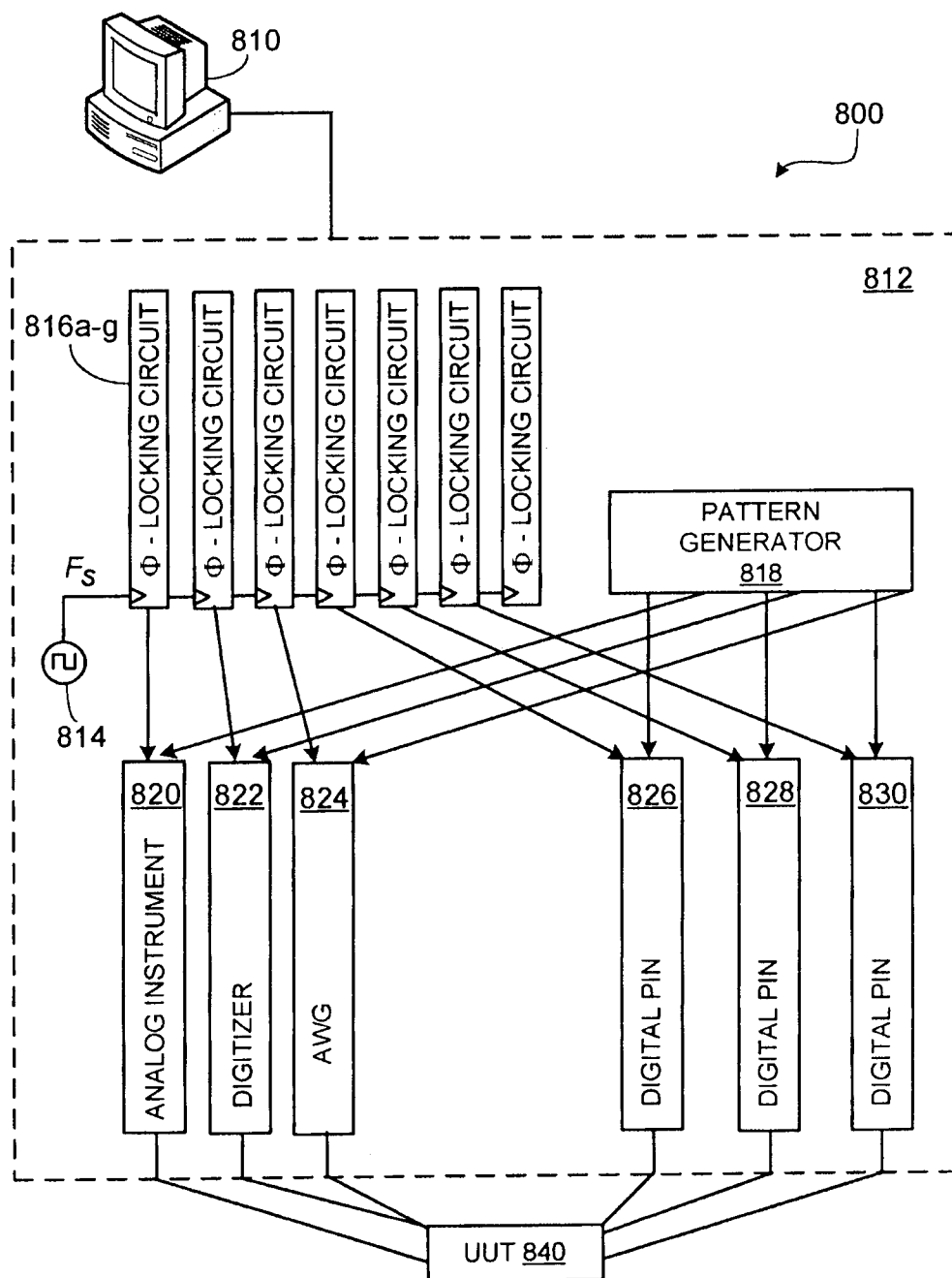
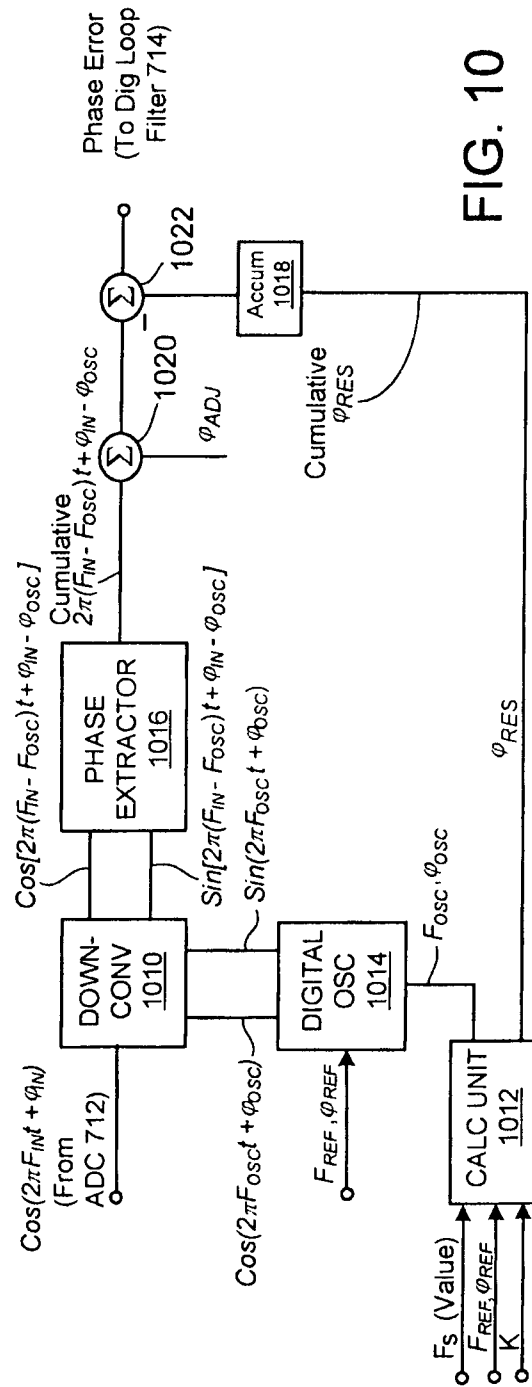
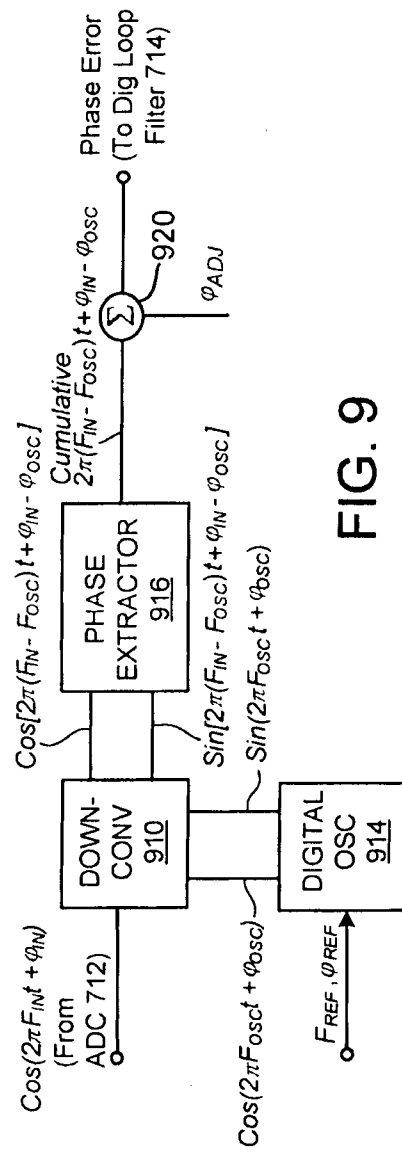


FIG. 8

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US07/74115

A. CLASSIFICATION OF SUBJECT MATTER

IPC: H03L 7/085(2006.01)

USPC: 331/1A,77

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 331/1A,77

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,068,628 A (Ghoshal) 26 Nov 1991 (26.11.1991), Figure, 1, 5, column 3, lines 1-5.	1,2,5-12,17-31

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Further documents are listed in the continuation of Box C.

☐

See patent family annex.

* Special categories of cited documents:		"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	
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"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

02 September 2008 (02.09.2008)

Date of mailing of the international search report

24 SEP 2008

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US07/74115

Continuation of B. FIELDS SEARCHED Item 3:
US-PGPUB, USPAT, EPO, JPO, DERWENT, IBM_TDB
search terms: phase lock oscillator, sample