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[54] **SAMPLE AND HOLD CIRCUIT FOR AN ELECTRIC ORGAN**

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[52] **U.S. Cl.**..... **84/1.01**, 84/DIG. 2, 84/DIG. 8, 84/DIG. 10, 84/DIG. 20

[51] **Int. Cl.**..... **G10h 1/00**, G10h 5/00

[58] **Field of Search** ..... 84/1.01, 1.03, 1.24, DIG. 2, 84/DIG. 8, DIG. 10, DIG. 20

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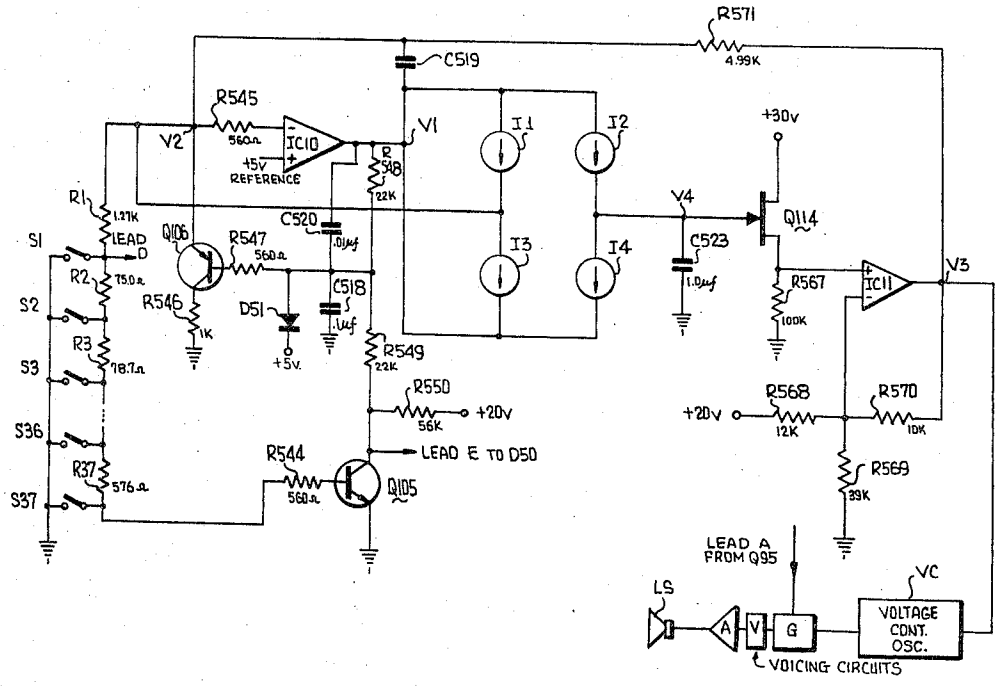
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[57] **ABSTRACT**

A sample and hold circuit for an electric organ, in which the voltage across a cascade or resistances, selected points of which may be grounded by key switches of an electric organ, is maintained at a fixed predetermined voltage by means of a feedback circuit and the voltage output of the feedback circuit is used to control the frequency of a voltage controlled tone signal oscillator, the value of the feedback voltage required being a function of the identity of the closed key switch which represents the highest note played, if plural key switches are closed.

18 Claims, 3 Drawing Figures



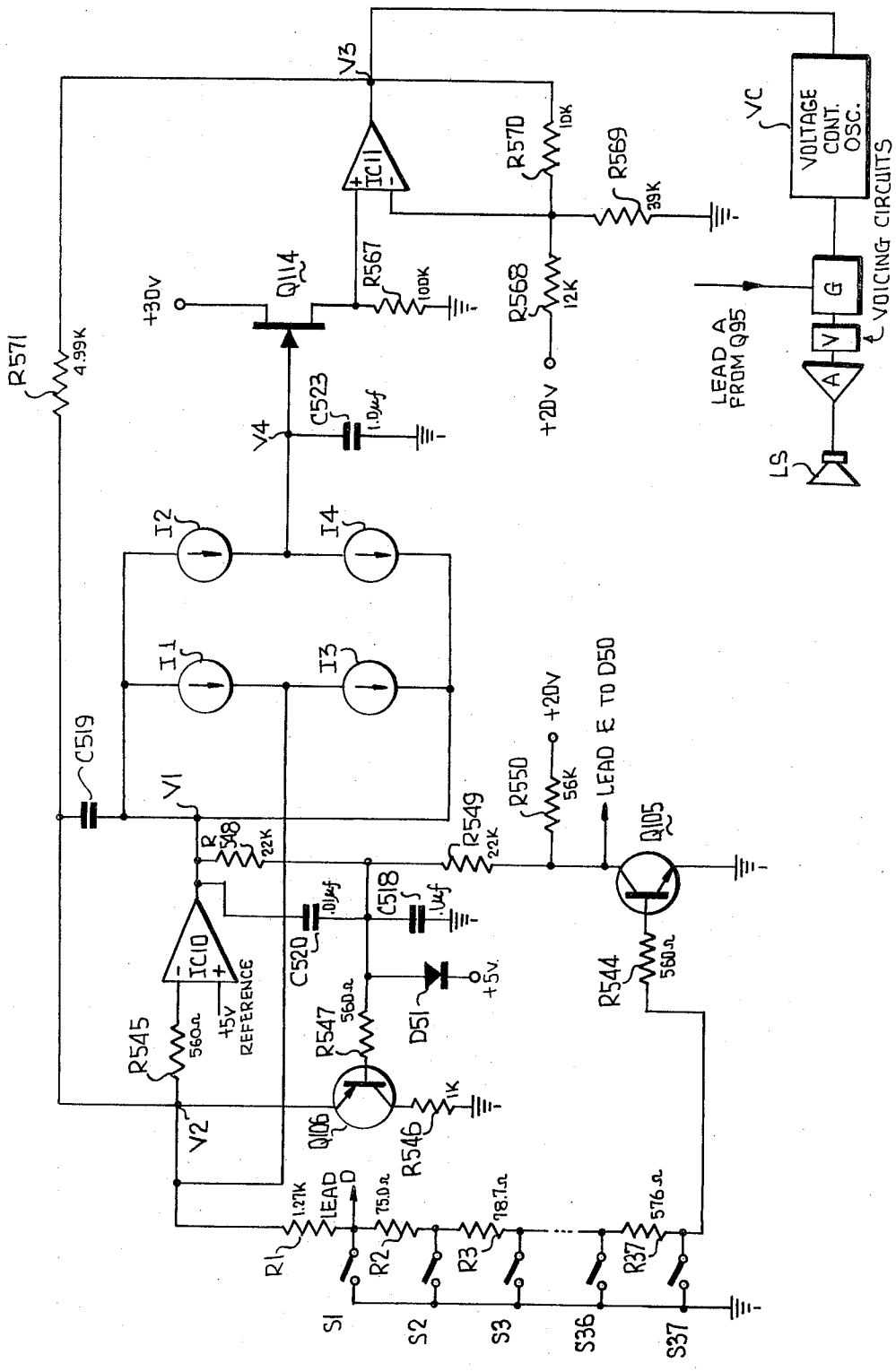

V3
IC11
R570
10K
R569
39K
VC
VOLTAGE CONT. OSC.
+30v
Q114
R567
100K
R568
12K
+20v
LEAD A FROM Q95
G
V
A
VOICING CIRCUITS
LS
R571
4.99K
V4
C523
1.0μf
I2
I4
I1
I3
C519
V1
R548
22K
R549
22K
R550
56K
+20v
LEAD E TO D50
Q105
C518
.1μf
C520
.01μf
IC10
+5V REFERENCE
R545
560Ω
R547
560Ω
D51
+5v.
R544
560Ω
Q106
R546
1K
V2
LEAD D
1.21K
R1
75.0Ω
R2
18.1Ω
R3
576Ω
R37
S1
S2
S3
S36
S37

FIG. 1

FIG.2

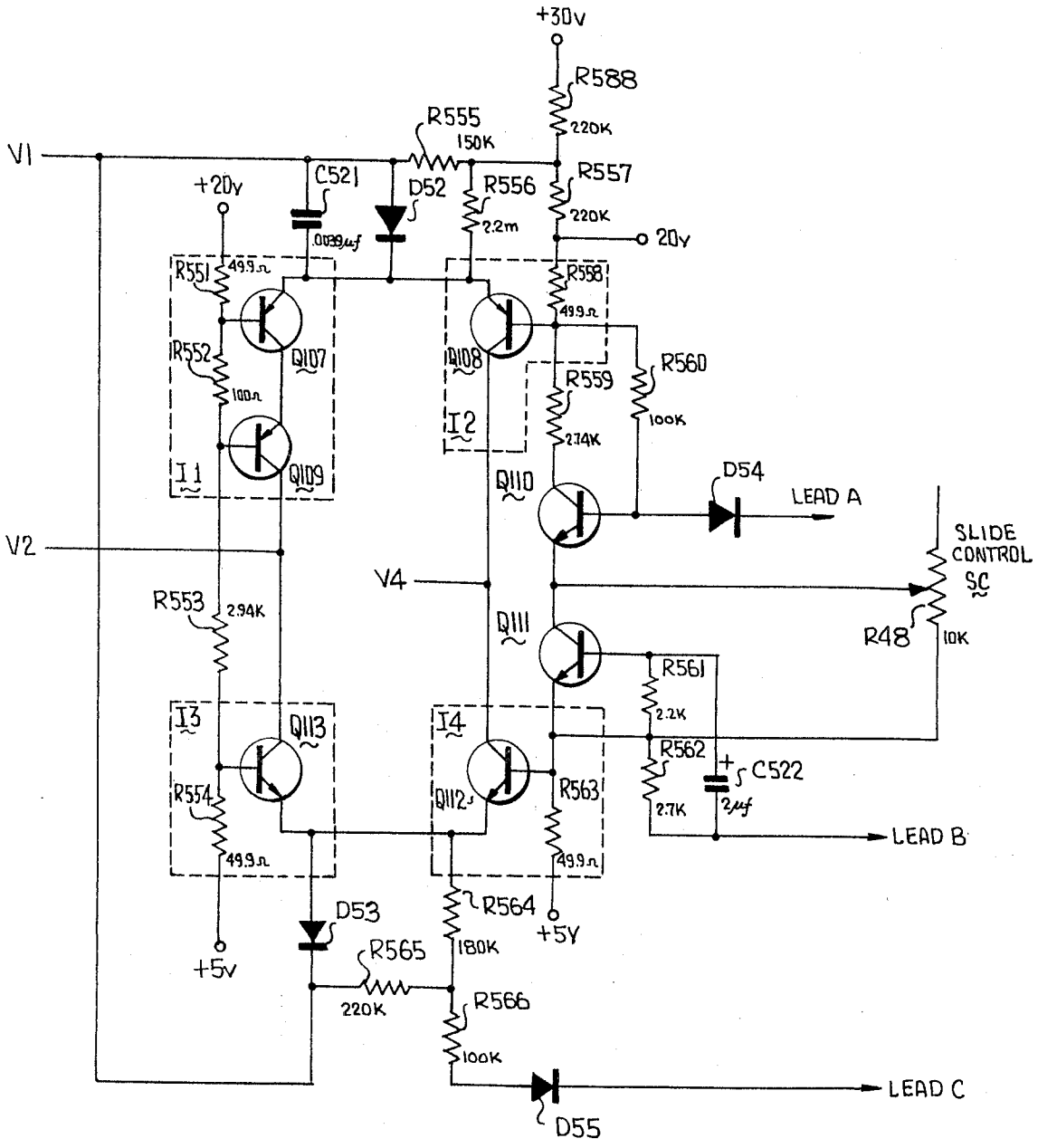
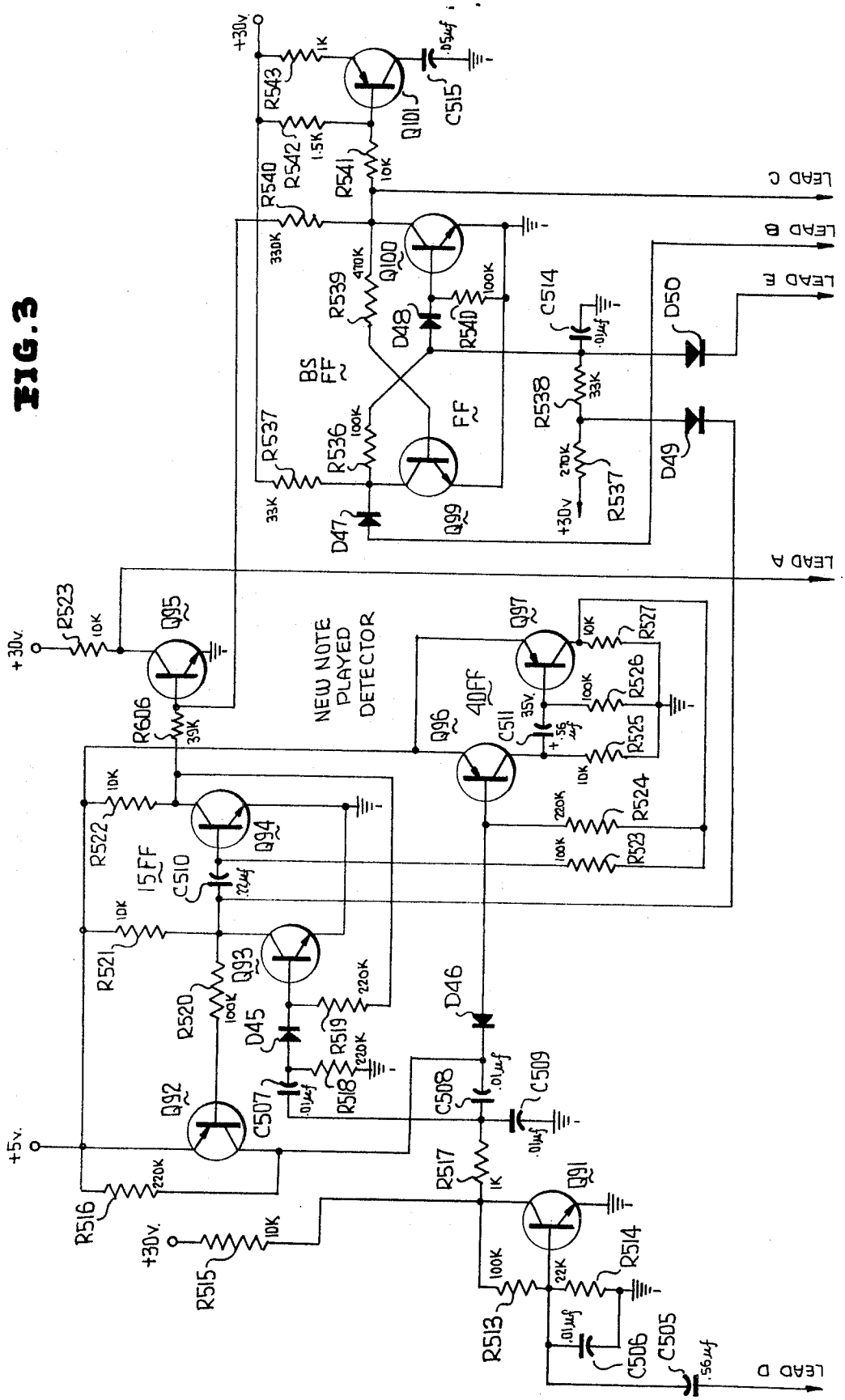

+30v
R588
220K
R555
150K
V1
+20v
C521
.0039μf
D52
R556
2.2m
R557
220K
20v
R551
49.9Ω
R552
100Ω
Q107
I1
Q109
Q108
I2
R558
49.9Ω
R559
2.74K
R560
100K
Q110
D54
LEAD A
V2
V4
SLIDE CONTROL
SC
R48
10K
R553
2.94K
Q111
R561
2.2K
I3
Q113
I4
Q112
R562
2.7K
C522
2μf
R554
49.9Ω
R563
49.9Ω
LEAD B
D53
R564
180K
+5v
+5v
R565
220K
R566
100K
LEAD C
D55

FIG. 3


+30v
R543
1K
Q101
C515
.05μf
R542
1.5K
R541
10K
R540
330K
Q100
R539
470K
100K
D48
R540
C514
.01μf
D50
LEAD C
LEAD B
LEAD E
BS FF
FF
R538
33K
R536
100K
R537
33K
Q99
D47
D49
+30v
270K
R537
LEAD A
+30v
R523
10K
Q95
R606
39K
NEW NOTE PLAYED DETECTOR
Q97
10K
R527
100K
R526
35V
C511
.56μf
R525
10K
Q96
40FF
R524
220K
R523
100K
10K
R522
Q94
15FF
C510
.22μf
10K
R521
Q93
R520
100K
220K
R519
D45
220K
R518
.01μf
C507
Q92
D46
C508
.01μf
C509
.01μf
+5v
220K
R516
+30v
10K
R515
R517
1K
Q91
100K
22K
R514
R513
.01μf
C506
C505
.56μf
LEAD D

SAMPLE AND HOLD CIRCUIT FOR AN ELECTRIC ORGAN

BACKGROUND

In the previous application for U.S. Pat., Ser. No. 263,649, filed June 16, 1972, in the name of David Bunger, assigned to the assignee of this application, there is disclosed a monophonic organic having provision for sounding only the highest note played, and for controlling the frequency of a single tone signal source in reponse to a voltage which is determined by that highest note played. The Bunger system includes a sample and hold circuit which is interposed between the source of control voltage which ultimately controls the tone signal source, and the voltage control terminal directly applied to that source for effecting frequency control. That sample and hold circuit must be precise, i.e., its output voltage must equal its input voltage. However, various diode drops occur in the sample and hold circuit, which must be compensated for. The diode drops, i.e., the voltage between base and emitter for a transistor, or the voltage across a diode, are temperature sensitive, and there occurs a failure of precise tracking as a function of temperature, which in turn results in imprecision of tuning.

The sample and hold system of the present application represents a solution to the problem of temperature dependence, but also eliminates inaccuracies of tuning which may result from variations of supply voltages, and of imprecision of amplifier gains, in that the output voltage of the system, representing a desired tone frequency, is controlled by a negative feedback loop extending around the entire sample and hold circuit, and in that the feedback loop is referenced to one fixed voltage.

SUMMARY OF THE INVENTION

A sample and hold circuit in a monophonic electric organ, in which organ keys control an array of resistances, and in which a negative feedback circuit extends from the output of the sample and hold circuit to the array of resistances and serves to maintain a point of the array of resistances at constant voltage regardless of the resistance to ground of the array.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic circuit diagram of an electric organ having a novel sample and hold circuit;

FIG. 2 is a schematic circuit diagram of elements of the circuitry of FIG. 1 which are shown schematically in FIG. 1; and

FIG. 3 is a schematic circuit diagram of control devices for controlling operation of the circuitry of FIGS. 1 and 2.

DETAILED DESCRIPTION

The system can be divided into three sections. The first is called the sample and hold section, and provides a voltage that corresponds to the key being played, or, if no keys are presently being played, to the last key that was played. This circuit has the ability to change voltages quickly or slowly depending upon the setting of a slide control. FIG. 1 is a simplified schematic of the sample and hold circuit and will be used to describe its operation.

FIG. 1 contains integrated circuits IC10 and IC11 which are operational amplifiers. The current sources I1 through I4 which are constructed with transistors and resistors are described in detail subsequently. The current sources are under the control of the voltage V1. When the voltage V1 is below 5 volts, current sources I3 and I4 are turned on. When the voltage V1 is between 5 volts and 20 volts, all four current sources are essentially turned off (open circuit). When the voltage V1 is above 20 volts, current sources I1 and I2 are turned on. In addition to providing an "On" — "Off" control, the voltage V1 determines the magnitude of these current sources. The ratio of I2 to I1 when these current sources are turned on is equal to the ratio of I4 to I3 when these current sources are turned on.

The operation of the sample and hold under various conditions is as follows. With any switch closed, transistor Q105 is turned off which allows D51 to become forward biased through R549 and R550 if V1 does not fall below 0.8 volt. This condition on V1 is always satisfied. Transistor Q106 is off because its emitter is held at 5 volts and its base is a diode drop above that voltage. These two transistors are now essentially out of the circuit.

The desired output voltage V3 with any key switch closed is the value that will cause the voltage V2 to be 5 volts. The voltage V2 is determined by the resistors voltage divider consisting of R571 and all switch resistors from R1 to the resistor immediately preceding the switch that is closed, and the output voltage V3. For example, with switch S3 closed and I1 through I4 equal to zero, which occurs while V1 is between 20 and 5 volts, the voltage V2 will be related to the output voltage by the following expression:

$$V2 = V3\,(R1 + R2 + R3/R1 + R2 + R571) \quad (1)$$

Since the desired value of V3 is that which results in V2 equal to 5 volts the following expression gives its value:

$$V3\ (S3\ \text{closed}) = 5\ (R1 + R2 + R3 + R571/R1 + R2 + R3) \quad (2)$$

If prior to the closing of switch S3, the output voltage V3 is higher than the desired value as defined by equation (2), equation (1) indicates that the voltage V2 will be higher than 5 volts. The voltage V2, however, will be prevented from rising by I3. For a very small increase in V2, V1 will fall below 5 volts and turn on current source I3 which will provide a shunt path around the switch resistors to lower V2. This negative feedback will cause V2 to assume the value that will maintain the current source I3 at the proper level. The above description uses the fact that if the positive (+) and negative (−) inputs of the operational amplifier are at the same voltage, the output voltage is 15 volts. Therefore, to maintain V1 below 5 volts, the negative input of the operational amplifier must be at a higher voltage than the positive input. Since the required change in voltage from nominal at V1 is 10 volts (15–5), the voltage difference required between the positive and negative inputs must be this voltage divided by the gain of the operational amplifier. This gain is infinity in theory and in practice is typically above 100,000. This results in a required voltage difference between the operational amplifier inputs of

$$\Delta v = (10\ \text{volts}/100{,}000) = 0.0001\ \text{volt}$$

This voltage Δv is called the differential input voltage and is added to the voltage at the positive input terminal to obtain the voltage V2, i.e., V2 = 5 volts + 0.0001

volts = 5.001 volts. The small value of this differential input voltage implies that for practical purposes, the differential voltage is zero and both terminals are at the same voltage. This assumption remains true whenever negative feedback like that provided by I3 is present.

The initial value of the current source I3 is now calculable because the value of V2 has been determined to be +5 volts. The current through R571 is known because its value is specified and the voltage across it is known. Likewise the current through the switch resistors is known and I3 must be the difference between these two.

$$I3 = (V3 - V2)/R571 - V2/(R1 + R2 + R3) \quad (3)$$

Since V2 = 5 volts,

$$I3 = [(V3 - 5)/R571 = [5/(R1 - 2 + R3)] \quad (4)$$

Equations (2) to (4) show that I3 equals zero if V3 is at the desired voltage and that I3 is dependent upon the difference between the actual value of the output voltage and the desired value. Current source I4 is dependent upon I3. Its value therefore also depends upon this error voltage. Current source I4 discharges capacitor C523 whose voltage is amplified by transistor Q114 and IC11 to become the output voltage V3. The output voltage V3, therefore, begins to fall and approaches the desired value. As the voltage V3 approaches the desired value, I3 and I4 are reduced which slows the discharge of C523. When the output voltage V3 reaches the desired value, both current sources are turned off and the discharge of C523 stops. The speed with which this process takes place is determined by the ratio of current source I4 to I3. This ratio is determined by the position of slide control SC and therefore is set by the operator. If this ratio is large, I4 is large and the output voltage converges quickly to the desired value. If, however, this ratio is small the output voltage converges slowly to the desired value. This voltage change has the same transient characteristics as a series RC combination (exponential) due to the feedback provided by I3 and I4.

If the output voltage is lower than the desired value before the switch is closed, or if a switch with a lower index number is closed after the output voltage has settled to the desired value, the system will correct itself in a similar manner. For these circumstances, however, V2 will attempt to be lower than 5 volts, which will force V1 above 20 volts, thereby turning on current sources I1 and I2. Current source I1 provides the negative feedback to control IC10 and corresponds to I3 in the previous discussion. Current source I2 provides charging current for capacitor C523 to allow the output voltage to reach the desired value, and corresponds to I4 in the previous discussion.

The above description may be said to be of the transient portions of the sample mode. After the transient portion is complete, which indicates that the output voltage is at the desired value for the particular switch closed, the system continues to maintain the correct output level. Any noise, leakage currents, or other disturbances that attempt to change the output level will appear at V2 and adjust V1 to turn on the proper current source so that the proper correction can be made. Thus, while a key is being held, V1 can be at any voltage between 5 and 20 volts. Capacitor C519 provides additional negative feedback from V1 to V2 which slows the rate of voltage change at V1. This is necessary to both protect against large noise spikes and to protect against noise from the key switches during opening and closing operations.

When all key switches are released it is necessary that the sample and hold circuit be transferred into the hold mode. This is accomplished by using the 5 volts at V2 through all key switch resistors connected in series to saturate Q105. With all key switches open the output voltage V3 would, unless prevented by control circuits, fall to a lower voltage than with any key switch closed. The voltage at V1 would fall and attempt to turn on I3 and I4. However, with Q105 saturated, when the voltage at V1 is equal to 10 volts transistor Q106 turns on via R548 and provides negative feedback to V2, which will hold V1 at 10 volts. With V1 at 10 volts all current sources I1 through I4 are zero and there exists no charging or discharging current for C523. The output voltage therefore remains at the value corresponding to the last key played. The hold time is determined by the ability of capacitor C523 to hold charge, which explains the need for the buffer amplifier consisting of Q114 and IC11. This amplifier has a DC gain of 2 with respect to 15 volts which means that a voltage of 18 volts at the positive terminal of IC11 will produce an output voltage of 21 volts. This gain reduces the voltage swing required at capacitor C523 to produce a given voltage range at the output. Resistors R568 and R569 provide the resistor divider necessary to supply an effective 15 volts with a 10K impedance to the junction of R570 and the negative input of IC11, which is required to give the amplifier this gain. Resistor R567 provides bias current for transistor Q114 and resistors R545, R547, R546 and R544 are current limiting resistors, which prevent destruction of their associated active components under accidental short circuit conditions. Capacitors C518 and C520 provide additional noise and switch bounce protection.

All modes of operation of the sample and hold circuit depend upon the operation of the four current sources I1 through I4. FIG. 2 is a schematic circuit diagram of these. The sections of this schematic that are labelled I1 through I4 are the actual current sources. The other components are part of all or several of the current sources and cannot be associated with any individual current source. The series combination of R551, R552, R553 and R554, which is connected between 20 volts and 5 volts, forms a bias network for transistors Q107, Q109 and Q113. The current through this divider chain is determined primarily by R553 because this resistor is much larger than the others in the chain. This current creates a voltage drop across R551 and R554 which establishes the base of Q107 a small amount below 20 volts (approximately 250 millivolts) and establishes the base of Q113 the same amount above 5 volts. The voltages at the bases of transistors Q108 and Q112 are established in a similar manner with the exceptions that, when Q110 is saturated and Q111 is off, which are their normal states, resistor R559 in series with the slide control potentiometer R48 determines the current. If the slide control R48 is adjusted such that the currents through both resistor divider chains are equal, the voltages at the bases of Q107 and Q108 will be equal since R551 is equal to R558. Under these conditions the base voltages of transistors Q112 and Q113 are also equal due to the equality of R554 and R563. As V1 rises above 20 volts the emitters of Q107 and Q108 also rise and these transistors turn on. These transistors are selected such that their base emitter voltages are

matched, which means that if the base emitter voltages are equal the collector currents are also equal. Since in the present discussion the base voltages are equal and the emitters are connected together, the collector currents must be equal and the ratio of I2 to I1 is unity. If the voltage V1 falls below 20 volts, transistors Q107 and Q108 are turned off because their base emitter junctions are reverse biased. For any voltage at V1 between 20 volts and 5 volts, Q113 and Q112 are off. When V1 falls below 5 volts, however, the base emitter junctions of these transistors are forward biased and they turn on. Since their bases are at the same voltage and their emitters are connected together, the collector currents are equal and the ratio of I4 to I3 is also unity.

If the slide control is adjusted so that the current determined by it is less than the current determined by R553, the voltage at the base of Q108 will be higher than the voltage at the base of Q107. Therefore, when these transistors are turned on, the reduced base emitter voltage of Q108, will cause its collector current to be less than that of Q107, and the ratio of I2 to I1 will be less than unity. Under these conditions, the base voltage of Q112 will be less than the voltage at the base of Q113. Therefore, when these transistors are turned on, the collector current of Q112 is less than the collector current of Q113 and the ratio of I4 to I3 will also be less than unity. Similar logic explains that if the slide control is adjusted such that the current determined by it is larger than the current through R553, the ratios of the current sources I2 to I1 and I4 to I3 are greater than unity. Since transistor current increases exponentially with base emitter voltage, V1 is never required to either rise much higher than 20 volts or fall much below 5 volts to produce the required currents.

Diodes D52 and D53 prevent base emitter reverse breakdown in their associated current sources when these current sources are off. Transistor Q109 maintains the operating condition of low collector emitter voltage for Q107 so that its characteristics of operations agree with those of Q113. Resistors R555, R556, R557, R588, R565, R564, R566, capacitors C521 and diode D55 provide bias for these current sources which improve stability of the system. They allow current sources I1 and I2 to remain on at an extremely low level with V1 between 20 volts and 15 volts, and they allow I3 and I4 to be on at an extremely low level with V1 between 15 volts and 5 volts. In previous discussions it was stated that all current sources were zero when V1 was between 5 volts and 20 volts. The current level of the current sources due to this bias current is much less than the current level when V1 is below 5 volts or above 20 volts and, therefore, for functional discussions, it was assumed to be zero. The cathode of D55 is at ground when in the sample mode and at 30 volts when in the hold mode. This switching is required so that the bias current provided by R564 and R566 is removed from the hold mode in which V1 is held at 10 volts.

The remaining components shown in FIG. 2 provide important switching controls. Q110 is saturated through R560 when the cathode of diode D54 is above 5 volts. In this mode the base bias of Q108 and Q112 is determined as described above. If, however, the cathode of D54 falls to zero volts, Q110 is turned off and the current that determines the bias voltages for the current sources I2 and I4 is reduced to zero. This creates a large difference in base emitter voltages for Q107 and Q108 and for Q113 and Q112 which essentially causes I2 and I4 to be zero. Under these conditions I1 or I3 can be turned on and therefore control IC10 of the sample and hold (FIG. 1) without changing the output voltage. Transistor Q111 is normally off which allows the slide control to determine the bias current. When no keys are played, the junction of R562 and C522 is held at ground potential by Q99 (FIG. 3), and a voltage of approximately 5 volts is developed across C522. When the first key is played, the junction of R562 and C522 is disconnected from ground by the turning off of Q99. Capacitor C522 discharges through the base emitter of Q111 and resistors R561 and R562 thereby saturating Q111 and shorting across the slide control potentiometer. Under these conditions, the base bias current for Q108 and Q112 is its largest value which makes the ratio of I2 to I1 and of I4 to I3 the largest value. Transistor Q111 will remain saturated for a time determined by the time constant of C522 and R562 after which it will turn off and allow the slide control to again determine the current sources ratio. Transistor Q111, therefore, provides control to revert to the fastest slide rate when the first key is played and then return to the slide rate determined by the slide control potentiometer for other keys that are added.

The remaining circuitry associated with the sample and hold consists of detection and timing circuits. Since the system plays only the highest note called for, it would be possible, due to plural switches not closing at exactly the same time, to jump from one frequency to another when a chord is played. This problem is corrected by the detection of any change in the number of keys played and the introduction of a delay period during which the output of the sample and hold circuit does not change. The required information is available at the junction of R1 and R2 (FIG. 1). Since the negative input of IC10, which is connected to the key switch resistor R1, is always at 5 volts, the voltage at the junction of R1 and R2 will depend upon the highest note (lowest switch number) played. When no keys are played this voltage is at its highest value. When any key is played, therefore, this voltage is lowered. If a higher key is now played (lower switch number) the voltage at this junction will be lowered even further. If this higher key is now released, the voltage will be increased. The voltage at this junction, therefore, has a negative transient when the first key is played and whenever a higher key is played. It also has a positive transient whenever a higher key is released, which allows a lower key to control the frequency, or whenever the last key played is released. These transients are used to trigger the delay circuits as follows: Transistors Q93 and Q94 form a 15 millisecond monostable flip-flop 15FF which can be triggered by a positive pulse through capacitor C507 and diode D45. Transistors Q96 and Q97 form a 40 millisecond monostable flip-flop 40FF which can be triggered by a negative pulse through capacitor C508 and diode D46. In addition to these Q99 and Q100 form a bistable flip-flop FF which distinguishes between no keys played and one or more keys played.

The combined switching process of all of these sections will now be examined. When no keys are played, Q105 (FIG. 1) is saturated which prevents Q100 in the bistable flip-flop FF from being turned on by grounding the anode of diode D50. This flip-flop is therefore set with Q99 on and Q100 off. This provides current

through R540 to hold Q95 on, and Q101 off. Diode D47 and saturated transistor Q99 allow capacitor C522 in the sample and hold circuit to charge up as described earlier. The other flip-flops are in their normal state. This provides current through R523 to hold Q94 on, and Q93 off which forces Q92 off. The collector of Q95 controls the on and off conditions of Q110 in the sample and hold circuit which was described earlier, and provides a trigger for the signal gates on lead A. When the key corresponding to switch S37 is played, a negative transient appears at the junction of R1 and R2. This transient is amplified and inverted by Q91 and associated components, and appears at its collector as a positive transient. This signal, due to its polarity, is blocked by D46 but is passed by D45 and saturates Q93. The saturation of Q93 transfers a negative pulse to the base of Q94 which forces this transistor out of saturation. The collector of Q94 now supplies current through R519 to the base of Q93. This positive feedback causes the flip-flop to latch up with Q93 on and Q94 off until the base of Q94 recovers through R523. While Q93 is on, Q92 is also on which places the cathode of D46 at 5 volts to prevent any noise from being passed by this diode. The closing of switch S37 also turns Q105 off, and therefore the bistable flip-flop can change states if triggered. The trigger required, however, comes from the +30 volts through R537 and R538 if diode D49 does not prevent it. This diode is connected to the collector of Q93, and when the transistor is saturated, as is now the case, the trigger is shorted to ground. After the bsae of Q94 recovers, this transistor saturates, which turns off Q93 and allows the current through R537 and R538 to change the state of the bistable flip-flop. Therefore Q99 turns off and capacitor C522 discharges through Q110 to short the slide control potentiometer SC. Transistor Q100 turns on, which turns on Q101 to provide a dc control voltage. Transistor Q100 also provides forward bias for D55. With Q94 and Q100 saturated, Q95 will turn off and allow the sample and hold to change voltage by providing reverse bias to D54. The collector of Q95 also supplies the information to the signal gate G in the circuit between voltage controlled oscillator VC and amplifier A and loudspeaker LS, and at this time the note will sound.

If switch S1 is now closed, another positive pulse will appear at the collector of Q91 and the 15 millisecond monostable flip-flop 15FF will again be triggered. Transistor Q95 will be saturated for 15 milliseconds which will remove the trigger "hold" mode and the state of the bistable flip-flop FF is changed. Transistor Q100 is turned off through diode D50 and the saturated transistor Q105. This supplies current through R540 to keep Q95 saturated after the 40 millisecond monostable 40FF has re-set, and it turns off Q101. Transistor Q99 is saturated which allows capacitor C522 to charge up so that when the next note is played the slide control can be shorted.

The output voltage V3 of the sample and hold circuit is applied to the voltage controlled oscillator VC. The voltage controlled oscillator basic circuitry is substantially the same as that disclosed in David A. Bunger's U.S. patent application, Ser. No. 213,939, filed Dec. 30, 1971, assigned to the assignee of this application, so that a detailed description is not required herein. This oscillator provides a square wave signal whose frequency depends upon the output voltage of the sample and hold circuit. This signal is applied to gate G and, when the proper gating signal is at the collector of Q95, is transferred to the voicing circuits V, amplifier A and loudspeaker LS.

What is claimed:

1. An electric organ, comprising a resistance, an array of keys of said organ, means responsive to actuation of selected keys of said array of keys for grounding selected parts of said resistance, said resistance having a preselected variable voltage ungrounded point of reference, means including a feedback circuit for maintaining the voltage of said preselected point of reference constant when any of said keys is actuated by feeding back current through said resistance in amplitude sufficient to maintain said voltage of said preselected point of reference constant, said feedback circuit including a storage capacitor shunt connected to ground at a location between said point of reference and a load point, a feedback resistance connected between said load point and said point of reference, and a voltage tone signal oscillator responsive to the voltage of said load point.

2. The combination according to claim 1, wherein is included a voltage comparator having a fixed reference input voltage and a variable input voltage terminal, means connecting said variable input voltage terminal to said point of reference, said voltage comparator having an output terminal connected to control voltage across said storage capacitor.

3. The combination according to claim 2, wherein is included an auxiliary feedback loop connected between said voltage comparator output terminal and said point of reference, said auxiliary feedback loop including current sources for supplying current to and draining current from said point of reference.

4. The combination according to claim 3, wherein is included means responsive to the voltage at said point of reference for supplying current to and draining current from said storage capacitor.

5. An electric organ, comprising an array of key switches, an adjustable resistance, means responsive to said key switches for adjusting the value of said adjustable resistance, amplifying means having its input connected to a preselected point of said resistance and having an output point, a resistive feedback loop extending from said output point to said preselected point, a source of reference voltage, means for developing an input error signal for said amplifier as the difference of said reference voltage and the voltage of said preselected point, a voltage controlled tone signal source connected to said output point, and means for acoustically transducing the signal output of said tone signal source.

6. The combination according to claim 5, wherein said amplifier includes a capacitive memory for sustaining the output of said amplifier.

7. An electric organ having a keyboard, a string of series connected resistances, means respnsive to selective actuation of keys of said keyboard for connecting to a point of reference potential selected junctions of said resistances, whereby said string of resistances has a total resistance which is a function of location of that selective junction which is farthest removed from said point of reference potential, a source of reference voltage, and means for injecting current into said string of resistances of magnitude selected to cause the voltage across said string of resistances substantially to equal

the voltage of said source of reference voltage for any selective actuations of said keys, a voltage controlled tone signal oscillator operative to generate a tone frequency as a function of a control voltage, means responsive to said means for injecting current for applying said control voltage to said voltage controlled oscillator, wherein is provided a voltage comparator for comparing said reference voltage with said voltage across said string of resistances, said voltage comparator having an output terminal, means responsive to the voltage at said output terminal for controlling said means for injecting current.

8. The combination according to claim **7,** wherein said last means includes a feedback path connected between said output terminal of said voltage comparator and said string of resistances.

9. The combination according to claim **9,** wherein said last means includes a further feedback circuit directly responsive to said control voltage for feeding back voltage to said string of resistances.

10. The combination according to claim **9** including a storage capacitor having a charge responsive to said voltage of said output terminal of said voltage comparator, and means for controlling the rate of change of said charge in response to a change of current flow into said string of resistances.

11. An electric organ, comprising an array of key switches, an adjacent resistance, means responsive to selective actuation of said key switches for adjusting the value of said adjustable resistance as a function of the selective actuation of said key switches, a voltage comparator having a reference input terminal and a variable input terminal, means applying a fixed voltage to said reference input terminal, means connecting a point of variable resistance to said varaible input terminal, said voltage comparator having an output terminal, a loop having a first section extending from said output terminal to a load terminal and a second section extending from said load terminal to said variable input terminal, said loop being arranged to tend to maintain the voltage at said variable input terminal equal to the voltage at said reference input terminal for any selective actuations of said keys, a voltage controlled tone signal oscillator connected to said load terminal, and means for acoustically transducting the signal output of said tone signal oscillator.

12. The combination according to claim **11,** wherein said first section includes a storage capacitor connected between a point of said first section and a point of reference potential, and an amplifier extending from said storage capacitor to said load terminal.

13. The combination according to claim **12,** wherein said adjustable resistance is a series of resistances connected in series, and wherein said key switches are respectively connected between the junctions of said series of resistances and a point of reference potential.

14. The combination according to claim **13,** wherein said points of reference potential are ground.

15. The combination according to claim **13,** wherein are provided four two terminal current sources, I_1, I_2, I_3, I_4, means connecting said current sources I_1, I_3 in series with each other, means connecting said current sources I_2I_4 in series with each other and in parallel with said current sources I_1, I_3, means connecting said adjustable resistances to the junction of said current sources I_1I_3, means connecting the junction of said current sources I_2) I_4 to said storage capacitor, means connecting the output terminal of said voltage comparator jointly to the unjoined terminals of all said current sources, said current sources I_1 and I_3 providing current flow in series with each other in the same sense and said current sources I_2 and I_4 providing current flow in series with each other in the same sense, and said current sources being responsive to the voltage at said junctions for controlling the relative amplitudes of current flowing through said current sources.

16. An electric organ, comprising a series connected array of resistances connected to a reference point, key switches for at will connecting junctions of said resistances to ground, a comparison circuit responsive to the voltage of said reference point and to a fixed reference voltage for generating an error signal, a memory capacitor, current charge and discharge means responsive to said error signal for respectively increasing and decreasing the charge in said capacitor, an output terminal, means respnsive to the voltage across said capacitor for applying an amplified version of said voltage across said capacitor to said output terminal, a resistive feedback circuit extending from said output terminal to said reference point, a voltage controlled tone signal oscillator conected to said output terminal and responsive to the voltage of said output terminal to generate tone frequency signals of variable frequency, and means for acoustically transducing said tone frequency signals.

17. The combination according to claim **16,** wherein is included means responsive to opening of all said key switches for disabling said means for respectively increasing and decreasing said charge in said capacitor.

18. The combination according to claim **17,** wherein is included means for controlling the rate of change of charge of said capacitor by said current increasing and decreasing means in response to opening or closure of any of said key switches.

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