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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95054 (US).

(72) Inventors: **GUO, Xin**; 6105 Castleknoll Drive, San Jose, CA 95129 (US). **ZHU, Feng**; 2852 Lexford Ave, San Jose, CA 95124 (US). **HOFFMAN, Eric, L.**; 2022 S. Fork Dr., Lafayette, CO 80026 (US). **LI, Jing-Jing**; 2200 Mission College Boulevard, Santa Clara, CA 95054 (US). **PELSTER, David, J.**; 1921 Corporate Center Cir., Ste. 3B, Longmont, CO 80501 (US).

(74) Agent: **VICTOR, David, W.**; Konrad Raynes Davda & Victor LLP, 350 S. Beverly Dr., Beverly Hills, CA 90212 (US).

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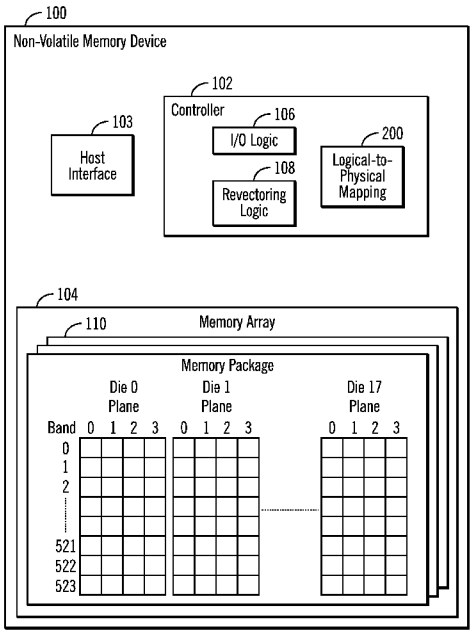


FIG. 1

(57) Abstract: Provided are a method and apparatus for remapping logical to physical addresses for a non-volatile memory having dies. Bands extend through the dies and planes in the dies extending through the bands define addressable blocks. A first remapping of a logical-to-physical mapping is performed by remapping logical addresses of blocks in a first end of the bands that map to defective physical blocks to map to good physical blocks at a second end of the bands. After performing the first remapping, a second remapping of the logical-to-physical mapping is performed by remapping logical addresses in the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands.

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METHOD AND APPARATUS FOR DEFECT MANAGEMENT IN A NON-VOLATILE MEMORY DEVICE

TECHNICAL FIELD

[0001] Embodiments described herein generally relate to a method and apparatus for defect management in a non-volatile memory device.

BACKGROUND

[0002] Solid state storage devices (for example, solid state drives) may be comprised of one or more packages of non-volatile memory dies, where each die is comprised of a plurality of bands and planes, such that a band extends across planes in multiple dies. Logical and physical addresses may map to a band, plane, and die. During manufacture, certain of the bands may have defects in less than all the planes of a die through which the band extends. A full plane retirement policy retires logical addresses for all the planes in a band within a die having the bad block. If a bad block is detected in a plane of a band in one die, then the logical addresses in all the planes in that particular die for the band may be retired and not available for use. This may eliminate significant amounts of spare space by eliminating logical addresses mapping to good planes in a band for a die.

[0003] There is a need in the art for improved techniques for managing bad blocks in the bands of a memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Embodiments are described by way of example, with reference to the accompanying drawings, which are not drawn to scale, in which like reference numerals refer to similar elements.

[0005] FIG. 1 illustrates an embodiment of a non-volatile memory device.

[0006] FIG. 2 illustrates an embodiment of a logical-to-physical mapping.

[0007] FIG. 3 illustrates an embodiment of a destination vector.

[0008] FIG. 4 illustrates an embodiment of operations to perform first and second remappings, i.e., revectorings, of the logical-to-physical mapping.

[0009] FIGs. 5a and 5b illustrate an embodiment of operations to perform the first remapping of the logical-to-physical mapping or first revectoring.

[0010] FIG. 6 illustrates an example of how the first remapping is performed to remap logical addresses in upper bands of the dies to lower bands.

[0011] FIGs. 7a and 7b illustrate an embodiment of operations to perform the second remapping of the logical-to-physical mapping or second revectoring.

[0012] FIG. 8 illustrates an example of how the second remapping is performed to remap logical addresses in lower bands of the dies to upper bands.

[0013] FIG. 9 illustrates a system in which the memory device of FIGs. 1 may be deployed.

DESCRIPTION OF EMBODIMENTS

[0014] Non-volatile memory dies are organized into a plurality of bands and planes, such that each die is comprised of planes and each of the bands extends across planes in multiple dies. Logical and physical addresses map to blocks, where each block is addressed by band, plane, and die. Prior art full plane retirement techniques retire all the logical addresses for all the planes in a band when the planes in one of the dies in a band have a bad block. Thus, for full plane retirement, many planes in the band having good blocks are also retired when all the planes in the band are retired.

[0015] To reduce the spare space loss that occurs with a full plane retirement policy, described embodiments remap logical addresses in the bands to different physical addresses to allow retirement of planes bands in a manner that minimizes the number of planes in the bands having good physical blocks. With described embodiments, in a first remapping step (also known as revectoring), source logical addresses at a first end of the bands, which extend across the dies, that map to defective physical blocks are remapped (also known as revectored) to the least number of full planes at a second end of the bands, and the destination logical addresses to which the source logical addresses are mapped are indicated as invalid, such as a logical defective block. In a second

remapping (also known as revectoring) step, the destination logical addresses of the first step having bad blocks due to the remapping, are redistributed to planes across all the bands at the first end to minimize the number of defective full planes per band, or minimize the number of bad dies in a band. This reduces spare space loss and the number of logical addresses that are lost as a result of retiring bad physical blocks.

[0016] Described embodiments provide a two-step revectoring or remapping operation. In a first remapping of the logical-to-physical mapping, logical addresses of blocks in a first end of the bands that map to defective physical blocks are mapped to good physical blocks at a second end of the bands. The logical addresses at the second end that map to blocks to which the logical addresses in the first end were mapped are indicated as bad logical blocks. After performing the first remapping, a second remapping (revectoring) of the logical-to-physical mapping is performed by remapping logical addresses in the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands. In this way, the remapped logical addresses in different dies of a band at the second end of bands are mapped to different destination bands in the first end of bands to distribute the number of bad logical addresses and minimize the number of bad planes in a band.

[0017] In the following description, numerous specific details such as logic implementations, opcodes, means to specify operands, resource partitioning/sharing/duplication implementations, types and interrelationships of system components, and logic partitioning/integration choices are set forth in order to provide a more thorough understanding of the present invention. It will be appreciated, however, by one skilled in the art that the invention may be practiced without such specific details. In other instances, control structures, gate level circuits and full software instruction sequences have not been shown in detail in order not to obscure the invention. Those of ordinary skill in the art, with the included descriptions, will be able to implement appropriate functionality without undue experimentation.

[0018] References in the specification to "one embodiment," "an embodiment," "an example embodiment," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not

necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Certain embodiments relate to storage device electronic assemblies. Embodiments include both devices and methods for forming electronic assemblies.

[0019] FIG. 1 illustrates an embodiment of a non-volatile memory device 100 having a controller 102, a host interface 103, and a memory array 104 of non-volatile memory cells. The non-volatile memory device 100 may function as both a memory device and/or a storage device in a computing system, and may be used to perform the role of volatile memory devices and disk drives in a computing system. In an embodiment, the non-volatile memory device 100 may comprise a solid state drive (SSD). The controller 102 includes Input/Output (I/O) logic 106 to manage read and write requests and direct such requests to the memory array 104. The I/O logic 106 adds read/write commands to a command queue (not shown), from which the commands are accessed and executed. A logical-to-physical mapping 200 provides a mapping of logical addresses to which I/O requests are directed and physical addresses in the memory array 104, which as shown may be expressed by band, plane and die. The I/O logic 106 determines the physical address from the logical address included in the I/O request to determine the physical block to which to direct the request. The host interface 103 connects the memory device 100 to a host system when the memory device 100 comprises an SSD. The memory device 100 may be installed or embedded within a host system, such as shown and described with respect to FIG. 9, or the memory device 100 may be external to the host system. The host interface 103 may comprise a bus interface, such as a Peripheral Component Interconnect Express (PCIe) interface, Serial AT Attachment (SATA), Non-Volatile Memory Express (NVMe), etc.

[0020] Initially, the logical-to-physical mapping 200 maps each logical address, expressed as a die, band and plane, to the physical address having the same die, band, and plane. Revectoring logic 108 modifies the mapping of logical to physical addresses to redistribute the mapping of logical addresses to bad blocks to minimize the number of defective full planes in every band.

[0021] FIG. 1 shows the memory array 104 comprised of one or more memory packages 110, where each package is comprised of a plurality dies, where there are 18 dies 0...17 in FIG. 1, each die comprised of addressable blocks, each addressable block identified by band and plane in the die. A band, e.g., each of bands 0....523, comprises a row of blocks extending across all the planes 0, 1, 2, 3 on all the dies 0...18.

[0022] The memory storage array 104 may comprise electrically erasable and non-volatile memory cells, such as flash storage devices. For instance, the memory storage array 104 may comprise NAND dies of memory cells, also known as NAND chips or packages. In one embodiment, the NAND dies may comprise multilevel cell (MLC) NAND flash memories that in each cell records two bit values, a lower bit value and an upper bit value. Alternatively, the NAND dies may comprise single level cell (SLC), multi-level cell (MLC), triple level cell (TLC) NAND memories, etc. The NAND dies, TLC, MLC, SLC, etc., may be organized in a three dimensional (3D) or two dimensional (2D) physical structure. The storage array 104 may also comprise, but is not limited to, MLC NAND flash memory, ferroelectric random-access memory (FeTRAM), nanowire-based non-volatile memory, three-dimensional (3D) crosspoint memory such as phase change memory (PCM), memory that incorporates memristor technology, Magnetoresistive random-access memory (MRAM), Spin Transfer Torque (STT)-MRAM, a single level cell (SLC) Flash memory and other electrically erasable programmable read only memory (EEPROM) type devices.

[0023] In one embodiment, the revectoring logic 108 may run in the factory before entering distribution channels in order to remap the logical addresses to physical addresses to minimize the number of bad dies in a band by modifying the mapping of logical addresses to physical addresses to redistribute the logical addresses that map to bad blocks in one band of logical addresses. The memory device 100 performance is improved if the number of bad planes in every band is minimized. The manufacturer may perform the remapping before the shipping of the memory devices 100. Alternatively, users of the memory device 100 may invoke the revectoring logic 108 in the memory device 100 product when reformatting the memory device 100 or during diagnostic and recovery operations. For instance, the revectoring logic 108 may be

invoked when the memory device 100 is installed in a computer system and the user invokes the reformatting process using a command interface or a graphical user interface.

[0024] FIG. 2 illustrates an embodiment of an instance of one logical-to-physical mapping 200_i in the logical-to-physical mapping 200 that provides a logical address 202, which may be expressed by die, band, and plane, and physical address 204, which may be expressed as die, band, and plane, to which the logical address 202 maps.

[0025] FIG. 3 illustrates an embodiment of a destination vector 300 used during the remapping, also referred to as revectoring, that includes a field $302_0, 302_1 \ldots 302_m$ that provides the destination band for the corresponding plane to which a logical address is remapped.

[0026] FIG. 4 illustrates an embodiment of operations performed by the revectoring logic 108 to remap, i.e., revector, the logical to physical addresses to minimize the number of bad planes in a band. The first revectoring or remapping of FIG. 4 remaps bad source logical addresses at a first end of the bands, which may comprise the earlier numbered bands, starting from a beginning band, to the physical blocks at a second end of the bands, i.e., from the last numbered band. In an alternative embodiment, the first end of bands having the source bands m ay comprise the later numbered bands or start from the last numbered band and the second end of bands may start from the beginning band.

[0027] Upon initiating the revectoring operations, the revectoring logic 108 performs (at block 402) a first remapping of the logical-to-physical mapping 200 by remapping logical addresses of blocks in a die at a first end of the bands that map to defective physical blocks to map to good physical blocks at a second end of the bands. In one embodiment, the first end of the bands comprises bands from a beginning band, i.e., one of the earlier numbered bands, to a last band of the bands and the second end of the bands comprises bands from the last band to the user start band. In a further embodiment, the first remapping remaps logical addresses from source bands starting sequentially from the beginning band in the first end of bands to destination bands

starting sequentially from the last band at the second end of bands while the source band is less than the destination band.

[0028] The revectoring logic 108 retires (at block 406) any bands at the second end of bands having logical addresses for all blocks in all the planes of all the dies map to defective logical blocks or bad physical blocks. After performing the first remapping, the logical addresses at the second end that previously mapped to the good physical blocks to which the logical addresses in the first end of bands were remapped are indicated as defective logical blocks. In this way, logical addresses that map to bad blocks are consolidated in the bands at a second end of the bands to consolidate the bad logical addresses at one end of the bands. Any bands at the second end that have all their logical addresses, in all planes and dies of the band, map to defective blocks may be retired.

[0029] After performing the first remapping and retiring any bands, the revectoring logic 108 performs (at block 408) a second remapping of the logical-to-physical mapping 200 by remapping logical addresses in the planes at the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands. As part of the second remapping, for each of the bands at the second end of the bands on the die subject to remapping, the revectoring logic maps (at block 410) logical addresses in the planes in the band that map to defective blocks to different bands at the first end of bands on the die so that the remapping of logical addresses in the planes of the band at the second end are redistributed to different bands at the first end of the bands on that same plane. The logical addresses in the destination band that mapped to good physical blocks to which the source logical addresses were remapped are indicated (at block 412) as defective logical blocks; the logical addresses in the destination band that mapped to good physical blocks to which the source logical addresses were remapped are indicated as defective logical blocks; the source logical addresses, which were previous destination logical addresses as part of the first remapping, are indicated as good blocks; and the link between the source block and previous destination block is removed, and a link between the source block and the new destination block is stored.

[0030] In one embodiment, the second remapping remaps logical addresses from source bands in a die starting sequentially from one of the bands at the second end not having all defective blocks to destination bands starting sequentially from the first end of the bands from a beginning band while the source band is greater than the destination band. In one embodiment, the second remapping maps the logical addresses in the planes for the source band at the second end on a die that map to bad blocks to different source bands on the same die so that the logical addresses in the band at the second end are remapped to different bands on the first end. In further embodiments, when remapping the logical address at the second end to the first end, the destination logical addresses have the same plane and die. In this way, the second remapping is performed to redistribute the logical addresses in the planes of a band at the second end that address defective blocks to map to good blocks to reduce a number of planes in the band on the die having defective blocks. The logical addresses at the second end subject to remapping may have been indicated as defective as a result of the first remapping.

[0031] FIGs. 5a and 5b illustrate an embodiment of operations to perform the first remapping of the logical-to-physical mapping, such as performed at blocks 402, 404, and 406 of FIG. 4. The revectoring logic 108 performs a loop of operations at block 502 through 536 for each die *i*, where *i* equals 0 to *n*, where *n* is the last number die, such as 17 as shown in FIG. 1. For each die *i*, the revectoring logic 108 performs a loop of operations at blocks 504 through 534, for each plane *j*, where *j* can be from 0 to *m*, where *m* is shown as three in FIG. 1. The destination band is then set (at block 506) to a last band of the bands, e.g., 523 as shown in FIG. 1, and the destination band 302_j in the destination vector 300 for plane *j* in die *i* is set to the last band. For each source band *k*, starting from the beginning band, a loop of operations is performed from blocks 510 to 532 while the source band is greater than the destination band to which the logical address will be remapped.

[0032] For source band *k*, if (at block 512) the source band is less than the destination band, then a determination is made (at block 5143) as to whether the logical address in source band *k*, plane *j* and die *i* maps to a defective physical or logical block. If so, then if (at block 516) the physical block at the current destination band for plane *j* in die *i* is

good, then control proceeds (at block 518) to block 520 in FIG. 5b where the revectoring logic 508 remaps the logical address for die *i*, plane j, and source band *k* to the current destination band for plane *j* in die *i*, which may be indicated in the destination vector 302_j for plane *j*. In alternative embodiments, the destination and source blocks can be set in different planes and/or dies. The destination band indicated in the destination vector 302_j for plane *j* is then decremented so the next logical address considered for die *i* and plane *j* is mapped to the next destination band. The current destination band for plane 300_j indicated in the destination vector 300 is set (at block 524) to the decremented destination band. The revectoring logic 108 may also indicate (at block 526) the logical address in the destination band that mapped to the good physical block to which the source logical address *i, j, k* was remapped as a defective logical block and indicate the source logical address *i, j, k* as a good logical block. Thus, a defective logical address (or block) comprises a logical address that no longer maps to a specific physical block and a defective physical block comprises a physical block on one die that cannot be accessed due to damage.

[0033] If (at block 512) the source band is not less than the destination band, then control proceeds to block 534 in FIG. 5b to process blocks in source bands for the next plane. If (at block 514) the logical address in the source band at die *i*, plane *j*, and source band *k* do not map to a defective block, then there is no need to remap the logical address and control proceeds to block 532 in FIG. 5b to process the next source band for die *i* and plane *j*. If (at block 516) the physical block at the current destination band for plane *j* is not good, meaning the logical address at the source band *k* cannot be remapped to a bad physical block, then the destination band is decremented (at block 528) and the current destination band 300_j for plane *j* in the destination vector 300 is set (at block 530) to the decremented destination band. In this way, source logical addresses in one plane that map to bad physical blocks are mapped to good physical blocks in different bands of the same plane.

[0034] After processing all possible source logical addresses for all the dies, planes, and bands, to consolidate logical addresses pointing to bad blocks in the last bands, the revectoring logic 108 retires (at block 538) any band at the second end of bands having

all blocks in all the planes of all the dies map to defective logical blocks or bad physical blocks.

[0035] FIG. 6 illustrates an example of the first mapping of FIGs. 4, 5a and 5b. The first revector process 602 shows arrows of logical addresses initially mapped to bad factory blocks that are remapped to good physical blocks in the same plane but on bands at the lower ends of b ands. The after revectoring 604 results of the first remapping or revectoring shows the band 523 having all factory defective or logical defective blocks as being retired. The square hatched boxes in the upper band show logical addresses remapped and the diagonal hashed boxes in band 523 shows logical addresses that are defective or do not point to a valid physical block. In this way, logical addresses in the upper bands that map to defective blocks are remapped to good blocks in the lower bands to consolidate the bad logical addresses in the lower band.

[0036] FIGs. 7a and 7b illustrate an embodiment of operations to perform the second remapping (revectoring) of the logical-to-physical mapping, such as performed at blocks 408 and 410 of FIG. 4. Upon initiating (at block 700) the second revectoring operation, after performing the first revectoring operation of FIGs. 5a and 5b, a loop of operations is performed at blocks 702 through 736 for each die *i*, where *i* equals 0 to *n*, where *n* is the last number die, such as 17 as shown in FIG. 1. The revectoring logic 108 sets (at block 704) the source band to the last retired band minus one, so that the revectoring starts from the last source band preceding any retired bands. The destination band is set (at block 706) to the beginning band, which may be a user selected start band or default value of one of the earlier number bands.

[0037] If (at block 707) the source band is not greater than the destination band and if (at block 708) the source band does not have any defects, then a determination is made (at block 710) as to whether the source band in die *i* has a defect. If so and if (at block 712) the source band is the beginning band, then the source band is set (at block 714) to the destination band minus one and the destination band is set to a beginning destination band, such as the beginning band at the first end of bands. If revectoring has not started on die *i*, i.e., the source band is the beginning band, then the destination band may be defective due to an overlap of the destination bands on the previous die and the source

bands on this die. By setting the source band to the destination band minus one, the source band on the current die *i* after the destination band on the previous die (*i*-1) will not be revectored in order to have only one defective die per band. Then for the rest of the source bands on this die *i*, the destination bands start over from the beginning band. If (at block 716) the destination band is still defective, then control proceeds to block 736 to perform the second revectoring (remapping) for the next die because there is no defect free band on the current die *i*. Otherwise, if (from the no branch of block 716) the destination band is not defective, then control proceeds back to block 707 to make sure the source band remains greater than the destination band in order to proceed with the remapping.

[0038] If (from the yes branch of block 707) the source band is greater than the destination band or if (at block 708) the source band does not have any defects, then control proceeds to block 736 to consider the next die *i*. If (at block 712) the source band is the starting band when the destination band in die *i* has a defect, then the revectoring logic 108 sets (at block 713) the destination band to the source band plus one and proceeds to block 736 to process the next die *i*. The situation at block 713 occurs when the source band and destination band meet in the middle, and in such case revectoring stops for the rest of the source bands in die *i*. If (from the yes branch of block 708 and the no branch of block 710) the source band has defects and the destination band does not, then control proceeds to block 722 in FIG. 7b to initiate revectoring.

[0039] Upon initiating revectoring at block 722, the revectoring logic 108 performs a loop of operations at blocks 722 through 730 (FIG. 7b), for each plane *j*, where *j* can be from 0 to *m*, where *m* is shown as three in FIG. 1. If (at block 724) the logical address in the source band in die *i* and plane *j* maps to a defective block, then the logical address at die *i*, plane *j*, and the current source band is remapped (at block 726) to the current destination band for plane *j* and die *i*. The logical address in the destination band that mapped to the good physical block to which the source logical addresses was remapped is indicated (at block 728) as a defective logical block, the source logical address is indicated as a good logical block, and the relation between the source and destination

logical addresses subject to the remapping is stored. If (at block 724) the logical address in the source band is not defective, then control proceeds to block 730 to consider the logical address in the next plane in the source band in die *i*. After remapping any logical addresses mapping to defective blocks in the planes of the current source band and die *i* to the destination band, the destination band is incremented (at block 732), the source band is decremented (at block 734), and control proceeds back to block 707 in FIG. 7a to perform the remapping for the next source band and destination band in die *i*.

[0040] The described operations of FIGs. 7a and 7b remap logical addresses in the planes of a current source band in a die *i* to a new destination band to redistribute any bad logical addresses in the planes in one band on the die to different destination bands on the die to minimize the number of defective full planes in every band of the die. In the second revectoring, the defects in the non-retired full planes of every die are revectored again to make the least number of defective full planes in every band. In this way, the defective full planes are spread across all the available bands of the die to reduce the number of runt bands in the die with a large number of defective full planes. Runt bands in a die comprise bands having a large number of defective planes.

[0041] FIG. 8 illustrates an example of the second revectoring (remapping) operation, i.e., revectoring of FIGs. 4, 7a, 7b, and 8b. The second revectoring process 802 shows arrows of logical addresses in the lower bands that have not been retired that map to bad logical or physical blocks being remapped to good physical blocks in the same plane but on bands at the upper bands. In this way, bad logical addresses in the planes of the lower bands are remapped to good physical addresses in the upper bands to redistribute the logical addresses in the lower bands to minimize the number of defective full planes across all available bands. The after revectoring 804 results of the second remapping or revectoring shows the logical addresses in the band 522 above the retired band 523 mapping to good physical addresses when previously they mapped to bad logical or physical blocks. However, the logical addresses in the upper bands that addressed the good blocks to which the logical addresses in the lower bands were remapped are shown as logically bad blocks, such as the logical addresses in band 3, plane 1, die 0; band 4,

plane 2, die 1; and band 5, plane 2, die 17. The square hatched boxes in the lower band show logical addresses remapped to good physical blocks and the diagonal hashed boxes in bands 3, 4, and 5 show logical addresses that are defective or do not point to a valid physical block as a result of the remapping. In this way, the defective full planes from the first die to the last die are sequentially remapped to the destination bands starting from the beginning band to the last non-retired band. If all the aforementioned destination bands are filled, the destination bands start over again from the user start band to revector the following defective full planes. The reduction of runt bands, bands with a large number of defective full planes on its dies, improves the performance and reduces the drive-to-drive variation of write time.

[0042] The described first and second revectoring (remapping) provides specific operations to first remap logical addresses having bad blocks in bands at a first end of bands to physical addresses at a second end of the bands having good blocks in the same plane and then redistribute the bad logical addresses at the second end of bands among bands at the first end. In alternative embodiments, different techniques may be used to map logical addresses in the first and second mapping into different planes and dies to accomplish the goals of grouping bad logical addresses into bands at one end, so that the bands may be retired, and then redistributing bad logical addresses at the second or lower end into bands at the first upper end on different dies, so as to minimize the number of defective full planes in a band on the dies.

[0043] FIG. 9 illustrates an embodiment of a system 900 in which the memory device 100 may be deployed as the system memory device 908 and/or a storage device 910. The system includes a processor 904 that communicates over a bus 906 with a system memory device 908 in which programs, operands and parameters being executed are cached, and a storage device 910, which may comprise a solid state drive (SSD) that stores programs and user data that may be loaded into the system memory 908 for execution. The processor 904 may also communicate with Input/Output (I/O) devices 912a, 912b, which may comprise input devices (e.g., keyboard, touchscreen, mouse, etc.), display devices, graphics cards, ports, network interfaces, etc. The memory 908 and storage device 910 may be coupled to an interface on the system 800 motherboard,

mounted on the system 800 mother board, or deployed in an external memory device or accessible over a network.

[0044] It should be appreciated that reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Therefore, it is emphasized and should be appreciated that two or more references to "an embodiment" or "one embodiment" or "an alternative embodiment" in various portions of this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined as suitable in one or more embodiments of the invention.

[0045] Similarly, it should be appreciated that in the foregoing description of embodiments of the invention, various features are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed subject matter requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description.

EXAMPLES

[0046] The following examples pertain to further embodiments.

[0047] Example 1 is an apparatus, comprising: a non-volatile memory having dies, wherein bands extend through the dies, and planes in the dies extending through the bands define addressable blocks; and memory control logic; and a logical-to-physical mapping to provide a mapping of logical addresses of blocks to physical addresses of blocks in the dies, wherein the logical to physical mapping is formed by the memory control logic performing a first remapping of the logical-to-physical mapping by remapping logical addresses of blocks in a first end of the bands that map to defective

physical blocks to map to good physical blocks at a second end of the bands and to perform a second remapping of the logical-to-physical mapping after performing the first remapping by remapping logical addresses in the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands.

[0048] In Example 2, the subject matter of Examples 1 and 3-10 can optionally include that the logical-to-physical mapping is further formed by the memory control logic further performing: in response to performing the first remapping of the logical-to-physical mapping, indicate as defective logical blocks the logical addresses at the second end of the bands that previously mapped to the good physical blocks to which the logical addresses in the first end of bands was remapped.

[0049] In Example 3, the subject matter of Examples 1, 2 and 4-10 can optionally include that the logical-to-physical mapping is further formed by the memory control logic further performing: retire at least one band at the second end of bands having all blocks in all the planes of all the dies whose logical addresses map to defective logical blocks and/or bad physical blocks, wherein the second remapping remaps the logical addresses in the second end of bands that do not include the retired bands.

[0050] In Example 4, the subject matter of Examples 1-3 and 5-10 can optionally include that the second remapping remaps the logical addresses to different bands at the first end of bands to redistribute the logical addresses in the band at the second end to different bands at the first end.

[0051] In Example 5, the subject matter of Examples 1-4 and 6-10 can optionally include that the second remapping remaps the logical addresses in the planes of the bands on one die to different destination bands on the die to provide a least number of defective full planes in every band.

[0052] In Example 6, the subject matter of Examples 1-5 and 7-10 can optionally include that the second remapping further indicates the logical addresses in the destination band that mapped to good physical blocks to which the source logical addresses were remapped as a defective logical block.

[0053] In Example 7, the subject matter of Examples 1-6 and 8-10 can optionally include that the first end of the bands comprises bands from a beginning band to a last

band of the bands and wherein the second end of the bands comprises bands from the last band to the beginning band.

[0054] In Example 8, the subject matter of Examples 1-7, 9, and 10 can optionally include that the first remapping remaps logical addresses from source bands starting sequentially from the beginning band in the first end of the bands to destination bands starting sequentially from the last band at the second end of the bands while the source band is less than the destination band.

[0055] In Example 9, the subject matter of Examples 1-8 and 10 can optionally include that the second remapping remaps logical addresses from source bands starting sequentially from one of the bands at the second end not having all defective blocks to destination bands starting sequentially from the first end of the bands starting sequentially from the beginning band while the source band is greater than the destination band.

[0056] In Example 10, the subject matter of Examples 1-9 can optionally include that the second remapping further comprises: in response to the source band beginning at a starting source band and the destination band having a defect, set the source band to the destination band minus one and set the destination band to a beginning destination band, and then performing the second remapping with respect to the set source band and the destination band.

[0057] Example 11 is a method for configuring non-volatile memory having dies, wherein bands extend through the dies, and planes in the dies extending through the bands define addressable blocks, comprising: performing a first remapping of a logical-to-physical mapping by remapping logical addresses of blocks in a first end of the bands that map to defective physical blocks to map to good physical blocks at a second end of the bands; and after performing the first remapping, performing a second remapping of the logical-to-physical mapping by remapping logical addresses in the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands.

[0058] In Example 12, the subject matter of Example 11 can optionally include at least one step of:

[0059] (1) wherein the logical-to-physical mapping is further formed by the memory control logic further performing: in response to performing the first remapping of the logical-to-physical mapping, indicate as defective logical blocks the logical addresses at the second end of the bands that previously mapped to the good physical blocks to which the logical addresses in the first end of bands was remapped; and/or

[0060] (2) wherein the logical-to-physical mapping is further formed by the memory control logic further performing: retire at least one band at the second end of bands having all blocks in all the planes of all the dies whose logical addresses map to defective logical blocks and/or bad physical blocks, wherein the second remapping remaps the logical addresses in the second end of bands that do not include the retired bands; and/or

[0061] (3) wherein the second remapping remaps the logical addresses to different bands at the first end of bands to redistribute the logical addresses in the band at the second end to different bands at the first end; and/or

[0062] (4) wherein the second remapping remaps the logical addresses in the planes of the bands on one die to different destination bands on the die to provide a least number of defective full planes in every band; and/or

[0063] (5) wherein the second remapping further indicates the logical addresses in the destination band that mapped to good physical blocks to which the source logical addresses were remapped as a defective logical block; and/or

[0064] (6) wherein the first end of the bands comprises bands from a beginning band to a last band of the bands and wherein the second end of the bands comprises bands from the last band to the beginning band; and/or

[0065] (7) wherein the first remapping remaps logical addresses from source bands starting sequentially from the beginning band in the first end of the bands to destination bands starting sequentially from the last band at the second end of the bands while the source band is less than the destination band; and/or

[0066] (8) wherein the second remapping remaps logical addresses from source bands starting sequentially from one of the bands at the second end not having all defective blocks to destination bands starting sequentially from the first end of the bands starting

sequentially from the beginning band while the source band is greater than the destination band; and/or

[0067] (9) wherein the second remapping further comprises: in response to the source band beginning at a starting source band and the destination band having a defect, set the source band to the destination band minus one and set the destination band to a beginning destination band, and then performing the second remapping with respect to the set source band and the destination band.

[0068] Example 13 is a memory controller coupled to a non-volatile memory having dies, wherein bands extend through the dies, and planes in the dies extending through the bands define addressable blocks, comprising: memory control logic that when executed performs operations, the operations comprising: perform a first remapping of a logical-to-physical mapping by remapping logical addresses of blocks in a first end of the bands that map to defective physical blocks to map to good physical blocks at a second end of the bands; and after performing the first remapping, perform a second remapping of the logical-to-physical mapping by remapping logical addresses in the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands.

[0069] In Example 14, the subject matter of Examples 13 and 15-17 can optionally include that the second remapping remaps the logical addresses to different bands at the first end of bands to redistribute the logical addresses in the band at the second end to different bands at the first end.

[0070] In Example 15, the subject matter of Examples 13, 14, 16, and 17 can optionally include that the second remapping remaps the logical addresses in the planes of the bands on one die to different destination bands on the die to provide a least number of defective full planes in every band.

[0071] In Example 16, the subject matter of Examples 13-15 and 17 can optionally include that the first end of the bands comprises bands from a beginning band to a last band of the bands and wherein the second end of the bands comprises bands from the last band to the beginning band, and wherein the first remapping remaps logical addresses from source bands starting sequentially from the beginning band in the first

end of the bands to destination bands starting sequentially from the last band at the second end of the bands while the source band is less than the destination band.

[0072] In Example 17, the subject matter of Examples 13-16 can optionally include that the first end of the bands comprises bands from a beginning band to a last band of the bands and wherein the second end of the bands comprises bands from the last band to the beginning band, and wherein the second remapping remaps logical addresses from source bands starting sequentially from one of the bands at the second end not having all defective blocks to destination bands starting sequentially from the first end of the bands starting sequentially from the beginning band while the source band is greater than the destination band.

[0073] Example 18 is an apparatus for configuring non-volatile memory having dies, wherein bands extend through the dies, and planes in the dies extending through the bands define addressable blocks, comprising: means for performing a first remapping of a logical-to-physical mapping by remapping logical addresses of blocks in a first end of the bands that map to defective physical blocks to map to good physical blocks at a second end of the bands; and means for performing the first remapping, performing a second remapping of the logical-to-physical mapping by remapping logical addresses in the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands.

[0074] In Example 19, the subject matter of Example 18 can optionally include means for indicating as defective logical blocks the logical addresses at the second end of the bands that previously mapped to the good physical blocks to which the logical addresses in the first end of bands was remapped in response to performing the first remapping of the logical-to-physical mapping.

[0075] Example 20 is an apparatus comprising means to perform a method as claimed in any preceding claim.

[0076] Example 21 is a machine-readable storage including machine-readable instructions, when executed, to implement a method or realize an apparatus or system as claimed in any preceding claim.

WHAT IS CLAIMED

1. An apparatus, comprising:

a non-volatile memory having dies, wherein bands extend through the dies, and planes in the dies extending through the bands define addressable blocks; and

memory control logic; and

a logical-to-physical mapping to provide a mapping of logical addresses of blocks to physical addresses of blocks in the dies, wherein the logical to physical mapping is formed by the memory control logic performing a first remapping of the logical-to-physical mapping by remapping logical addresses of blocks in a first end of the bands that map to defective physical blocks to map to good physical blocks at a second end of the bands and to perform a second remapping of the logical-to-physical mapping after performing the first remapping by remapping logical addresses in the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands.

2. The apparatus of claim 1, wherein the logical-to-physical mapping is further formed by the memory control logic further performing:

in response to performing the first remapping of the logical-to-physical mapping, indicate as defective logical blocks the logical addresses at the second end of the bands that previously mapped to the good physical blocks to which the logical addresses in the first end of bands was remapped.

3. The apparatus of claim 2, wherein the logical-to-physical mapping is further formed by the memory control logic further performing:

retire at least one band at the second end of bands having all blocks in all the planes of all the dies whose logical addresses map to defective logical blocks and/or bad physical blocks, wherein the second remapping remaps the logical addresses in the second end of bands that do not include the retired bands.

4. The apparatus as in any one of claims 1, 2 or 3, wherein the second remapping remaps the logical addresses to different bands at the first end of bands to redistribute the logical addresses in the band at the second end to different bands at the first end.

5. The apparatus of claim 4, wherein the second remapping remaps the logical addresses in the planes of the bands on one die to different destination bands on the die to provide a least number of defective full planes in every band.

6. The apparatus of claim 5, wherein the second remapping further indicates the logical addresses in the destination band that mapped to good physical blocks to which the source logical addresses were remapped as a defective logical block.

7. The apparatus as in any one of claims 1, 2 or 3, wherein the first end of the bands comprises bands from a beginning band to a last band of the bands and wherein the second end of the bands comprises bands from the last band to the beginning band.

8. The apparatus of claim 7, wherein the first remapping remaps logical addresses from source bands starting sequentially from the beginning band in the first end of the bands to destination bands starting sequentially from the last band at the second end of the bands while the source band is less than the destination band.

9. The apparatus of claim 7, wherein the second remapping remaps logical addresses from source bands starting sequentially from one of the bands at the second end not having all defective blocks to destination bands starting sequentially from the first end of the bands starting sequentially from the beginning band while the source band is greater than the destination band.

10. The apparatus as in any one of claims 1-3, wherein the second remapping further comprises:

in response to the source band beginning at a starting source band and the destination band having a defect, set the source band to the destination band minus one and set the destination band to a beginning destination band, and then performing the second remapping with respect to the set source band and the destination band.

11. A method for configuring non-volatile memory having dies, wherein bands extend through the dies, and planes in the dies extending through the bands define addressable blocks, comprising:

performing a first remapping of a logical-to-physical mapping by remapping logical addresses of blocks in a first end of the bands that map to defective physical blocks to map to good physical blocks at a second end of the bands; and

after performing the first remapping, performing a second remapping of the logical-to-physical mapping by remapping logical addresses in the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands.

12. The method of claim 11, further comprising:

in response to performing the first remapping of the logical-to-physical mapping, indicating as defective logical blocks the logical addresses at the second end of the bands that previously mapped to the good physical blocks to which the logical addresses in the first end of bands was remapped.

13. The method of claim 12, further comprising:

retiring at least one band at the second end of bands having all blocks in all the planes of all the dies whose logical addresses map to defective logical blocks and/or bad physical blocks, wherein the second remapping remaps the logical addresses in the second end of bands that do not include the retired bands.

14. The method as in any one of claims 11-13, wherein the second remapping remaps the logical addresses to different bands at the first end of bands to redistribute the logical addresses in the band at the second end to different bands at the first end.

15. The method of claim 14, wherein the second remapping remaps the logical addresses in the planes of the bands on one die to different destination bands on the die to provide a least number of defective full planes in every band.

16. The method of claim 15, wherein the second remapping further indicates the logical addresses in the destination band that mapped to good physical blocks to which the source logical addresses were remapped as a defective logical block.

17. The method as in any one of claims 11-13, wherein the first end of the bands comprises bands from a beginning band to a last band of the bands and wherein the second end of the bands comprises bands from the last band to the beginning band.

18. The method as in any one of claims 11-13, wherein the second remapping further comprises:

in response to the source band beginning at a starting source band and the destination band having a defect, setting the source band to the destination band minus one and set the destination band to a beginning destination band, and then performing the second remapping with respect to the set source band and the destination band.

19. An apparatus for configuring non-volatile memory having dies, wherein bands extend through the dies, and planes in the dies extending through the bands define addressable blocks, comprising:

means for performing a first remapping of a logical-to-physical mapping by remapping logical addresses of blocks in a first end of the bands that map to defective physical blocks to map to good physical blocks at a second end of the bands; and

means for performing the first remapping, performing a second remapping of the logical-to-physical mapping by remapping logical addresses in the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands.

20. The apparatus of claim 19, further comprising:

means for indicating as defective logical blocks the logical addresses at the second end of the bands that previously mapped to the good physical blocks to which the logical addresses in the first end of bands was remapped in response to performing the first remapping of the logical-to-physical mapping.

21. A memory controller coupled to a non-volatile memory having dies, wherein bands extend through the dies, and planes in the dies extending through the bands define addressable blocks, comprising:

memory control logic that when executed performs operations, the operations comprising:

perform a first remapping of a logical-to-physical mapping by remapping logical addresses of blocks in a first end of the bands that map to defective physical blocks to map to good physical blocks at a second end of the bands; and

after performing the first remapping, perform a second remapping of the logical-to-physical mapping by remapping logical addresses in the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands.

22. The memory controller of claim 21, wherein the second remapping remaps the logical addresses to different bands at the first end of bands to redistribute the logical addresses in the band at the second end to different bands at the first end.

23. The memory controller of claim 22, wherein the second remapping remaps the logical addresses in the planes of the bands on one die to different

destination bands on the die to provide a least number of defective full planes in every band.

24. The memory controller as in any one of claim 21-23, wherein the first end of the bands comprises bands from a beginning band to a last band of the bands and wherein the second end of the bands comprises bands from the last band to the beginning band, and wherein the first remapping remaps logical addresses from source bands starting sequentially from the beginning band in the first end of the bands to destination bands starting sequentially from the last band at the second end of the bands while the source band is less than the destination band.

25. The memory controller as in any one of claims 21-23, wherein the first end of the bands comprises bands from a beginning band to a last band of the bands and wherein the second end of the bands comprises bands from the last band to the beginning band, and wherein the second remapping remaps logical addresses from source bands starting sequentially from one of the bands at the second end not having all defective blocks to destination bands starting sequentially from the first end of the bands starting sequentially from the beginning band while the source band is greater than the destination band.

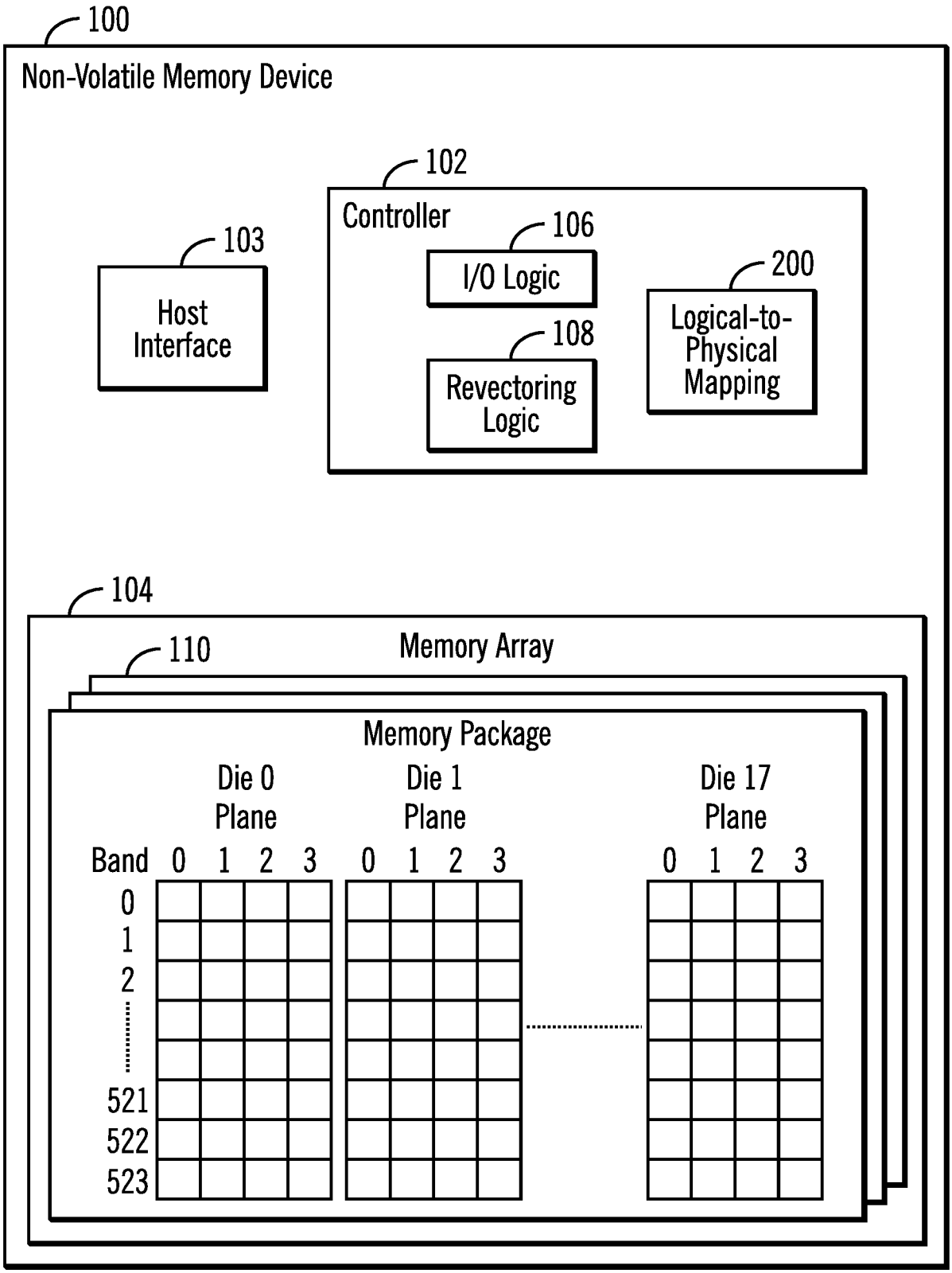

100
Non-Volatile Memory Device
102
Controller
106
I/O Logic
108
Revectoring Logic
200
Logical-to-Physical Mapping
103
Host Interface
104
110
Memory Array
Memory Package
Die 0 Plane
Die 1 Plane
Die 17 Plane
Band
0 1 2 3
0 1 2 3
0 1 2 3
0
1
2
521
522
523

FIG. 1

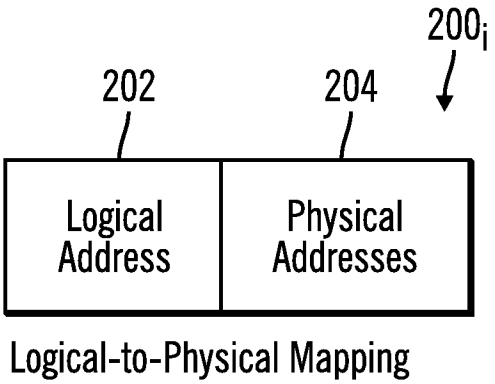

200i
202
204
Logical Address
Physical Addresses
Logical-to-Physical Mapping

FIG. 2

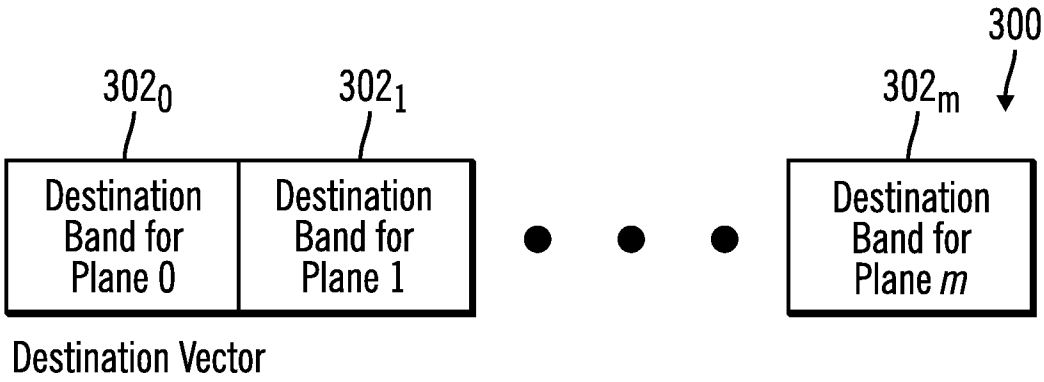

300
302₀
302₁
302m
Destination Band for Plane 0
Destination Band for Plane 1
Destination Band for Plane m
Destination Vector

FIG. 3

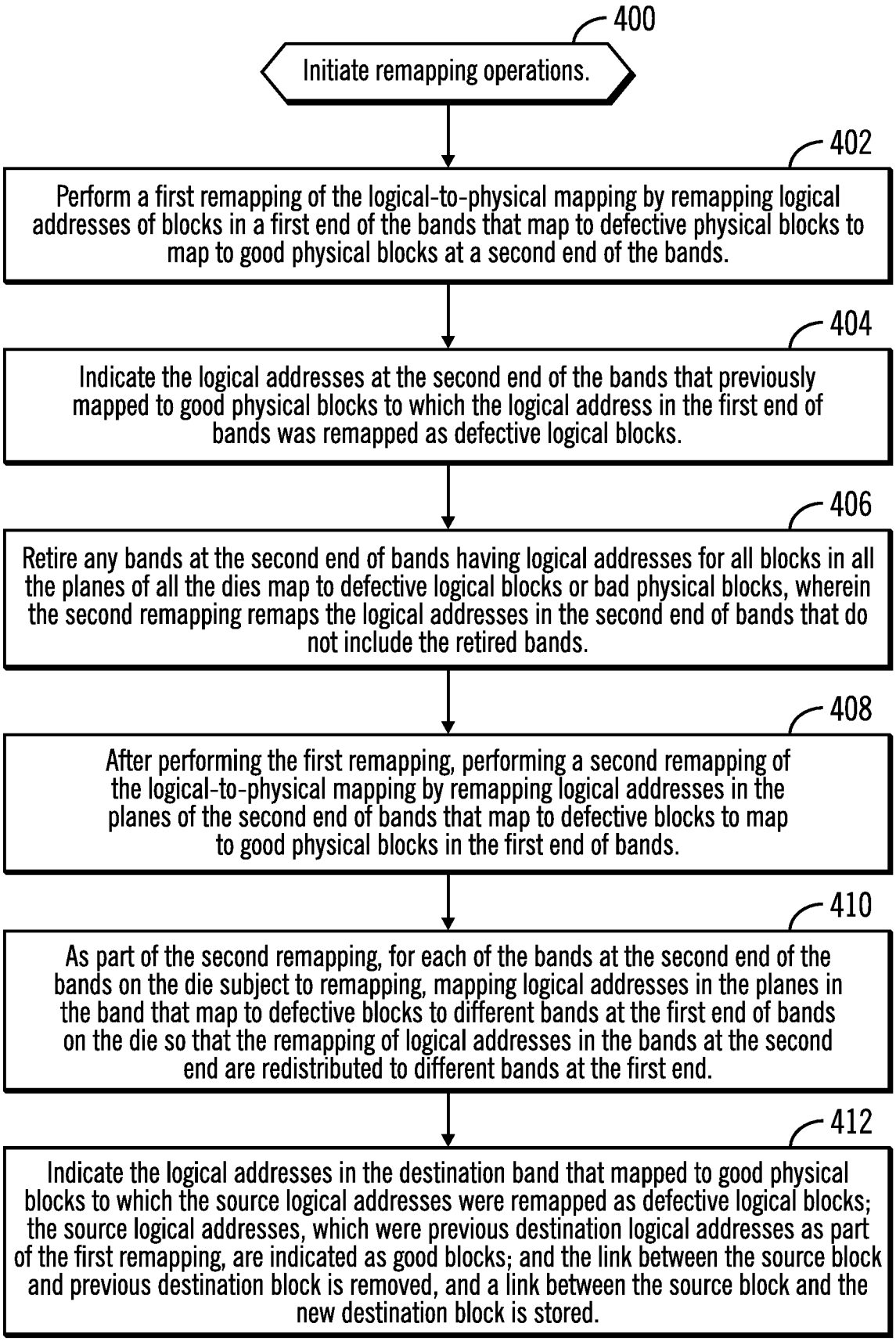

400
Initiate remapping operations.
402
Perform a first remapping of the logical-to-physical mapping by remapping logical addresses of blocks in a first end of the bands that map to defective physical blocks to map to good physical blocks at a second end of the bands.
404
Indicate the logical addresses at the second end of the bands that previously mapped to good physical blocks to which the logical address in the first end of bands was remapped as defective logical blocks.
406
Retire any bands at the second end of bands having logical addresses for all blocks in all the planes of all the dies map to defective logical blocks or bad physical blocks, wherein the second remapping remaps the logical addresses in the second end of bands that do not include the retired bands.
408
After performing the first remapping, performing a second remapping of the logical-to-physical mapping by remapping logical addresses in the planes of the second end of bands that map to defective blocks to map to good physical blocks in the first end of bands.
410
As part of the second remapping, for each of the bands at the second end of the bands on the die subject to remapping, mapping logical addresses in the planes in the band that map to defective blocks to different bands at the first end of bands on the die so that the remapping of logical addresses in the bands at the second end are redistributed to different bands at the first end.
412
Indicate the logical addresses in the destination band that mapped to good physical blocks to which the source logical addresses were remapped as defective logical blocks; the source logical addresses, which were previous destination logical addresses as part of the first remapping, are indicated as good blocks; and the link between the source block and previous destination block is removed, and a link between the source block and the new destination block is stored.

FIG. 4

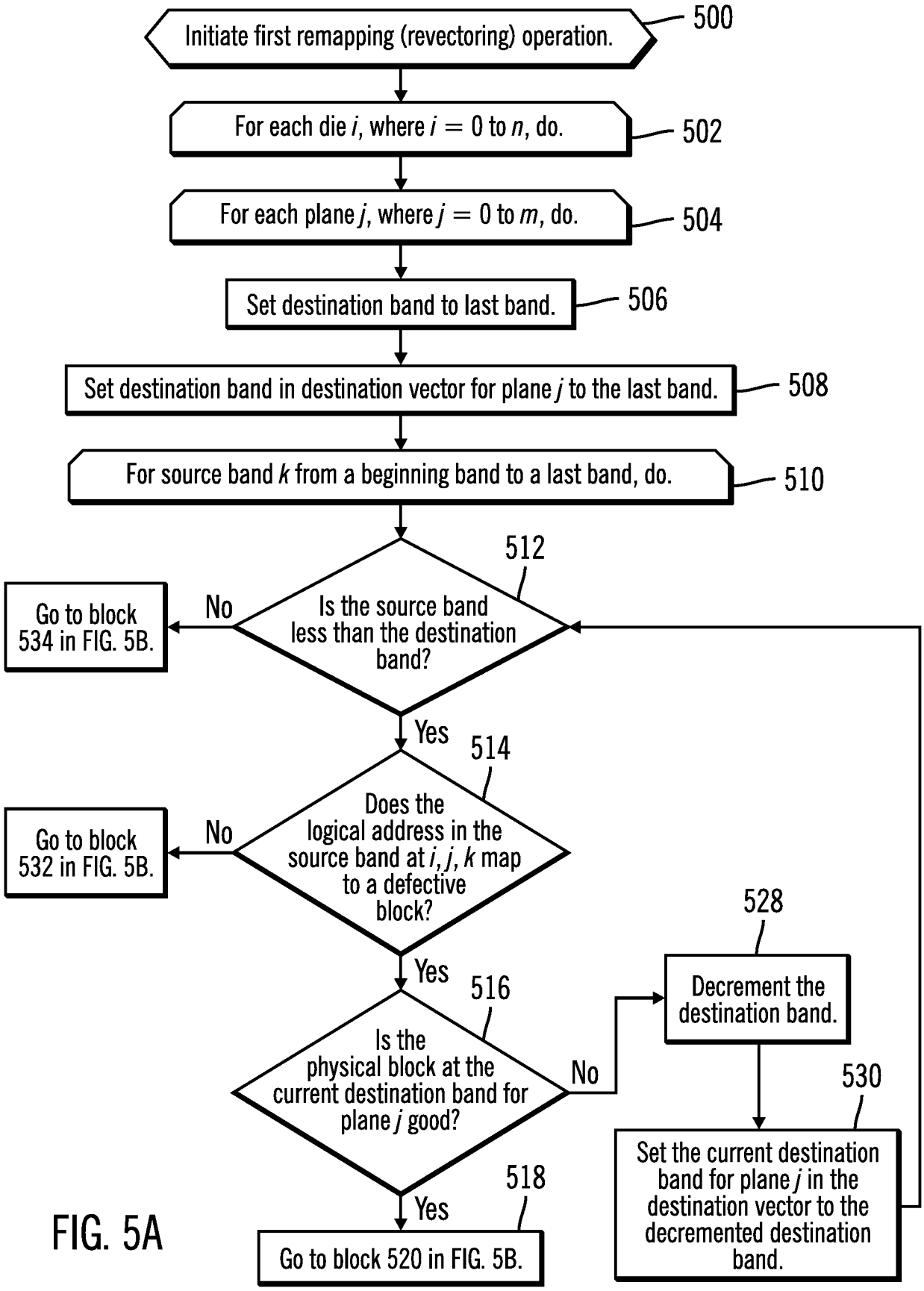

Initiate first remapping (revectoring) operation.
500
For each die i, where i = 0 to n, do.
502
For each plane j, where j = 0 to m, do.
504
Set destination band to last band.
506
Set destination band in destination vector for plane j to the last band.
508
For source band k from a beginning band to a last band, do.
510
512
Is the source band less than the destination band?
No
Go to block 534 in FIG. 5B.
Yes
514
Does the logical address in the source band at i, j, k map to a defective block?
No
Go to block 532 in FIG. 5B.
Yes
516
Is the physical block at the current destination band for plane j good?
No
528
Decrement the destination band.
530
Set the current destination band for plane j in the destination vector to the decremented destination band.
Yes
518
Go to block 520 in FIG. 5B.

FIG. 5A

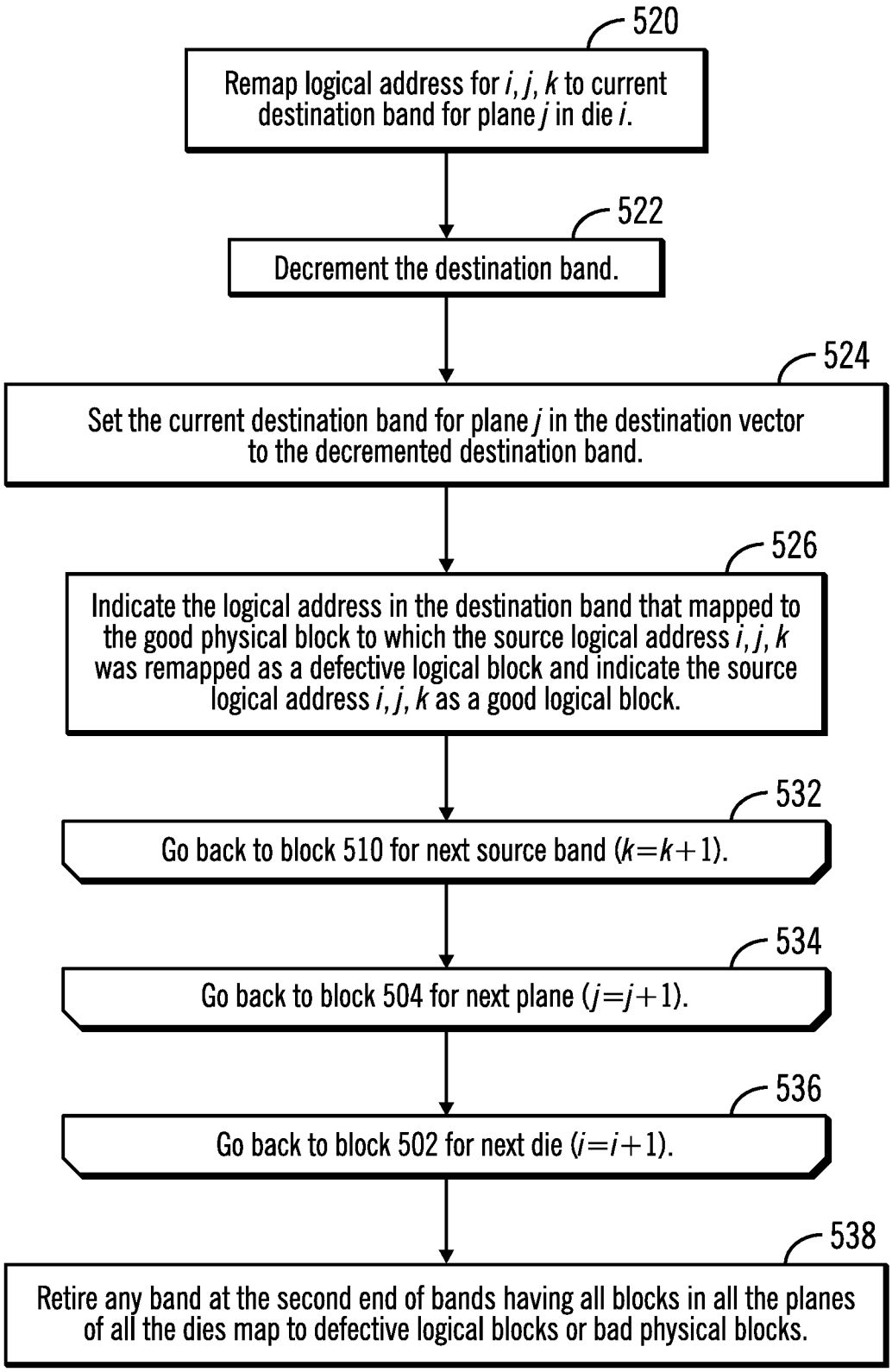

520
Remap logical address for i, j, k to current destination band for plane j in die i.
522
Decrement the destination band.
524
Set the current destination band for plane j in the destination vector to the decremented destination band.
526
Indicate the logical address in the destination band that mapped to the good physical block to which the source logical address i, j, k was remapped as a defective logical block and indicate the source logical address i, j, k as a good logical block.
532
Go back to block 510 for next source band (k=k+1).
534
Go back to block 504 for next plane (j=j+1).
536
Go back to block 502 for next die (i=i+1).
538
Retire any band at the second end of bands having all blocks in all the planes of all the dies map to defective logical blocks or bad physical blocks.

FIG. 5B

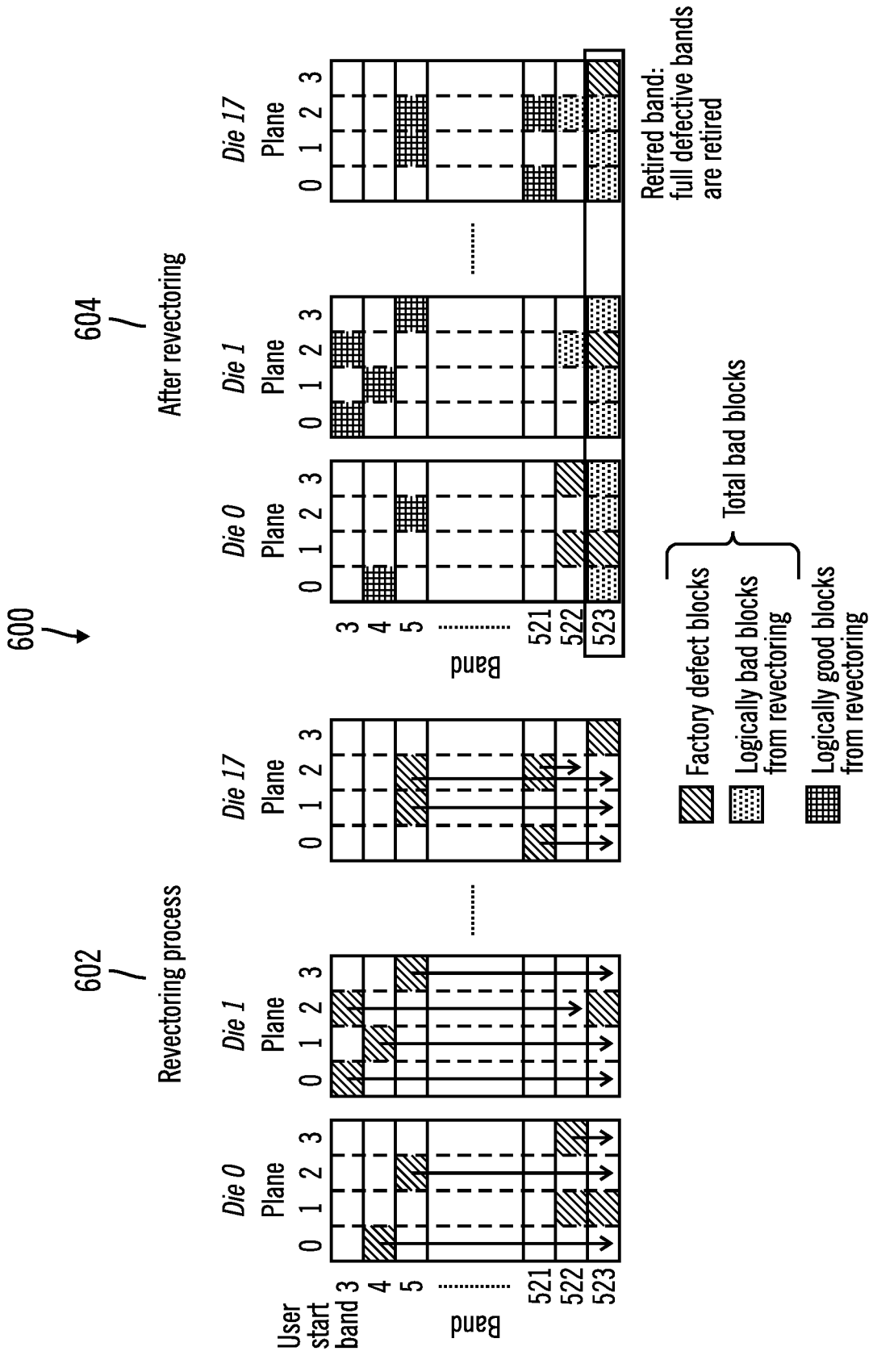

600
602
Revectoring process
604
After revectoring
Die 0
Die 1
Die 17
Plane
0 1 2 3
User start band 3
4
5
521
522
523
Band
Retired band: full defective bands are retired
Factory defect blocks
Logically bad blocks from revectoring
Total bad blocks
Logically good blocks from revectoring

FIG. 6

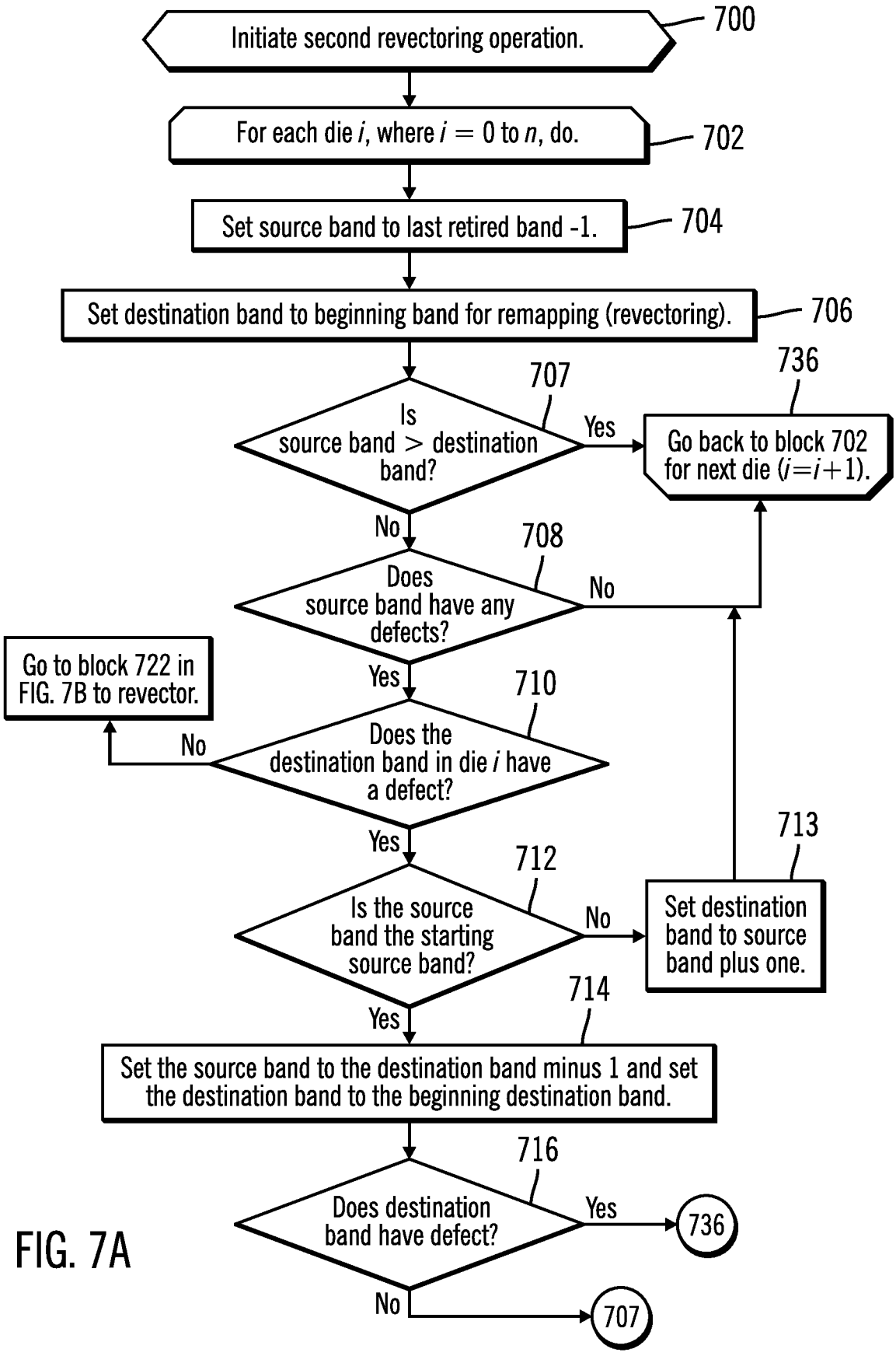

Initiate second revectoring operation.
700
For each die i, where i = 0 to n, do.
702
Set source band to last retired band -1.
704
Set destination band to beginning band for remapping (revectoring).
706
707
Is source band > destination band?
Yes
736
Go back to block 702 for next die (i=i+1).
No
708
Does source band have any defects?
No
Yes
Go to block 722 in FIG. 7B to revector.
710
No
Does the destination band in die i have a defect?
Yes
713
712
Is the source band the starting source band?
No
Set destination band to source band plus one.
Yes
714
Set the source band to the destination band minus 1 and set the destination band to the beginning destination band.
716
Does destination band have defect?
Yes
736
No
707

FIG. 7A

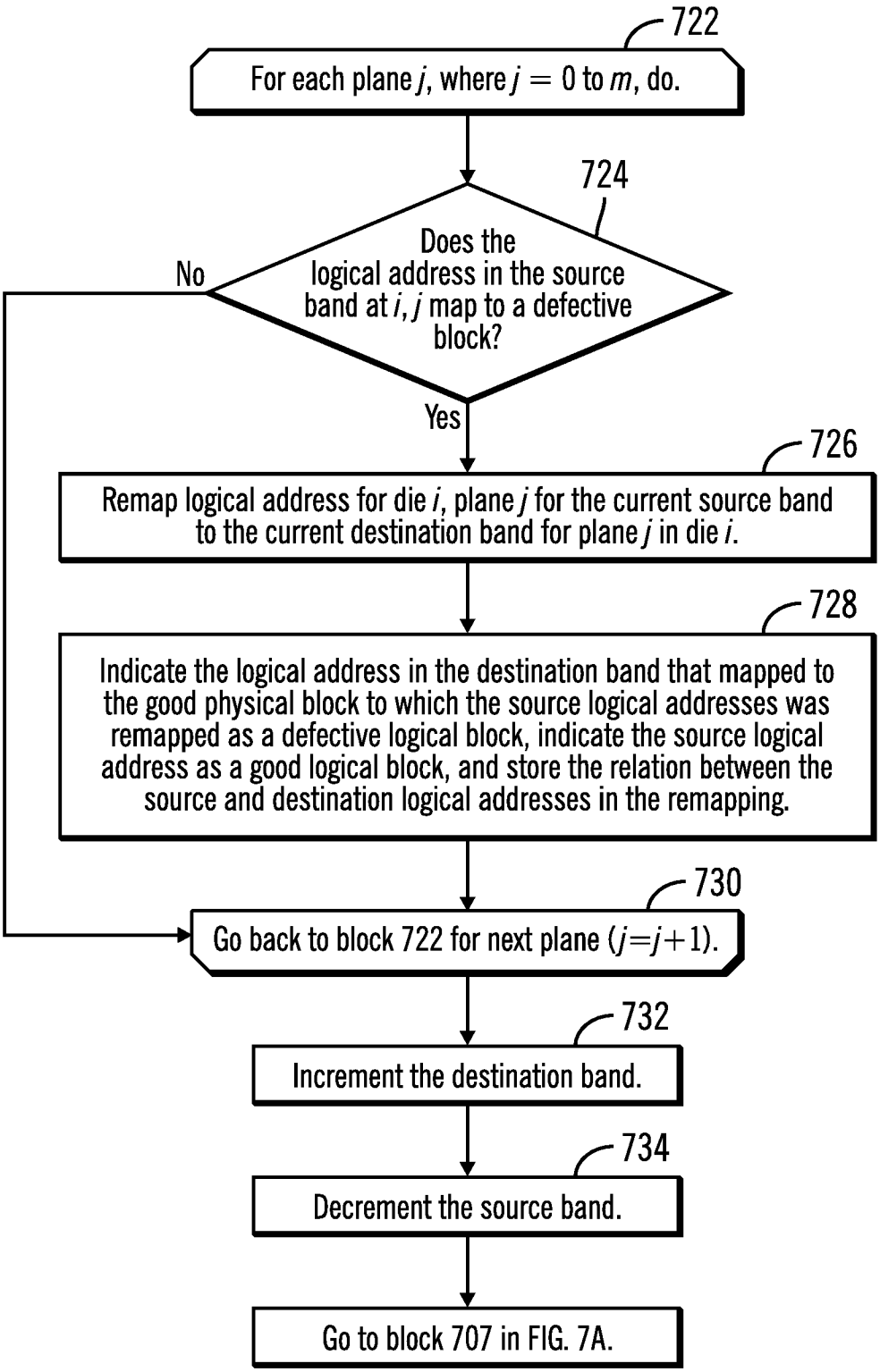

722
For each plane j, where j = 0 to m, do.
724
Does the logical address in the source band at i, j map to a defective block?
No
Yes
726
Remap logical address for die i, plane j for the current source band to the current destination band for plane j in die i.
728
Indicate the logical address in the destination band that mapped to the good physical block to which the source logical addresses was remapped as a defective logical block, indicate the source logical address as a good logical block, and store the relation between the source and destination logical addresses in the remapping.
730
Go back to block 722 for next plane (j=j+1).
732
Increment the destination band.
734
Decrement the source band.
Go to block 707 in FIG. 7A.

FIG. 7B

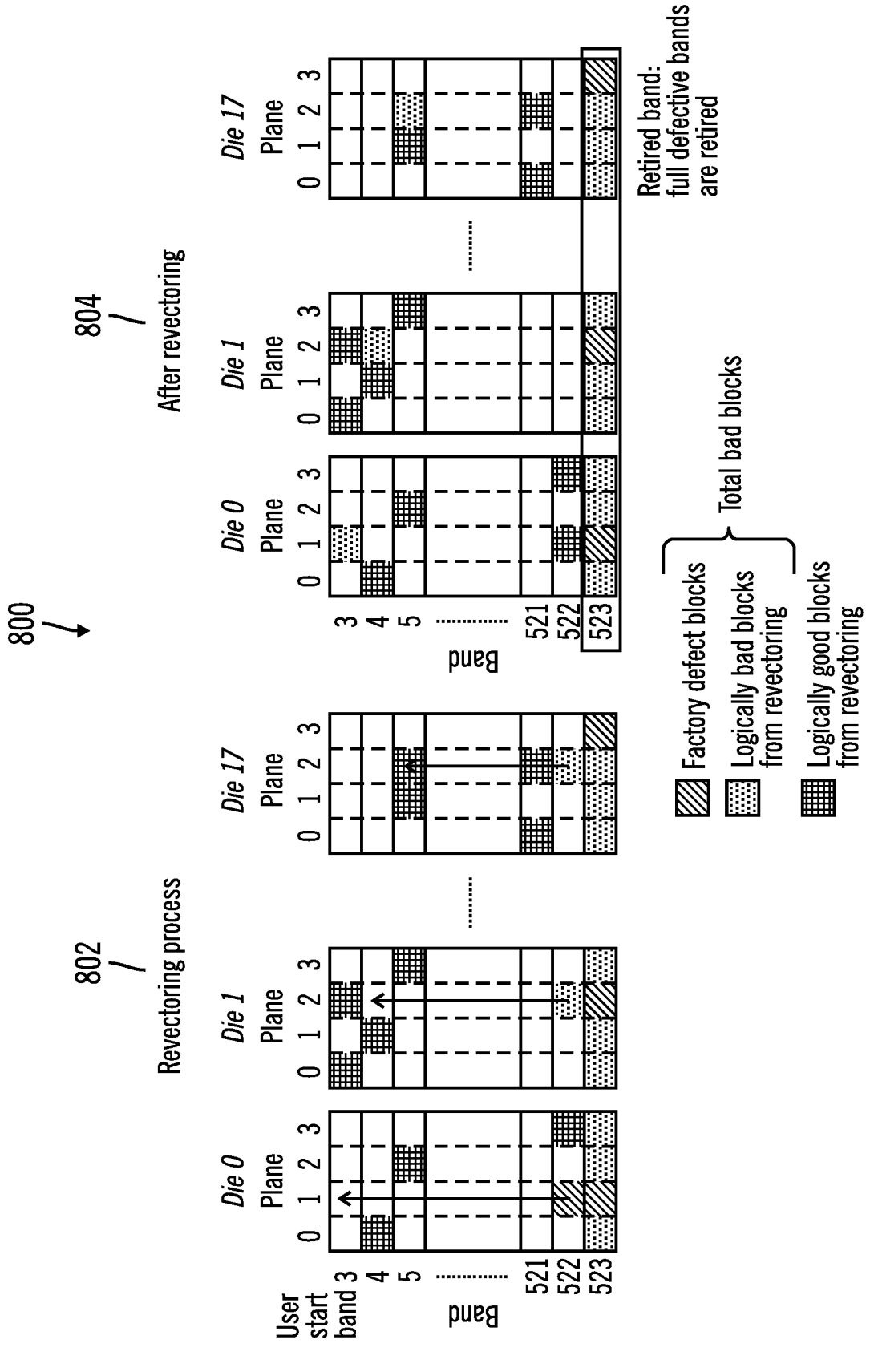

800
802
Revectoring process
804
After revectoring
Die 0
Die 1
Die 17
Plane
0 1 2 3
User start band 3
4
5
521
522
523
Band
Retired band: full defective bands are retired
Factory defect blocks
Logically bad blocks from revectoring
Logically good blocks from revectoring
Total bad blocks

FIG. 8

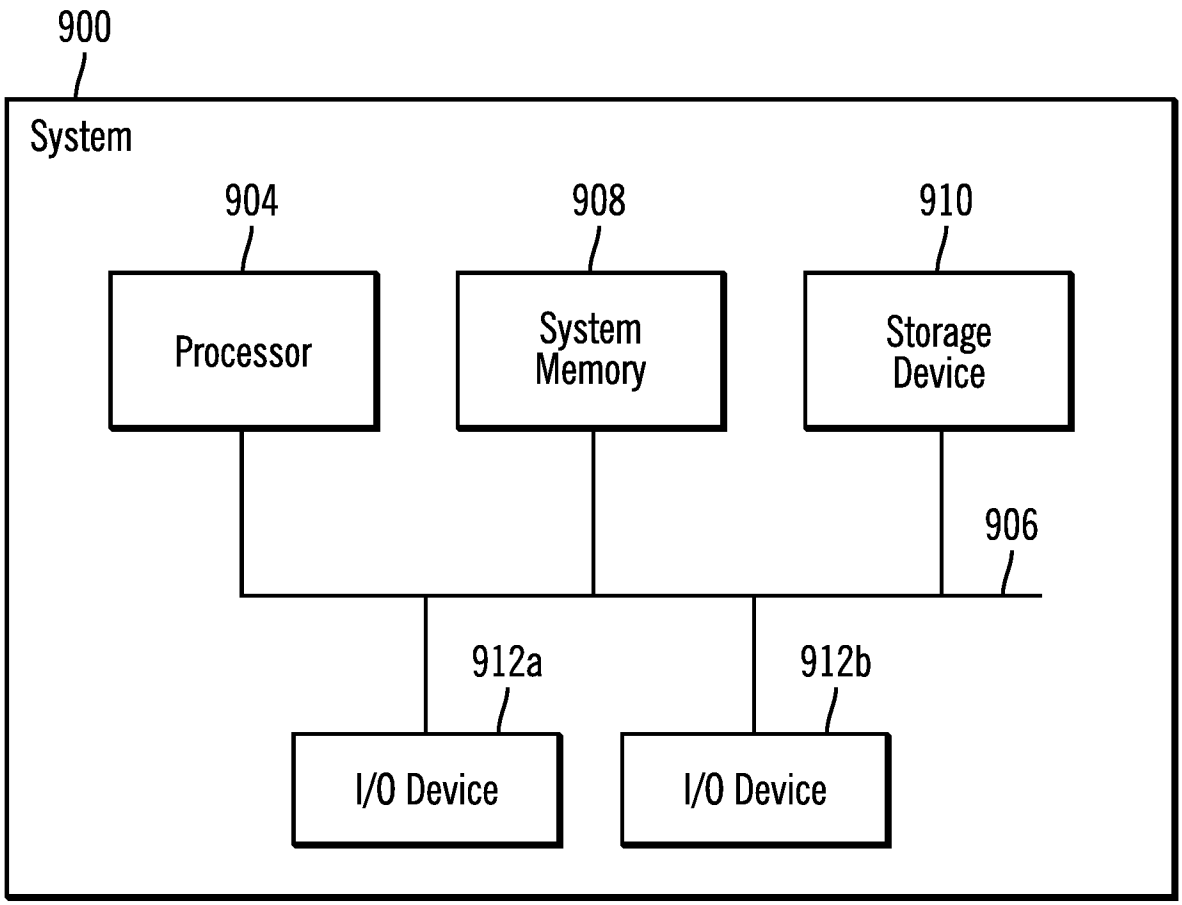

900
System
904
908
910
Processor
System Memory
Storage Device
906
912a
912b
I/O Device
I/O Device

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/041654

A. CLASSIFICATION OF SUBJECT MATTER

G06F 12/02(2006.01)i, G06F 11/07(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 12/02; G11C 16/26; H03M 13/05; G06F 11/10; G06F 11/16; G06F 11/20; G06F 11/07

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: non-volatile memory, band, dies, plane, block, logical-to-physical mapping, remapping, revectoring, defective, retire

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0281687 A1 (APPLE INC.) 18 September 2014 See paragraphs [0018]-[0079]; claims 1, 11; and figures 3-4.	1-25
A	US 2014-0164881 A1 (LSI CORPORATION) 12 June 2014 See paragraphs [0014]-[0054]; and figures 1-4.	1-25
A	US 2015-0149818 A1 (PRANAV KALAVADE et al.) 28 May 2015 See paragraphs [0013]-[0040]; and figures 1a-4.	1-25
A	US 2013-0128666 A1 (CHRIS AVILA et al.) 23 May 2013 See paragraphs [0028]-[0042]; and figures 1A-7.	1-25
A	US 2010-0115376 A1 (OFIR SHALVI et al.) 06 May 2010 See paragraphs [0124]-[0132]; and figure 6.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 October 2016 (07.10.2016)	**11 October 2016 (11.10.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHIN, Sang Bum
Telephone No. +82-42-481-8398

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