**FORMING GATES WITH VARYING LENGTH USING SIDEWALL IMAGE TRANSFER**

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Semiconductor devices and methods of forming the same include forming mandrels on a first region and a second region of a gate layer. First spacers are formed on sidewalls of the mandrels. The mandrels are etched away to expose inner sidewalls of the first spacers. Second spacers are formed on sidewalls of the first spacers. First spacers in only the first region are etched away to expose inner sidewalls of the second spacers in the first region. The gate layer is etched using the remaining first spacers and the second spacers as a mask to form first gates in the first region and second gates in the second region. The first gates have a gate length than the second gates.
Form layers of dummy gate stack 1102

Mask spacers in one region 1112

Form mandrels 1104

Etch away first spacers in unmasked region 1114

Form first spacers on mandrel sidewalls 1106

Etch away mask 1116

Etch away mandrels 1108

Etch dummy gate stack to form dummy gates 1118

Forming second spacers on first spacer sidewalls 1110

Complete devices 1120

FIG. 11
FORMING GATES WITH VARYING LENGTH USING SIDEWALL IMAGE TRANSFER

BACKGROUND

[0001] The present invention relates to semiconductor devices and the formation thereof and, more particularly, to reducing variation between devices by using sidewall image transfer to form gate structures.

Description of the Related Art

[0002] Conventional semiconductor fabrication uses lithography techniques to form structures. The lithography technique used, including for example the lasers and chemicals used in a given photolithography process, dictates limits on the size of features that can be created. In particular, any lithography process will have a minimum feature size that represents the smallest structure that the process can create.

[0003] One result of the physical limits of a lithographic process is line edge roughness. Line edge roughness characterizes variations in a structure below the resolution of the fabrication process. This roughness is unpredictable and is a cause of variation in the operational properties from one device to the next.

[0004] While line edge roughness contributes little to devices that have relatively large structures (e.g., a gate length of about 200 nm), fully depleted channel structures enable gate length scaling to much smaller lengths (e.g., a gate length of about 30 nm or below). At such lengths, line edge roughness can contribute significantly to device variation.

SUMMARY

[0005] A method for forming semiconductor devices includes forming mandrels on a first region and a second region of a gate layer. First spacers are formed on sidewalls of the mandrels. The mandrels are etched away to expose inner sidewalls of the first spacers. Second spacers are formed on sidewalls of the first spacers. First spacers in only the first region are etched away to expose inner sidewalls of the second spacers in the first region. The gate layer is etched using the remaining first spacers and the second spacers as a mask to form first gates in the first region and second gates in the second region. The first gates have a gate length than the second gates.

[0006] A method for forming semiconductor devices includes forming mandrels on a first region and a second region of a gate layer. First spacers are formed on sidewalls of the mandrels. The mandrels are etched away to expose inner sidewalls of the first spacers. Second spacers are formed on sidewalls of the first spacers at a thickness that provides a gap between adjacent second spacers that has a same length as a thickness of the first spacers. The second region is masked and the first spacers are etched away in only the first region to expose inner sidewalls of the second spacers in the first region. The second region is unmasked after etching away first spacers. The gate layer is etched using the remaining first spacers and the second spacers as a mask to form first gates in the first region and second gates in the second region. The first gates have a gate length than the second gates.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0007] A chip includes a plurality of first transistors in a first region and a plurality of second transistors in a second region. A gap between adjacent first transistors has a same width as a gap between adjacent second transistors. Gates of the second transistors have a length substantially the same as twice a length of two adjacent first transistors plus the distance between said two adjacent first transistors.

[0008] These and other features and advantages will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

DETAILED DESCRIPTION

[0009] The disclosure will provide details in the following description of preferred embodiments with reference to the following figures wherein:

[0010] FIG. 1 is a cross-sectional diagram of a step in forming semiconductor devices in accordance with the present principles;

[0011] FIG. 2 is a cross-sectional diagram of a step in forming semiconductor devices in accordance with the present principles;

[0012] FIG. 3 is a cross-sectional diagram of a step in forming semiconductor devices in accordance with the present principles;

[0013] FIG. 4 is a cross-sectional diagram of a step in forming semiconductor devices in accordance with the present principles;

[0014] FIG. 5 is a cross-sectional diagram of a step in forming semiconductor devices in accordance with the present principles;

[0015] FIG. 6 is a cross-sectional diagram of a step in forming semiconductor devices in accordance with the present principles;

[0016] FIG. 7 is a cross-sectional diagram of a step in forming semiconductor devices in accordance with the present principles;

[0017] FIG. 8 is a cross-sectional diagram of a step in forming semiconductor devices in accordance with the present principles;

[0018] FIG. 9 is a cross-sectional diagram of a step in forming semiconductor devices in accordance with the present principles;

[0019] FIG. 10 is a cross-sectional diagram of a step in forming semiconductor devices in accordance with the present principles; and

[0020] FIG. 11 is a block/flow diagram of a method of forming semiconductor devices in accordance with the present principles.

Embodiments of the present invention employ sidewall image transfer to form semiconductor device structures and reduce length variations. In addition, devices having different gate lengths are formed using a single fabrication process. Short feature lengths are formed by employing double sidewall image transfer to form tightly contacted feature pitches, while relatively long feature lengths are formed using sidewall image transfer in the double sidewall image transfer process.

Referring now to the drawings in which like numerals represent the same or similar elements and initially
to FIG. 1, a step in forming a semiconductor device is shown. A semiconductor-on-insulator substrate is formed by an insulator layer 102 and a semiconductor layer 104. In an alternative embodiment, the substrate may be formed from a bulk semiconductor. The semiconductor layer 104 may be a silicon-containing material. Illustrative examples of silicon-containing materials suitable for the semiconductor layer 104 or for a bulk semiconductor may include, but are not limited to, silicon, silicon germanium, silicon carbide, polysilicon, epitaxial silicon, amorphous silicon, and multilayers thereof. Although silicon is predominantly used in wafer fabrication, alternative semiconductor materials can be employed, such as, but not limited to, germanium, gallium nitride, cadmium telluride and zinc selenide.

[0023] Further alternatives for the semiconductor layer 104 include III-V compound semiconductors. The term “III-V compound semiconductor” denotes a semiconductor material that includes at least one element from Group III of the Periodic Table of Elements (International Union of Pure and Applied Chemistry Group 13) and at least one element from Group V of the Periodic Table of Elements (International Union of Pure and Applied Chemistry Group 15). Typically, the III-V compound semiconductors are binary, ternary or quaternary alloys including III-V elements.

Examples of III-V compound semiconductors that can be used in the present embodiments include, but are not limited to alloys of gallium arsenic, aluminum arsenide, indium gallium arsenide, indium aluminum arsenide, indium aluminum arsenic antimonide, indium aluminum arsenic phosphorus, indium gallium arsenic phosphorus and combinations thereof.

[0024] A dummy gate dielectric layer 106 is formed on the semiconductor layer 104. It is specifically contemplated that the dummy gate dielectric layer 106 may be formed from silicon dioxide, but it should be understood that any appropriate insulating material may be used instead. A dummy gate material layer 108 is formed on the dummy gate dielectric layer 106. It is specifically contemplated that the dummy gate material layer 108 may be formed from amorphous silicon, but it should be understood that any material having the appropriate etch selectivity, as discussed below, may be used instead. A hardmask layer 110 is formed on the dummy gate material layer 108. Although it is specifically contemplated that silicon nitride may be used for the hardmask layer 110, any appropriate hardmask material may be used instead. Exemplary alternative hardmask materials include silicon oxides, silicon oxynitrides, silicon carbides, silicon carbonitrides, and spin-on dielectrics such as silsequioxanes, siloxanes, and boron phosphate silicate glass.

[0025] It should be noted that, in an alternative embodiment, the dummy gate dielectric layer 106 and the dummy gate layer 108 may be formed from actual gate materials, as discussed below, rather than the dummy gate materials set out above.

[0026] Each of layers 106, 108, and 110 may be formed by any appropriate deposition process including, e.g., chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), or gas cluster ion beam (GCIB) deposition. CVD is a deposition process in which a deposited species is formed as a result of a chemical reaction between gaseous reactants at greater than room temperature (e.g., from about 25° C. about 900° C.). The solid product of the reaction is deposited on the surface on which a film, coating, or layer of the solid product is to be formed. Variations of CVD processes include, but are not limited to, Atmospheric Pressure CVD (APCVD), Low Pressure CVD (LP CVD), Plasma Enhanced CVD (PECVD), and Metal-Organic CVD (MOCVD) and combinations thereof may also be employed. In alternative embodiments that use PVD, a sputtering apparatus may include direct-current diode systems, radio frequency sputtering, magnetron sputtering, or ionized metal plasma sputtering. In alternative embodiments that use ALD, chemical precursors react with the surface of a material one at a time to deposit a thin film on the surface. In alternative embodiments that use GCIB deposition, a high-pressure gas is allowed to expand in a vacuum, subsequently condensing into clusters. The clusters can be ionized and directed onto a surface, providing a highly anisotropic deposition.

[0027] Referring now to FIG. 2, a step in forming a semiconductor device is shown. The figure shows two regions, a first region 202 and a second region 204. The first region 202 is used to form, e.g., digital logic devices, while the second region is used to form, e.g., analog devices. This distinction is relevant because devices used in digital logic and static random access memory (SRAM) may benefit from having shorter gate lengths, while analog devices and embedded dynamic random access memory (eDRAM) may benefit from longer gate lengths.

[0028] Mandrels 206 are formed on the hardmask layer 110. It is specifically contemplated that the mandrels 206 may be formed from amorphous silicon, but it should be understood that any appropriate material with an appropriate etch selectivity, as described below, will be appropriate. The mandrels 206 may be formed by any appropriate lithographic process. In particular, a layer of mandrel material may be deposited on the hardmask layer 110 and subsequently etched using photolithography to define the mandrels 206. Although it is specifically contemplated that the lateral length of the mandrels 206 can range from about 50 nm to about 100 nm, greater and lesser lengths are also contemplated.

[0029] Referring now to FIG. 3, a step in forming a semiconductor device is shown. First spacers 302 are formed on the sidewalls of the mandrels 206. The first spacers 302 may have an exemplary thickness of about 12 nm to about 50 nm, but it is also contemplated that the thickness may be thicker or thinner. It is specifically contemplated that amorphous carbon may be used to form the first spacers 302, but it should be understood that any alternative material may be used that has etch selectivity with the hardmask 110 and the mandrels 206. As used herein, the term “etch selectivity” in reference to a material removal process denotes the rate of material removal for a first material is greater than the rate of removal for at least another material of the structure to which the material removal process is being applied.

[0030] The first spacers 302 may be formed by conformally depositing a layer of spacer material using, e.g., CVD, and then using a timed, anisotropic etch to remove the spacer material from horizontal surfaces. One exemplary etch includes reactive ion etching (RIE). Reactive Ion Etching (RIE) is a form of plasma etching in which etching the surface to be etched is placed on the RF-powered electrode. Moreover, during RIE the surface to be etched takes on a potential that accelerates the etching species extracted from plasma toward the surface, in which the
chemical etching reaction is taking place in the direction normal to the surface. Other examples of anisotropic etching that can be used at this point of the present invention include ion beam etching, plasma etching or laser ablation.

[0031] Referring now to FIG. 4, a step in forming a semiconductor device is shown. The mandrels 206 from both the first region 202 and the second region 204 are removed using, e.g., a wet or dry etch that is selective to the mandrel material. The etch exposes the inner sidewalls of first spacers 302. The first spacers 302 then become the mandrels for the next step. In one embodiment, where the mandrel material is amorphous silicon and the first spacer is amorphous carbon, an amorphous silicon mandrel can selectively be removed by an aqueous solution containing ammonia.

[0032] Referring now to FIG. 5, a step in forming a semiconductor device is shown. Second spacers 502 are formed on the sidewalls of the first spacers 302. The second spacers may have an exemplary thickness between about 10 nm and about 30 nm, but greater and lesser thicknesses are also contemplated. It is specifically contemplated that an oxide such as silicon dioxide may be used to form the second spacers 502, but it should be understood that any appropriate material that has etch selectivity with the first spacers 302 may be used. It is specifically contemplated that the second spacers 502 are formed to a thickness such that a gap 504 between the second spacers 502 of adjacent structures has a same length as the thickness of the first spacers 302. The second spacers 502 may be formed by conformally depositing a layer of spacer material using, e.g., CVD, and then using a timed, anisotropic etch such as RIE to remove the spacer material from horizontal surfaces.

[0033] Referring now to FIG. 6, a step in forming a semiconductor device is shown. The second region 204 is masked with mask 602. The mask 602 may be formed from any appropriate masking material that has etch selectivity with the first spacers 302 and the second spacers 502.

[0034] Referring now to FIG. 7, a step in forming a semiconductor device is shown. The first spacers 302 in the first region 202 are removed using, e.g., a wet or dry etch that is selective to the first spacer material and does not affect the second spacer material. The etch exposes the inner sidewalls of second spacers 502 in the first region 202 and leaves the short structures 504. The first spacers 302 in the second region 204 are unaffected due to the presence of the mask 602.

[0035] In an embodiment where the first spacers 302 are formed from amorphous carbon, they can be removed by using a plasma etch process that includes oxygen plasma. Alternatively, amorphous carbon can be selectively removed using a dry etch with nitrogen and hydrogen.

[0036] Referring now to FIG. 8, a step in forming a semiconductor device is shown. The hardmask layer 110 and the dummy gate layer 108 are anisotropically etched using, e.g., RIE to remove material outside that covered by the first spacers 302 or by the second spacers 502. This produces relatively short structures 902 in the first region 202, where only the second spacers 502 remain, and relatively long structures 904 in the second region 204, where the first spacers 302 and the second spacers 502 combined define the device length. While it is specifically contemplated that the short structures 902 and long structures 904 represent dummy gate structures to be used toward the eventual formation of transistor devices, it should be understood that other semiconductor structures may be used instead. It should also be noted that the length of the short structures 902 is dictated solely by the thickness of the second spacers 502, while the length of the long structures 904 is dictated by twice the thickness of the second spacers 502 plus the thickness of the first spacers 302.

[0038] Referring now to FIG. 10, a final step in the formation of semiconductor devices is shown. The dummy gates 902 and 904 have been replaced by full gate stacks. Each gate stack includes a gate dielectric 1004. The gate stack of the first region 202 has a gate 1002 with a shorter gate length than the gate 1008 in the gate stack of the second region 204. A gate spacer 1006 is formed over the gate stack. It should be noted that, in an embodiment that uses real gate materials for the starting gate stack, this replacement gate step can be omitted.

[0039] As used herein, a “gate dielectric” is a layer of an insulator between the semiconductor layer 204 and the gate conductor 1002/1008. It is specifically contemplated that the gate dielectric may be a high-k dielectric, but any appropriate insulating material may be used instead. A high-k dielectric is a material having a dielectric constant k that is greater than that of silicon dioxide. Exemplary high-k dielectric materials include hafnium oxides, zirconium oxides, lanthanum oxides, aluminum oxides, titanium oxides, strontium titanate oxides, lanthanum aluminum oxides, yttrium oxides, hafnium oxynitrides, zirconium oxynitrides, lanthanum oxynitrides, aluminum oxynitrides, titanium oxynitrides, strontium titanium oxynitrides, lanthanum aluminum oxynitrides, yttrium oxynitrides, and multilayers thereof.

[0040] The gates 1002/1008 themselves may be formed from any appropriate gate material. In one exemplary embodiment, the gates 1002/1008 may be formed from polysilicon, but it should be understood that alternative gate materials may include polycrystalline germanium, polysilicon/metal silicide, germanium, silicon germanium, silicon germanium carbide, metal silicides, metallic nitrides, metals such as tungsten, iridium, rhenium, ruthenium, titanium, tantalum, hafnium, molybdenum, niobium, nickel, or aluminum, or any other appropriate conductive material.

[0041] Additional structures may be formed in the semiconductor layer 104 including, e.g., doped source and drain regions 1010. Doped source and drain regions 1010 are formed by implanting dopant atoms in the semiconductor layer and may be of either p-type or n-type. As used herein, “p-type” refers to the addition of impurities to an intrinsic semiconductor that creates deficiencies of valence electrons. In a group-IV semiconductor substrate, examples of p-type dopants, i.e., impurities, include but are not limited to: boron, aluminum, gallium and indium. As used herein, “n-type” refers to the addition of impurities that contributes free electrons to an intrinsic semiconductor. In a silicon containing substrate example of n-type dopants, i.e., impurities, include but are not limited to antimony, arsenic and phosphorous. The concentration of dopant within the doped region may for example be from about 1011 to about 1015 atoms/cm².

[0042] Electrical contacts (not shown) are formed to contact the source/drain regions 1010 and the gates 1002/1008 as appropriate to complete the device. Contact formation may include the formation of a silicide on the surfaces of the
source/drain regions 1010 and the gates 1002/1008. Silicide formation may include deposition of a refractory metal such as nickel or titanium onto the surface of a silicon-containing material or wafer. Following deposition, the structure is then subjected to an anneal using for example by rapid thermal annealing. During thermal annealing, the deposited metal reacts with silicon forming a conductive metal silicide.

[0043] It should be noted that the present embodiments describe fin field effect transistors (FinFETs). It should be understood that, while tall, narrow fin gates are specifically contemplated, any appropriate fin geometry may be used instead.

[0044] It is to be understood that the present invention will be described in terms of a given illustrative architecture having a wafer; however, other architectures, structures, substrate materials and process features and steps may be varied within the scope of the present invention.

[0045] It will also be understood that when an element such as a layer, region or substrate is referred to as being “on” or “over” another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” or “directly over” another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present.

[0046] A design for an integrated circuit chip may be created in a graphical computer programming language, and stored in a computer storage medium (such as a disk, tape, physical hard drive, or virtual hard drive such as in a storage access network). If the designer does not fabricate chips or the photolithographic masks used to fabricate chips, the designer may transmit the resulting design by physical means (e.g., by providing a copy of the storage medium storing the design) or electronically (e.g., through the Internet) to such entities, directly or indirectly. The stored design is then converted into the appropriate format (e.g., GDSII) for the fabrication of photolithographic masks, which typically include multiple copies of the chip design in question that are to be formed on a wafer. The photolithographic masks are utilized to define areas of the wafer (and/or the layers thereon) to be etched or otherwise processed.

[0047] Methods as described herein may be used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

[0048] Reference in the specification to “one embodiment” or “an embodiment” of the present principles, as well as other variations thereof, means that a particular feature, structure, characteristic, and so forth described in connection with the embodiment is included in at least one embodiment of the present principles. Thus, the appearances of the phrase “in one embodiment” or “in an embodiment”, as well any other variations, appearing in various places throughout the specification are not necessarily all referring to the same embodiment.

[0049] It is to be appreciated that the use of any of the following “/”, “and/or”, and “at least one of”, for example, in the cases of “A/B”, “A and/or B” and “at least one of A and B”, is intended to encompass the selection of the first listed option (A) only, or the selection of the second listed option (B) only, or the selection of both options (A and B). As a further example, in the cases of “A, B, and/or C” and “at least one of A, B, and C”, such phrasing is intended to encompass the selection of the first listed option (A) only, or the selection of the second listed option (B) only, or the selection of the third listed option (C) only, or the selection of the first and the second listed options (A and B) only, or the selection of the first and third listed options (A and C) only, or the selection of the second and third listed options (B and C) only, or the selection of all three options (A and B and C). This may be extended, as readily apparent by one of ordinary skill in this and related arts, for as many items listed.

[0050] Referring now to FIG. 11, a method of forming semiconductor devices is shown. Block 1102 forms the layers of the dummy gate stack shown in FIG. 1. In particular, block 1102 forms the dummy gate dielectric 106, the dummy gate layer 108, and the hardmask layer 110 using, e.g., successive CVD processes. Block 1104 deposits mandrels 206 on the hardmask layer 110 using any appropriate lithographic process.

[0051] Block 1106 forms the first spacers 302 on the sidewalls of mandrels 206. This may be performed by conformally depositing the material of the first spacers 302 (e.g., amorphous carbon) using a CVD process and then using a timed anisotropic etch to remove the first spacer material from the horizontal surfaces. Block 1108 etches away the mandrels 206 using any appropriate etch process, exposing the inner sidewalls of the first spacers 302.

[0052] Block 1110 forms the second spacers 502 on the sidewalls of the first spacers 302. This may be performed by conformally depositing the material of the first spacers 302 (e.g., amorphous carbon) using a CVD process and then using a timed anisotropic etch to remove the second spacer material from the horizontal surfaces. Block 1112 then masks the spacers in, e.g., second region 204 while block 1114 etches away the first spacers 302 in unmasked first region 202. Block 1116 etches away the mask by any appropriate etching process.

[0053] Block 1118 etches down into the dummy gate stack using the remaining first spacers 302 and the second spacers 502 as a mask. This etch is an anisotropic etch that leaves dummy gates 902 and 904 in place, with the dummy gates 902 in the first region 202 having a shorter gate length than the dummy gates 904 in the second region 204. Block 1120 completes the transistor devices by replacing the dummy gates 902/904 with true gates 1092/1098, forming source/drain regions 1010, and forming electrical contacts as needed.
Having described preferred embodiments of forming gates with varying length using sidewall image transfer (which are intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments disclosed which are within the scope of the invention as outlined by the appended claims. Having thus described aspects of the invention, with the details and particularity required by the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.

1. A method for forming semiconductor devices, comprising:
   forming mandrels on a first region and a second region of a gate layer;
   forming first spacers on sidewalls of the mandrels;
   etching away the mandrels to expose inner sidewalls of the first spacers;
   forming second spacers on sidewalls of the first spacers;
   etching away first spacers in only the first region to expose inner sidewalls of the second spacers in the first region;
   and
   etching the gate layer using the remaining first spacers and the second spacers as a mask to form first gates in the first region and second gates in the second region, wherein the first gates have a smaller gate length than a gate length of the second gates.

2. The method of claim 1, further comprising masking the second region before etching away the first spacers.

3. The method of claim 2, further comprising unmasking the second region after etching away the first spacers.

4. The method of claim 1, wherein the first gates and second gates are dummy gates.

5. The method of claim 4, further comprising replacing the first dummy gates and the second dummy gates with respective first and second transistor gate stacks having gate lengths equal to the gate lengths of the respective first and second dummy gates.

6. The method of claim 5, further comprising forming a gate dielectric before replacing the first and second dummy gates.

7. The method of claim 1, wherein the mandrels are formed from amorphous silicon, the first spacers are formed from amorphous carbon, and the second spacers are formed from an oxide.

8. The method of claim 1, wherein forming the second spacers comprises forming the second spacers at a thickness that provides a gap between adjacent second spacers that has a same length as a thickness of the first spacers.

9. The method of claim 1, further comprising forming source and drain regions on a substrate layer under the gate layer.

10. A method for forming semiconductor devices, comprising:
    forming mandrels on a first region and a second region of a gate layer;
    forming first spacers on sidewalls of the mandrels;
    etching away the mandrels to expose inner sidewalls of the first spacers;
    forming second spacers on sidewalls of the first spacers;
    etching away first spacers in only the first region to expose inner sidewalls of the first spacers;
    forming second spacers on sidewalls of the first spacers;
    etching away first spacers in only the first region to expose inner sidewalls of the second spacers in the first region;
    unmasking the second region after etching away first spacers;
    and
    etching the gate layer using the remaining first spacers and the second spacers as a mask to form first gates in the first region and second gates in the second region, wherein the first gates have a gate length greater than a gate length of the second gates.

11. The method of claim 10, wherein the first gates and second gates are dummy gates.

12. The method of claim 11, further comprising replacing the first dummy gates and the second dummy gates with respective first and second transistor gate stacks having gate lengths equal to the gate lengths of the respective first and second dummy gates.

13. The method of claim 12, further comprising forming a gate dielectric before replacing the first and second dummy gates.

14. The method of claim 10, wherein the mandrels are formed from amorphous silicon, the first spacers are formed from amorphous carbon, and the second spacers are formed from an oxide.

15. The method of claim 10, further comprising forming source and drain regions on a substrate layer under the gate layer.

16-20. (canceled)

21. A method for forming semiconductor devices, comprising:
    forming amorphous silicon mandrels on a first region and a second region of a gate layer;
    forming amorphous carbon first spacers on sidewalls of the mandrels;
    etching away the mandrels to expose inner sidewalls of the first spacers;
    forming oxide second spacers on sidewalls of the first spacers at a thickness that provides a gap between adjacent second spacers that has a same length as a thickness of the first spacers;
    masking the second region;
    etching away first spacers in only the first region to expose inner sidewalls of the second spacers in the first region;
    unmasking the second region after etching away first spacers; and
    etching the gate layer using the remaining first spacers and the second spacers as a mask to form first gates in the first region and second gates in the second region, wherein the first gates have a gate length greater than a gate length of the second gates.

22. The method of claim 21, wherein the first gates and second gates are dummy gates.

23. The method of claim 22, further comprising replacing the first dummy gates and the second dummy gates with respective first and second transistor gate stacks having gate lengths equal to the gate lengths of the respective first and second dummy gates.

24. The method of claim 23, further comprising forming a gate dielectric before replacing the first and second dummy gates.

25. The method of claim 21, further comprising forming source and drain regions on a substrate layer under the gate layer.