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(54) Title: WORD LINE CONTROL METHOD, WORD LINE CONTROL CIRCUIT DEVICE AND SEMICONDUCTOR MEMORY

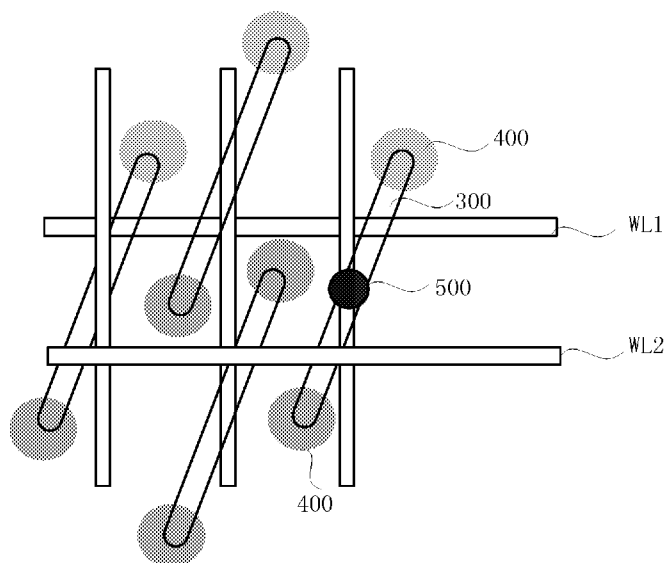


FIG. 2

(57) Abstract: A word line control method, a word line control circuit device, and a semiconductor memory are provided. The method includes: acquiring a row address input signal; acquiring a test mode signal; performing logical and decoding operations on the row address input signal and the test mode signal to generate a row address control signal, wherein the row address control signal includes at least two valid activation signals; and simultaneously activating at least two non-adjacent word lines based on the at least two valid activation signals. The row address control signal obtained allows simultaneous activation of at least two non-adjacent word lines. Since none of any two non-adjacent word lines share a common contact area, a test will not be affected by the disconnection of a contact area or the presence of high impedance, thus improving test accuracy.

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WORD LINE CONTROL METHOD, WORD LINE CONTROL CIRCUIT DEVICE AND SEMICONDUCTOR MEMORY

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based on and claims priority of the Chinese Patent Application No. 201811351053.2, filed on November 14, 2018 and entitled “WORD LINE CONTROL METHOD, WORD LINE CONTROL CIRCUIT DEVICE AND SEMICONDUCTOR MEMORY.” The above-referenced application is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present invention relates generally to the field of semiconductor integrated circuit (IC) technologies, and more specifically, to a word line control method, a word line control circuit device and a semiconductor memory.

BACKGROUND

[0003] A finished memory chip usually has some defects, such as low storage capacitance, wherein the capacitance of each storage capacitor may be half of that of a standard storage capacitor, or disconnection of contact area or presence of high impedance between storage capacitors. Those skilled in the art usually resort to certain tests to identify those defects. For example, in order to determine whether the capacitance of a storage capacitor is low, the current common practice is to simultaneously activate two capacitors by activating two adjacent word lines each connecting to the respective one of the two capacitors. If the measured capacitance is equal to the standard storage capacitance, it can be determined that both of the two storage capacitors are defective with low capacitance. To simultaneously activate two adjacent word lines is based on the consideration that tests can still be completed in case of the malfunction of one of the two word lines. Thus, if the measured capacitance is lower than the standard

storage capacitance, it can be determined that one of the storage capacitors is defective with low capacitance.

[0004] However, the abovementioned approach is not perfect in identifying low storage capacitance. Since two adjacent storage capacitors share a same contact area, once the contact area malfunctions, it is no longer possible to ascertain whether the storage capacitors are defective with low capacitance by activating either one or both of the word lines.

[0005] It is to be noted that the information disclosed in this Background section is only for providing a better understanding of the background or context of the present invention, and therefore may contain information that does not form the prior art that is already known to a person of ordinary skill in the art.

SUMMARY

[0006] The present invention provides a word line control method, a word line control circuit device, and a semiconductor memory, to overcome or mitigate one or more of the problems described in the Background section.

[0007] In one aspect, an embodiment of the present invention provides a word line control method. The word line control method may comprise: acquiring a row address input signal; performing logical and decoding operations on the row address input signal to generate a row address control signal; and simultaneously activating at least two non-adjacent word lines based on the at least two valid activation signals. The row address control signal may include at least two valid activation signals.

[0008] In some embodiments, the aforementioned method may further comprise: acquiring a test mode signal. Performing logical and decoding operations on the row address input signal to generate a row address control signal may comprise: performing the logical and decoding operations on the row address input signal and the test mode signal to generate the row address control signal.

[0009] In some embodiments, the row address input signal may include a plurality of row

address signals. Performing logical and decoding operations on the row address input signal and the test mode signal to generate a row address control signal may comprise: performing an inverse operation on the test mode signal to generate an inverted test signal; selecting one of the plurality of row address signals, and performing a NAND operation on the selected row address signal and the inverted test signal to generate an inverted output row address; performing inverse operations on all the row address signals to generate corresponding inverted row address signals; performing a NAND operation on the inverted row address signal corresponding to the selected row address signal and the inverted test signal to generate a non-inverted output row address; and decoding the inverted output row address, the non-inverted output row address, unselected row address signals and unselected inverted row address signals to obtain the row address control signal.

[0010] In some embodiments, decoding the inverted output row address, the non-inverted output row address, unselected row address signals and unselected inverted row address signals to obtain the row address control signal may comprise: performing a primary decoding process on the inverted output row address, the non-inverted output row address, the unselected row address signals and the unselected inverted row address signals to obtain a first row address control signal; and performing a secondary decoding process on the first row address control signal to obtain a second row address control signal, configured for simultaneously activating the at least two non-adjacent word lines. The first row address control signal may include the at least two valid activation signals, configured for simultaneously activating the at least two non-adjacent word lines.

[0011] In a second aspect, an embodiment of the present invention provides a word line control circuit device. The word line control circuit device may comprise a test mode input circuit, a row address input circuit, and a logic decoding processor. The test mode input circuit may have an output coupled, together with an output of the row address input circuit, to a signal input of the logic decoding processor. The logic decoding processor may have a signal output coupled to a plurality of word lines in a memory array. The test mode input circuit may be

configured to receive a test mode signal. The row address input circuit may be configured to receive a plurality of row address signals, and the logic decoding processor may be configured to perform logical and decoding operations on the plurality of row address signals and the test mode signal to generate a row address control signal. The row address control signal may include at least two valid activation signals, configured for simultaneously activating at least two non-adjacent word lines.

[0012] In some embodiments, the test mode input circuit may comprise a test mode input, a first inverter, and a test mode output. The test mode input may be configured to receive the test mode signal. The first inverter may be configured to perform an inverse operation on the test mode signal to generate an inverted test signal. The test mode output may be configured to output the inverted test signal.

[0013] In some embodiments, the row address input circuit may comprise a plurality of row address signal lines, and a plurality of second inverters coupled to the corresponding one of the row address signal lines, respectively. Each of the row address signal lines may be configured to receive the corresponding one of the row address signals from the row address input signal, respectively. The second inverters may be configured to perform inverse operations on the row address signals to generate a plurality of inverted row address signals.

[0014] In some embodiments, the logic decoding processor may comprise a first NAND gate, a second NAND gate, and a decoding device. The first NAND gate may be configured to perform a NAND operation on the selected one of the row address signals and the inverted test signal to generate an inverted output row address. The first NAND gate may include a first input coupled to the one of the row address signal lines corresponding to the selected row address signal, a second input coupled to the test mode output and configured to receive the inverted test signal, and a first output. The second NAND gate may be configured to perform a NAND operation on one of the inverted row address signals corresponding to the selected row address signal and the inverted test signal to generate a non-inverted output row address. The second NAND gate may include a third input coupled to an output of one of the second

inverters corresponding to the selected row address signal, a fourth input coupled to the test mode output, and a second output. The decoding device may be configured to decode the inverted output row address, non-inverted output row address, unselected row address signals and unselected inverted row address signals to obtain the row address control signal. The row address control signal may include the at least two valid activation signals, configured for simultaneously activating at least two non-adjacent word lines.

[0015] In some embodiments, the decoding device may comprise a first decoder. The first decoder may have a set of non-inverted inputs and a set of inverted inputs. The first output may be coupled to a corresponding one of the inverted inputs, and the second output may be coupled to a corresponding one of the non-inverted inputs.

[0016] In some embodiments, the decoding device may further comprise a second decoder and a third decoder. The second decoder may have a set of non-inverted inputs configured for receiving the unselected row address signals, and a set of inverted inputs configured for receiving the unselected inverted row address signals. The third decoder may have a set of non-inverted inputs configured for receiving the unselected row address signals, and a set of inverted inputs configured for receiving the unselected inverted row address signals.

[0017] In some embodiments, the decoding device may further comprise a fourth decoder. The fourth decoder may have inputs coupled to the output of the first decoder, the second decoder and the third decoder. The inputs of the first decoder, the second decoder and the third decoder may constitute the signal input of the logic decoding processor. The fourth decoder may have outputs constituting the signal output of the logic decoding processor that is coupled to the word lines.

[0018] The present invention further provides a semiconductor memory. The semiconductor memory may comprise a word line control circuit device. The word line control circuit device may comprise a row address input circuit and a logic decoding processor. The logic decoding processor may have a signal output coupled to a plurality of word lines in a memory array. The row address input circuit may be configured to receive a plurality of row address signals, and

the logic decoding processor may be configured to perform logical and decoding operations on the plurality of row address signals to generate a row address control signal. The row address control signal may include at least two valid activation signals, configured for simultaneously activating at least two non-adjacent word lines.

[0019] In some embodiments, the word line control circuit device may further comprise a test mode input circuit configured to receive a test mode signal. The logic decoding processor may be configured to perform logical and decoding operations on the plurality of row address signals and the test mode signal to generate the row address control signal. The test mode input circuit may have an output coupled, together with an output of the row address input circuit, to a signal input of the logic decoding processor.

[0020] In some embodiments, in the word line control circuit device, the test mode input circuit may comprise a test mode input, a first inverter, and a test mode output. The test mode input may be configured to receive the test mode signal. The first inverter may be configured to perform an inverse operation on the test mode signal to generate an inverted test signal. The test mode output may be configured to output the inverted test signal.

[0021] In some embodiments, in the word line control circuit device, the row address input circuit may comprise a plurality of row address signal lines, and a plurality of second inverters coupled to the corresponding one of the row address signal lines, respectively. Each of the row address signal lines may be configured to receive the corresponding one of the row address signals from the row address input signal, respectively. The second inverters may be configured to perform inverse operations on the row address signals to generate a plurality of inverted row address signals.

[0022] In some embodiments, in the word line control circuit device, the logic decoding processor may comprise a first NAND gate, a second NAND gate, and a decoding device. The first NAND gate may be configured to perform a NAND operation on the selected one of the row address signals and the inverted test signal to generate an inverted output row address. The first NAND gate may include a first input coupled to the one of the row address signal lines

corresponding to the selected row address signal, a second input coupled to the test mode output and configured to receive the inverted test signal, and a first output. The second NAND gate may be configured to perform a NAND operation on one of the inverted row address signals corresponding to the selected row address signal and the inverted test signal to generate a non-inverted output row address. The second NAND gate may include a third input coupled to an output of one of the second inverters corresponding to the selected row address signal, a fourth input coupled to the test mode output, and a second output. The decoding device may be configured to decode the inverted output row address, non-inverted output row address, unselected row address signals and unselected inverted row address signals to obtain the row address control signal. The row address control signal may include the at least two valid activation signals, configured for simultaneously activating at least two non-adjacent word lines.

[0023] In some embodiments, in the word line control circuit device, the decoding device may comprise a first decoder. The first decoder may have a set of non-inverted inputs and a set of inverted inputs. The first output may be coupled to a corresponding one of the inverted inputs, and the second output may be coupled to a corresponding one of the non-inverted inputs.

[0024] In some embodiments, in the word line control circuit device, the decoding device may further comprise a second decoder and a third decoder. The second decoder may have a set of non-inverted inputs configured for receiving the unselected row address signals, and a set of inverted inputs configured for receiving the unselected inverted row address signals. The third decoder may have a set of non-inverted inputs configured for receiving the unselected row address signals, and a set of inverted inputs configured for receiving the unselected inverted row address signals.

[0025] In some embodiments, in the word line control circuit device, the decoding device may further comprise a fourth decoder. The fourth decoder may have inputs coupled to the output of the first decoder, the second decoder and the third decoder. The inputs of the first decoder, the second decoder and the third decoder may constitute the signal input of the logic

decoding processor. The fourth decoder may have outputs constituting the signal output of the logic decoding processor that is coupled to the word lines.

[0026] The technical solutions provided by the present invention offer the following advantages: the row address control signal obtained, under test mode, from the logical and decoding operations performed on the row address input signal and the test mode signal enable simultaneous activation of at least two non-adjacent word lines. Since none of any two non-adjacent word lines share a common contact area, the tests will not be affected by disconnection of the contact area or presence of high impedance, thus improving test accuracy.

[0027] The information disclosed in this Summary section is illustrative only and is not restrictive of the present invention in any way. In addition to the above illustrative aspects, embodiments and features, further aspects, embodiments and features will become readily apparent by reference to the appended drawings and following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] Unless otherwise specified, the same reference numbers used throughout the appended drawings refer to the same or analogous components or elements. And the appended drawings are not necessarily drawn to scale. It is to be understood that these appended drawings present only some embodiments of the present invention, and shall not be construed as a limitation to the scope of the present invention.

[0029] Fig. 1 is a schematic flowchart of a word line control method in accordance with one embodiment of the present invention.

[0030] Fig. 2 is a schematic diagram showing a structure of the word lines in accordance with prior arts.

[0031] Fig. 3 is a schematic diagram showing a structure of the word lines in accordance with one embodiment of the present invention.

[0032] Fig. 4 is a schematic flowchart of another word line control method in accordance with one embodiment of the present invention.

[0033] Fig. 5 is a schematic diagram showing a structure of a word line control circuit device in accordance with one embodiment of the present invention.

[0034] Fig. 6 is a schematic diagram showing a structure of another word line control circuit device in accordance with one embodiment of the present invention.

[0035] List of Reference Numerals in Drawings:

10: Test Mode Input Circuit; 11: Test Mode Input; 12: Test Mode Output;
 20: Row Address Input Circuit; 22: Output of Row Address Input Circuit;
 30: Logic Decoding Processor; 40: Word Line;
 32: Signal Input of Logic Decoding Processor; 33: Signal Output of Logic Decoding Processor;
 201: Row Address Signal Line; 100: First Inverter; 200: Second Inverter;
 310: First NAND Gate; 320: Second NAND Gate; 330: Decoding Device;
 311: First Input; 312: Second Input; 313: First Output;
 321: Third Input; 322: Fourth Input; 323: Second Output;
 331: First Decoder; 332: Second Decoder; 333: Third Decoder;
 334: Fourth Decoder; 335: Output of First Decoder;
 336: Output of Second Decoder; 337: Output of Third Decoder.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0036] Described below are merely certain exemplary embodiments. As will be recognized by those skilled in the art, the embodiments disclosed herein may be modified in various manners without departing from the spirit or scope of the present invention. Accordingly, the appended drawings and description shall be regarded as intrinsically exemplary rather than restrictive.

[0037] Although directional and spatial terms such as “central”, “longitudinal”, “lateral”, “lengthwise”, “widthwise”, “thickness-wise”, “upper”, “lower”, “front”, “rear”, “left”, “right”, “vertical”, “horizontal”, “top”, “bottom”, “interior”, “exterior”, “clockwise”,

“counterclockwise”, “axial”, “radial”, “circumferential”, etc. may be used herein to describe a directional and spatial relationship shown in the figures, they are used merely to facilitate and simplify the description of the present invention, and do not indicate or imply the stated components or elements must be arranged, constructed or operated in particular orientations. Therefore, they shall not be construed as limiting the present invention.

[0038] In addition, the terms “first”, “second”, etc. are used herein only for the purpose of illustration, and shall not be construed as indicating or implying relative importance or implicitly indicating the number of technical features indicated. Therefore, a feature described with “first”, “second” or the like may include one or more of the features, either explicitly or implicitly. As used herein, the term “a plurality of” has the meaning of “two or more”, unless specifically defined otherwise.

[0039] In the present invention, unless specifically defined or limited otherwise, the terms “attached”, “coupled”, “connected”, “fixed”, or the like shall be construed in a broad sense. For example, it may comprise a fixed connection, a detachable connection, or an integration; or a mechanical connection, an electrical connection, or a communication connection; or a direct connection, or an indirect connection through an intermediate medium; or an internal connection of two components or an interaction of two components. The specific meanings of the above terms in the present invention can be understood by those skilled in the art on a case-by-case basis.

[0040] In the present invention, unless defined or limited otherwise, when a first feature is described as being “on” or “under” a second feature, it may be in direct contact with the second feature, or in non-direct contact with the second feature through other features. Moreover, when a first feature is described as being “over”, “overlying” or “above” a second feature, it may either be situated normally or obliquely over the second feature, or be located at a horizontal level higher than that of the second feature. Similarly, when a first feature is described as being “under”, “underlying” or “beneath” a second feature, it may either be situated normally or obliquely under the second feature, or be located at a horizontal level lower than that of the

second feature.

[0041] Many different embodiments or examples are provided below for implementing the present invention. Specific examples of components and arrangements are described below to simplify the disclosure of the present invention. These are merely embodiments and examples, and are not intended to limit the scope of the present invention. In addition, the present invention may repeat reference numerals and/or letters in various embodiments. This repetition is for the purpose of simplicity and clarity, and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. Further, although the present invention provides examples of various particular processes and materials, those of ordinary skill in the art will recognize the use of other processes and/or materials.

[0042] EMBODIMENT 1

[0043] Referring to Fig. 1, one embodiment of the present invention provides a word line control method. The word line control method may comprise the following steps.

[0044] In step S10, a row address input signal may be acquired.

[0045] In step S20, a test mode signal may be acquired.

[0046] In step S30, logical and decoding operations may be performed on the row address input signal and the test mode signal to generate a row address control signal. The row address control signal may include at least two valid activation signals.

[0047] In step S40, at least two non-adjacent word lines may be simultaneously activated based on the at least two valid activation signals.

[0048] The row address control signal obtained, under test mode, from the logical and decoding operations performed on the row address input signal and the test mode signal enable simultaneous activation of at least two non-adjacent word lines. Referring to Fig. 2, two storage capacitors 400 electrically coupled to sources of respective access transistors share a common active area 300, while two adjacent word lines share a common contact area 500 serving as a drain. Referring to Fig. 3, since two non-adjacent word lines, for example WL1 and WL3, do not share a common contact area 500, the tests will not be affected by disconnection of contact

area 500 or presence of high impedance, thus improving test accuracy.

[0049] In some embodiments, referring to Fig. 4, the row address input signal may include a plurality of row address signals. The step of performing logical and decoding operations on the row address input signal and the test mode signal to generate a row address control signal may include the following steps.

[0050] In step S101, an inverse operation may be performed on the test mode signal to generate an inverted test signal.

[0051] In step S102, one of the plurality of row address signals may be selected, and a NAND operation may be performed on the selected row address signal and on the inverted test signal to generate an inverted output row address.

[0052] In step S103, inverse operations may be performed on all the row address signals to generate corresponding inverted row address signals.

[0053] In step S104, a NAND operation may be performed on the inverted row address signal corresponding to the selected row address signal and on the inverted test signal to generate a non-inverted output row address.

[0054] In step S105, the inverted output row address, the non-inverted output row address, unselected row address signals and unselected inverted row address signals may be decoded to obtain the row address control signal.

[0055] In some embodiments, referring to Fig. 6, the test mode signal may be set to logic status “1” to activate the test mode, when an inverse operation may be performed on the test mode signal to generate the inverted test signal. The row address input signal RA<8:0> may include nine row address signals indicated as RA0-RA8. Inverse operations may be performed on all row address signals to generate the inverted row address signals, indicated as RAN0-RAN8. A NAND operation may be performed on the row address signal randomly selected from RA0-RA8, for example, RA1, and the inverted test signal to generate the inverted output row address RANint1. Another NAND operation may be performed on the inverted row address signal RAN1 corresponding to the selected row address signal RA1 and the inverted

test signal to generate the non-inverted output row address RA_{int1}. RAN_{int1}, Raint₁, RA₀, RA₂-RA₈, RAN₀ and RAN₂-RAN₈ may be input to the decoders to generate the row address control signal including the same number of signals as the amount of the word lines under control, such as 512 word lines. The row address control signal may include at least two valid activation signals, configured for simultaneously activating at least two random non-adjacent word lines out of the 512 word lines.

[0056] In some embodiments, referring to Fig. 4, the step of decoding the inverted output row address, non-inverted output row address, unselected row address signals and unselected inverted row address signals to obtain the row address control signal may include the following steps.

[0057] In step S201, a primary decoding process may be performed on the inverted output row address, the non-inverted output row address, the unselected row address signals and the unselected inverted row address signals to obtain a first row address control signal. The first row address control signal may include the at least two valid activation signals, configured for simultaneously activating the at least two non-adjacent word lines.

[0058] In step S202, a secondary decoding process may be performed on the first row address control signal to obtain a second row address control signal, configured for simultaneously activating the at least two non-adjacent word lines.

[0059] In some embodiments, referring to Fig. 6, the primary decoding process may be carried out by three 3-to-8 decoders. RAN_{int1} and RA_{int1} may be input to one of the 3-to-8 decoders to generate first control signals including at least two valid activation signals, configured for simultaneously activating at least two non-adjacent word lines. The other two 3-to-8 decoders may be input RA₀, RA₂-RA₈, RAN₀ and RAN₂-RAN₈, and output second control signals and third control signals. The first control signals, second control signals and third control signals may constitute the first row address control signal.

[0060] Apparently, in addition to that described in the above example, the primary decoding process may be alternatively accomplished in other suitable manners, as long as the above

effects can be achieved, without departing from the scope of the present invention.

[0061] EMBODIMENT 2

[0062] Referring to Fig. 5, another embodiment of the present invention provides a word line control circuit device. The word line control circuit device may include a test mode input circuit 10, a row address input circuit 20 and a logic decoding processor 30. A test mode output 12 of the test mode input circuit 10, and an output of row address input circuit 22 may be coupled to a signal input 32 of the logic decoding processor 30. A signal output 33 of the logic decoding processor 30 may be coupled to a plurality of word lines 40 in a memory array. The test mode input circuit 10 may be configured to receive a test mode signal. The row address input circuit 20 may be configured to receive a plurality of row address signals. And the logic decoding processor 30 may be configured to perform logical and decoding operations on the plurality of row address signals and test mode signal to generate a row address control signal. The row address control signal may include at least two valid activation signals, configured for simultaneously activating at least two non-adjacent word lines 40.

[0063] In some embodiments, referring to Fig. 6, the test mode input circuit 10 may include a test mode input 11, a first inverter 100 and the test mode output 12. The test mode input 11 may be configured to receive the test mode signal. The first inverter 100 may be configured to perform an inversion operation on the test mode signal to generate an inverted test signal. And the test mode output 12 may be configured to output the inverted test signal.

[0064] In some embodiments, the row address input circuit 20 may include a plurality of row address signal lines 201, and a plurality of second inverters 200 coupled to the row address signal lines 201, respectively. The row address signal lines 201 may be configured to receive the corresponding one of the row address signals from the row address input signal, respectively. And the second inverters 200 may be configured to perform inverse operations on the row address signals to generate a plurality of inverted row address signals.

[0065] In some embodiments, referring to Fig. 6, the row address input circuit 20 may include nine row address signal lines 201, each of which may be configured to receive a

corresponding one of the row address input signal RA0-RA8. The nine row address signal lines 201 may be coupled to nine second inverters 200, respectively. The outputs 202 of the nine second inverters 200 may be configured to output the inverted row address signals RAN0-RAN8. Apparently, the number of row address signal lines 201 in the row address input circuit 20 is not limited to that described herein and may be modified depending on the number of row addresses to be input, without departing from the scope of the present invention.

[0066] In some embodiments, the logic decoding processor 30 may include a first NAND gate 310, a second NAND gate 320 and a decoding device 330.

[0067] The first NAND gate 310 may be configured to perform a NAND operation on a selected one of the row address signals and the inverted test signal to generate an inverted output row address. The first NAND gate 310 may include a first input 311, a second input 312 and a first output 313. The first input 311 may be coupled to a selected one of the row address signal lines 201, the second input 312 may be coupled to the test mode output 12 and configured to receive the inverted test signal, and the first output 313 may be coupled to the decoding device 330.

[0068] The second NAND gate may be configured to perform a NAND operation on one of the inverted row address signals corresponding to the selected row address signal and the inverted test signal to generate a non-inverted output row address. The second NAND gate 320 may include a third input 321, a fourth input 322 and a second output 323. The third input 321 may be coupled to the output 202 of one of the second inverters 200 corresponding to the selected row address signal line 201, the fourth input 322 may be coupled to the test mode output 12, and the second output 323 may be coupled to the decoding device 330.

[0069] The decoding device 330 may be configured to decode the inverted output row address, non-inverted output row address, unselected row address signals and unselected inverted row address signals to obtain the row address control signal. The row address control signal may include the at least two valid activation signals, configured for simultaneously activating the at least two non-adjacent word lines. The decoding device 30 may have: a

decoding input coupled to the first output 313, the second output 323, the unselected row address signal lines 201 and the outputs 202 of the unselected second inverters; and a decoding output coupled to the word lines 40.

[0070] The first NAND gate 310 may perform a NAND operation on the inverted test signal and the selected row address signal RA1 and output the inverted output row address RANint1. The second NAND gate 320 may perform a NAND operation on the inverted row address signal RAN1 corresponding to the selected row address signal RA1 and the inverted test signal to generate the non-inverted output row address RAint1.

[0071] In some embodiments, the decoding device 30 may include a first decoder 331 having a set of non-inverted inputs and a set of inverted inputs. The first output 313 may be coupled to a corresponding one of the inverted inputs and the second output 323 may be coupled to a corresponding one of the non-inverted inputs. The decoding device 330 may further include a second decoder 332 and a third decoder 333. The second decoder 332 may have a set of non-inverted inputs for receiving the row address signals and a set of inverted inputs for receiving the inverted row address signals. The third decoder 333 may have a set of non-inverted inputs for receiving the row address signals and a set of inverted inputs for receiving the inverted row address signals.

[0072] Specifically, the first decoder 331 may have three non-inverted inputs RA0, RA1, RA2, and three inverted inputs RAN0, RAN1, RAN2. The inputs RA0 and RA2 may be coupled to the row address signal lines 201 in the row address input circuit 20 for receiving the row address signals RA0 and RA2, respectively. The inputs RAN0, RAN2 may be coupled to the outputs 202 of the second inverters in the row address input circuit 20 for outputting RAN0 and RAN2, respectively. Additionally, the input RA1 of the first decoder 331 may be coupled to the second output 323 of the second NAND gate 320 from which the non-inverted output row address RAint1 is output, and the input RAN1 of the first decoder 331 may be coupled to the first output 313 of the first NAND gate 310 from which the inverted output row address RANint1 is output.

[0073] The second decoder 332 may include three non-inverted inputs RA3, RA4, RA5 and three inverted inputs RAN3, RAN4, RAN5. The inputs RA3, RA4, RA5 may be coupled to the three row address signal lines 201 in the row address input circuit 20 for receiving the row address signals RA3, RA4, RA5, respectively. And the inputs RAN3, RAN4, RAN5 may be coupled to the outputs 202 of the three second inverters in the row address input circuit 20 for outputting RAN3, RAN4 and RAN5, respectively.

[0074] The third decoder 333 may include three non-inverted inputs RA6, RA7, RA8 and three inverted inputs RAN6, RAN7, RAN8. The inputs RA6, RA7, RA8 may be coupled to the three row address signal lines 201 in the row address input circuit 20 for receiving the row address signal RA6, RA7, RA8, respectively. And the inputs RAN6, RAN7, RAN8 may be coupled to the outputs 202 of the three second inverters in the row address input circuit 20 for outputting RAN6, RAN7 and RAN8, respectively.

[0075] The decoding device 30 may further include a fourth decoder 334. The fourth decoder 334 may have inputs coupled to output of the first decoder 335, output of the second decoder 336, and output of the third decoder 337. The input of the first decoder 331, input of the second decoder 332, and input of the third decoder 333 may constitute the signal input 32 of the logic decoding processor 30. The fourth decoder 334 may have outputs constituting the signal output 33 of the logic decoding processor 30 that is coupled to the word lines 40. The fourth decoder 334 may be configured to output a second row address control signal for activating/deactivating the respective word lines, and simultaneously activating the at least two non-adjacent word lines 40 based on the aforementioned at least two valid activation signals.

[0076] Referring to Fig. 6, the memory array may include 516 word lines 40, indicated as WL0-WL512. The number of the word lines 40 may vary within an appropriate range, depending on actual needs, without departing from the scope of the present invention.

[0077] EMBODIMENT 3

[0078] The present invention also provides a semiconductor memory. The semiconductor memory may include the word line control circuit devices as defined above.

[0079] Described above are merely a few specific embodiments of the present invention, the scope of which is, however, not limited to these embodiments disclosed herein and is intended to embrace all changes and substitutions easily conceivable by those of ordinary skill in the art based on the present disclosure. Therefore, the scope of the present invention shall be defined by the appended claims.

CLAIMS

1. A word line control method, comprising:
 - acquiring a row address input signal;
 - performing logical and decoding operations on the row address input signal to generate a row address control signal, wherein the row address control signal includes at least two valid activation signals; and
 - simultaneously activating at least two non-adjacent word lines based on the at least two valid activation signals.
2. The method of claim 1, further comprising:
 - acquiring a test mode signal,
 - and wherein performing logical and decoding operations on the row address input signal to generate a row address control signal comprises:
 - performing the logical and decoding operations on the row address input signal and the test mode signal to generate the row address control signal.
3. The method of claim 2, wherein the row address input signal includes a plurality of row address signals, and wherein performing logical and decoding operations on the row address input signal and the test mode signal to generate a row address control signal comprises:
 - performing an inverse operation on the test mode signal to generate an inverted test signal;
 - selecting one of the plurality of row address signals, and performing a NAND operation on the selected row address signal and the inverted test signal to generate an inverted output row address;
 - performing inverse operations on all the row address signals to generate corresponding inverted row address signals;
 - performing a NAND operation on the inverted row address signal corresponding to the

selected row address signal and the inverted test signal to generate a non-inverted output row address; and

decoding the inverted output row address, the non-inverted output row address, unselected row address signals and unselected inverted row address signals to obtain the row address control signal.

4. The method of claim 3, wherein decoding the inverted output row address, the non-inverted output row address, unselected row address signals and unselected inverted row address signals to obtain the row address control signal comprises:

performing a primary decoding process on the inverted output row address, the non-inverted output row address, the unselected row address signals and the unselected inverted row address signals to obtain a first row address control signal, wherein the first row address control signal includes the at least two valid activation signals, configured for simultaneously activating the at least two non-adjacent word lines; and

performing a secondary decoding process on the first row address control signal to obtain a second row address control signal, configured for simultaneously activating the at least two non-adjacent word lines.

5. A word line control circuit device, comprising:

a test mode input circuit, configured to receive a test mode signal;

a row address input circuit, configured to receive a plurality of row address signals; and

a logic decoding processor, configured to perform logical and decoding operations on the plurality of row address signals and the test mode signal to generate a row address control signal, wherein the row address control signal includes at least two valid activation signals, configured for simultaneously activating at least two non-adjacent word lines,

wherein the test mode input circuit has an output coupled, together with an output of the row address input circuit, to a signal input of the logic decoding processor,

and wherein the logic decoding processor has a signal output coupled to a plurality of word lines in a memory array.

6. The device of claim 5, wherein the test mode input circuit comprises:

a test mode input, configured to receive the test mode signal;

a first inverter, configured to perform an inverse operation on the test mode signal to generate an inverted test signal; and

a test mode output, configured to output the inverted test signal.

7. The device of claim 6, wherein the row address input circuit comprises:

a plurality of row address signal lines, configured to receive the corresponding one of the row address signals from the row address input signal, respectively; and

a plurality of second inverters coupled to the corresponding one of the row address signal lines, respectively, and configured to perform inverse operations on the row address signals to generate a plurality of inverted row address signals.

8. The device of claim 7, wherein the logic decoding processor comprises:

a first NAND gate, configured to perform a NAND operation on the selected one of the row address signals and the inverted test signal to generate an inverted output row address;

a second NAND gate, configured to perform a NAND operation on one of the inverted row address signals corresponding to the selected row address signal and the inverted test signal to generate a non-inverted output row address; and

a decoding device, configured to decode the inverted output row address, the non-inverted output row address, unselected row address signals and unselected inverted row address signals to obtain the row address control signal, wherein the row address control signal includes the at least two valid activation signals, configured for simultaneously activating at least two non-adjacent word lines,

wherein the first NAND gate includes a first input coupled to the one of the row address signal lines corresponding to the selected row address signal, a second input coupled to the test mode output and configured to receive the inverted test signal, and a first output,

and wherein the second NAND gate includes a third input coupled to an output of one of the second inverters corresponding to the selected row address signal, a fourth input coupled to the test mode output, and a second output.

9. The device of claim 8, wherein the decoding device comprises a first decoder, wherein the first decoder has a set of non-inverted inputs and a set of inverted inputs, and wherein the first output is coupled to the corresponding one of the inverted inputs and the second output is coupled to the corresponding one of the non-inverted inputs.

10. The device of claim 9, wherein the decoding device further comprises a second decoder and a third decoder,

wherein the second decoder has a set of non-inverted inputs configured for receiving the unselected row address signals, and a set of inverted inputs configured for receiving the unselected inverted row address signals,

and wherein the third decoder has a set of non-inverted inputs configured for receiving the unselected row address signals, and a set of inverted inputs configured for receiving the unselected inverted row address signals.

11. The device of claim 10, wherein the decoding device further comprises a fourth decoder, wherein the fourth decoder has inputs coupled to the outputs of the first decoder, the second decoder and the third decoder,

wherein the inputs of the first decoder, the second decoder and the third decoder constitute the signal input of the logic decoding processor,

and wherein the fourth decoder has outputs constituting the signal output of the logic

decoding processor that is coupled to the word lines.

12. A semiconductor memory comprising a word line control circuit device, wherein the word line control circuit device comprises:

a row address input circuit, configured to receive a plurality of row address signals; and

a logic decoding processor, configured to perform logical and decoding operations on the plurality of row address signals to generate a row address control signal, wherein the row address control signal includes at least two valid activation signals configured for simultaneously activating at least two non-adjacent word lines,

wherein the logic decoding processor has a signal output coupled to a plurality of word lines in a memory array.

13. The semiconductor memory of claim 12, wherein the word line control circuit device further comprises:

a test mode input circuit, configured to receive a test mode signal,

wherein the logic decoding processor is configured to perform logical and decoding operations on the plurality of row address signals and the test mode signal to generate the row address control signal,

and wherein the test mode input circuit has an output coupled, together with an output of the row address input circuit, to a signal input of the logic decoding processor.

14. The semiconductor memory of claim 13, wherein in the word line control circuit device, the test mode input circuit comprises:

a test mode input, configured to receive the test mode signal;

a first inverter, configured to perform an inverse operation on the test mode signal to generate an inverted test signal; and

a test mode output, configured to output the inverted test signal.

15. The semiconductor memory of claim 14, wherein in the word line control circuit device, the row address input circuit comprises:

a plurality of row address signal lines, configured to receive the corresponding one of the row address signals from the row address input signal, respectively; and

a plurality of second inverters coupled to the corresponding one of the row address signal lines, respectively, and configured to perform inverse operations on the row address signals to generate a plurality of inverted row address signals.

16. The semiconductor memory of claim 15, wherein in the word line control circuit device, the logic decoding processor comprises:

a first NAND gate, configured to perform a NAND operation on the selected one of the row address signals and the inverted test signal to generate an inverted output row address;

a second NAND gate, configured to perform a NAND operation on one of the inverted row address signals corresponding to the selected row address signal and the inverted test signal to generate a non-inverted output row address; and

a decoding device, configured to decode the inverted output row address, the non-inverted output row address, unselected row address signals and unselected inverted row address signals to obtain the row address control signal, wherein the row address control signal includes the at least two valid activation signals, configured for simultaneously activating at least two non-adjacent word lines,

wherein the first NAND gate includes a first input coupled to the one of the row address signal lines corresponding to the selected row address signal, a second input coupled to the test mode output and configured to receive the inverted test signal, and a first output, and wherein the second NAND gate includes a third input coupled to an output of one of the second inverters corresponding to the selected row address signal, a fourth input coupled to the test mode output, and a second output.

17. The semiconductor memory of claim 16, wherein in the word line control circuit device, the decoding device comprises a first decoder, wherein the first decoder has a set of non-inverted inputs and a set of inverted inputs, and wherein the first output is coupled to the corresponding one of the inverted inputs and the second output is coupled to the corresponding one of the non-inverted inputs.

18. The semiconductor memory of claim 17, wherein in the word line control circuit device, the decoding device further comprises a second decoder and a third decoder,

wherein the second decoder has a set of non-inverted inputs configured for receiving the unselected row address signals, and a set of inverted inputs configured for receiving the unselected inverted row address signals,

and wherein the third decoder has a set of non-inverted inputs configured for receiving the unselected row address signals, and a set of inverted inputs configured for receiving the unselected inverted row address signals.

19. The semiconductor memory of claim 18, wherein in the word line control circuit device, the decoding device further comprises a fourth decoder,

wherein the fourth decoder has inputs coupled to the outputs of the first decoder, the second decoder and the third decoder,

wherein the inputs of the first decoder, the second decoder and the third decoder constitute the signal input of the logic decoding processor,

and wherein the fourth decoder has outputs constituting the signal output of the logic decoding processor that is coupled to the word lines.

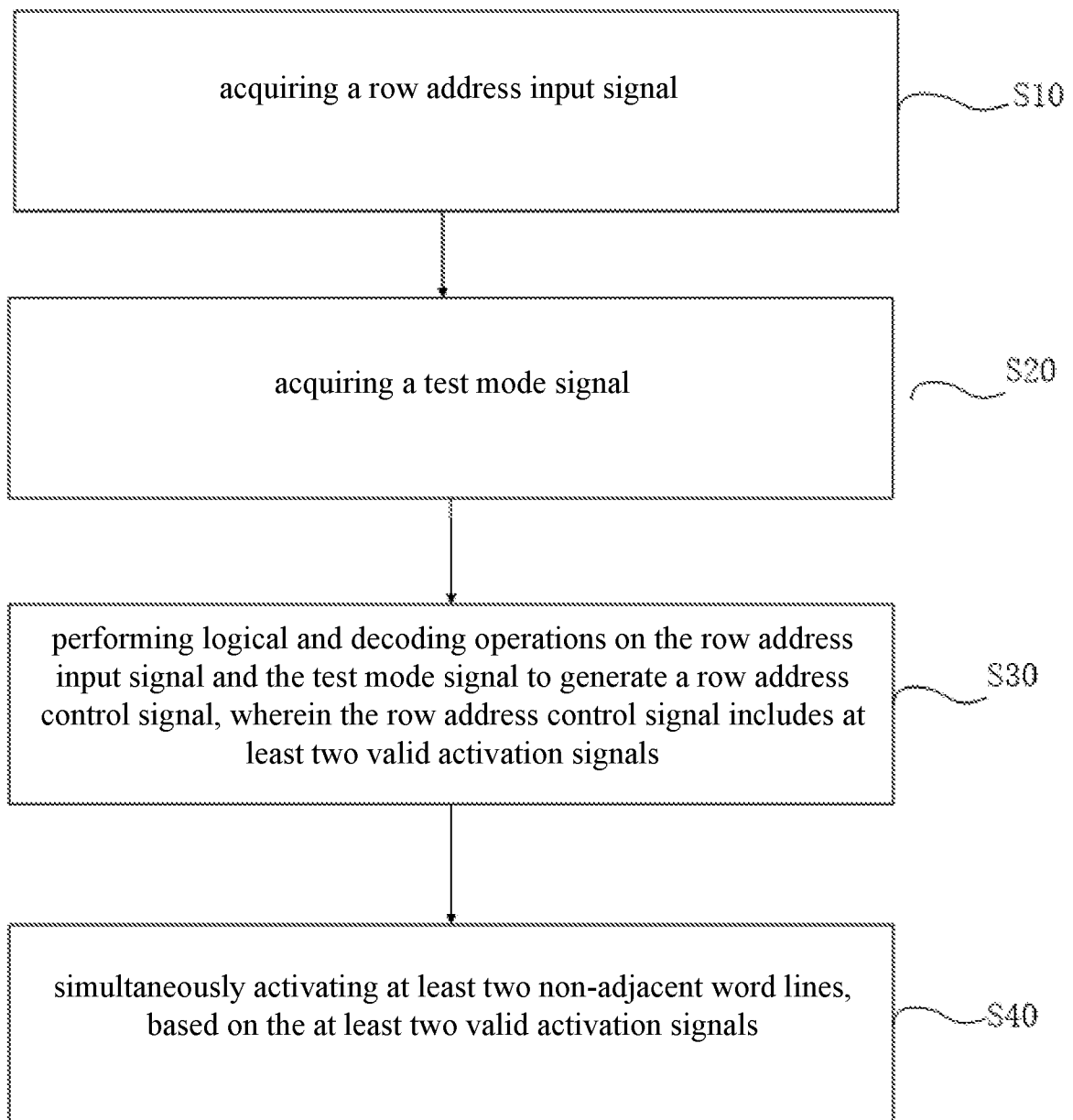


FIG. 1

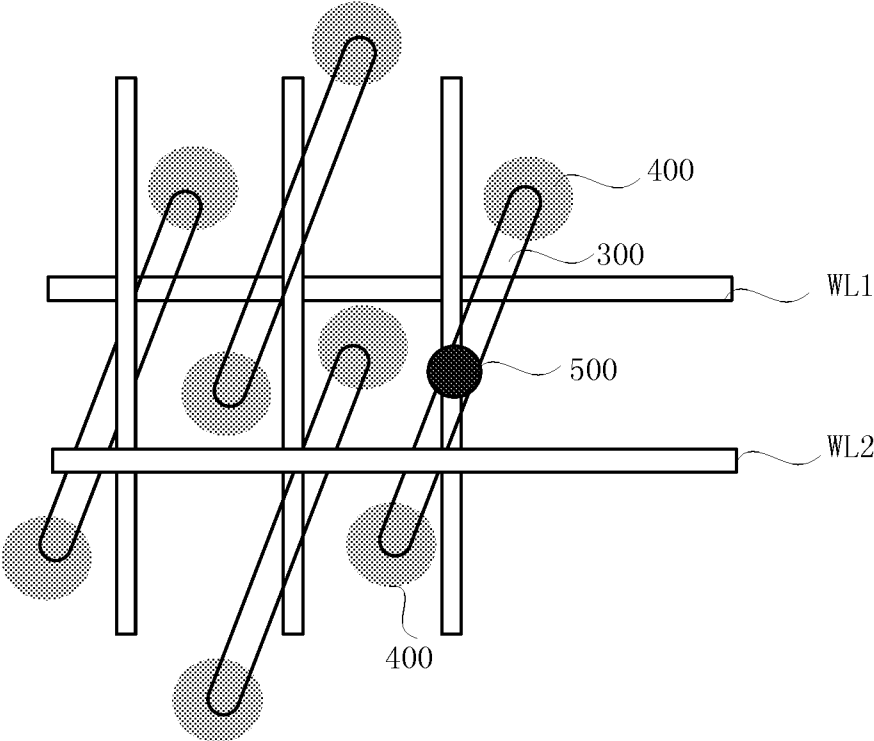


FIG. 2

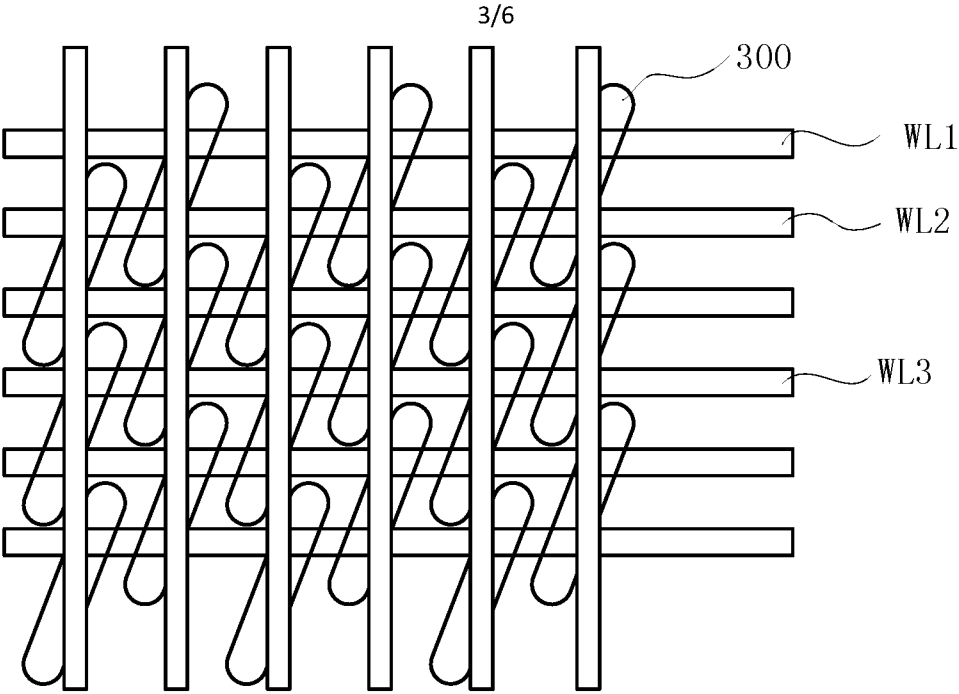


FIG. 3

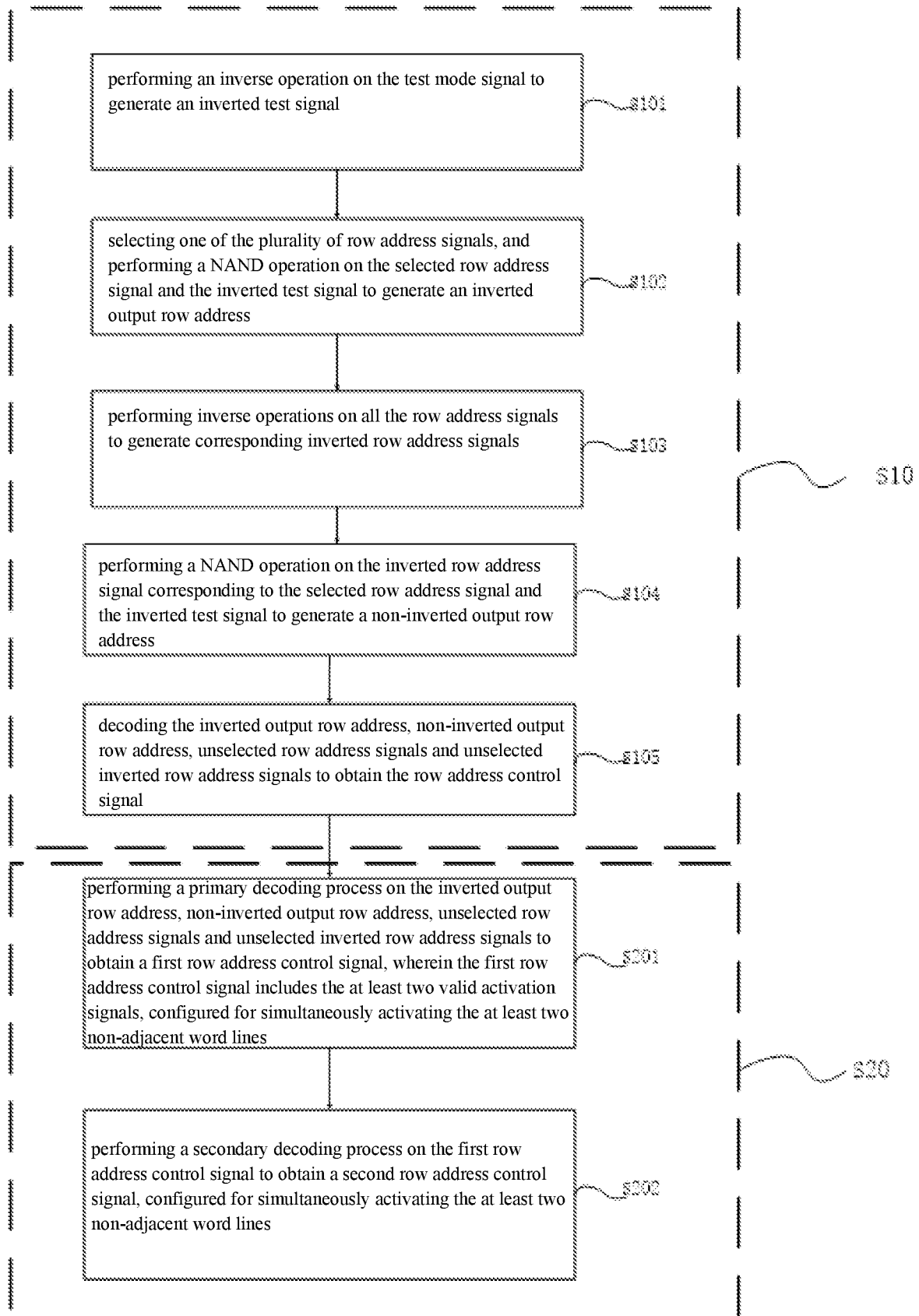


FIG. 4

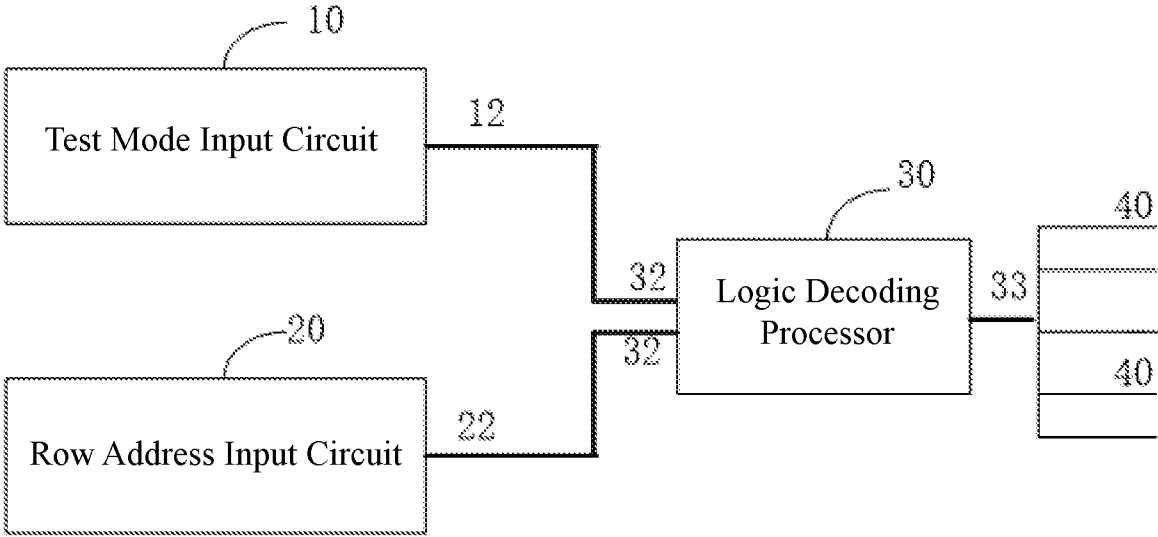


FIG. 5

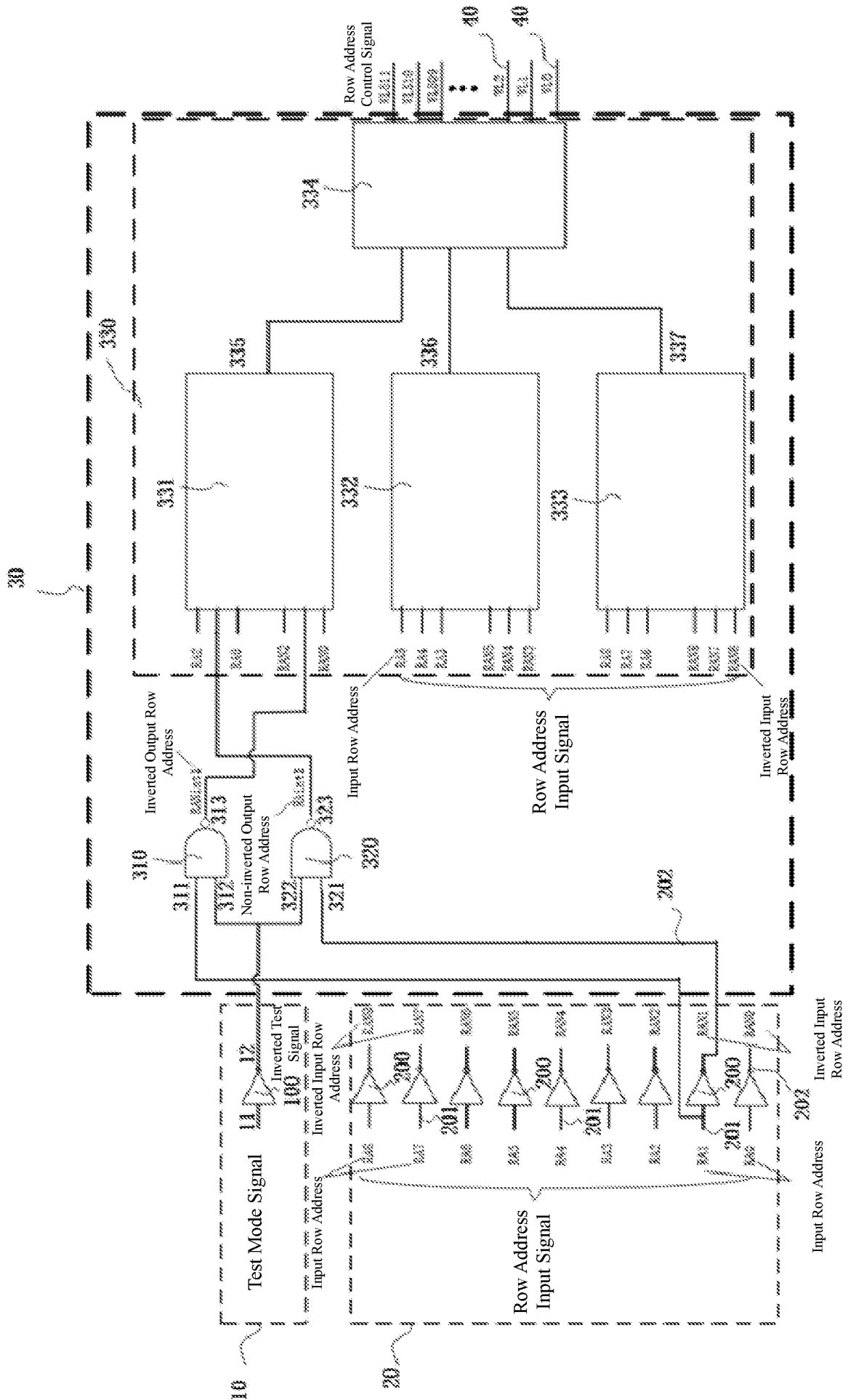


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/116063

A. CLASSIFICATION OF SUBJECT MATTER

G11C 29/12(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, EPODOC, WPI: word, line, control, row, address, memory, decode, signal, valid, activation, simultaneously, non-adjacent, test, contact, area

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 208834750 U (CHANGXIN MEMORY TECHNOLOGIES, INC.) 07 May 2019 (2019-05-07) abstract, description, paragraphs [0048]-[0086]	1-19
A	CN 102760496 A (YIYANG TECHNOLOGY CO., LTD.) 31 October 2012 (2012-10-31) abstract, description, paragraphs [0038]-[0051]	1-19
A	US 2014254285 A1 (EGUCHI, Richard K. et al.) 11 September 2014 (2014-09-11) the whole document	1-19
A	US 2015043292 A1 (SK HYNIX INC.) 12 February 2015 (2015-02-12) the whole document	1-19
A	US 2017047113 A1 (SAMSUNG ELECTRONICS CO., LTD.) 16 February 2017 (2017-02-16) the whole document	1-19



Further documents are listed in the continuation of Box C.



See patent family annex.

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“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

14 January 2020

Date of mailing of the international search report

06 February 2020

Name and mailing address of the ISA/CN

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/116063

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