Dec. 9, 1969 R. A. GANGE ET AL 3,483,517

BALANCED MATRIX DRIVER ARRANGEMENT

Filed Dec. 22, 1966 3 Sheets-Sheet 1

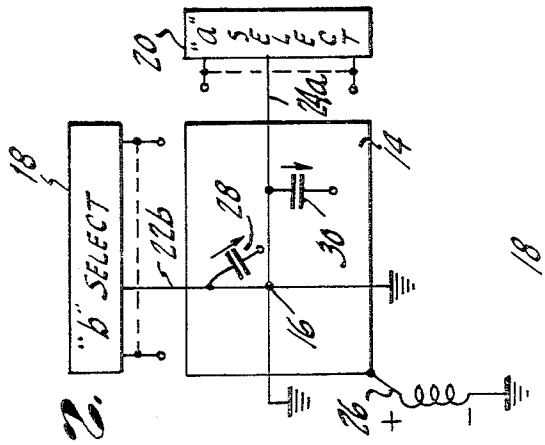


Fig. 2.

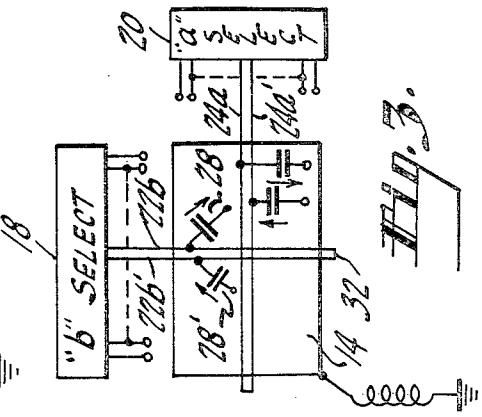


Fig. 3.

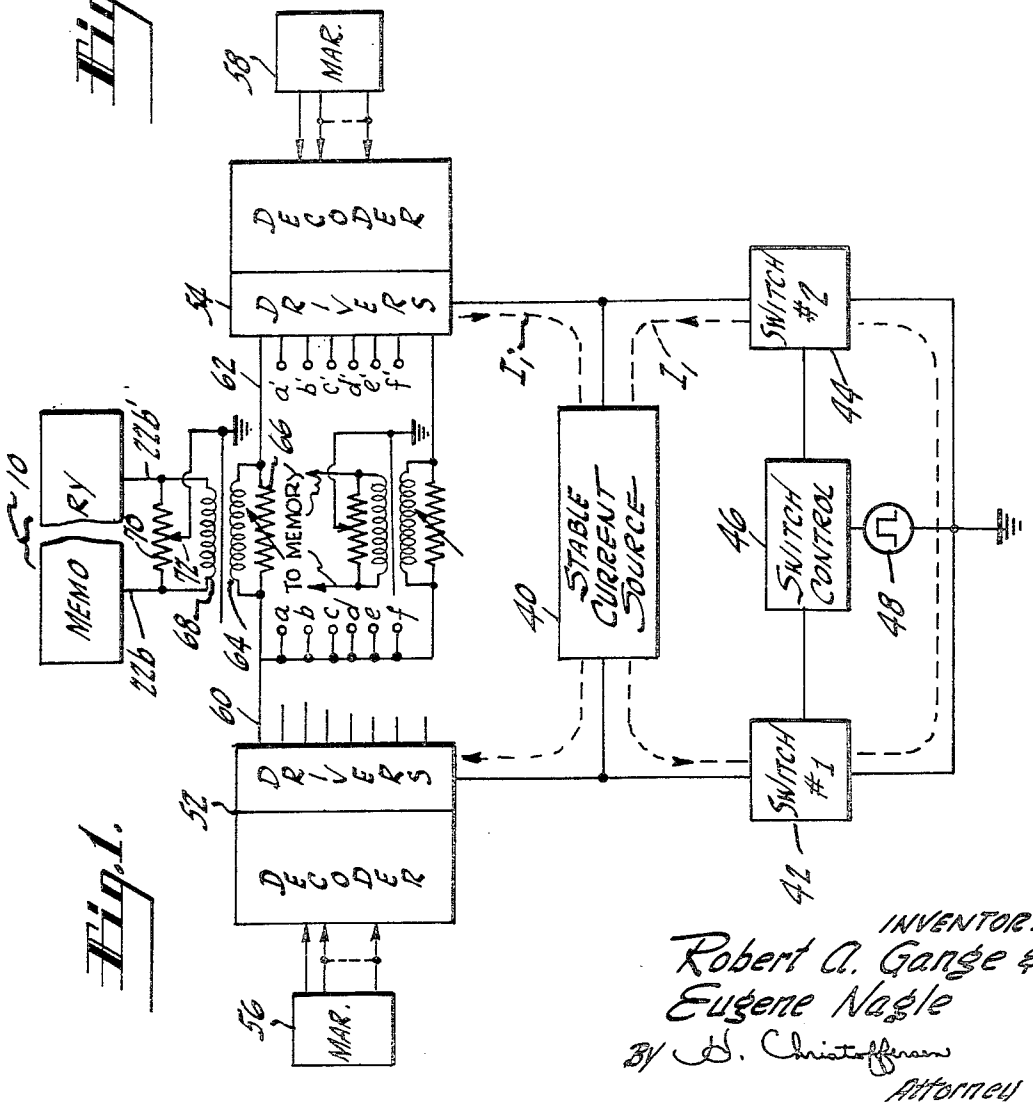


Fig. 1.

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Dec. 9, 1969 R. A. GANGE ET AL 3,483,517

BALANCED MATRIX DRIVER ARRANGEMENT

Filed Dec. 22, 1966 3 Sheets-Sheet 2

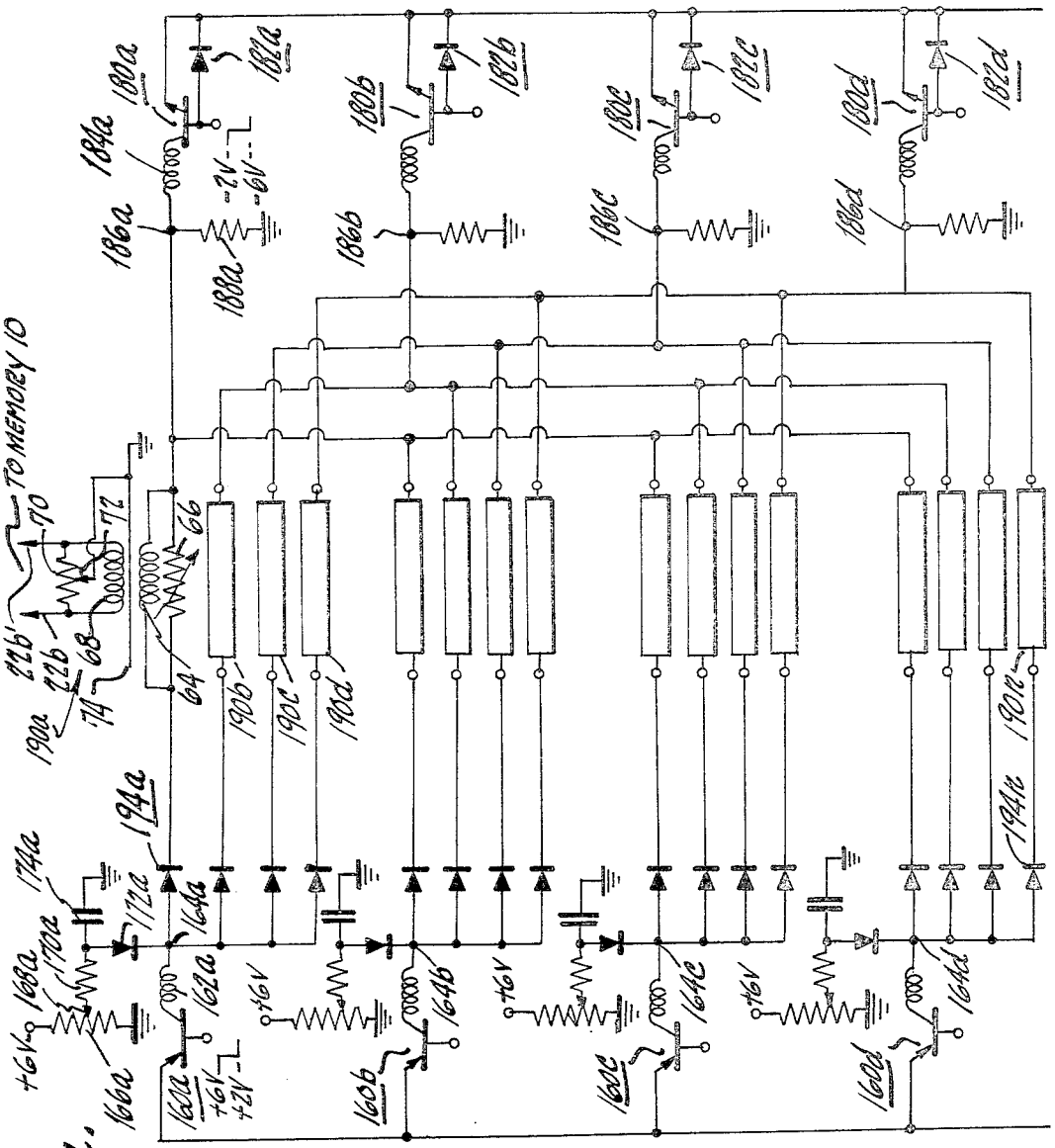


Fig. 4a.

CODE

Fig. 4a.	Fig. 4b.

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BALANCED MATRIX DRIVER ARRANGEMENT

Filed Dec. 22, 1966 3 Sheets-Sheet 3

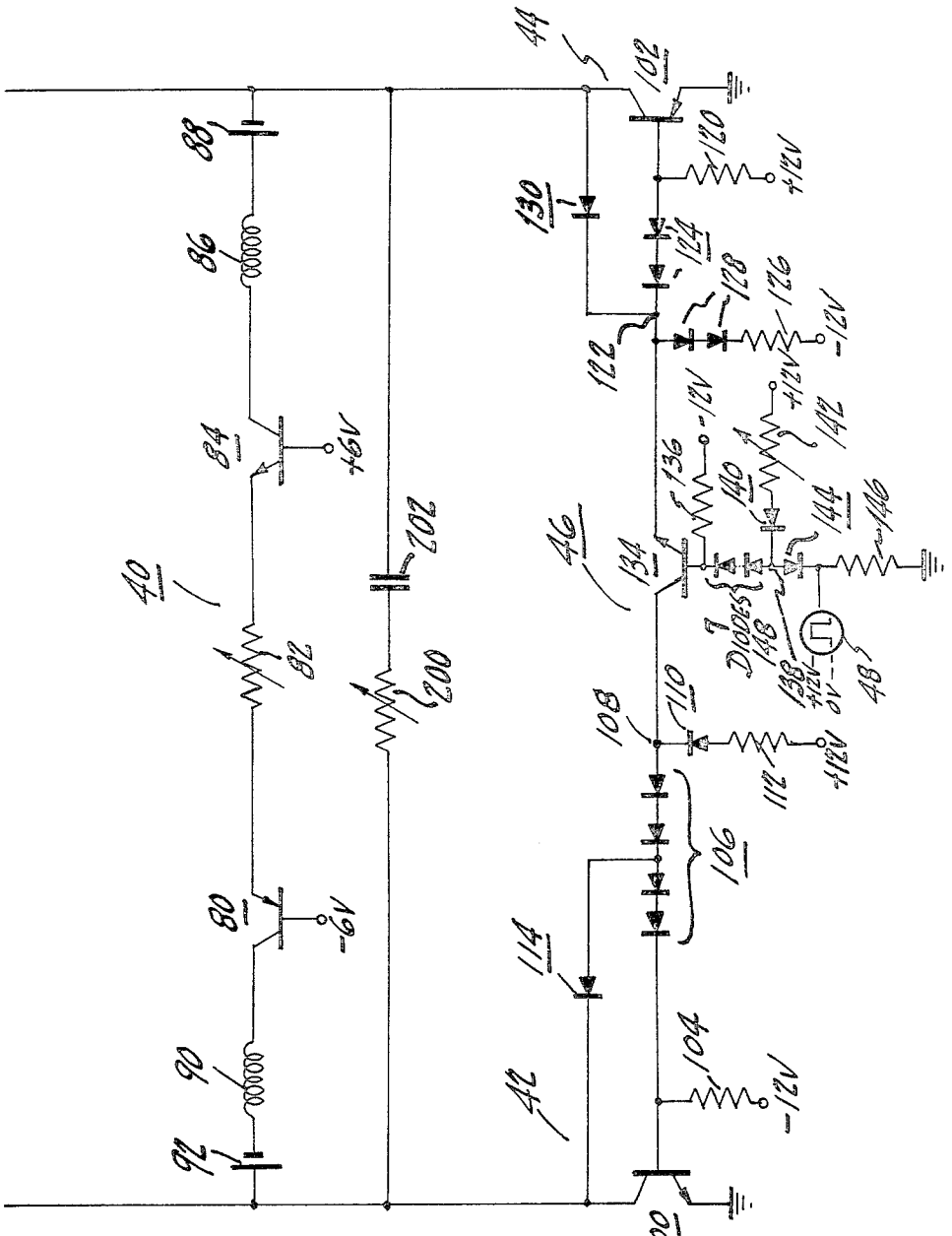


Fig. 4b.

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BALANCED MATRIX DRIVER ARRANGEMENT

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Int. Cl. H04q 1/56
U.S. Cl. 340—166 9 Claims

This invention relates to a novel matrix-driver arrangement which is especially useful in providing balanced outputs to the drive lines of a cryoeleceric memory.

In cryoelectric memories, the sense or output signals are of very small amplitude. Consequently, great care must be exercised to avoid the generation of noise and spurious signals introduced by way of the decoder, driver and memory drive lines lest false output signals result. Memory drive lines which are unbalanced with respect to the system ground ar a major source of noise and spurious signals since currents flowing in these lines induce voltages in the memory ground plane and sense lines through capacitive coupling. These unwanted signals can be eliminated or at least greatly reduced by employing drive lines which are structurally balanced, i.e., symmetrical, with respect to the ground plane and by driving these lines from a source which is electrically balanced with respect to the drive lines.

It is one object of this invention to provide an improved memory and memory drive arrangement which is both electrically and structurally balanced.

It is another object of this invention to provide an improved drive system which produces balanced output signals from an essentially single ended source.

It is a further object of this invention to provide an improved matrix-driver arrangement in which the drivers function also as the last stage of a decoder and in which a stable current is steered through a selected driver in response to an interrogate or control signal.

It is yet another object of this invention to provide a matrix-driver arrangement of the type immediately aforementioned, in which the stable current source and the interrogate signal circuitry are combined in the same small package as the matrix-drivers to reduce component count and enable compactness, all of which features are compatible with the noise requirements of a cryoelectric memory system.

In apparatus embodying the invention, each of a first set of amplifier-driver devices has a like electrode connected in common to one terminal of a stable source of current, and each one of a second set of amplifier-drivers has one like electrode connected in common to the other terminal of the stable source. A second electrode of each driver in the first set is connected to the second electrode of each driver in the second set by way of the primary winding of a separate output transformer, and the ends of each transformer's secondary winding are electrically balanced with respect to a reference, e.g. system ground. Any output transformer may be selected by applying enabling signals to the control electrodes of the two associated amplifier-drivers.

Further, a signal-responsive current shunting or diverting path is connected across the stable current source and operates in the absence of a control signal to draw all of the current from the stable source. An applied control signal interrupts the shunting path, whereupon the source current flows through that one of the transformer primary windings whose associated amplifier-drivers are receiving enabling signals.

In the accompanying drawing, like reference characters denote like components; and

FIGURE 1 is a block diagram of a memory and matrix-driver arrangement embodying the invention;

FIGURE 2 is a simplified diagram of a memory system in which the drive lines are unbalanced;

FIGURE 3 is a simplified diagram of a memory system employing balanced drive lines; and

FIGURES 4(*a*) and 4(*b*) together constitute FIGURE 4, of which FIGURE 4(*a*) is a schematic diagram of the matrix-drivers, and FIGURE 4(*b*) is a schematic diagram of a stable current source and a current shunting path.

A balanced matrix-driver arrangement and memory system embodying the invention is illustrated in block form in FIGURE 1. This arrangement is especially useful in providing balanced output signals to a cryoelectric memory **10** of the type which employs drive lines operated in pairs, which drive means are structurally balanced with respect to the memory ground plane or planes. A suitable example of such a memory is illustrated and described in the copending application of Robert A. Gange, Ser. No. 584,433, filed Oct. 5, 1966 for "Cryoelectric Memories," which by reference thereto is made a part hereof.

As explained in that copending application, so-called *a*, *b* cryoelectric memory systems prior to the ones described in the copending application employed single conductors as the memory drive lines. Such a prior art system is illustrated in rudimentary form in FIGURE 2 of the present application. Such a system generally comprises one or more ground planes **14**, only one of which is illustrated, each of which has a large number of cryoelectric memory or storage elements thereon. Each of these storage elements, for example the storage element represented by shaded area **16**, is linked by two drive lines, one line from a unit **18** labelled "*b* SELECT," and one line from a unit **20** labelled "*a* SELECT." These selection units may include decoders and drivers, as is well-known in the art. For purposes of convenience, only the drive lines **22***b* and **24***a* which link the element **16** are illustrated in FIGURE 2. It will be noted that each of these lines is grounded at its far end, whereby the lines are unbalanced with respect to the ground plane **14**.

The selection units **18** and **20** and the system ground usually are located outside the low temperature bath, e.g. cryostat, while the ground planes **14** and the portions of the drive lines linking same are located within the cryostat. The line **26** which connects the ground plane **14** to system ground may be several feet in length, whereby this line **26** appears as an inductor to any signals induced in the ground plane **14**.

There is capacitive coupling between each of the drive lines, e.g. lines **22***b* and **24***a*, and the ground plane **14**, and by way of the ground plane to the sense line or lines (not illustrated). These distributed capacitances are illustrated for convenience as lumped capacitors **28**, **30**. Each time a positive going signal is applied to the drive line **22***b*, whether the signal be a drive current, noise, etc., capacitor **28** charges in the polarity direction indicated. Since one end of this line **22***b* is grounded and the positive signal is applied at the other end, a voltage gradient is present along the line, and all of the distributed capacitances charge in the same polarity direction. The same is true for any positive going signal on the other line **24***a*. These charge currents must flow to system ground by way of the lead **26**, and the inductance thereof results in a voltage being induced on the ground plane **14**. The movement of voltage of the ground plane occurs with greater severity in the absence of connection **26**. Also, a voltage is induced on the sense line due to this capacitance, and the induced signal may be of much greater amplitude than the small amplitude sense signals which are induced on the sense line during a read operation.

As described in the copending application, the aforementioned induced signals are avoided in a memory system of the type illustrated therein which employs two con-

ductors for each drive line. The manner in which this is accomplished is illustrated in simple form in FIGURE 3. The improved system is one in which the drive lines are structurally and electrically balanced with respect to the ground plane **14**. One of the two conductors of the drive line may be thought of as an "outgoing" conductor and the other a "return" conductor. For example, the single *b* drive line shown in full includes an outgoing conductor **22***b* and a return conductor **22***b'*. The voltages applied at the ends of this line by the selection unit are balanced with respect to system ground. That is to say, when it is desired to energize this line, the free end of conductor **22***b* has a voltage +V applied thereto and the free end of conductor **22***b'* has a voltage −V of equal and opposite polarity applied thereto. The center point **32** of the line then is a virtual ground. Since the line is structurally balanced with respect to the ground plane **14**, equal portions of the conductors **22***b* and **22***b'* overlie the ground plane **14**, and since the voltages on the two different conductors **22***b* and **22***b'* are of equal and opposite polarity, the capacitors **28** and **28'** conduct charge current in opposite directions with respect to the ground plane **14**. As a result, the net current flowing in the ground plane **14** due to the signal on this pair of conductors is zero, since the two charge currents cancel one another. As a consequence, no current flows in the ground lead **26**, there is no voltage induced on the ground plane **14** and no spurious signal coupled to or induced in the sense line. The above description assumes that the conductors **22***b* and **22***b'* (and all other pairs of drive lines) are structurally and electrically balanced with respect to system ground, and assumes further a balanced drive source for the lines. It is the purpose of the present invention to provide such a balanced driver arrangement, which may be used as the "*b* SELECT" unit **18** or the "*a* SELECT" unit **20**.

With reference again to FIGURE 1, the arrangement embodying the invention comprises a stable current source **40** which has connected across the terminals thereof a current diverting or shunting path which may comprise a first signal controlled switch **42** in series with a second signal controlled switch **44**. The junction of these two switches may be connected to system ground. A switch control **46** receives "interrogate" or control signals from a source **48** and, in response thereto, opens or closes the switches concurrently. In the absence of a control signal, both of the switches are closed to provide a low impedance shunt path which draws all of the current supplied by the source **40**. In response to a control signal, switch control **46** operates to open the switches **42** and **44**, whereby the current from source **40** may flow through drivers (to be described) to produce signals on a selected memory drive line.

The arrangement further includes two sets of decoder-drivers **52**, **54** in which the drivers function also as matrix switches. Each of the decoders **52**, **54**, receives binary input signals, as from a memory address register **56**, **58**. Although these registers are separately illustrated in the drawing, it should be understood that, in actual practice, each of the decoders may receive different inputs from a single memory address register or other addressing means. The uppermost output **60** of the decoder-driver unit **52** is connected to the uppermost output **62** of the other decoder-driver unit **54** by way of the parallel combination of a transformer primary winding **64** and an adjustable resistor **66**. The secondary winding **68** of this transformer has its opposite ends connected to different ones of a pair of conductors of a memory drive line, for example the conductors **22***b*, **22***b'* (or **24***a*, **24***a'*) of FIGURE 3. Connected across the secondary winding **68** is a potentiometer **70** which has a movable arm **72** connected to system ground, which arm **72** may be positioned so that the voltages applied to the conductors **22***b* and **22***b'* are equal in amplitude and opposite in polarity with respect to system ground.

In like manner, the uppermost output **60** of the driver **52** is connected through separate transformer primary windings and paralleling resistors to each of the other outputs of the decoder-driver **54**. Only one of the latter connections is shown in full for convenience of drawing; however, it will be understood that similar connections appear between points *a* . . . *f* and *a'* . . . *f'*, respectively. Similarly, each of the other outputs of the decoder-driver **52** is connected to each of the outputs of the decoder-driver **54** by way of separate transformer primary windings and parallel resistors, whereby the drivers function also as matrix switches. These connections may be understood more fully by referring to FIGURE 4.

FIGURE 4 is made up of FIGURES 4(*a*) and 4(*b*) which are, respectively, schematic drawings of the matrix-drivers **52**, **54** and the current source **40** with its associated switches **42**, **44**. Refer now to FIGURE 4(*b*). The current source **40** is illustrated at the top of this drawing as comprising a PNP transistor **80** having its base returned to a suitable bias potential, such as −6 volts, and having its emitter connected by way of a variable resistor **82** to the emitter of an NPN transistor **84**. This latter transistor has its base connected to +6 volts, for example, the two base voltages being of the proper magnitude and polarity to bias the transistors **80** and **84** in a conducting condition. The collector of transistor **84** is connected by way of an inductor **86**, which may be a wire through a ferrite bead, to the positive terminal of a battery **88**. Similarly, the collector of the other transistor **80** is connected by way of an inductor **90** to the negative terminal of a battery **92**. Inductors **86** and **90** help to prevent any oscillations during switching. The values of the batteries and other components in the circuit just described are selected to provide a stable source of current.

The first switch **42** is illustrated as an NPN transistor **100** having its emitter grounded and having its collector connected to the positive terminal of battery **92**. The other switch **44** is illustrated as a PNP transistor **102** having its emitter grounded and having its collector connected to the negative terminal of battery **88**. Transistor **100** has its base returned by way of a base biasing resistor **104** to a bias point of −12 volts. Additionally, the base is connected through a series of level shifting diodes **106** to a junction point **108**, which junction point is connected by the series combination of a level shift diode **110** and a resistor **112** to a source of +12 volts. A further diode **114** is connected between the collector of transistor **100** and an intermediate point on the diode chain **106**.

The base of the other transistor **102** is returned by way of a biasing resistor **120** to +12 volts, and is connected via a pair of series connected level shifting diodes **124** to a junction point **122**. A resistor **126** and a pair of level shift diodes **128** are serially connected between junction **122** and a source of −12 volts. A further diode **130** is connected between the collector of transistor **102** and junction point **122**.

The switch control **46** (FIGURE 1) is schematically illustrated in FIGURE 4(*b*) as comprising an NPN transistor **134** having its collector connected to the junction **108** and its emitter connected to the junction **122**. The base of this transistor is returned by way of a base bias resistor **136** to the −12 volt supply. Several similarly poled level shifting diodes **148** are serially connected between the base of transistor **134** and a junction point **138**. A diode **140** and a resistor **142** are connected between junction point **138** and the +12 volt supply. Another diode **144** and a resistor **146** are serially connected between junction point **138** and system ground, with the point between resistor **146** and the cathode of diode **144** connected to the source **48** of interrogate or control pulses.

Suitable circuitry for the matrix-drivers **52** and **54** are illustrated at the left and right sides, respectively, of FIGURE 4(*a*). Driver unit **52** comprises a plurality

of PNP transistors, four transistors **160***a*, **160***b*, **160***c* and **160***d* being shown for convenience. The emitters of these transistors are connected in common and to the positive terminal of the battery **92** (FIGURE 4(*b*)). The collector circuit of each of these transistors includes a similar clamping arrangement, and the clamping arrangement for transistor **160***a* will be described as illustrative of all others. Transistor **160***a* has its collector electrode connected to a junction **164***a* by way of an inductor **162***a*, which may be a wire through a ferrite bead. A potentiometer **166***a* is connected between circuit ground and a source of +6 volts. Sliding arm **168***a* of the potentiometer is coupled to the junction **164***a* by the series combination of a resistor **170***a* and a diode **172***a*. A capacitor **174***a* is connected between circuit ground and the junction of resistor **170***a* and the anode of diode **172***a*. When transistor **160***a* is in a nonconducting condition, this clamping arrangement provides a voltage at the juction point **164***a* which has about the same value as the voltage thereat when the transistor is conducting, thereby helping to prevent noise. The wire through ferrite bead **162***a* helps to prevent any oscillations on the output lines connected to the junction **164***a*.

The other set of drivers, located at the right-hand side of FIGURE 4(*a*), comprises a plurality of NPN transistors, four transistors **180***a* . . . **180***d* being shown. In general, the number of transistors in this set is the same as the number of transistors in the first set. Each of the transistors **180***a* . . . **180***d* has its emitter connected to the negative terminal of battery **88** (FIGURE 4(*b*)). A diode **182***a* . . . **182***d* is connected across the emitter-base junction of each of the transistors **180***a* . . . **180***d*, respectively, and is poled to conduct forward current in the same direction, relative to the base electrode, as the emitter-base junction of the transistor. Each transistor has a similar collector circuit. By way of example, transistor **180***a* has its collector connected by way of an inductor **184***a*, such as a wire through a ferrite bead, to a junction point **186***a*. This inductor helps to prevent oscillations in the output lines connected at junction point **186***a*. A resistor **188***a* is conected between that junction point and circuit ground.

Each of the transistors **160***a* . . . **160***d* in the first set has its collector connected to the collector of each and every transistor in the second set by way of a similar network. Only the network **190***a* connecting the collectors of transistor **160***a* and transistor **180***a* is shown in detail for convenience of drawing. The other networks, which are similar, are represented in the drawing by rectangular boxes **190***b* . . . **190***n*. In the illustrative example, wherein there are four transistors in each of the driver sets, there is a total of sixteen networks connected between the colectors of the various transistors. In the more general case, wherein there are N transistors in each set, there is a total of N^2 intercoupling networks, and thus N^2 outputs from the arrangement. Thus, the transistors **160***a* . . . **160***d* and **180***a* . . . **180***d*, in addition to functioning as drivers, also operate as matrix switches. In this manner, a large number of outputs is available for a very small number of transistors.

The network **190***a* connected between the junction point **164***a* in the collector circuit of transistor **160***a* and the junction point **186***a* in the collector circuit of transistor **180***a* comprises the parallel combination of a variable resistor **66** and the primary winding **64** of an output transformer. Resistor **66** is provided for trimming the line current. The right hand end of the parallel combination is connected directly to junction point **186***a*; the left hand end is coupled to junction point **164***a* via a diode **194***a*.

The secondary winding **68** of this transformer has its opposite ends connected to the two different conductors of a drive line in the cryoelectric memory. By way of example, these two conductors may be the conductors **22***b* and **22***b*′ illustrated in FIGURE 3. A potentiometer **70** is connected across the secondary winding and has its adjustable arm **72** connected to system ground, whereby the adjustable arm **72** may be positioned so that the voltages at the opposite ends of the secondary winding **68** are of equal amplitude and opposite polarity relative to system ground. An electrostatic shield **74** reduces electrostatic coupling between the primary and secondary windings of the transformer. Electrostatic coupling is further reduced by minimizing voltage swings across the primary of the transformer. This latter feature is realized by the collector clamping arrangement previously described.

Consider now the operation of the FIGURE 4 arrangement. Ordinarily the base electrodes of all but one of the transistors **160***a* . . . **160***d* in the first set are maintained at +6 volts, and the base electrodes of all except one of the transistors **180***a* . . . **180***d* in the second set are maintained at −6 volts. These voltages, for example, may be provided by the outputs of decoders. Any given one of the output networks **190***a* . . . **190***n* may be selected by applying input voltages of +2 volts and −2 volts at the bases of the transistors in the first and second sets which are associated with that output network. By way of example, output network **190***a* is selected by applying +2 volts at the base of transistor **160***a* and −2 volts at the base of transistor **180***a*; input network **190***d* is selected by applying +2 volts at the base of transistor **160***a* and −2 volts at the base of transistor **180***d*, etc.

Ordinarily, the control signal source **48** (FIGURE 4(*b*)) supplies an input of ground potential at the cathode of diode **144**. Diode **144** conducts current from the +12 volt supply via resistor **142** and diode **140**. Assuming silicon diodes, the voltage at junction **138** may be about +0.7 volt for this condition. Due to the level shift diodes **148**, the voltage at the base of control transistor **134** is approximately −4 volts. For this condition, transistor **134** is maintained in a nonconducting condition by the voltage applied at its emitter electrode from the biasing arrangement in the base input circuit of transistor **102**. Transistor **102** is biased into conduction, and its base electrode is about −0.7 volt. The voltage at junction **122** is approximately −2.1 volts, which voltage is more positive than the voltage at the base of transsistor **134**. Diode **130**, connected between the collector of transistor **102** and junction point **122**, prevents transistor **102** from becoming saturated, thereby preventing minority carrier storage in this transistor, and enabling this transistor to be turned off with minimum delay. A further function of this diode **130** is that it essentially clamps the voltage at the collector of transistor **102** at approximately −1.4 volts rather than at ground potential when transistor **102** is conducting. The importance of this feature will be discussed hereinafter.

With control transistor **134** biased in a nonconducting condition, transistor **100** is rendered conductive. The feedback diode **114** prevents saturation of the transistor **100**. Additionally, this diode clamps the collector voltage at approximately +1.4 volts, whereas the voltage at the collector would fall close to ground potential if the transistor **100** were allowed to saturate.

With +1.4 volts at the collector of transistor **100** and −1.4 volts at the collector of transistor **102**, the emitter-base junctions of all of the transistors **160***a* . . . **160***d* and **180***a* . . . **180***d* (FIGURE 4 (*b*)) are reverse biased. All of the current from the stable current source **40** then flows through the transistors **100** and **102**.

Let it be assumed that transistor **160***a* has a base input voltage of +2 volts and transistor **180***a* has a base input voltage of −2 volts. All of the other transistors **160***b* . . . **160***d* have base inputs of +6 volts and all of the other transistors **180***b* . . . **180***d* have base inputs of −6 volts. When an interrogate or control pulse from source **48** is applied at the base input terminal of control transistor **134**, diode **144** becomes reverse biased. The voltage at the base of transistor **134** at this instant in time is a function of the values of resistors **136** and **142**. Resistor **136** is chosen to be much much greater than the value of tran-

sistor **142**, whereby the voltage at the base of transistor **134** rises in a positive direction and turns on the transistor **134**.

The more positive voltage which appears at the emitter of transistor **134** when transistor **134** conducts biases off transistor **102**. Further, the voltage at the collector of transistor **134** becomes less positive when transistor **134** conducts, the transistor **100** becomes biased in a nonconducting condition. The current hunting path through transistors **100** and **102** then is interrupted, and the current from stable source **40** becomes available to the selected drivers (transistors **160***a* and transistor **180***a*). The voltage at the emitter of transistor **160***a* rises from +1.4 volts to approximately +2.7 volts, and the voltage at the emitter of transistor **180***a* falls from −1.4 volts to −2.7 volts, or a total voltage change of approximately 2.6 volts across the terminals of the current source **40**. In the absence of the feedback diodes **114** and **130** (FIGURE 4 (*b*)) this change in voltage would be approximately 5.4 volts. Thus, the feedback diodes **114** and **130** limit the voltage swing across the current source to a small value during switching. This has the effect of requiring less current from the source to charge any capacitance on the common lines from the collector of transistor **100** to the emitters of the decoders **160***a* . . . **160***d* and the line from the collector of transistor **102** to the emitters of transistor **180***a* . . . **180***d*. More current then is available initially to the decoders than would otherwise be the case, thereby allowing for a fast rise time of the output signal. Moreover, this small change in voltage results in a stiffer current source.

Current from the stable source **40** flows, in the conventional sense, from the positive terminal of battery **92**, through the emitter-collector path of transistor **160***a*, diode **194***a*, resistor **66** and primary winding **64**, and thence through the collector-emitter path of transistor **180***a* to the negative terminal of battery **88**. This change in current through primary winding **64** induces a voltage across secondary winding, **68**, the voltages at the opposite ends of the latter being of equal ampiltude and of opposite polarity relative to system ground Transistor **160***a* saturates; however, its collector voltage changes very little, if any, due to the action of the collector clamping arrangement.

Transistor **180***a* is prevented from saturating by the external diode **182***a* across its emitter-base junction. Although the voltage changes at collector junction **186***a*, there is practically no change in current through the nonselected output networks connected thereto because of the large values of resistance in the collector clamping arrangements of nonconducting transistors **160***b* . . . **160***d*. The various diodes **194***b* . . . **194***n* prevent sneak current path through nonselected output networks **190***b* . . . **190***n*.

In a similar manner, any other output network **190***b* . . . **190***n* can be energized selectively by applying enabling signals at the bases of the transistors associated therewith. Of course, only one output network is selected at any one time.

In addition to various inductors, etc., described previously, for preventing oscillations and noise, it has been found that even greater stability is achieved by connecting a resistor **200** and a capacitor **202** in series across the terminals of the current source **40** (FIGURE 4(*b*)) to damp any oscillations that might occur. The value of resistor **200** is selected to be about equal to the net resistive impedance R between these terminals, and the value C of capacitor **202** is chosen so that, in relation to the value L of net inductance across those terminals, $R^2=L/C$.

What has been illustrated and described is an arrangement for providing balanced output signals from a single-ended source, in which the drivers function also as matrix switches, and in which the number of outputs can be easily increased at the expense of a much smaller increase in the number of drivers, whereby component count is held to a low number. Further, the single current source and steering control therefore may be combined in the same small package as the driver circuitry to enable compactness. All of these features are compatible with the noise requirements of a balanced cryoelectric memory system.

What is claimed is:

1. The combination comprising:

a stable current source having an input terminal and an output terminal;

first and second groups of junction points;

a first set of signal responsive switch means each having a current carrying path connected between said output terminal and a different one of the junction points in the first group;

a second set of signal responsive switch means each having a current carrying path connected between said input terminal and a different one of the junction points in the second set;

a plurality of output transformers each having a primary winding and a secondary winding, each of the plurality of the primary windings being connected in circuit between a different combination of two junction points, one of which is in the first group and the other of which is in the second group;

means connected across the two ends of each secondary winding for balancing the voltages at the two ends with respect to a reference potential;

input means applying enabling signals to any selected one of the switch means in the first set and any selected one of the switch means in the second set concurrently; and

a signal responsive current diverting path, exclusive of the switch means, connected across the input and output terminals of the stable source and having control means for rendering said path blocked or unblocked selectively, said path in the unblocked condition receiving the current from said stable source.

2. The combination as claimed in claim **1**, wherein the switch means in the first and second sets are amplifying devices.

3. The combination as claimed in claim **1**, wherein the switch means in the first set are transistors of one conductivity type each having one like electrode connected to the output terminal of the stable source, and wherein the switch means in the second set are transistors of the opposite conductivity type each having one like electrode connected to the input terminal of the stable source.

4. The combination as claimed in claim **1**, wherein the balancing means connected across the ends of a secondary winding is a potentiometer having a movable tap maintained at said reference potential.

5. The combination as claimed in claim **4**, wherein there are N switch means in the first set, N switch means in the second set, and N sets of N output transformers each, wherein all of the primary windings of a set have one end connected to the same junction point in the first group, and wherein each of the primary windings in any given group has its other end connected to a different one of the junction points in the second group.

6. The combination as claimed in claim **4**, including a cryoelectric memory having at least one ground plane, drive lines linking said ground plane and being structurally balanced with respect thereto, and means connecting each secondary winding across the ends of a different one of said drive lines.

7. The combination as claimed in claim **6**, wherein the switch means in the first set are transistors of one conductivity type, and wherein the switch means in the second set are transistors of the opposite conductivity type.

8. The combination as claimed in claim **6**, wherein each of said transformers has an electrostatic shield between its primary and secondary windings.

9. The combination as claimed in claim 4, including separate clamping means connected at each of the junction points of one of the groups of junction points, each clamping means providing, in the inoperative state of the associated switch means, a votlage at its associated junction point which has the same value as the voltage thereat when the associated switch means is operative.

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