United States Patent [19]

Charbonnier

[11] **3,811,092**

[45] **May 14, 1974**

[54] **VARIABLE-RATIO ELECTRONIC COUNTER-DIVIDER**

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Oct. 18, 1971 France 71.37407

[52] **U.S. Cl.** **328/39,** 328/43, 328/48

[51] **Int. Cl.** **H03k 23/06**

[58] **Field of Search** 328/39–58

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Assistant Examiner—R. E. Hart
Attorney, Agent, or Firm—William Anthony Drucker

[57] **ABSTRACT**

In a digital frequency dividers with a programmable ratio, there is provided two serially connected division scales, the first scale being set so that its division ratio shifts in whole units under the action of control signals applied thereto, the second scale including a fixed-capacity counter set to count permanently and to apply to the first scale a control signal which is enabled for a predetermined number of counts of the second scale.

Such a divider is adapted for operation at frequencies higher than that of the prior art dividers, and will be used in frequency generators.

15 Claims, 12 Drawing Figures

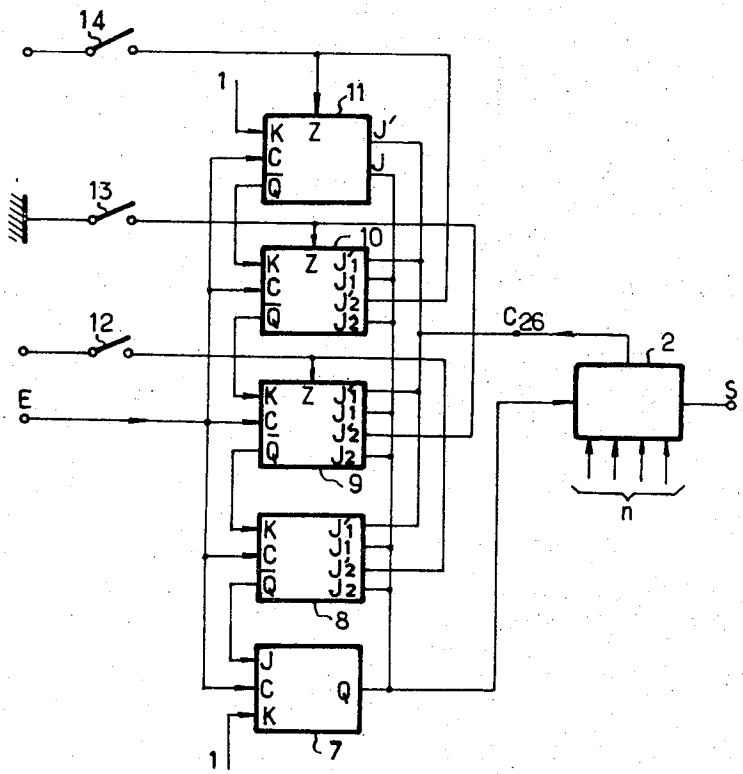


FIG. 1

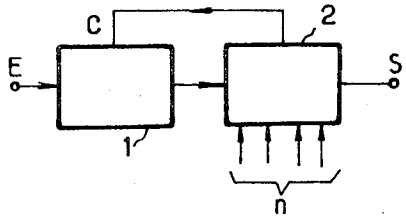


FIG. 2

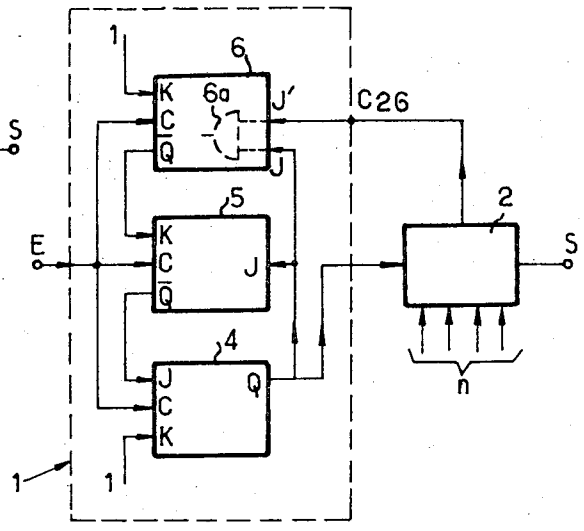


FIG. 3

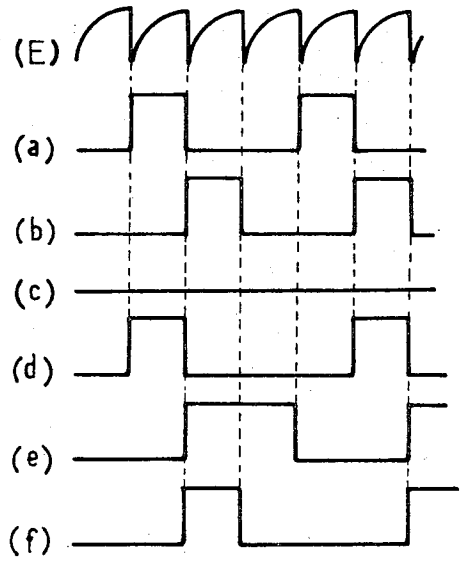


FIG. 4

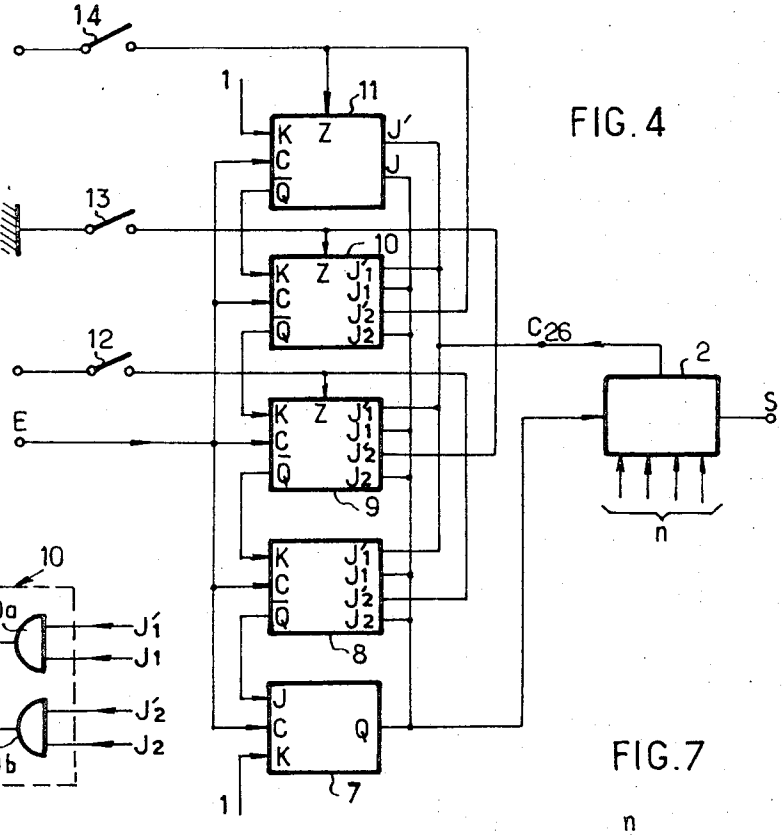


FIG. 5

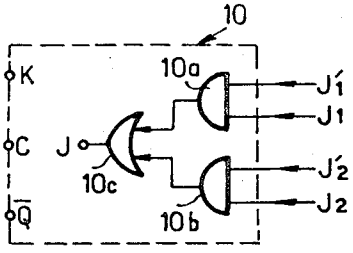


FIG. 6

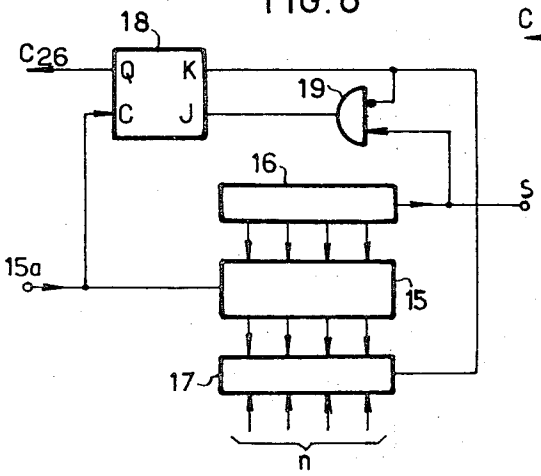


FIG. 7

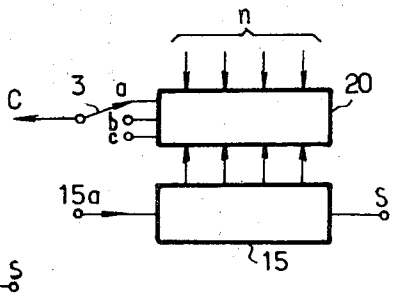


FIG. 8

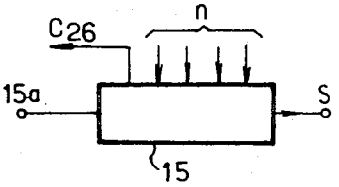
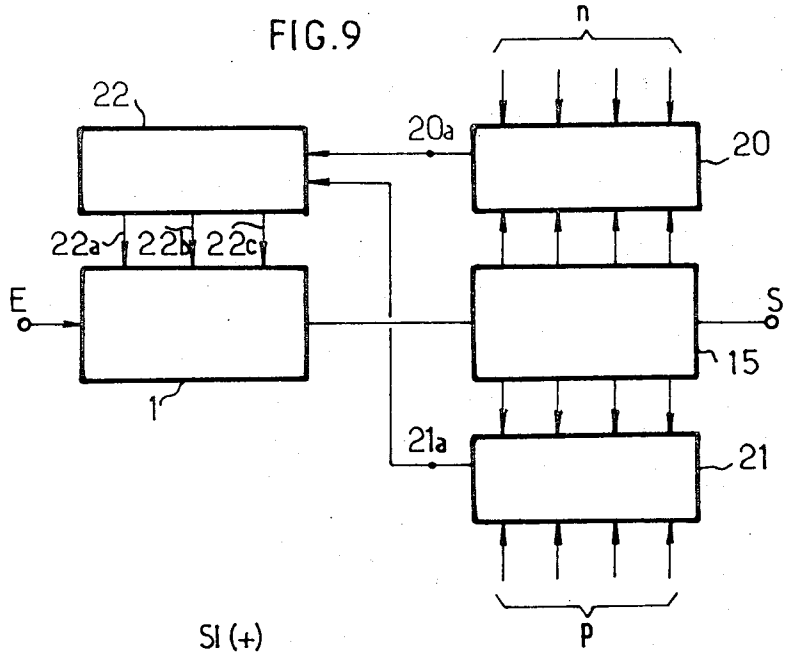


FIG.9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22
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20
22a
22b
22c
E
S
15
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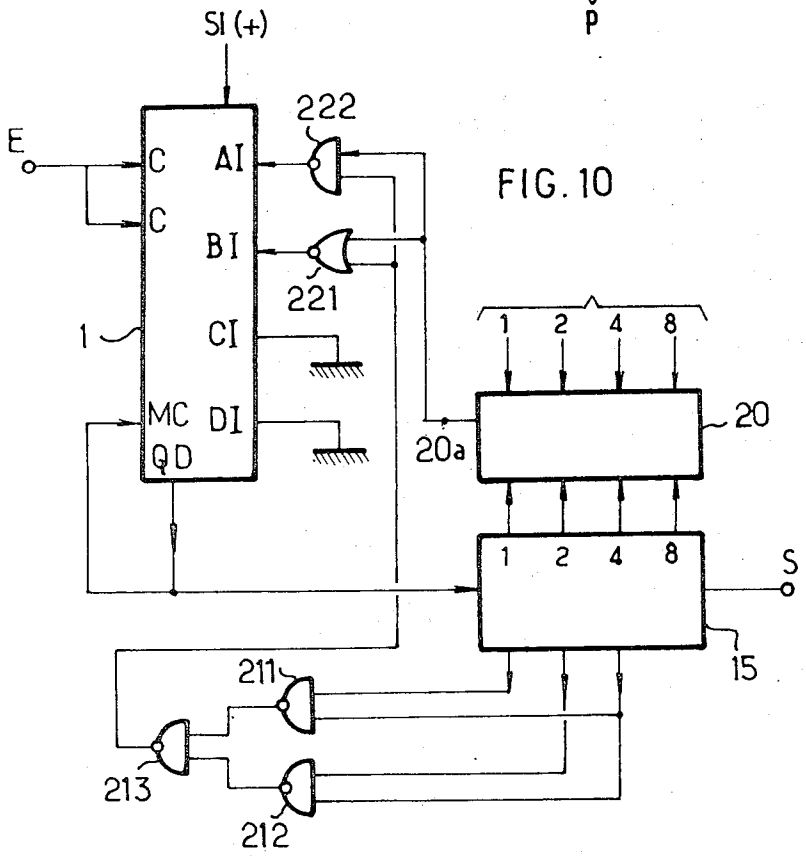
21a
21
P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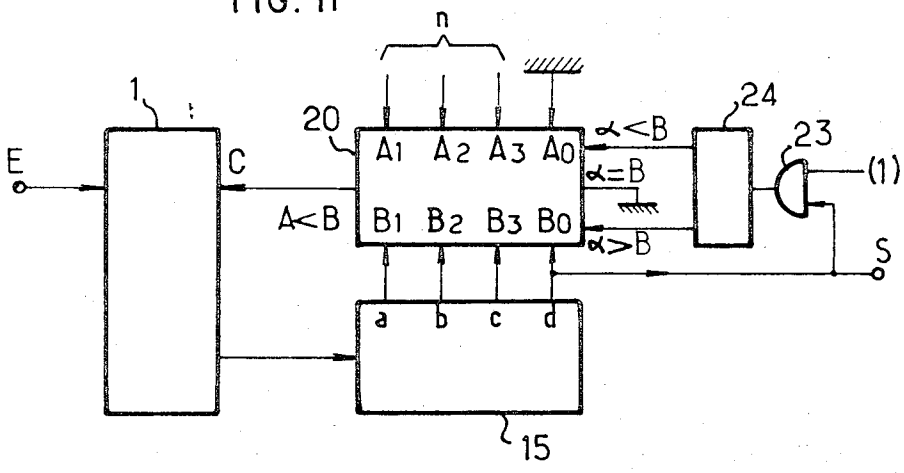
C
AI
C
BI
221
1
CI
MC
DI
QD
1
2
4
8
20
20a
1
2
4
8
S
15
211
213
212

FIG. 10

FIG. 11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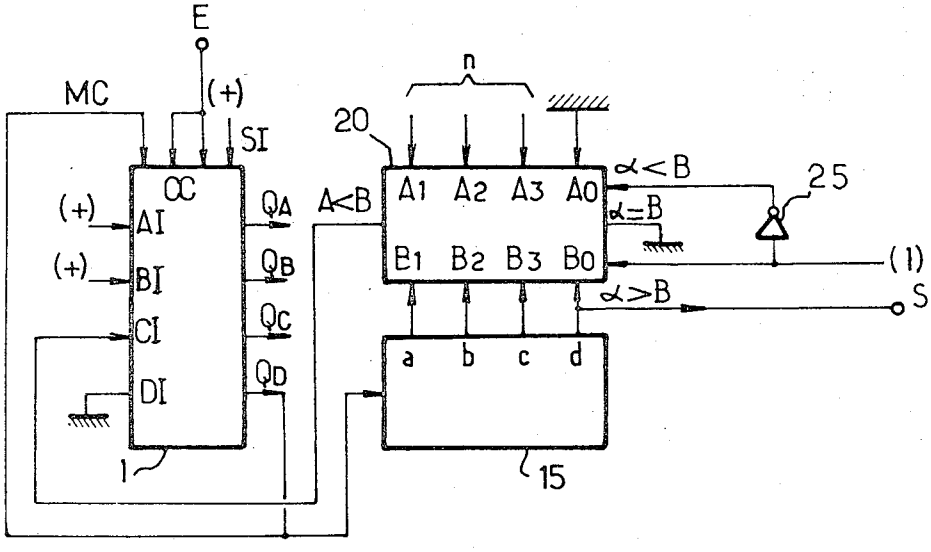
1
20
24
23
E
C
A1 A2 A3 A0
α<B
α=B
A<B
B1 B2 B3 B0
α>B
(1)
S
a b c d
15

FIG.12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CC
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CI
DI
QA
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QC
QD
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α<B
α=B
B1 B2 B3 B0
α>B
(1)
S
a b c d
1
15

VARIABLE-RATIO ELECTRONIC COUNTER-DIVIDER

This invention relates to the variable capacity electronic counters used in frequency dividers.

In some applications of digital frequency dividers with a ratio which can be programmed as a function of an instruction number, e.g. the phase servo-control loops which are comprised in some frequency generators, it would be useful to be able to make the variable-capacity counter which constitutes the basic element of these dividers work at higher frequencies than those which are currently made possible by known connections.

A known connection consists e.g. of associating with the counter a coincident circuit with a predetermined digital value N. At the Nth pulse, the coincident circuit returns the counter to zero. The connection's resolution time is then equal to the sum of the coincident circuit's response time, to which must be added the counter's return-to-zero time and its re-sensitization time. This resolution time is thus considerably increased at the moment of coincidence. Now, the maximum frequency that the divider can handle is the inverse of its working cycle's longest resolution time.

To reduce this resolution time, various methods have been used and, notably, the one termed "alternate operation" which consists of associating, in order to obtain a capacity N, two capacity counters, N-P and P respectively, the first counting N-P pulses, switching to the second counter then being effected until the latter has reached the counter P, at which moment a further switch is made to the first counter. Whenever they coincide, one of the counters is returned to zero, and during this return to zero, the other counter has time to be re-sensitized, which reduces the connection's resolution time.

Nevertheless, this method does not enable the device's maximum resolution time, which is governed by the sensing time of the counters' N-P or P state and the switching times, to be reduced as much as one would wish.

The invention proposes the making of a divider wherein the resolution time is constant and reduced to the response time of a J K flip-flop, which makes it possible to work at considerably higher frequencies than those made possible by known connections. The frequency divider in accordance with the invention includes first and second division scales connected in series, and is chiefly characterised in that the first scale is set so that its division ratio shifts in whole values under the action of control signals, the second scale including a fixed-capacity counter set to count permanently and to transmit to the first scale a control signal which is enabled for a predetermined number of counts of the second scale. In accordance with a particular form of embodiment, the second scale moreover includes means of comparing the counter's count with at least one instruction number to enable at least one control signal and also shift the division ratio by at least one unit.

In accordance with another peculiarity of the invention, the counter comprises a −N scale followed by a −two scale, and the comparator is set to compare the binary number expressed by the logical levels of the parallel outputs of the −N scale with a binary number $n - a/2$, n being the instruction number and a a zero value when is even, and equal to 1 when n is odd, and the device comprises means, associated with the comparator, of enabling or otherwise the comparator output signal, according to the parity of n, said means only acting for N of the counter's counts.

A better understanding of the invention will be obtained from the following description.

In the attached drawing:

FIG. 1 is a basic diagram of a divider connection in accordance with a first form of embodiment of the invention;

FIG. 2 shows a first form of embodiment of the leading division scale which it comprises;

FIG. 3 shows the wave shapes of the output signal of the circuit in FIG. 2;

FIG. 4 shows a variant of the division scale;

FIG. 5 shows the connection of the J inputs of the flip-flops of the circuit in FIG. 4;

FIG. 6 shows a first form of embodiment of the counter-divider comprised in the connection in FIG. 1;

FIGS. 7 and 8 show two variants of this counter-divider;

FIG. 9 is a basic diagram of a counter-divider in accordance with a second form of embodiment;

FIG. 10 illustrates a particular form of embodiment given as an example;

FIG. 11 is a basic diagram of a counter-divider in accordance with a third form of embodiment of the invention; and

FIG. 12 illustrates a more particular form of embodiment, designed to provide a division ratio varying between 20 and 29.

FIG. 1 shows a leading divider 1 which receives at E the frequency F pulses whose frequency is to be divided, and whose output drives a tailing counter-divider 2 which delivers the divided frequency at its output S.

Dividers 1 and 2 are of the type known as division scale ("scale-of-two" with a ratio 2, etc.).

The counter 2 has a capacity N and is set, as soon as it reaches a count n, to send an information to a control input C of the divider 1.

The divider 1 is set so as to have a division ratio (M) so long as this information is not enabled, and to pass to the capacity (M+1) when this information is enabled.

Moreover, it is not essential for the switching information to be enabled during the N−n last counts of each cycle of the counter 2. To obtain the required result, it is sufficient for said information to be enabled, during each cycle, for a certain number (N−n) of counts of the counter 2 and disabled for the n other counts of the cycle, these two series of counts being able to be interleaved in any way.

In fact, during the N−n counts, each output pulse of the divider 1 will be generated by M input pulses, while during the n counts, each output pulse of the divider 1 will be generated by (M+1) input pulses. Finally, the N counts of each cycle of the counter 2, at the end of which it will be returned to zero and will supply at pulse at its output S, will correspond to: $(M+1)n + M(N-n) = MN + n$ input pulses of the connection.

If the number n is programmed by means of an instruction number, the division ratio $MN + n$ of the connection will itself be programmed.

For example, it is possible to take $M = 3$, $N = 10$ and n variable from 0 to 9, which gives a ratio variable from 30 to 39.

In this example, the counter **2** works on a frequency 3 or 4 times weaker than the input frequency, and does not comprise any return-to-zero device for a variable capacity. The result is that it can be made very simply and inexpensively, without thereby limiting the connection's working frequency; for the latter to depend only on the divider **1**, it is sufficient that the coincidence device between the count of the counter **2** and the instruction n should, in the example in question, be capable of switching at least at the frequency F/3, which is easy to achieve. The connection's limit working frequency is then completely independent of n.

FIG. **2** shows a preferred form of embodiment of the divider **1**, in the case where M + 3.

It includes three flip-flops **4–5–6** of the J K type, whose clock inputs C are driven in synchronism by the input signal E. The flip-flops **4** and **6** have their K inputs connected to a one logical level, while the K input of the flip-flop **5** is connected to the $\overline{Q}$ output of the flip-flop **6**. The $\overline{Q}$ output of the flip-flop **5** is connected to the J input of flip-flop **4**, while the Q output of the flip-flop **4** is connected on the one hand to the input of the counter **2** and on the other hand to the J inputs of the flip-flops **5** and **6**.

The latter is moreover of the type comprising two inputs J and J' driving an internal AND gate **6***a*. The J' input is connected to the switching terminal **C26** of the counter **2**.

FIG. **3** shows, at (a), (b) and (c) respectively, the wave shapes of the Q outputs of the flip-flops **4**, **5** and **6**, when the level is applied at J' (which corresponds to the n first counts of the counter **2**) and at (d), (e), (f), the same outputs when the one level is applied at J' (which corresponds to the (N–n) last counts of the counter **2**). The input signal has been shown at (E).

It is obvious that the wave front descending from the first clock pulse (E) makes, in both cases, flip-flop **4** alone rise (the J input of the two others being at zero).

As soon as it has risen, it makes the J input of the flip-flop **5** pass to this One level, and, in the second case (J' + 1) the J input of the flip-flop **6** as well.

In the first case ($J' = 0$) the J input of the flip-flop **6** remains **25** at zero. The result is that when the wavefront descends from the next clock pulse and the flip-flop **4** is de-actuated, the flip-flop **5** will be actuated, and the flip-flop **6** remain de-actuated.

The actuating of the flip-flop **5** makes its $\overline{Q}$ output, and hense the J input of the flip-flop **4**, go to zero. The flip-flop **6** not being actuated, its $\overline{Q}$ output, and thus the K input of the flip-flop **5**, is at One level. The result is that when the wavefront descends from the next clock pulse, the flip-flop **5** will be de-actuated. The J input of the flip-flop **4** will then go from One level, so that at the next clock pulse, the flip-flop **4** will again be actuated.

Finally, we see that in this first case where ($J' = 0$) the Q output of the flip-flop 4 supplies a signal (a) whose frequency is one-third of the clock frequency.

In the second case ($J' = 1$), at the second clock pulse, not only flip-flop **5** but also flip-flop **6** will be actuated. The result is that the K input of flip-flop **5** and the J input of flip-flop **4** go to zero.

At the third pulse, flip-flops **4** and **5** will therefore not change their condition, while flip-flop **6** will be de-actuated, which makes the K input of flip-flop **5** go to one.

At the fourth pulse, flip-flop **5** will therefore be de-actuated, and the other two will not change their condition. The J input of flip-flop **4** therefore goes to One, sot that at the fifth pulse, the flip-flop **4** is again actuated.

Finally, we see that in this second case (where $J' = 1$), the Q output of the flip-flop **4** supplies a signal (d) whose frequency is one-quarter of the clock frequency.

In other words, with 3 flip-flops one does get $M = 3$. To obtain $M = 4$, it would be sufficient to add an intermediate flip-flop set and connected like flip-flop **5**; for $M = 6$, two intermediate flip-flops would be needed, etc.

It should be noted that the informations on the J inputs of the top flip-flops **5–6** are taken into account by the leading flip-flop **4**, and therefore by the connection just before the wavefront descending from the Q signal of the flip-flop **4**. For the resolution time of the connection to depend in the end only on the response time of flip-flop **4**, it is therefore sufficient for the J inputs of the other flip-flops to be able to be positioned during the period of the signal (a). In particular, this counter **2** and its circuit for comparing count and instruction must simply work at the maximum at frequency F/M. A very cheap counter **2**, suitable to work e.g. at 12.5 MHz, thus makes it possible to achieve a divider which can work in the given example $M = 3$ at $F = 37.5$ MHz. FIG. **4** shows a divider making it possible to programme the division ratio, either from 20 to 29 or from 30 to 39 or from 40 to 49 or from 50 to 59, according to the position of the switches **12, 13, 14.**

The leading counter is made up of five flip-flops **7** to **11**, connected as in FIG. **2** as regards their terminals C, K, $\overline{Q}$ and, in the case of flip-flop **7**, terminals J and Q. Like flip-flop **6** in FIG. **2**, flip-flop **11** has two terminals J and J', connected to an internal AND gate (not shown) while flip-flops **8, 9** and **10** each have four terminals **J1, J'1, J2, J'2**, connected to an internal logical unit which has been shown separately in FIG. **5.** This logical unit includes two AND gates **10***a*, **10***b* and an OR gate **10***c* to form the J K flip-flop **18**, whose C input is connected to the terminal **15***a* and whose Q output is connected to the switching terminal **C26** of the divider **1.** An AND gate **19** enables the J input only when the coincidence at **0** is present, and its input connected to the output of **17** comprises a logical inverter element, without the coincidence at n being so. In this way, when $n = 0$, the J and K inputs of the flip-flop are prevented from being enabled simultaneously, which would make it deliver a toothed waveform at the clock frequency.

In fact, this flip-flop is required to deliver a signal enabled for the n first pulses of each cycle received by the circuit **15** and disabled for the N–n last pulses.

This is indeed the case since, when there is coincidence at n, the K input is enabled, which de-actuates the flip-flop. At the end of the cycle, the J input is enabled, which reactuates the flip-flop.

In the second form of embodiment (FIG. **7**), the element **20** is a binary amplitude comparator, which compares the binary instruction number n of the corresponding binary number with the count of the counting

circuit **15**. According to whether the former is greater than, equal to or less than the latter, the output terminal *a* or *b* or *c* is enabled. A device symbolised by the block **3** enables either output *a* or output *b* or output *c* or the logical sum of outputs *b* and *c* to be connected to terminal **C26**.

In the first case, so long as the circuit **15** has not reached the count *n*, the terminal **C26** is enabled, so that the divider has a ratio equal to $MN + n$, as explained above.

In the second case, it is for the $N-n$ last pulses of the cycle that the terminal **C26** is enabled.

The division ratio is thus $Mn+(M+1)N-n = (M+1)N-n$.

In the third case, it is for the $N-n-1$ last pulses of the cycle that the terminal **C26** is enabled, whence a division ratio of $(n+1)\ M + (N - n - 1)\ (N + 1) = (M + 1)\ N-n-1$

Finally, we see that this connection enables a direct spectrum and two inverted spectra to be obtained with the same instruction, which is useful in some applications. An inverted spectrum could also have been obtained with the connection in FIG. **6** by connecting the terminal **C26** to the $\bar{Q}$ output of the flip-flop **18**.

The connection in FIG. **8** does not make it possible to obtain an inverted spectrum. On the other hand, it simply includes a counting circuit **15** of a particular type, known as a bit rate multiplier (or more commonly by the English abbreviation B.R.M.).

Such a circuit has a counting capacity N and whean an *n* instruction is applied to it, it delivers at an output (connected here to **C26**) *n* output pulses per counting cycle. The result is that the divider **1** will be enabled at the rate of $M + 1$ *n* times per cycle, whence the ratio $(M + 1)\ n + M\ (N - n) = MN + n$.

Other forms of embodiment of the dividers **1** and **2** may be devised by a technician, without departing from the spirit of the invention. The values of M, N and *n* may be any whatsoever. It is even possible, providing the forms of embodiment in FIGS. **6** or **8** are used, to make *n* vary between 0 and 10, which will give a division ratio going e.g. from 30 to 40 (or, more generally, from 10 M to 10 $(M+1)$, known counter-dividers do not enable this result to be obtained.

The device described with reference to FIGS. **1** to **7** allows a division ratio in the form $MN + n$ or $(M+1)N - n$ or $(M+1)N - n = 1$ to be obtained.

In general, $N = 10$ and *n* programmable from 0 to 9 will be taken.

M will then be the tens digit of the number which expresses the division ratio. If, e.g., $M = 4$, the division ratio will be programmable from 40 to 49 or from 50 to 41 or from 49 to 40.

In some applications, it would be useful to have available a divider with a ratio programmable e.g. from 43 to 52 or, more generally, in the form $MN + n + p$, i.e. from any digit of the units.

For this purpose it is sufficient to add to a connection whose second scale is in accordance with FIG. **7**, a second binary amplitude comparator comparing the count of the counter with the instruction number *p* and a logical circuit which supplies a supplementary control signal suitable to shift the division ratio of the first scale by two units.

FIG. **9** again shows the elements already described above, bearing the same reference numbers, i.e.:

a leading divider **1** which receives at E the frequency F pulses whose frequency is to be divided, and whose output drives a counter **15**, preferably a decimal one, with one or several decades. This counter **15** delivers the divided frequency at its output S.

a first binary amplitude comparator **20** which compares a binary instruction number *n* with the binary number corresponding to the count of the counter **15**.

Moreover, the connection in FIG. **9** includes:

a second binary amplitude comparator **21** which compares a binary instruction number *p* with the binary number corresponding to the count of the counter **15**.

a logical circuit **22**, made so as to enable its output **22***a*, its output **22***b*, or its output **22***c* according to the condition of the respective outputs **20***a* and **21***a* of the comparators.

More specifically, **22***a* will be enabled when **20***a* and **21***a* are simultaneously enabled: **22***b* will be enabled when only one of the two outputs **22***a* or **22***b* is enabled.

The leading divider **1** is set so that its division ratio is equal to M+2, M+1 or M, according to whether the control input **22***a*, **22***b* or **22***c* is enabled. For a specific value of *p*, so long as *n* is programmed at a value lower than *p*, the working of the connection is as follows:

the counter **15** counts the pulses coming from the divider **1**.

During the *n* first counts, the count of 15 is less than *n* and *p*, so that the outputs **20***a* and **21***a* are simultaneously enabled and the division ratio of 1 is equal to M+2.

During the $p-n$ ensuing counts, the count of 15 is less than *p* but greater than *n*, so that only the output **21***a* is enabled and the division ratio of 1 is equal to $n+1$.

During the $N-n-(p-n)=N-p$ last counts, the count of 15 is greater than *p* and *n*, so that neither of the two outputs **20***a* and **21***a* is enabled: the division ratio of 1 is then equal to *n*. The result is, finally, that during a comple cycle of the counter **15**, for which a pulse is picked up at its output S, the number of pulses applied to the input E was: $(M+2)n + (M+1)\ (p-n)=MN+p+n$.

It is obvious, since *p* and *n* play a symmetrical part in this formula, that the result is the same when $n \gtrless p$.

For example, for $N=10$ (which is the case in the non-limiting example described), the counter **15** was decimal and having a single decade $M=4$ and $p=3$, we get a division ratio variable from 43 to 52 by programming *n* from 0 to 9.

The same result would, of course, be obtained by taking $n=3$ and programming *p* from 0 to 9.

Making the circuits is within the capacity of a technician.

In particular, as we shall see below, the divider **1** can easily be made by means of shift registers of known type. FIG. **12** shows a diagram of an example of a simple embodiment corresponding to $M=3$ and $p=3$.

The binary comparator **2** in FIG. **2** can then be made in the form of three NAND gates **211**-**212**-**213**, connected to the weight outputs **1**, **2** and **4** of the counter **15** as the diagram shows. It is obvious that the output of gate **213** is at One level when at least one of its two inputs is at zero level. Now, the output of gate **211** is at zero level when the weight outputs **1** and **4** of the counter **15** are enabled, i.e. for count 5; the output of

gate **211** is at zero level when the weight outputs **2** and **4** of counter **15** are enabled, i.e. for count 6 and the two outputs of gates **211** and **212** are simultaneously at zero level when the weight outputs **1, 2** and **4** of counter **15** are enabled, i.e. for count 7.

During three conditions out of 10 of counter **15,** the output of gate **213** is thus enabled.

The logical circuit **22** in FIG. **9** is made in the form of a NOR gate **221** and a NAND gate **222,** connected to the output *a* of the binary amplitude comparator **20** and to the output of the gate **213** in the manner shown.

The outputs of gates **221** and **222** are respectively connected to the parallel inputs B1 and A1 of a shift register **1** whose two other parallel inputs C1 and D1 are at Zero level (symbolised by a grounding). These two clock inputs CC are connected to the input terminal E of the connection; the series input SI is put at One level (symbolised by the sign +); the QD parallel output is on the one Hand connected to the input of the counter **15** and on the other hand applied to the mode control line MC. The other parallel outputs, not connected, are not shown.

The working of such a register is well known.

When the terminal MC is at One level, the informations present at the parallel inputs are transferred to the outputs by the first clock pulse, therefore QD goes to zero. The result is that MC goes to zero. The clock pulses then have the effect of transferring to B1 the information present at A1, to C1 the information present at B1, and to QD the information present at D1. If B1 is enabled, three pulses are needed to make this transfer. If A1 is enabled, B1 not being so, four pulses are needed to make this transfer.

Finally, we see that the register **1** will act as a divider by 3 when B1 is enabled (irrespective of the condition of A1); as a divider by 4 when A1 is enabled, B1 not being so; and as a divider by 5 when neither A1 nor B1 is enabled.

Now, it is obvious that if the outputs of the comparator **20** and of the gate **213** are simultaneously at Zero level, the two inputs A1 and B1 will be enabled, whence a 3 division ratio of the register **1.** When the output **20***a* goes to a One value, the output of the gate **213** remaining at Zero level or vice versa, only the input A1 is enabled, whence a 4 division ratio. When the outputs of the comparator **20** and of the gate **213** are simultaneously enabled, the two inputs A1 and B1 will be at Zero level (whence a 5 division ratio).

The result is that, for $n<5$, the division ratio of the register will be equal to **4** for the *n* first counts and for the counts **5–6–7** of the counter **15,** while it will be equal to 3 for the counts **8** and **9** and for the $5-n$ counts following the *n* first. Whence a division ratio of the connection equal to $4\ (n+3) + 3\ (2+5-n) = 33+n$.

Every time *n* increases by one unit while still remaining below 8, the division ratio of the register goes from 4 to 5 for one of the states **5–6–7** of the counter **15,** so that the division ratio of the connection also increases by one unit, thus remaining equal to $33+n$.

When *n* goes from 7 to 8 from 8 to 9, the division ratio of the register goes from 3 to 4 for one of the states **8** and **9** of the counter **15,** so that the division ratio of the connection still remains equal to $33+n$.

This ratio therefore varies from 33 to 42 when *n* is programmed from 0 to 9. To obtain a variation of 33 to 43, it is sufficient to apply a dummy code to the inputs of **20.**

It goes without saying that various variants of the connection may be devised by a technician, without departing from the spirit of the invention.

In particular, the shift register **1** shown in FIG. **9** could be used as a first division scale in any one of the connections illustrated in FIGS. **1** to **8** (for example, this shift register can be the 74–95 type manufactured by the Company "TEXAS Instruments Inc.").

Moreover, the comparators do not necessarily use the binary code and can moreover be made in the form of a suitable logical circuit.

In the connections illustrated in FIGS. **1** to **10,** the output signal may be very dissymetrical; in fact, as the division ratio of the first scale varies during the second scale's counting cycle, the durations of the two half-periods of the output signal can correspond to two input pulse numbers which are substantially different from each other.

The result is obviously that the extraction of the fundamental component of such a signal poses tricky filtration problems, especially as regards the even harmonics.

The purpose of the connection illustrated in FIGS. **11** and **12** is to eliminate this disadvantage and obtain a strictly symmetrical output signal for the even division ratios and, for the odd division ratios, an output signal such that the duration of one of the two half-periods does not exceed by more than one step the duration of the other (the step being the duration of an input pulse of the connection).

FIG. **11** shows a first division scale **1** fitted with a pulse input E and a control input C which, when it is enabled, makes the division ratio go from an $M + 1$ value to an M value. The output of this first scale drives a counter **15** fitted with an output S which constitutes the output of the connection. A binary amplitude comparator **20** receives, at its inputs A_1, A_2 and A_3, the respective weight codes **2, 4** and **8** of a binary coded instruction number *n*. The code **1** is applied to an input of an AND gate **23.** The output A<B of the comparator is connected to the input C of scale **1.**

A zero logical level (which is symbolised by the ground) is permanently applied to the One weight input A_0 of the comparator **20.**

The counter **15** consists of a scale-of-five with outputs *a, b* and *c* with respective weights **1, 2** and **4,** respectively connected to the inputs B_1, B_2 and B_3 of the comparator **20,** and a scale-of-two whose output *d* is connected on the one hand to the output S and on the other hand to the other input of the gate **23.**

The output of the gate **23** is connected to a logical circuit **24** with two outputs, respectively connected to the two inputs $a>B$ and $a<B$ of the comparator **20.** The input $a = B$ of the comparator **20** is permanently at Zero level (symbolised by the ground).

The comparator **20** consits e.g. of the Texas Instruments Inc. integrated circuit type 7485. It is known that, in such a connection, the input have the following decreasing priorities: $A_3\ B_3$, $A_2\ B_2$, $A_1\ B_1$, $A_0\ B_0$ and finally $a>B$, $a=B$ or $a<B$. This means that, when $A_3<B_3$, the output A<B is enabled irrespective of the logical levels of the other inputs. Similarly, if $A_3 = B_3$ and $A_2<B_2$, the output A B is enabled irrespective of the logical levels of the other inputs. For the inputs $A>B$, $a = B$ or $A<B$ to have an influence on the comparator,

it is necessary to have $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$ and $A_0 = B_0$.

If we consider a counting cycle of the counter **15**, during the 5 first counts the output d is at Zero level, while it is at One level during the 5 last counts.

If n is even, the code (1) will never be enabled. The logical circuit **24** is set, when its input is thus at Zero level, to enable its output $a < B$. On the other hand, if n is odd, the code (1) is enabled, so that the input of the circuit **24** is enabled during the five last counts of the counter **15**. The circuit **24** is set so that it then enables its output $a>B$. It should be noted that the comparator **20** will compare the weight digits **1, 2** and **4** of the count of the counter **15** with the weight digits **2, 4** and **8** of the instruction n. In other words, it will in fact make a comparison between a binary number A between 1 and 5 supplied by the counter **15** and a binary number also between 1 and 5, and equal to $(n-a)/2$ with $a = 0$ if n is even and $a = 1$ if n is odd.

During the five last counts of the counter **15**, d is at One level, therefore greater than A_0. So long as the count abc is less than $(n-a)/2$, we have: $a<A_1$, $b<A_2$, $c<A_3$ and, consequently, the output $A<B$ is not enabled. The scale **1** thus divides by $M+1$. When the count abc is equal to $(n-a)/2$, we get: $a = A_1$, $b = A_2$, $c = A_3$ and $d>A_0$; consequently the output $A<B$ is enabled, and the scale **1** divides by M. When the count abc is greater than $(n-a)/2$, the output $A<B$ is, of course, also enabled. Finally, the number of pulses at the input E counter by the connection is, during this second half of the cycle, equal to:

$$M\,[5-(n-a/2)]+(M+1)(n-a/2)$$

During the first half of the cycle, d is at Zero level, therefore equal to A_0.

As long as the binary number expressed by the digits abc is less than $(n-a)/2$, the output A<B of the comparator is of course enabled, so that the division ratio of the scale **1** is equal to M. When the binary number abc is greater than $(n-a)/2$ the division ratio of the scale **1** is equal to $M+1$.

When the binary number abc is equal to $(N-a)/2$ $a = A_1$, $b = A_2$, $c = A_3$ and $d = A_0$. In this case, it is therefore the condition of the inputs $a>B$ and $a<B$ which determines the enabling of the output $A<B$.

If n is even, the output $a<B$ being enabled, $A<B$ is too and the division ratio of the scale **1** is M. Consequently, the division ratio of the connection is then equal to: $2M\,(5-n/2)+n\,(M+1)$.

The output signal picked up at S is then strictly symmetrical, since it corresponds to the same number of input of input pulses for each of the two halves of the cycle.

If n is odd, the output $a>B$ being enabled, A<B is not when the number abc is equal to $(n-a)/2$. During the second half of the cycle, the counter **15** therefore then counts one input pulse more than during the first half (the output signal is therefore quasi-symmetrical).

In other words, the division ratio is then:

$$M[5-(n-1/2)]+(M+1)(n-1)/2+M[5-(n-1/2)-1]+(M+1)[(n-1)/2+1)$$

which can also be written:

$$M\,[5-(n-a/2)]+(M+1)\,(n-a)/2+M\,[5-(n+a/2)]+(M+1)(n+a)/2$$

It will be noted that this latter formula also covers the case where n is even, since then $n = 0$.

For the counter **15**, a divider by N could be used followed by a scale-of-two and the formula giving the division ratio of the connection would then become:

$$M\,[N-(n-a/2)]+(M+1)(n-a)/2+M\,[N-(n+a/2)]+(M+1)(n+a)/2$$

As an example, for $M = 2$, the division ratio will vary from **20** to **29** for n varying from 0 to 9.

FIG. **12** shosw a simplified connection designed to obtain this particular result.

It can be seen that the code **1** of the number n is then applied directly to the input $a<B$ of the comparator **20** and, after inversion by a logical inverter **25**, to the input $a>B$. The scale **1** is made in the form of a shift register with a series input SI at One level, its clock inputs CC connected to each other to constitute the input E of the connection, its parallel inputs **A1, B1** at One level, its parallel input **D1** at Zero level, and its parallel input **C1** connected to the enabling terminal $A<B$.

The parallel output QD is connected on the one hand to the input of the counter **15** and on the other hand to the mode control input MC of the register.

It is known that in such a register, when MC is at One level, the informations at the inputs **A1 . . . D1** are respectively transferred over the outputs QA . . . QD to the first clock pulse. This first pulse therefore gives $Q_A = Q_B = 1$ and $Q_D = 0$. If A<B is enabled, it moreover gives $Q_C = 1$. As $Q_D = 0$, MC goes to Zero level. At that moment, the informations Q_A Q_B and Q_C are transferred to Q_D by shifting. In other words, at the second clock pulse Q_D goes to One level. The register thus works on a scale-of-two.

If A<B is not enabled, there will be, after the first pulse, $Q_C = 0$. It is therefore only at the third pulse that the information **1** present at Q_B will be transferred to Q_D, thus bringing the register back to its initial state. It will therefore work, in this case, on a scale-of-three.

As regards the second scale (15 – 20 – 25), its working is the same as that of the scale (15 – 20 – 23 – 24) in FIG. **11**. In effect, with n even, the inverter **25** enables the input L>B of the comparator **20**, while with n odd, it enables the input L>B.

It goes without saying that various modifications may be made to the connections described and shown, without departing from the spirit of the invention.

I claim:

1. Frequency divider comprising a first and a second division scales each having one pulse input and one pulse output, the pulse output of the second scale being connected to the pulse output of the first scale, wherein the first scale has a control input and is set so that its division ratio shifts in whole units under the action of control signals applied to its control input, the second scale including a fixed-capacity counter set to count permanently and to transmit to the first scale control input a control signal and means for enabling the control signal for a predetermined number of the counts displayed by the second scale.

2. Frequency divider in accordance with claim **1**, characterised in that the second scale includes a decimal counter and a binary amplitude comparator which compares the count of said counter with said predetermined number.

3. Frequency divider in accordance with claim **1**, characterised in that the second scale includes a bit rate multiplier.

4. Frequency divider in accordance with claim **1**, characterized in that the second scale moreover in-

cludes means for comparing the count of the fixed-capacity counter with at least one instruction number to enable at least one control signal and thus shift the division ratio by at least one unit.

5. Frequency divider in accordance with claim 4, characterised in that at least one of the instruction numbers is variable.

6. Frequency divider in accordance with claim 4, characterised in that, the counter being decimal, a first instruction number varies between 0 and $10^n - 1$, a second instruction number being fixed and less than $10^n - 1$.

7. Counter-divider in accordance with claim 4, wherein said means are binary amplitude comparators associated with a logical circuit.

8. Frequency divider comprising a first and a second division scales each having one pulse input and one pulse output, the pulse output of the second scale being connected to the pulse output of the first scale, wherein the first scale has a control input and is set so that its division ratio shifts in whole units under the action of control signals applied to its control input, the second scale including a fixed-capacity counter set to count permanently and to transmit to the first scale control input a control signal and means for enabling the control signal for a predetermined number of the counts displayed by the second scale, the first scale including a number of J K flip-flops at least equal to the value which its division ratio assumes when the control signal is not enabled, the said flip-flops having clock impulse driven in synchronism by the frequency to be divided, the said flip-flops further having J and K inputs and Q and Q outputs, the Q output of the first flip-flop driving the J inputs of the other flip-flops and the pulse input of the second scale, the $\overline{Q}$ output of each of said other flip-flops driving the K input of the next flip-flop down with the exception of the first, the $\overline{Q}$ output of the second flip-flop driving the J input of the first, the K inputs of the first and last flip-flops being connected to a One logical level, the last flip-flop having a further input J^x to which said control signal is applied.

9. Frequency divider in accordance with claim 8, characterised in that the first scale comprises means for varying its division ratio by grounding some of the inputs of the flip-flops which it comprises.

10. Frequency divider comprising a first and a second division scales each having one pulse input and one pulse output, the pulse output of the second scale being connected to the pulse output of the first scale, wherein the first scale has a control input and is set so that its division ratio shifts in whole units under the action of control signals applied to its control input, the second scale including a fixed-capacity counter set to count permanently and to transmit to the first scale control input a control signal and means for enabling the control signal for a predetermined number of the counts displayed by the second scale, the second scale including a decimal counter having first and second outputs, means for generating a One logical level respectively at said first output when the count of the decimal counter coincides with said predetermined number and at a second output when the said count coincides with the zero value, and a J K flip-flop supplying said control signal and having K and J inputs connected to said first and second outputs respectively.

11. Frequency divider in accordance with claim 10, wherein said first output is connected on the one hand to the K input of the flip-flop and on the onther hand, via a logical inverter, to a first input of an AND gate having first and second inputs, said second output being directly connected to the second input of the AND gate, said AND gate having an output connected at the J input of the said flip-flop.

12. Frequency devider comprising a first and a second division scales each having one pulse input and one pulse output, the pulse output of the second scale being connected to the pulse output of the first scale, wherein the first scale has a control input and is set so that its division ratio shifts in whole units under the action of control signals applied to its control input, the second scale including a fixed-capacity counter set to count permanently and to transmit to the first scale control input a control signal and means for enabling the control signal for a predetermined number of the counts displayed by the second scale, the first division scale comprising a shift register of the type having a mode control input which, according to whether or not it is enabled, makes it possible to obtain the transfer in parallel of information from the parallel inputs to the corresponding parallel outputs thereof, or to obtain the gradual transfer of the information from one parallel output thereof to the following ones, one of the parallel outputs of said shift register being connected to the fixed-capacity counter and to the said mode control input and means for comparing the count of the fixed-capacity counter with at least one instruction number to enable at least one control signal and thus shift the division ratio by at least one unit, the said comparing means being connected to some of the parallel inputs.

13. Frequency divider comprising a first and a second division scales each having one pulse input and one pulse output, the pulse output of the second scale being connected to the pulse output of the first scale, wherein the first scale has a control input and is set so that its division ratio shifts by one unit under the action of control signals applied to its control input, the second scale including a fixed-capacity counter set to count permanently and to transmit to the first scale control input a control signal, the second scale further including a binary amplitude comparator comparing the count of said fixed-capacity counter with an instruction number to generate said control signals, the fixed-capacity counter comprising a scale-of-N followed by a scale-of-two, and the binary amplitude comparator being set to compare the binary number expressed by the logical levels of the parallel outputs of the scale-of-N with a binary number $n - a/2$, n being the instruction number and "a" a nil value when n is even, and a value equal to 1 when is odd, and means, associated with the comparator, for enabling or not enabling the output signal of the comparator, according to the parity of n, said means only acting for N of the counts of the fixed-capacity counter.

14. Frequency divider in accordance with claim 13, characterised by a comparator comprising K couples of inputs with respectively decreasing priorities, the $(K - 2)$ first inputs on one side of the comparator receiving logical levels which define the respective binary digits of the instruction number, with the exception of the binary units digit, while the next input receives a predetermined logical level, the $(K - 1)$ first inputs of the other side of the comparator being connected to the respective outputs of the fixed-capacity counter, the last

couple of inputs of the comparator being connected to means for enabling or not enabling, according to whether the instruction number is even or odd, those of the inputs of said couple which will enable the output signal of the comparator for N of the counts of the fixed-capacity counter.

15. Frequency-divider in accordance with claim **14**, characterised by a decimal counter comprising a scale-of-five followed by a scale-of-two, and by a binary comparator having a first couple of inputs which respectively receive the 1 weight output of the counter and the 8 code of the instruction number, a second couple of inputs which respectively receive the 2 weight output of the counter and the 4 code of the instruction number, a third couple of inputs which respectively receive the 1 weight output of the counter and the 2 code of the instruction number, a fourth couple of inputs which respectively receive the 5 weight output of the counter and a Zero logical level, and a fifth couple of inputs respectively connected to the 1 code of the instruction number, directly and via a logical inverter, said couples of inputs having priorities decreasing in the order in which they are enumerated.

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