(54) Title: TWO-STEP ANALOG-TO-DIGITAL CONVERTER

Two-step analog-to-digital converter, for the conversion of an input analog signal (Vin) in a N bit digital code, consisting of a sample and hold circuit (S/H), a resistive ladder (SR), a set of comparators (COMP), a set of control (LCC), coding (COD) and storage or latch (LT, LTU) digital circuits. The converter reuses the same resistive ladder (SR) and the same comparators (COMP) for both conversion steps of input signal (Vin).

(57) Abstract
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TWO-STEP ANALOG-TO-DIGITAL CONVERTER

The present invention refers to a two-step analog-to-digital converter for the conversion of an analog electric signal into a digital electric signal. In the first step the most significant bits (MSBs) are coded and in the second step the last significant bits (LSBs) of the digital code are determined.

This converter relies on flash technique, where the input to be coded is simultaneously compared to a plurality of reference voltages.

Some known implementations of the two-step flash conversion, require two resistive ladders, one for the MSBs and the other one for the LSBs. The comparators employed in the two subsequent conversion steps are the same.

This implementation is disadvantageous as regards silicon die size, considering also that the resistive ladder value derives its lower limit from power dissipation specification.

It is also necessary to generate two extra reference voltages, scaled down by $2^{N/2}$ with respect to full scale values, where $N$ is the conversion bit number. These voltages bias the additional ladder and have to determine the reference levels for the LSBs with the same accuracy as the levels for the MSBs on main resistance. Possible inaccuracies in this operation can originate the loss of intrinsic monotonic nature of potentiometric converters, as well as a downturn of the converter absolute linearity tied to the accuracy of the division of the full scale voltage by the resistive ladder.

To avoid these drawbacks, some known solutions propose a conversion scheme where the LSBs are determined by using the same resistive ladder of the MSBs coarse conversion, introducing an amplifier circuit with gain equal to $2^{N/2}$. This amplifier has a loop gain-bandwidth product equal to the product between the open loop cut off frequency and the feedback factor, which is close to $1/2^{N/2}$. This involves the design of an operational amplifier having a potential
operation speed $2^{N/2}$ times higher than the one actually employed, with the simultaneous charge of a high slew rate specification due to the high input capacitive load, equal to $2^{N/2}\cdot C_{\text{in}}$, where $C_{\text{in}}$ is the input capacitance.

The object of the present invention is to realize the analog-to-digital conversion as previously described, by using a single resistive ladder overcoming the drawback of the previous solutions. The converter forming the object of the present invention gets to obtain good operation speed, low power dissipation and limited silicon die size while preserving the monotonic nature of potentiometric converters.

These targets are reached through the invention consisting of an analog-to-digital converter for the conversion of an analog input signal to a N bit digital code, including:

- a sample and hold circuit receiving at its input the analog signal to be coded;
- a ladder of resistances connected in series among them whose extrem terminals are connected to two reference voltage sources for the generation of intermediate comparison voltages;
- a set of comparators for comparison of the input signal and said intermediate reference thresholds;
- a set of latches connected to the outputs of said comparators;
- a coder to combine a digital code to the said comparators output configuration, according to previously defined rules;
- a storage buffer for the digital code produced; characterized by the fact that said ladder consists of $2^N$ elementary resistances clustered in $2^{N/2}$ segments, each one formed by $2^{N/2}$ elementary resistances and that said comparators are $2^{N/2} - 1$ in number, selectively connectable to the taps of segments by means of a plurality of switches, and to the taps of each single elementary resistance of a segment via
one of the switch block controlled by a selection combinatorial logic circuit whose inputs are connected to the outputs of said latches.

According to the invention, it is supposed the reuse of the same resistive ladder for the conversion both of the MSBs and of the (LSBs) without adding further analog circuitry, switching subsequently the same set of comparators from the main resistive ladder to one of its segments. It is thus obtained a considerable save in the silicon die size and a limited power dissipation.

The invention shall be now described making reference to a preferred realization form, shown in the figures enclosed, where:

Fig. 1 shows a general block diagram of a converter according to the invention;

Fig. 2 shows in detail the architecture of the resistive ladder;

Fig. 3 shows a block diagram of another realization form of the converter according to the invention; and

Fig. 4 shows the time trend of the control phases $\Phi_1$-$\Phi_4$ and of the S/H control phase.

Referring in particular to Figgs. 1 and 3, the converter according to the invention includes a resistive ladder labelled SR, a set of comparators or comparing elements ($2^m - 1$ in number), clustered in the COMP block.

More in detail, each comparator can selectively be connected to the taps of segments GR (case A), to the taps of the single elementary resistances Rei of a chosen segment GR (case B) and to the output of the sample and hold circuit S/H (case C). In case A the connection is made through a plurality of switches SWG; in case B it is made by a controlled switch block (SWF) selected by a combinatorial circuit (LCC) whose inputs matches the outputs of said latches LT; finally in case C, through a plurality of switches SWI. The connection to the reference voltages and to the input voltage takes place on different times.
The \(2^{N/2}-1\) outputs of comparators are connected to the same number of latches or hold circuits forming the LT block, and from these ones to the encoder COD whose generated code is stored in the output latches LTU. It is also provided a combinatorial logic circuitry LCC between the block LT and switch blocks SWF.

The converter components shall now be described more in detail.

The resistive ladder SR is made of \(2N\) elementary resistances \(R_e\) of equal value, where \(N\) is the number of bits by which the analog signal shall be coded, clustered in \(2^{N/2}\) segments, each one consisting of \(2^{N/2}\) elementary resistances (see Fig. 2).

The terminals of the ladder SR are connected to two reference voltages \(V_{\text{ref1}}\) and \(V_{\text{ref2}}\) defining the dynamic range of the input signal. Voltage values available at the taps of the main segments GR represent the decisional thresholds for the conversion of the MSBs and are forced at the comparators COMP through the closing of the \(2^{N/2}-1\) switches forming SWG. Voltages available at the taps of the elementary resistances \(R_e\) inside each segment GR represent the reference levels for the determination of the LSBs. In this case the connection to comparators is assured by SWF blocks, each one consisting of \(2^{N/2}-1\) switches, under the control of the logic LCC.

The comparators of the COMP block are preferably of the type forming the object of the patent application of the same applicant under the title: "Low power dissipation autozeroed comparator circuit" reference to which has to be made for further details. However, other comparing circuits of the known type can be employed.

The S/H circuit essentially includes a capacitance referred to an analog ground voltage, followed by a unit gain de-coupling element. The middle point of the resistive ladder RS, labelled \(V_{\text{ref}}\) in Fig. 1, is selected as reference analog ground.
We shall now describe the operation of a complete conversion cycle requiring four clock-signals or phases shown in Fig. 4.

During phase #1, comparators COMP are autozeroed, and their reference inputs are connected to the $2^{N/2}-1$ reference voltages available at the taps of segments GR, indicated also as coarse reference voltages. At the same time, the input signal $V_{in}$ is sampled and stored in the S/H circuit.

During subsequent phase #2, the inputs of comparators are switched to the output of the S/H circuit, in such a way that each comparator makes the comparison between the sample of the input signal to be coded and one of the reference levels generated by the resistive ladder SR. The output of each comparator, assumes, for instance, the high level when the input signal sample is higher than the reference threshold present at the other input.

On the basis of the $2^{N/2}-1$ logic outputs of comparators, the digital encoder COD determines the N/2 MSBs, according to the selected coding system. This coding system can be of different type and is not described here in detail.

During the same phase #2, the outputs of comparators are also feed to the LCC selection combinatorial logic and used to identify one of the main resistive segments GR, and more in detail the one whose upper tap corresponds to a reference voltage immediately higher than the value of the input voltage $V_{in}$. The LCC logic generates $2^{N/2}-1$ control signals, controlling in parallel the switch blocks SWF, connected to the taps of the elementary resistances $R_{e}$ of each main resistive segment GR.

During phase #3, second autozero phase of the converter, only one of the aforesaid control signal is activated, and it determines the connection of the $2^{N/2}-1$ comparators COMP already used, to the new fine reference values internal to the segment GR identified by the LCC logic.
At the beginning of phase $4$, second comparison phase, the inputs of comparators are switched again to S/H output to determine the remaining N/2 LABS referring to the voltage $V_{in}$ stored on the capacitance $C_i$.

The converter according to the invention requires a number of switches on the resistive ladder equal to the sum of $2^{n/2}-1$ (for the MSBs determination) and of $2^{n/2}*(2^{n/2}-1)$ (for LSBs determination). These switches conduct current only during a brief transient, therefore they do not affect the voltage value of the point where references for comparison are withdrawn.

According to a preferred realization form of the invention, shown in Fig. 3, however the number of switches can be reduced, and this without adding further control logic circuitry. The same references used in Fig. 1 have been used in Fig. 3 for the components performing equal or similar functions.

This realization form presents a single switch block SWF connected to the resistances of the middle GR segment of the resistive ladder, whose lower tap is referred to the analog ground voltage ($V_{ref}$).

Furthermore the capacitance $C_i$ of the sample and hold circuit (S/H) has a plate which can be connected to the input voltage to be converted ($V_{in}$), and the other plate selectively connectable to a lowering voltage ($V_{low}$) chosen by a combinatorial logic LCA, and to the analog ground voltage ($V_{ref}$).

According to this realization form, during the second conversion step, the conversion of the difference between the input voltage $V_{in}$ and the reference one resulting immediately lower than $V_{in}$, is performed. This difference ranges between 0 and $\delta v$, with $\delta v = (V_{ref1} - V_{ref2})/2^{n/2}$ and is referred to the analog ground.

The operation of the analog-to-digital converter of Fig. 3 is the following.
During phase $\phi_1$ the operation is alike that of the converter of Fig. 1.

During phase $\phi_2$ coding of the MSBs takes place as before. Furthermore, the selection of an appropriate voltage $V_{low}$ takes place in this phase, maintaining the voltage to convert during the second conversion step, within the same predetermined voltage interval $\delta v$, for any input voltage. The lowering voltage $V_{low}$ is selected among a finished set of possible values made of the voltages at the taps of GR segments, including $V_{ref1}$.

Referring to the structure of the S/H circuit shown in Fig. 3, the voltage $V_x$ at the S/H output is equal to $(V_{in} + V_{low} - V_{ref})$, where $V_{ref}$ corresponds to the middle point of the resistive ladder. Two cases occur which shall be described below, making reference to a 2.5V analog ground voltage $V_{ref}$.

Case A

$V_{in} - 2.5V + n\delta v < V_{in} < 2.5 + (n+1)\delta v$

with $n$ integer ranging from 0 to $N/2$.

In this case it is selected $V_{low} = 2.5 - n\delta v$ and voltage $V_x$ becomes:

lower limit $2.5+n\delta v-n\delta v=2.5$

$V_x=V_{in}-2.5+2.5-n\delta v$

upper limit $2.5+(N+1)\delta v-n\delta v=2.5+\delta v$

Case B

$V_{in} \leq 2.5V 2.5 - (n + 1)\delta v < V_{in} < 2.5 - n\delta v$

In this case it is selected $V_{low} = 2.5 + (n + 1)\delta v$ and voltage $V_x$ becomes:

lower limit $2.5-(n+1)\delta v+(n+1)\delta v=2.5$

$V_x=V_{in}-2.5+2.5+(n+1)\delta v$

upper limit $2.5-n\delta v+(n+1)\delta v=2.5+\delta v$

Depending on comparators outputs the selection logic LCA, generates the $2^{N/2}$ control signals to determine $V_{low}$ by means of switches $SW$, being active one signal at a time. Determining the new level of scaled down input voltage is affected by error, due to the parasitic capacitance of the top plate of the hold capacitance $C_I$, which determines the
conversion accuracy. In the implemented realization form this limit is equal to 8 bits.

During phase $\phi_3$, second autozero phase, comparator inputs, already used for the MSBs, are switched to the voltages of fine reference. These thresholds are obtained at the taps of the elementary resistances $R_e$ of the CR resistive segment, referred at the bottom to 2.5 V ($V_{\text{ref}}$) and at the top to $(2.5 + \delta V)$ V. At the same time, the bottom plate of the hold capacitance $C_i$ of S/H is connected to the $V_{\text{low}}$ voltage previously identified.

Finally, during phase $\phi_4$ the operation is similar to the one previously described referring to Fig. 1. During this phase the capacitance $C_i$ of S/H is referred to $V_{\text{low}}$.

With the described structure, the number of switches which persist on the ladder is equal to the sum of $2^{n/2} - 1$ (for the MSBs determination) and of $2^{n/2} - 1 + 2^{n/2}$ (for the LSBs determination).
CLAIMS

1. Analog-to-digital converter for the conversion of an input analog signal (Vin) to a N bits digital code, including:
   a sample and hold circuit (S/H) receiving at its input the analog signal (Vin) to be coded;
   a ladder of resistances (SR) connected in series among them, whose extreme terminals are connected to two reference voltage sources (Vref1, Vref2) for the generation of intermediate comparison voltages;
   a set of comparators (COMP) connectable for the comparison among the input signal and said intermediate reference thresholds;
   a plurality of latches (LT) connected to the outputs of said comparators;
   a coder (COD) to associate a digital code to the output configuration of said comparators, according to preset rules;
   a storage buffer (LTU) to store the digital code produced;
   characterized by the fact that said ladder consists of 2N elementary resistances (Re) clustered in 2^{N/2} segments (GR), each one made of 2^{N/2} elementary resistances, and that said comparators (COMP) are 2^{N/2} -1 in number, selectively connectable to the taps of segments (GR) by means of a plurality of switches (SWG), and to the taps of the single elementary resistances (Re) of a segment through one of the switch blocks (SWF) controlled by a selection combinatorial logic circuit (LCC) whose inputs are connected to the outputs of said latches (LT).

2. Analog-to-digital converter according to claim 1, characterized by the fact to require 2^{N/2} switch blocks, the outputs of said selection combinatorial logic circuit (LCC) forming the enabling signals for only one of said switch blocks.
3. analog-to-digital converter according to claim 1, characterized by the fact to require a single switch block (SWF) to connect the reference inputs of comparators (COMP) to the elementary resistances (Re) of a predetermined segment (GR), and by the fact that the sample and hold circuit (S/H) receives as reference a lowering voltage (Vlow) selected by the combinatorial logic circuit (LCA) and the analog ground voltage (Vref) corresponding to the voltage of the middle point of the resistive ladder (SR).

4. Analog-to-digital converter according to claim 3, characterized by the fact that said predetermined resistive segment (GR) is the one referred at the bottom to the analog ground (Vref).

5. Analog-to-digital converter according to claim 3 or 4, characterized by the fact that the sample and hold circuit (S/H) includes a storage capacitor having a plate which can be connected to the input voltage to convert (Vin), and the other plate which can be connected to said lowering voltage (Vlow) and to the analog ground voltage (Vref).

6. Analog-to-digital converter according to claims 3, 4 or 5, characterized by the fact that said lowering voltage (Vlow) is selected among $2^{n/2}$ possible values depending on the value of the input voltage (Vin), in such a way to reduce the second conversion step to the same predetermined resistive segment (GR), regardless of the value of the input voltage (Vin).
AMENDED CLAIMS
[received by the International Bureau on 2 March 1992 (02.03.92);
original claims 1-3 cancelled; remaining claims renumbered
accordingly (2 pages)]

1. Analog-to-digital converter for the conversion of an
input analog signal (Vin) to a N bits digital code, including:

- a sample and hold circuit (S/H) receiving at its input
  the analog signal (Vin) to be coded;

- a ladder of resistances (SR) consisting of 2^N
  elementary resistances (Re) clustered in 2^N/2 segments (GR),
  each one made of 2^N/2 elementary resistances connected in
  series among them, whose extreme terminals are connected to
  two reference voltage sources (Vref1, Vref2) for the
  generation of intermediate comparison voltages;

- a set of 2^N/2 -1 comparators (COMP) connectable for the
  comparison among the input signal and said intermediate
  reference thresholds;

- a plurality of latches (LT) connected to the outputs
  of said comparators;

- a coder (COD) to associate a digital code to the
  output configuration of said comparators, according to
  preset rules;

- a storage buffer (LTU) to store the digital code
  produced;

characterized by the fact to include a switch block
(COMP) to the elementary resistances (Re) of a
predetermined segment (GR), and by the fact that the sample
and hold circuit (S/H) receives as reference a lowering
voltage (Vlow) and the analog ground voltage (Vref)
corresponding to the voltage of the middle point of the
resistive ladder (SR), said lowering voltage (Vlow) being
selected by a combinatorial logic circuit (LCA), connected
to the outputs of said latches (LT), by means of one of the
switches of another switch block (SW) able to connect the
taps of segments (GR) to the lower plate of the capacitor
(Ci) of the sample and hold circuit (S/H).

2. Analog-to-digital converter according to claim 1,
characterized by the fact that said predetermined resistive
segment (GR) is the one referred at the bottom to the analog ground (Vref).

3. Analog-to-digital converter according to claim 1 or 2, characterized by the fact that the sample and hold circuit (S/H) includes a storage capacitor having a plate which can be connected to the input voltage to convert (Vin), and the other plate which can be connected to said lowering voltage (Vlow) and to the analog ground voltage (Vref).

4. Analog-to-digital converter according to claims 1, 2 or 3, characterized by the fact that said lowering voltage (Vlow) is selected among $2^{k/2}$ possible values depending on the value of the input voltage (Vin), in such a way to reduce the second conversion step to the same predetermined resistive segment (GR), regardless of the value of the input voltage (Vin).
STATEMENT UNDER ARTICLE 19

In view of the cited references we have deleted claims 1 and 2 and previous claim 3 is based on the preamble of previous claim 1; all claims have been renumbered.

The description should be amended according to the amended claims; the drawings are unchanged.
**I. CLASSIFICATION OF SUBJECT MATTER**

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Int.Cl. 5 H03M1/14

**II. FIELDS SEARCHED**

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<tr>
<td>X</td>
<td>PATENT ABSTRACTS OF JAPAN vol. 10, no. 61 (E-387)(2118) 11 March 1986 &amp; JP,A,60 214 120 (NIPPON DENKI) 26 October 1985 see abstract</td>
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<td>IEEE JOURNAL OF SOLID-STATE CIRCUITS. vol. 24, no. 2, April 1989, NEW YORK US pages 241 - 249; J.DOERNBERG ET AL. 'A 10-bit 5-Msample/s CMOS Two-Step Flash ADC' see page 242, right column, line 10 - page 242, right column, line 24; figure 1</td>
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**IV. CERTIFICATION**

Date of the Actual Completion of the International Search

19 DECEMBER 1991

Date of Mailing of this International Search Report

02. 01. 00

International Searching Authority

EUROPEAN PATENT OFFICE

Signature of Authorized Officer

KHAZAM U.J.
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<td>IBM TECHNICAL DISCLOSURE BULLETIN. vol. 32, no. 3B, August 1989, NEW YORK US</td>
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<tr>
<td></td>
<td>pages 348 - 349; 'N Bit Sampling Half Flash Analog-to-digital Converter Using only 2**N/2 Comparators'</td>
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<td>pages 1492 - 1497; M.K. MAYES ET AL.: 'A Multistep A/D Converter Family with Efficient Architecture'</td>
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<td>see page 1495, left column, line 3 - page 1496, left column, line 36; figures 5,6</td>
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