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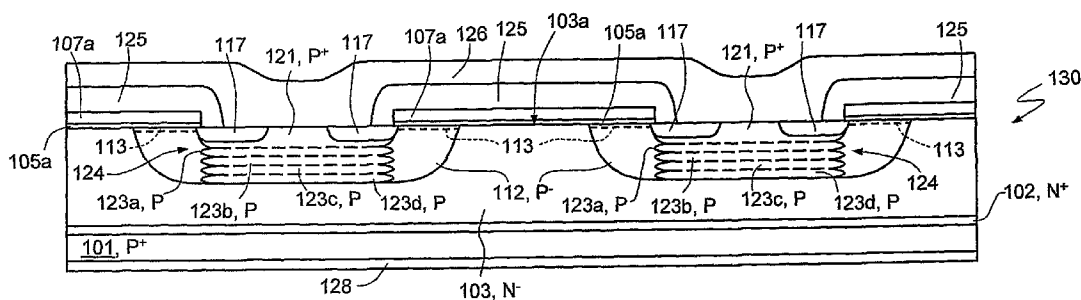
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(54) Title: IGBT TRANSISTOR WITH PROTECTION AGAINST PARASITIC COMPONENT ACTIVATION AND MANUFACTURING PROCESS THEREOF



(57) Abstract: An IGBT transistor includes a drift region (103), at least one body region (112) housed in the drift region (103) and having a first type of conductivity, and a conduction region (124), which crosses the body region (112) in a direction perpendicular to a surface (103a) of the drift region (103) and has the first type of conductivity and a lower resistance than the body region (112). The conduction region (124) includes a plurality of implant regions (121, 123a-123d), arranged at respective depths (D1-D4) from the surface (103a) of the drift region (103).

"IGBT TRANSISTOR WITH PROTECTION AGAINST PARASITIC COMPONENT
ACTIVATION AND MANUFACTURING PROCESS THEREOF"

TECHNICAL FIELD

5 The present invention relates to an IGBT transistor with protection against activation of parasitic components and to a manufacturing process thereof.

BACKGROUND ART

10 As is known, in IGBT transistors the maximum current in the conduction state is limited by the presence of an intrinsic parasitic thyristor. For greater clarity, reference may be made to Figure 1, which shows the structure of a conventional IGBT transistor, designated by the reference number 1. The
15 IGBT transistor 1 comprises a drift region 2 of an N⁻-type, made in which is a body region 3, of a P⁻-type. In turn the body region 3 houses two symmetrical source regions 5, of an N⁺-type. The body region 3 and the source regions 5 are aligned to a surface 2a of the drift region 2 and are
20 contacted by an emitter line 7. Gate regions 8 are arranged on the surface 2a, at sides of and partly overlying the body region 3, and are separated from the underlying structures by gate-oxide regions 9. More precisely, the gate regions 8 are each aligned to a respective one of the source regions 5, and
25 portions of the body region 3 immediately underlying the gate regions 8 define channel regions 10. The gate regions 8 are directly connected to one another and are provided with a gate terminal (not shown). The IGBT transistor 1 further comprises a collector region 12, of a P⁺-type, separated from the drift
30 region 2 by a transition region 13, of an N⁺-type. Finally, a collector contact 15 coats the collector region 13 throughout its extension.

From an electrical standpoint, the body region 3, the drift
35 region 2, and the collector region 13 define a PNP transistor 17, controlled by an NMOS transistor 18 formed by the source

regions 5, the body region 3 (in particular, the channel regions 10) and the drift region 2. In addition, a further parasitic NPN transistor 19 is present, formed by the source regions 5, the body region 3 (outside the channel regions 10) and, once again, the drift region 2. In practice, the PNP transistor 17, the MOS transistor 18 and the NPN transistor 19 form a thyristor 20. In use, the current of the IGBT transistor 1 is substantially determined by a conduction current I_D (of holes, in this case) of the PNP transistor 17 and by a control current I_C (of electrons), which flows through the NMOS transistor 18. The NPN transistor 19 must be normally off. The body region 3, however, has a low doping level and hence a relatively high internal resistance R_i . Consequently, the conduction current I_D may cause a voltage drop between the source regions 5 and the body region 3 (which form the emitter and the base, respectively, of the NPN transistor 19) such as to turn the NPN transistor 19 on. In this case, the thyristor 20 is activated, and the current flows directly towards the emitter line 7, independently of the MOS transistor 18, and hence can no longer be controlled by means of the gate terminal 11. In addition, activation of the transistor 20 limits the maximum current of the IGBT transistor 1, especially at high temperatures.

In order to overcome this problem, it has been proposed to reduce the resistance of the body region 3 by means of deep diffusion of a dopant species. In particular, the treatment concerns that portion of the body region 3 where mainly the conduction current I_D is present. The dopant species is introduced through the openings between the gate regions 8 and diffuses towards the drift region 2. However, the diffusion is substantially isotropic and hence can easily alter doping of the channel region 10, in effect increasing the threshold voltage of the MOS transistor 18. The phenomenon hence limits the depth that the diffusion can reach and, consequently, also the benefit that can be achieved.

According to an alternative solution, a shallow implantation self-aligned to the gate regions 20 is performed and is followed by a diffusion for a short time. In this way, doping of the channel regions 10 and the value of the threshold voltage of the MOS transistor 18 are preserved, but it is possible to obtain only a modest reduction in the resistance of the body region 3.

10 DISCLOSURE OF INVENTION

The aim of the present invention is to provide an IGBT transistor and a manufacturing process thereof which will be free from of the limitations described.

According to the present invention an IGBT transistor and a manufacturing process of an IGBT transistor are provided, as defined in Claims 1 and 11, respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention, an embodiment thereof will now be described, purely by way of non-limiting example, with reference to the attached drawings, wherein:

- Figure 1 is a cross-sectional view through a known IGBT transistor;

- Figures 2 and 3 are cross-sectional views through a semiconductor wafer, in successive steps of a process of fabrication according to the present invention;

- Figure 4 is a top plan view of the wafer of Figure 3, at a different scale;

- Figures 5-12 show the same view as that of Figures 2 and 3, in successive fabrication steps;

- Figure 13 is a top plan view of the wafer of Figure 12, at a different scale; and

- Figure 14 is a cross-sectional view through an IGBT transistor according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

With reference to Figure 2, number 100 designates a semiconductor wafer comprising a substrate 101, which in the embodiment described herein has a P⁺-type conductivity. By an epitaxial growth, a transition region 102, of an N⁺-type, and a drift region 103, of an N⁻-type, are made in succession starting from the substrate 101. For example, the drift region 103 has a doping level of approximately 10¹⁴ atoms/cm³. Then, a gate-oxide layer 105, having a thickness of some hundreds of nanometres, is formed on the free surface 103a of the drift region 103, by means of a thermal oxidation of short duration. Then, a conductive polysilicon layer 107 is deposited on the wafer 100.

As is shown in Figure 3, a resist layer is deposited and delineated so as to form a first mask 108 having first windows 109, in the form of strips that extend perpendicular to the plane of the drawing. The conductive layer 107 and the gate-oxide layer 105 are etched and removed through the first windows 109 of the first mask 108 so as to expose the drift region 103. After etching, residual portions of the conductive layer 107 define gate regions 107a, spaced apart by openings 110 and separated from the drift region 103 by gate-oxide regions 105a. In addition, the gate regions 107a are connected to one another through a continuous portion 107b, as shown in Figure 4 (here the first mask 108 is not illustrated).

Next (Figure 5), a P-type dopant species is introduced into the drift region 103 through the openings 110 and made to diffuse by means of a thermal process. Given that the dopant species diffuses in a substantially isotropic way, body regions 112 are formed, of a P⁻-type, which extend laterally on the outside of respective windows 110 and reach a pre-set depth. Portions of the body region immediately underlying the respective gate-oxide regions 105a define channel regions 113 (represented with a dashed line in Figure 5).

The first mask 108 is removed, and in its place a second mask 114 is provided, as shown in Figure 6. On each body region 112, the second mask 114 has two second windows 115, which
5 extend in a direction perpendicular to the plane of the drawing. The second windows 115 leave respective strips exposed and are aligned to respective gate regions 107a, which delimit the body region 112.

10 Then, an N⁺-type implantation is carried out using the second mask 114. In this step, through the second windows 115 of the second mask 115, source regions 117 of an N⁺-type are formed, having, for example, a level of doping of 10^{20} atoms/cm³. In each body region 112 two source regions 117 are made, aligned
15 to respective gate regions 110. The channel regions 113 are defined between the source regions 117 and the drift region 103, immediately underneath the gate-oxide regions 105a.

With reference to Figure 7, after removal of the second mask
20 114, a third mask 118 is defined, having third windows 120 that expose at the centre strips of respective body regions 112, but coat at least in part the source regions 117. Also the windows 120 extend in a direction perpendicular to the plane of the drawing. The third mask 118 is then configured so
25 as to leave a margin of distance L between the exposed part of the body region 112 and the gate regions 107a.

Using the third mask 118, a surface implantation of a P⁺-type is first carried out so as to create a surface implant region
30 121 of a P⁺-type, having approximately the same doping level as the source regions 117 (approximately 10^{20} atoms/cm³), but opposite conductivity. Furthermore, the energy of the implantation is such that the peak of the doping density of the surface implant region 121 is found slightly underneath
35 the source regions 117.

As shown in Figures 8-11, a plurality of P-type deep implantations (four in the embodiment described herein) is then carried out, once again using the third mask 118. Each implantation is performed at an higher energy than the previous one; hence the dopant species implanted penetrate to a greater depth in the body regions 112, thus forming a conduction region 124 that defines a continuous, high-conductivity path throughout the body region 112, in a direction perpendicular to the surface 103a of the drift region 103.

In detail (Figure 8), following upon the first deep implantation, a first buried implant region 123a is provided, underneath the surface implant region 121 and contiguous thereto (at a depth D1). The second and third deep implantations (Figures 9 and 10) give rise to a second deep implant region 123b and to a third deep implant region 123c, respectively, at increasing depths D2, D3 from the surface 103a of the drift region 103, as shown in Figures 9 and 10. Finally (Figure 11), the fourth implantation is carried out at the maximum energy as compared to the previous ones and forms a fourth deep implant region 123d at a depth D4, contiguous to the drift region 103.

The buried implant regions 123a-123d are arranged at increasing depths, are contiguous to one another and moreover have an intermediate doping level between the body region 112 and the surface implant region 121 (for example, approximately 10^{19} atoms/cm³). Consequently, the conduction region 124, comprising the buried implant regions 123a-123d and the surface implant region 121, defines a continuous conductive path through the body region 112 in a direction perpendicular to the surface 103a of the drift region 103. The conduction region 124 has a resistance smaller than the body region 112.

At the end of the sequence of implantations, the third mask

118 is removed, and an ultra-rapid thermal process is carried out, for example bringing the wafer 100 to a temperature of between 1000°C and 1150°C for 10-30 s. During the ultra-rapid thermal process, the dopant species introduced into the wafer 5 100 are electrically activated, but do not have enough time to diffuse and consequently remain where they are.

With reference to Figure 12, a dielectric layer 125, for example, a silicon-oxide layer, is then deposited and 10 selectively etched in order to define insulating regions, which incorporate the gate regions 107a and leave the body regions 112 and portions of the source regions 117 exposed. In addition, in a way known and not shown, the dielectric layer 125 is opened also on top of the gate regions 107a in areas 15 which are to form emitter electrical contacts.

Then, a metal layer is deposited and delineated by a photolithographic process in order to provide an emitter line 126, which extends within the openings 110 and electrically 20 connects the body regions 112 and the source regions 117 to one another. In addition, also a gate line 127 is defined, connected to the gate regions 107a (Figure 13).

Finally (Figure 14), the substrate 101 is thinned to a pre- 25 determined thickness and coated with a metal layer forming a collector electrode 128. The wafer 100 is divided up into dice, each of which comprises a respective IGBT transistor 130 having the structure illustrated in Figure 14.

30 The process described advantageously enables provision of an IGBT transistor in which latch-up of the intrinsic parasitic thyristor requires a particularly high current density. In fact, the highly conductive paths traversing entirely the body regions 112 enable drawing high currents without causing any 35 significant voltage drops between the body regions 112 themselves and the source regions 117 housed therein.

In addition, doping of the channel regions 113 is preserved. The deep implantations are, in fact, carried out maintaining a margin of distance from the respective gate regions 107, which
5 delimit the channel regions 113. The dopant species introduced into the body regions are subjected to inevitable phenomena of scattering associated to the implantation, and hence the surface implant region 121 and deep implant regions 123a-123b can be slightly misaligned with respect to the third mask 118.
10 However, the margin of distance is sufficient to prevent the dopant species from reaching the channel regions 113, thus maintaining the doping substantially unaltered. Consequently, also the threshold voltage can be controlled easily.

15 Finally, it is evident that modifications and variations can be made to the IGBT transistor and to the manufacturing process described herein, without departing from the scope of the present invention, as defined in the annexed claims.

20 In particular, the conductive path through the body regions 112 can be obtained by an arbitrary number of implantations. In addition, the deep implants could be obtained starting from the deepest, then decreasing the implantation energy, or even in any other arbitrary order.

CLAIMS

1. An IGBT transistor comprising:

- a drift region (103);

5 - at least one body region (112) housed in said drift region (103) and having a first type of conductivity; and

- a conduction region (124), crossing said body region (112) in a direction perpendicular to a surface (103a) of said drift region (103) and having said first type of conductivity and a
10 lower resistance than said body region (112);

characterized in that said conduction region (124) comprises a plurality of implant regions (121, 123a-123d), arranged at respective depths (D1-D4) from said surface (103a) of said drift region (103).

15

2. The transistor according to Claim 1, wherein said implant regions (121, 123a-123d) comprise a surface implant region (121) and a plurality of buried implant regions (123a-123d) contiguous to one another.

20

3. The transistor according to Claim 2, wherein one of said deep implant regions (123d) is contiguous to said drift region (103).

25

4. The transistor according to Claim 2 or Claim 3, wherein said conduction region (124) has a higher doping level than said body region (103).

30

5. The transistor according to Claim 4, wherein said deep implant regions (123a-123d) have an intermediate doping level between said body region (112) and said surface implant region (121).

35

6. The transistor according to any one of the preceding claims, wherein said drift region (103) has a second type of conductivity, opposite to said first type of conductivity.

7. The transistor according to Claim 6, comprising at least one source region (117) housed in said body region (11) and having said second type of conductivity.

5

8. The transistor according to Claim 7, comprising gate regions (107a) arranged on said drift region and defining an opening (110) above said conduction region (124).

10 9. The transistor according to Claim 8, wherein said conduction region (124) is arranged centrally with respect to said opening (110).

10. The transistor according to Claim 8 or Claim 9, wherein
15 said body region (103) extends around said opening (110) and is separated from said gate regions (107a) by gate-oxide regions (105a) and wherein portions of said body region (103) immediately underlying said gate-oxide regions (105a) define channel regions (113).

20

11. A process for manufacturing an IGBT transistor (100), comprising the steps of:

- providing, in a semiconductor wafer (100), a drift region (103);
 - 25 - forming, in said drift region (103), at least one body region (112) having a first type of conductivity; and
 - forming a conduction region (124), crossing said body region (112) in a direction perpendicular to a surface (103a) of said drift region (103) and having said first type of conductivity
30 and a resistance lower than that of said body region (112);
- characterized in that said step of forming said conduction region (124) comprises:
- carrying out a plurality of implantations of dopant species in said body region (112) at respective depths (D1-D4) from
35 said surface (103a) of said drift region (103).

12. The process according to Claim 11, wherein said step of carrying out a plurality of implantations comprises carrying out a surface implantation for forming a surface implant region (121) and a plurality of deep implantations for providing respective deep implant regions (123a-123d).

13. The process according to Claim 12, wherein said conduction region (124) has a higher doping level than said body region (103).

10

14. The process according to Claim 13, wherein said deep implant regions (123a-123d) have an intermediate doping level between said body region (112) and that of said surface implant region (121).

15

15. The process according to any one of Claims 10-13, wherein said drift region (103) has a second type of conductivity, opposite to said first type of conductivity.

16. The process according to Claim 11-15, comprising the step of subjecting said semiconductor wafer (100) to a thermal process for electrically activating the implanted dopant species, wherein said thermal process has a duration such as to prevent diffusion of the implanted dopant species.

25

17. The process according to Claim 16, wherein a duration of said thermal process is between 10 s and 30 s.

18. The process according to Claim 16 or Claim 17, wherein said thermal process comprises heating said wafer (100) up to a temperature of between 1000°C and 1150°C.

19. The process according to any one of Claims 11-18, comprising the steps of:

- forming a gate-oxide layer (105) on said drift region (103);
- depositing a conductive polysilicon layer (107) on said

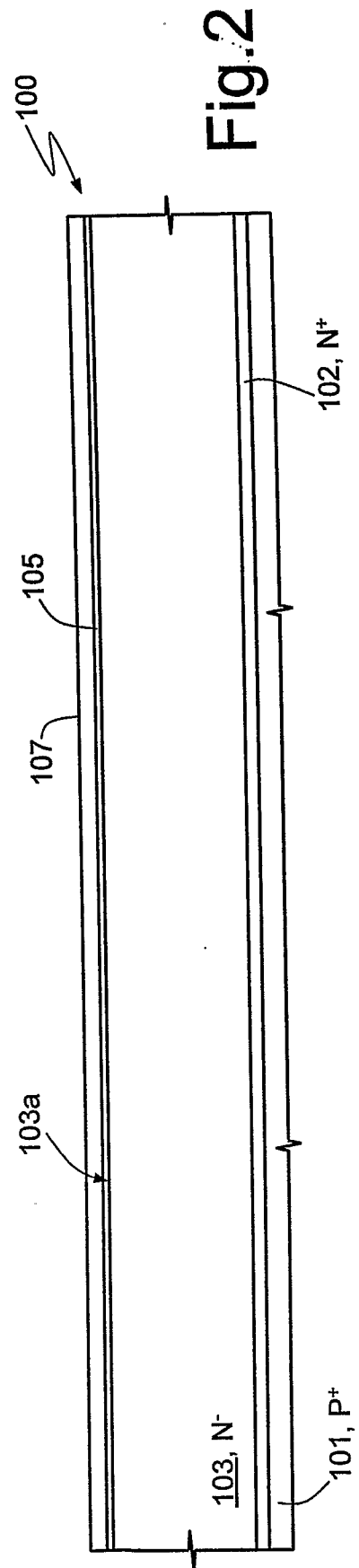
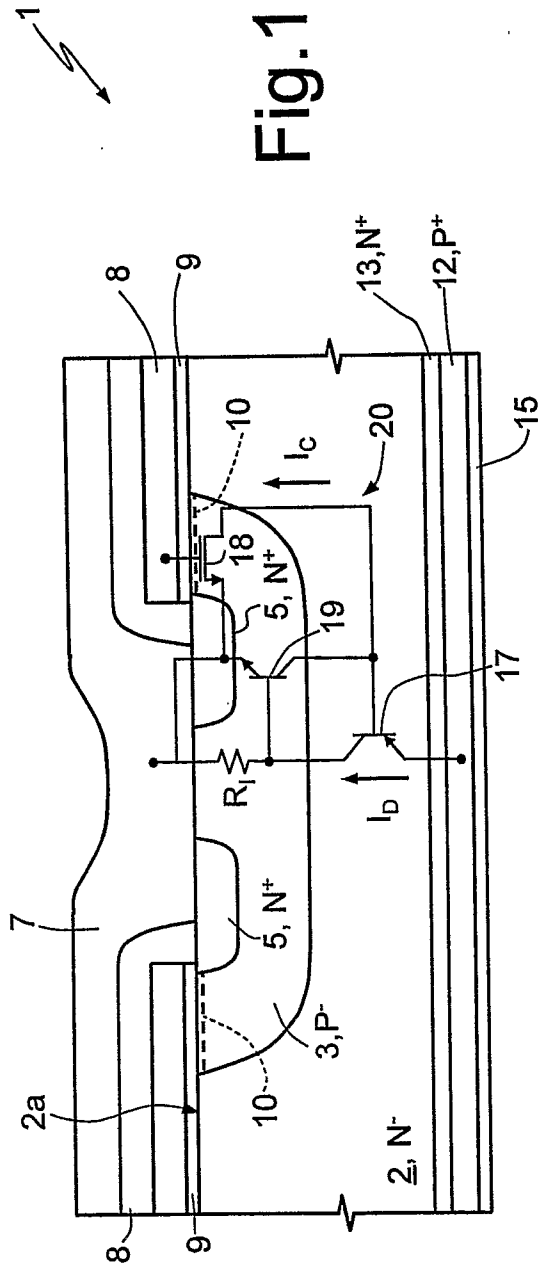
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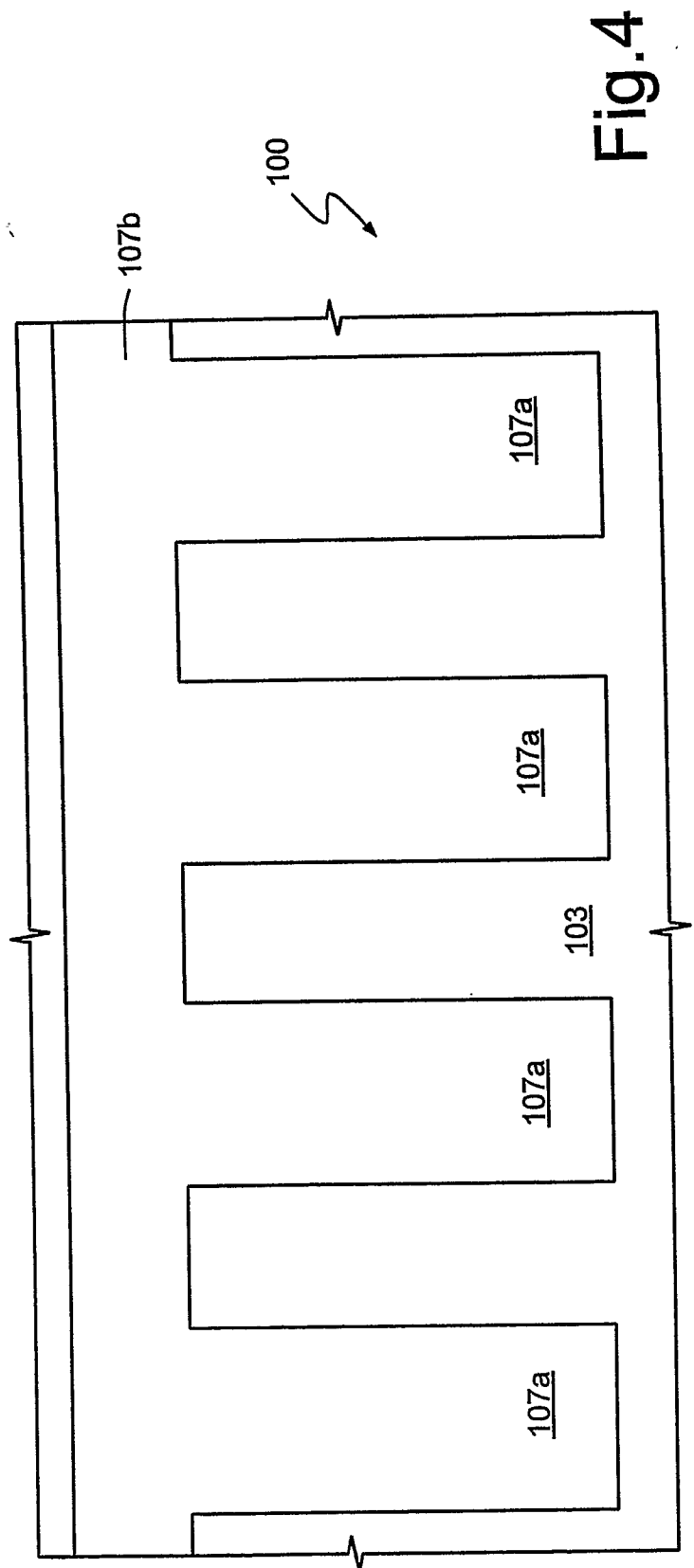
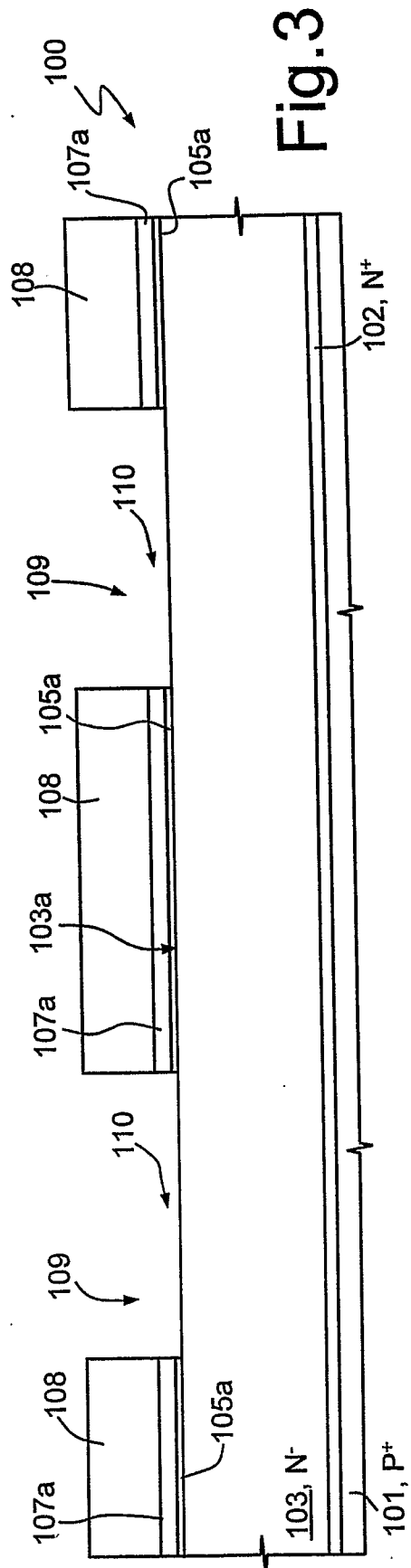
gate-oxide layer (105); and

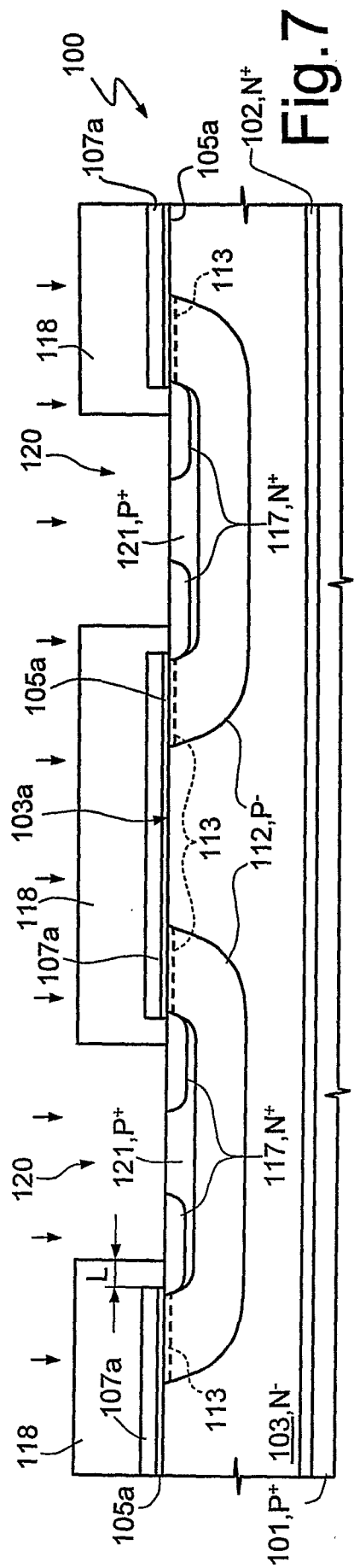
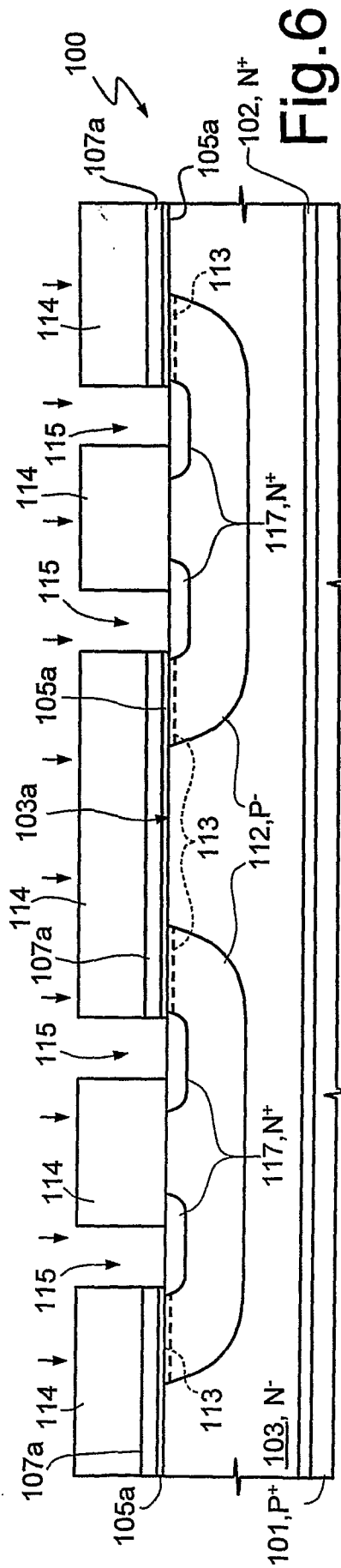
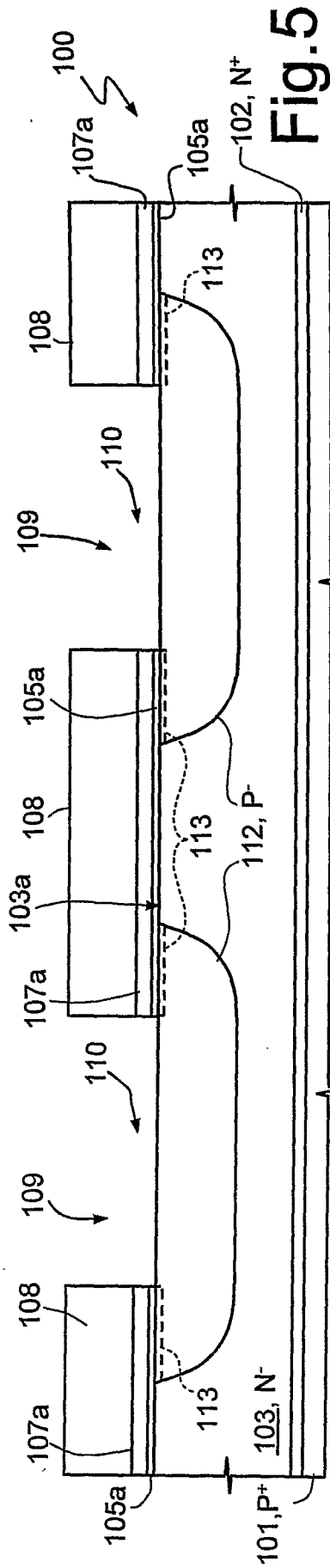
- shaping said conductive layer (107) and said gate-oxide layer (105) for forming gate regions (107a), separated from said drift region (103) by respective gate-oxide regions (105a) and defining openings (110) above said drift region (103).

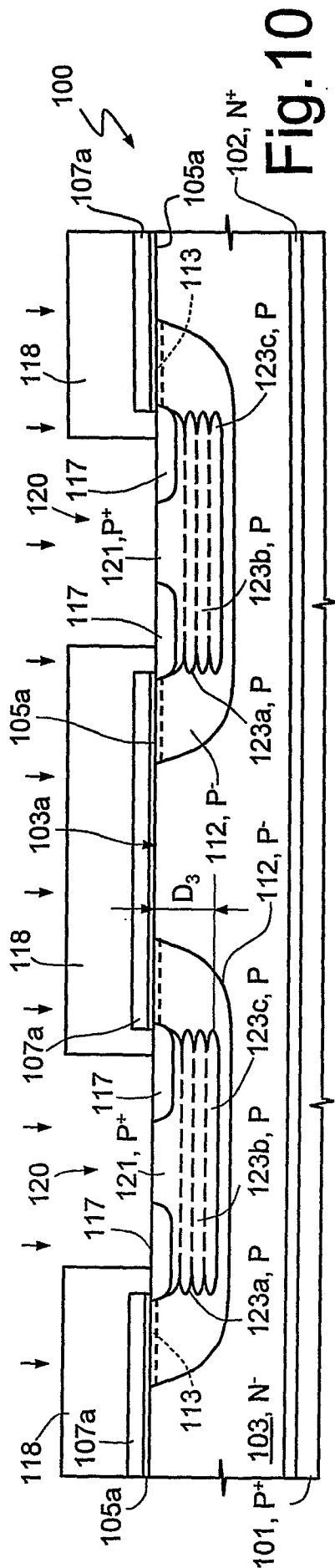
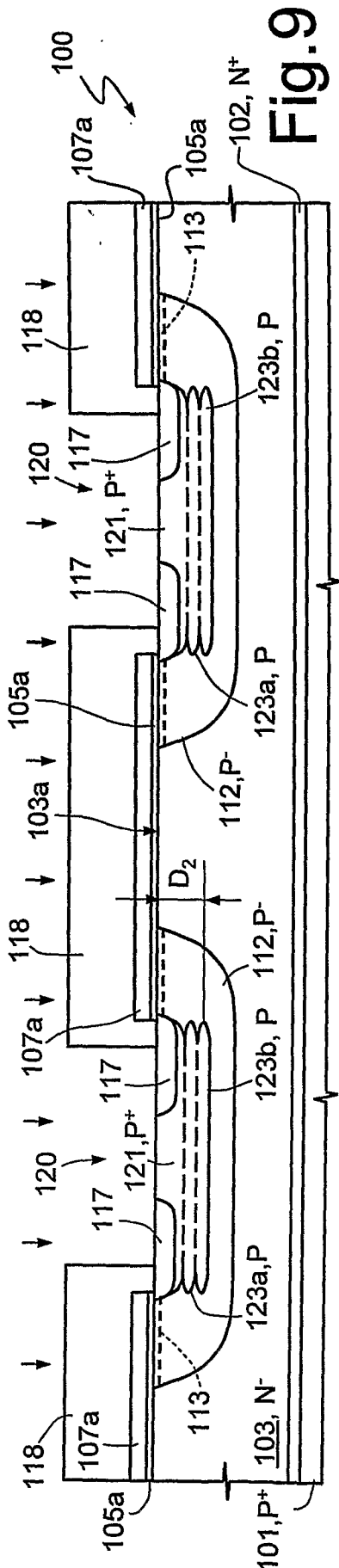
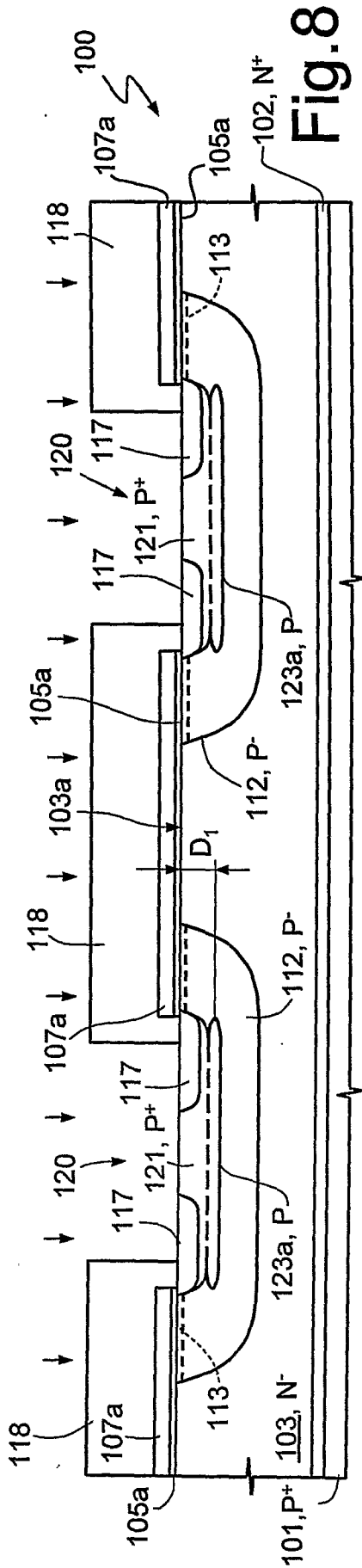
20. The process according to Claim 19, wherein said step of forming said body region (112) comprises:

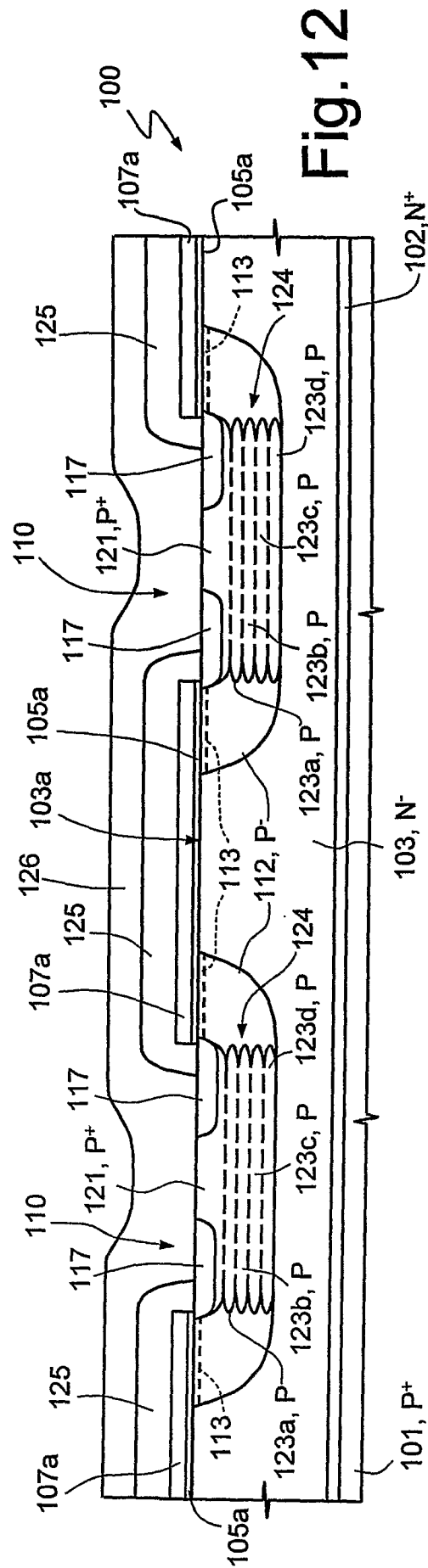
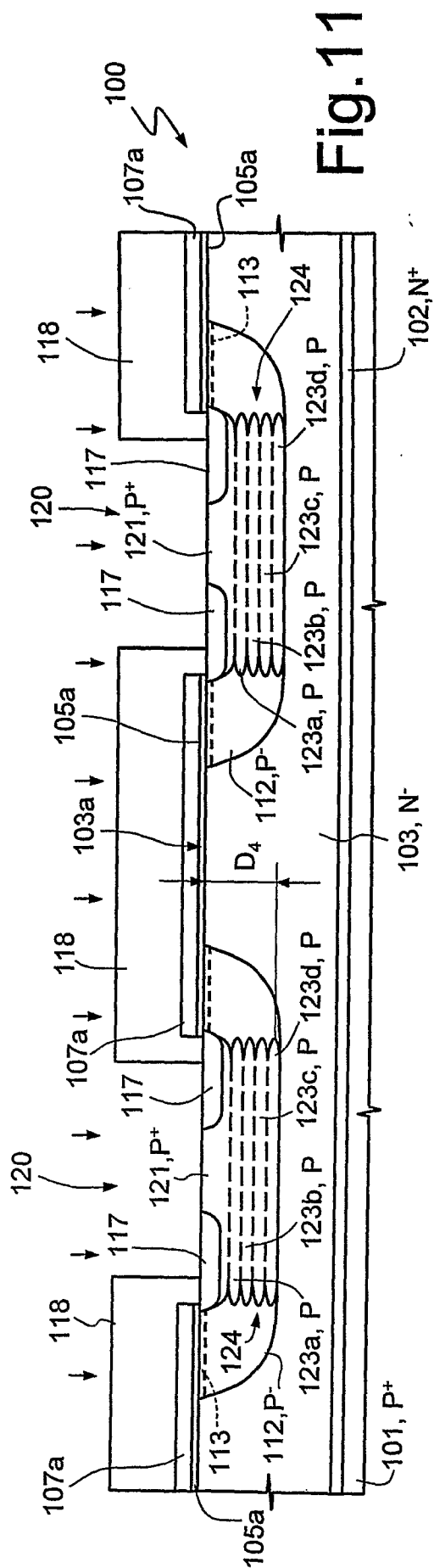
- introducing dopant species into said drift region (103) through said openings (110); and
- diffusing the dopant species introduced.











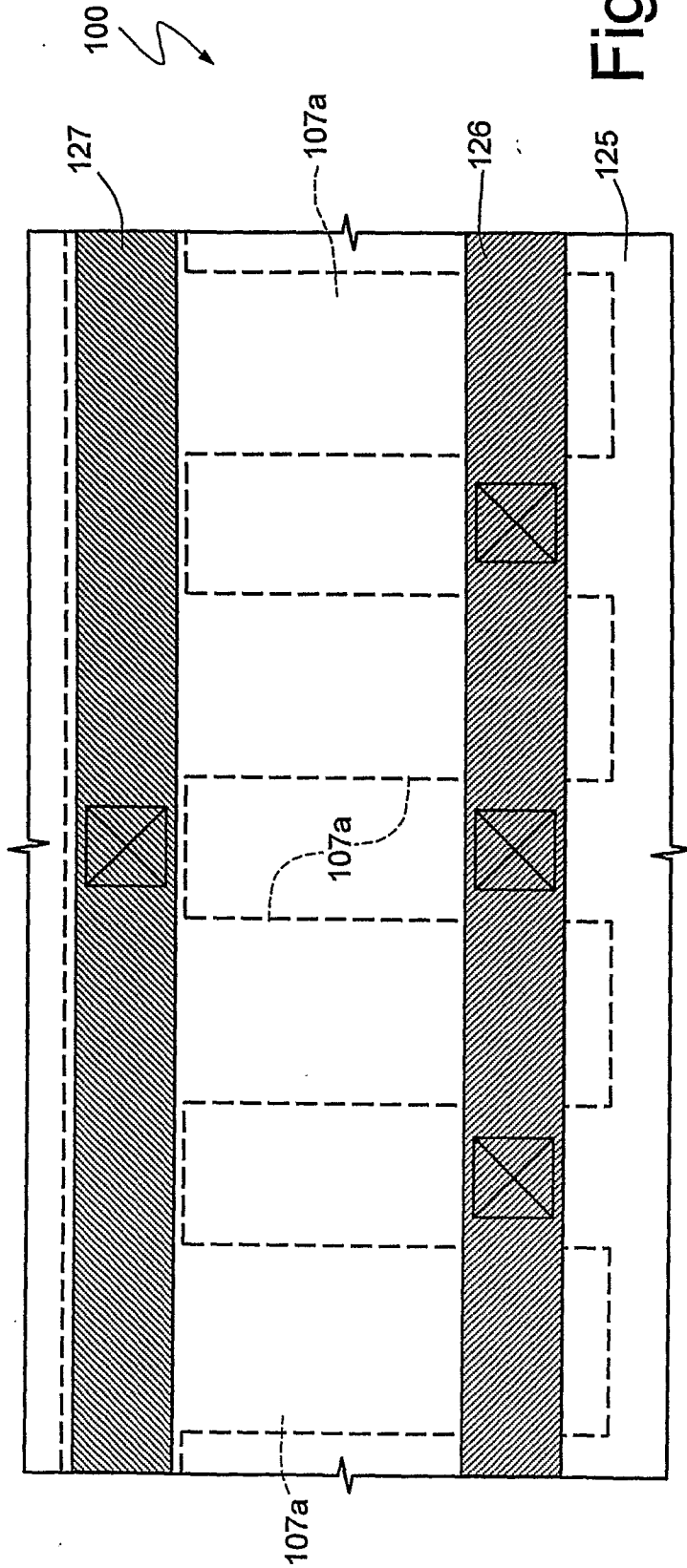


Fig. 13

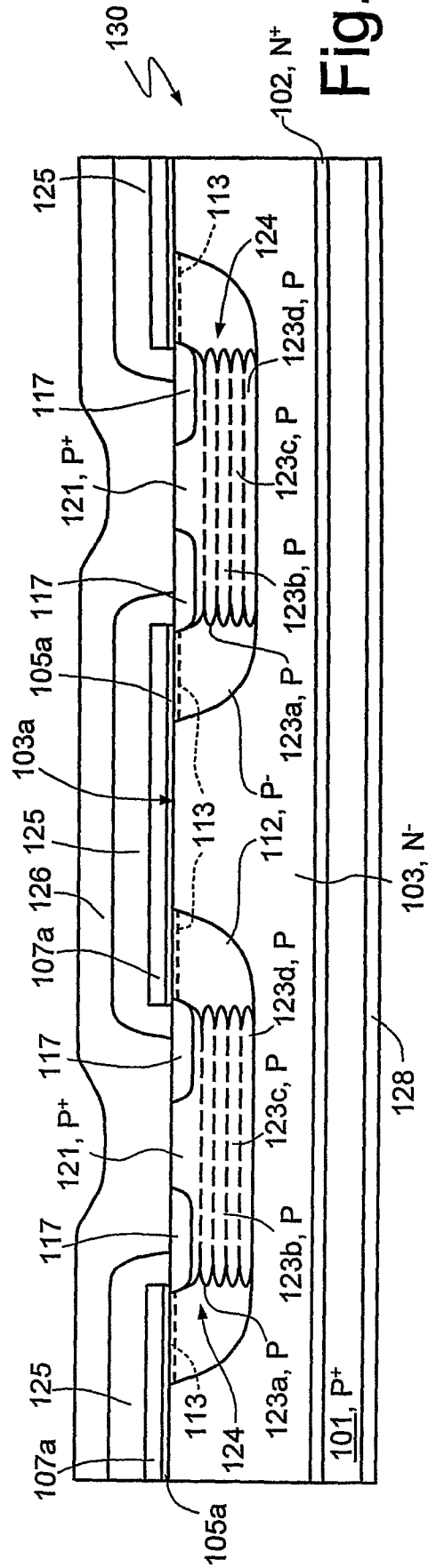


Fig. 14

INTERNATIONAL SEARCH REPORT

International application No

PCT/IT2006/000350

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L29/739 H01L21/331 H01L29/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 034 336 A (SEKI YASUKAZU [JP]) 23 July 1991 (1991-07-23) the whole document	1-20
X	US 4 809 047 A (TEMPLE VICTOR A K [US]) 28 February 1989 (1989-02-28) the whole document	1-20
X	EP 0 616 369 A1 (FUJI ELECTRIC CO LTD [JP]) 21 September 1994 (1994-09-21) the whole document	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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