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(54) Benævnelse: **Symmetrering af elektriske spændinger ved elektriske kondensatorer i en seriekobling**

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Description

Balancing electric voltages of electric capacitors connected in series

The present invention relates to a circuit arrangement for balancing electric voltages of electric capacitors in a series circuit according to the precharacterising clause of claim 1. Furthermore, the invention relates to a method for balancing electric voltages of electric capacitors in a series circuit according to the precharacterising clause of claim 7.

Generic circuit arrangements and methods are in principle known, so that no separate printed evidence relating hereto is required. It is known in a series circuit of capacitors to achieve a balancing with electric resistors which are connected in parallel with each capacitor. Within the meaning of this application balancing of the electric voltage of the capacitors means that the electric capacitors connected in series are essentially applied with the same electric voltage. Without measures for balancing the electric voltage of the electric capacitors connected in series, an unbalanced application of voltage results as a function of electric leakage currents of the electric capacitors and/or suchlike. The resistors connected in parallel can be used to largely avoid or suppress the effects causing the voltage deviations.

With the afore-cited passive manner of balancing by means of electric resistors, this is achieved in that a transverse current which amounts to a multiple of the respective leakage current of the electric capacitors flows through the electric resistors. The extent of the transverse current is preferably selected so that the effects causing an imbalance fade into the background in terms of relevance. As a result, a balancing of the electric voltages of the capacitors connected in series is forced. At the same time, a sustained power loss is produced during the intended operation, however, which, on the one hand, reduces a degree of efficiency of the series circuit and on the other hand produces heat which has to be discharged from the circuit arrangement. The disadvantageous effects are relevant and bothersome particularly with series circuits of capacitors in intermediate circuits of electric energy converters such as inverters, frequency converters, pulsed direct voltage converters and/or suchlike, which operate with high outputs in the range of a few kilowatts.

Particularly with facilities which operate with high outputs, high voltages are accordingly also required in intermediate circuits, in which a series circuit comprising capacitors, for instance electrolytic capacitors, is often unavoidable for design reasons. This is because inter alia for cost and procurement reasons capacitors from a series production are to be used. In most instances such capacitors are however not directly suited to use for the intended operation, particularly because their rated voltage is significantly below the rated voltage of the intermediate circuit. A series circuit of such capacitors is therefore the usual measure of structuring a corresponding intermediate circuit. The afore-cited problems occur here. With this power range, no insignificant losses occur with the use of a passive balancing.

WO 2012/042401 A2 discloses a method, a circuit and a topology for the use of this circuit in a Li-ion battery or another battery, the individual cells of which profit from an energy balance. The entire battery system is characterised by a high degree of efficiency compared with implementations in known battery systems, wherein the heat load can in particular be reduced. Here the circuit activities are continuous and bidirectional in respect of each cell.

It is accordingly the object of the invention to achieve an improved balancing of the electric voltages in capacitors connected in series.

As a solution, according to a first aspect of the invention a circuit arrangement according to the independent claim 1 is proposed. According to a second aspect of the invention, a method according to the further independent claim 7 is proposed. Advantageous embodiments are defined in the dependent claims.

With the invention, it is in particular proposed in terms of circuit arrangement that the circuit arrangement has in each case a half bridge module connected to each of the electric capacitors, which provides a central terminal, and a clock generator for operating all half bridge modules in cyclic operation, wherein a respective first terminal of an electric coil assigned individually to the respective half bridge module is connected to the central terminal of each half bridge module, and a second terminal of this electric coil is connected accordingly to one of two terminals of the capacitor connected in parallel to the corresponding half bridge module, wherein the clock generator is designed to operate the half bridge modules in synchrony in cyclic operation, wherein the electric coils are coupled magnetically such that the magnetic fluxes generated by the electric coils add together.

With these measures, it is possible for a balancing of the electric voltages of the electric capacitors connected in series to be achieved, without a significant power loss being required as with the prior art. By means of the inventive circuit arrangement, it is namely possible to exchange charges between the individual capacitors, in order to be able to achieve a voltage balancing of the electric capacitors connected in series. This has proven advantageous in that with the aid of a transformer formed by the electric coils provision is made for a uniform voltage division of the capacitors. As soon as an imbalance with respect to the electric voltages is present on the electric capacitors connected in series, there is a transformation from the electric capacitor with the highest voltage to the electric capacitor with the lower voltage. The winding ratio of windings of the electric coil is preferably one. It has proven here to be particularly advantageous that according to the invention the energy conversion principle is carried out according to the push-pull principle. This allows the transformer formed by the electric coils to be embodied very compactly, since it is not applied with magnetic flux density in a unipolar manner, but instead in a bipolar manner. For the purpose of magnetic coupling the electric coils are preferably arranged on a shared ferromagnetic core, for instance a laminated iron core, preferably however a ferrite core and/or suchlike. The invention therefore involves active balancing.

A half bridge module within the meaning of the application is preferably a physical unit which has two semiconductor switches connected in series. Here, the semiconductor switches connected in series are each connected in parallel to the corresponding, electric capacitor. The half bridge module can naturally also be formed from discrete electronic components. In principle the half bridge module therefore refers to a circuit topology.

A semiconductor switch within the meaning of this disclosure is a preferably electronically controllable switching element, for instance a transistor, a thyristor, combination circuits hereof, in particular with parallel-connected free-wheel diodes, for instance a metal oxide semiconductor field effect transistor (MOSFET), an isolated gate bipolar transistor (IGBT), preferably with integrated free-wheel diodes, or suchlike.

The central terminal of a half bridge module is a terminal which is connected in an electrically conducting manner to the connection point of the semiconductor switches connected in series.

The switching operation of a semiconductor switch means that in a switched-on state, a very low electric resistance is provided between the terminals of the semiconductor switch which form a switching path, so that a high current flow is possible with very small residual voltage. In the switched-off state, the switching path of the semiconductor switch is highly resistive, in other words it provides a high electric resistance, so that even with a high electric voltage present at the switching path, essentially no or only a very low, in particular negligible current flow is present. The linear operation, which is not used in cyclic operation, however, differs herefrom. The respective switching state can be assumed by means of a corresponding electric potential on a control electrode of the semiconductor switch.

Synchronous cyclic operation of the half bridge modules thus means that all semiconductor switches connected to a positive terminal, compared with the other terminal of the half bridge module, are clocked essentially at the same time, in other words, are switched on or off. The same applies in principle also to the opposing semiconductor switches of the respective half bridge modules. The semiconductor switches of a half bridge module are switched on alternately, so that a transverse current through the two semiconductor switches is largely avoided. In this way simple control can be achieved, because the clock generator only needs to produce two clock signals, namely a clock signal for the upper semiconductor switch and a clock signal for the lower semiconductor switch of the respective half bridge modules. As a result, all half bridge modules can be operated with these signals. The clock generator preferably provides that the clock signals for the semiconductor switches have a dead time, so that on account of physical properties, possible shared switch-on times can be avoided. One such time difference between a trailing edge of one of the control signals and the subsequent rising edge of the other of the two control signals is called the dead time. However, the dead time is generally essentially smaller than the respective switch-on or switch-off times of the semiconductor switches.

The clock generator can be formed by an electronic circuit, for instance a computer unit, which is controlled by means of a programme, but also a hardware circuit, combinations hereof or the like. The semiconductor switches of the half bridge modules have control electrodes connected to control terminals, by way of which the corresponding clock signals can be supplied. A galvanic isolation unit is preferably provided, in order to be able to control the half bridge modules connected at a different electrical potential with a shared clock signal of the clock generator. One such galvanic isolation can be achieved using optocouplers, transmitters and/or suchlike, for instance.

A series capacitor is connected in each case between the second terminals of the electric coils and the terminals of the corresponding electric capacitors. As a result, resonances can be formed, which improve the energy-related coupling. The respective series capacitor can therefore be operated as a resonance capacitor during operation of the circuit arrangement.

An advantageous development provides that the circuit arrangement has an auxiliary coil, which is coupled magnetically to the electric coils. As a result, it is possible to generate an auxiliary voltage which can be used to supply energy to the circuit arrangement. Furthermore, the auxiliary coil can also provide energy for the electronic supply of the entire device or provide the operation of cooling facilities, in particular ventilators. This embodiment has then proven particularly advantageous if, with facilities with large voltages above 1,000 volts, cooling facilities are to be operated which are only designed for low voltage in the interest of standardisation. In this case it is therefore not necessary to provide a separate energy supply for the electronic supply or these cooling facilities. Overall, this embodiment allows for the provision of a separate energy supply for units to be supplied, irrespective of the presence of small voltages or low voltages in the interest of standardisation. A separate energy transformation need not be provided, therefore. The auxiliary coil can be connected to a rectifier, which provides a direct voltage. For this purpose, a push-pull rectification, but also a bridge rectification, can be provided. The direct voltage can moreover be smoothed by means of a capacitor.

It has proven to be particularly advantageous if the auxiliary coil has a central tapping. This allows a push-pull rectification to be provided and thus utilisation of the magnetic field, such as with a bridge rectification, to be achieved, wherein however reduced losses can be achieved in the rectifier compared with the bridge rectification. In addition, a smoothing of the rectified electric voltage can also be provided here by means of a capacitor.

Furthermore, it is proposed that the circuit arrangement has a control transformer for the control-side coupling of the half bridge module to the clock generator. For this purpose, for each semiconductor switch of the half bridge modules the control transformer can have a separate winding for connection to a control terminal of the respective semiconductor switch. At the same time it can be provided that there is provision for only one single control transformer for all half bridge modules, particularly preferably for all semiconductor switches of all half bridge modules. This allows all semiconductor switches of all half bridge modules to be controlled particularly easily. There can be provision here for suitable dead times to be generated by system properties, which allow both semiconductor switches of each half bridge module to be able to be actuated by way of a shared control transformer.

In order to be able to better monitor the function of the circuit arrangement, it is proposed that the circuit arrangement has current measuring units for each of the half bridge modules, which each have a measuring circuit connected to the series capacitors. Accordingly, a separate current measuring unit is preferably available for each half bridge module. The current measuring unit allows the current stress of the half bridge module to be recorded and a corresponding measured value to be supplied to the clock generator. This allows protective functions to be realised, particularly if for instance one or more of the capacitors indicate failure during the intended operation. A failure can occur for instance in that the respective electric capacitor is no longer able to conduct its rated voltage. A failure can also be caused by an electric capacitor being overloaded with respect to other technical parameters, for instance with respect to the temperature, with respect to a pulsed load and/or suchlike.

The clock frequency of the control signals of the clock generator is preferably selected so that pulse stresses in the series circuit comprising electric capacitors can also be sufficiently reliably detected and a corresponding balancing measure by means of the clock generator can be promptly introduced so that an unbalanced voltage division among the capacitors of the series circuit can largely be avoided. Particularly preferably it should be possible to prevent at least one, even only brief, exceeding of the rated voltage of the electric capacitors. The pulse duty factor of the switch-on times of the two semiconductor switches of a respective half bridge module is preferably 1. A reliable balancing can be achieved as a result.

It is proposed, particularly advantageously, that the measuring circuit has a rectifier unit. As a result, the value provided by the measuring circuit can be easily processed by the clock generator. In particular, this embodiment allows the value provided by the measuring circuit to be digitised and fed to a digital signal processing by means of the clock generator.

Another option provides that a respective second half bridge module is connected in parallel with each of the half bridge modules and that the second terminals of the electric coils are connected to in each case corresponding central terminals of the second half bridge modules. The second terminals of the electric coil are therefore connected to the respective central terminals of the second half bridge modules instead of the terminal of the respective electric capacitor. As a result, operation can be achieved in terms of a full bridge, as a result of which the degree of efficiency of the circuit arrangement can be further improved. Furthermore, advantages also result with respect to the balancing dynamics and the design of the magnetic coupling of the electric coils.

In terms of method, it is proposed in particular that with a method for balancing electric voltages of electric capacitors in a series circuit, a half bridge module connected in each case to each of the electric capacitors and providing a central terminal is operated in synchrony with all further half bridge modules in cyclic operation by means of a clock generator, wherein magnetic fluxes are generated by means in each case of electric coils coupled magnetically to one another and assigned individually to the electric capacitors, wherein the electric coils with in each case a first terminal are connected to central terminals of the corresponding half bridge modules and with, in each case, a second terminal are connected to the electric capacitors connected in parallel in each case such that the magnetic fluxes generated by the electric coils add together.

As a result, the advantages already discussed in connection with the circuit arrangement according to the invention are achieved.

According to one development, it is proposed that an auxiliary voltage is generated by means of an auxiliary coil. By means of the auxiliary voltage, a voltage supply for the clock generator and/or the half bridge modules and/or the entire device can be provided. The auxiliary voltage can be regulated, for instance, by the auxiliary voltage being measured, being compared with a comparison value and a difference being used to set a clock frequency of the clock generator. As a result, aside from the synchronisation function, it is also possible at the same time to realise a voltage supply function with a regulated voltage supply.

Furthermore, it is proposed that a value of the auxiliary voltage is set by means of a clock frequency of the clock generator. The clock frequency can correspond to the frequency of the clock signals for the semiconductor switches of the half-bridge modules. The clock frequency is preferably selected to be only so large as is required for the desired auxiliary voltage. It can however also be set by taking additional boundary conditions into account such as, for instance, dynamic conditions.

Further advantages and features can be taken from the following description of exemplary embodiments on the basis of the following figures. The same reference characters refer to the same components and functions in the figures

in which:

FIG 1	shows a schematic basic circuit diagram for a circuit arrangement for balancing electric voltages in capacitors connected in series according to the prior art,
FIG 2	shows a schematic basic circuit diagram of a first embodiment of a circuit arrangement for balancing electric voltages in capacitors connected in series according to the invention,
FIG 3	shows a schematic basic circuit diagram of a circuit arrangement based on the exemplary embodiment according to FIG 2, wherein an auxiliary voltage is additionally generated,
FIG 4	shows a schematic representation of a basic circuit diagram of an equivalent circuit diagram for the transformer according to FIG 3,

FIG 5 shows a schematic basic circuit diagram of a further embodiment of a circuit arrangement according to the invention, wherein three capacitors connected in series are balanced with respect to their electric voltage,

FIG 6 shows a schematic view of a basic circuit diagram for a circuit arrangement according to the invention based on the exemplary embodiment according to FIG 3,

FIG 7 shows a schematic basic circuit diagram of a further embodiment of a circuit arrangement according to the invention based on the exemplary embodiment according to FIG 3, but with a single control-side transmitter for all semiconductor switches of all half bridge modules in a schematic basic circuit diagram view,

FIG 8 shows a schematic basic circuit diagram of a further embodiment of the invention based on the exemplary embodiment according to FIG 3, but additionally with a current measuring unit for each of the half bridge modules

and

FIG 9 shows a schematic basic circuit diagram of another embodiment for balancing electric voltages in capacitors connected in series, wherein a full bridge circuit is provided for each primary-side winding.

FIG 1 shows a schematic basic circuit diagram for a circuit arrangement 10 according to the prior art with two capacitors connected in series 12, 14, to which an electric voltage 20 is applied. The capacitors 12, 14 are an integral part of an intermediate circuit (not specified further) of an electronic energy converter (not shown further). The capacitors 12, 14 are preferably embodied as electrolytic capacitors.

To ensure that voltage is applied to the electric capacitors 12, 14 essentially symmetrically, in other words with essentially the same electric voltage, an electric resistor 16, 18 is additionally connected in parallel with each of the capacitors 12, 14, The resistance values of the electric resistors 16, 18 are selected so that they amount to a multiple of residual currents of the electrolytic capacitors 12, 14. This ensures that the electric voltage 20 is essentially halved between the two electrolytic capacitors 12, 14.

This circuit is frequently found in frequency converters with a voltage intermediate circuit, in which, on account of the level of the electric voltage, a number of capacitors are connected in series. Typically, the maximum electric strength of the electrolytic capacitors used is not sufficient for the intermediate circuit voltage which is applied to the series circuit. For reliable operation, it is therefore necessary to ensure a symmetrical voltage division in the series circuit of the electrolytic capacitors 12, 14, since on account of different leakage currents of the electrolytic capacitors 12, 14, unpermitted voltage stresses on at least one of the electrolytic capacitors 12, 14 may result.

The resistance circuit which can be seen in FIG 1 avoids this, wherein significant power loss prevails however, if on the one hand with the same leakage currents of the electrolytic capacitors 12, 14 a balancing would not be necessary and on the other hand with maximally different leakage currents the symmetry by even larger currents through the electric resistors 16, 18 must be taken into account.

FIG 2 shows a circuit arrangement 30 according to the invention in a schematic basic circuit diagram, which avoids the disadvantages of the circuit according to FIG 1. For this purpose, the circuit arrangement 30 according to FIG 2 uses a transformer 34 which has two galvanically isolated electric coils 36, 38. The two electric coils 36, 38 are attached to a shared ferrite core, not referred to in more detail, and have the same number of windings and the same winding direction.

As apparent from the circuit according to FIG 2, with the circuit arrangement 30 the electric voltage should be applied to the electrolytic capacitors 12, 14 in symmetry, as already shown in FIG 1. The series circuit comprising these electrolytic capacitors 12, 14 is in turn applied with the electric intermediate circuit voltage 20.

For this purpose, a half bridge module 44 with in each case two semiconductor switches 46, 48 connected in series is connected in parallel with each of the two electrolytic capacitors 12, 14. Here, the semiconductor switches 46, 48 are formed by MOSFETs. These are connected in series. In principle the half bridge module 44 does not need to be realised as a physical unit but can instead also be formed by components which interconnected discretely with one another, here semiconductor switches 46, 48 connected in series.

Each of the half bridge modules 44 has a central terminal 110. This is the terminal at which the two semiconductor switches 46, 48 are connected electrically to one another. The individually assigned electric coils 36, 38 are connected to a first terminal at the central terminal 110 in each case. A second terminal of the electric coils 36, 38 is connected in series with a corresponding series capacitor 40, 42, which series capacitor is in turn connected to a terminal of the electrolytic capacitors 12, 14. Here, the terminal is connected to the lower electric potential, but it can likewise be connected to the higher potential. The electric coils 36, 38 have windings with the same number of windings and the same winding direction.

The circuit arrangement 30 further comprises a clock generator 32, which generates clock signals 50, 52 (A, B) as control signals which actuate the semiconductor switches 46, 48 of the half bridge modules 44. Provision is made here for the semiconductor switch 46 of the half bridge modules 44 to be controlled by the clock signal 50 and the other semiconductor switch 48 of the half bridge modules 44 to be controlled by means of the corresponding clock signal 52. The clock signals 50, 52 are embodied here to be complementary and have a pulse duty factor of approx. 50 percent.

The circuit arrangement 30 can be used to achieve a uniform voltage distribution among the electrolytic capacitors 12, 14. As soon as an imbalance is present in this regard, the electrolytic capacitor with the higher voltage is transformed into the electrolytic capacitor with the lower voltage. The ratio of the number of windings of the electric coils 36, 38 is 1. Here the invention accordingly uses the conversion principle in the form of the push-pull principle.

FIG 3 shows a further circuit arrangement 60 according to the invention, which is essentially based on the circuit arrangement 30 according to FIG 2. Reference is therefore only made below to the differences compared with the exemplary embodiment relating to FIG 2. With respect to the further aspects, reference is made to the preceding embodiments relating to the exemplary embodiment according to FIG 2.

In the present embodiment according to FIG 3, provision is made for the transformer 34 to have a third electric coil 22, the winding of which provides a central tapping 24. The winding ends of the electric coil 22 are conducted via diodes 26, 28 to a first terminal of an electric capacitor 54, which is connected with its further terminal to the central terminal 24. An auxiliary voltage 56 which is fed to the clock generator 32 is therefore provided on the electric capacitor 54. This voltage is used here to supply electric energy to the clock generator 32, so that a separate power supply for the clock generator 32 can be spared.

In this embodiment, the capacitors 40, 42, in conjunction with scatter inductances between the electric coils 36, 38 with respect to the electric coil 22, represent resonance circuits. The capacitor 54 is used to smooth the rectified voltage. The level of the electric voltage 56 can be set by the clock frequency of the clock generator 32. The clock signals 50, 52 (A, B) of the clock generator 32 are two rectangular signals displaced by 180 degrees with a pulse duty factor of approx. 50 percent.

The underlying functional principle of the circuit arrangement 60 according to FIG 3 is produced with the aid of the schematic representation of an equivalent circuit diagram according to FIG 4. The clock generator 32 controls the two half bridge modules 44 with a rectangular signal according to the push-pull principle. All semiconductor switches 46 connect at the same time alternately to all semiconductor switches 48. On account of the pulse duty factor of 50 percent, the half voltage with respect to the corresponding electrolytic capacitors 12, 14 establishes on the capacitors 40, 42 in each case. If the voltages at the electrolytic capacitors 12, 14 are balanced out, the transformer 34 transforms the alternating voltages from the half bridge modules 44 via the electric coils 36, 38 to the electric coil 22. The same level of current is taken from the two electrolytic capacitors 12, 14 in each case.

If the electrolytic capacitor 12 conducts a higher voltage than the electrolytic capacitor 14, the half bridge module 44 assigned to the electrolytic capacitor 12 forwards the higher voltage to the electric coil 38 by way of the electric coil 36 of the transformer 34, as a result of which a balancing of the voltages of the electrolytic capacitors 12, 14 is introduced by way of the half bridge module 44 which is assigned to the electrolytic capacitor 14. There is therefore a coupling of the voltages to the electrolytic capacitors 12, 14. The coupling is determined decisively by the scatter inductance between the electric coils 36, 38 of the transformer 34, the capacitors 40, 42 and the clock frequency of the clock generator 32.

In principle the circuit arrangement 60, like the circuit arrangement 30, can also be embodied without a regulated output voltage, as a result of which the circuit outlay can be reduced. A selection of the resonance inductance and resonance capacitance does not need to be restricted as a result. This would then serve as a limitation of the current rate of rise or for an artificial central point of the capacitor bridge. As a result, the frequency of the converter, in particular of the clock generator 32, only needs to be increased in the event of overcurrent. One such case can take place for instance with the start-up to a discharged capacitor 54, with a short-circuit, with large imbalance between the electric voltages of the electrolytic capacitors 12, 14 or suchlike.

FIG 5 shows a further embodiment of a circuit arrangement 70 according to the invention, which is based on the circuit arrangement 60 according to FIG 3. Reference is therefore made in addition to the embodiments relating to this exemplary embodiment.

In addition to the exemplary embodiment according to FIG 3, with this embodiment three electrolytic capacitors 12, 14, 62 are connected in series and applied with the electric intermediate circuit voltage 20. A clock generator 32 which controls the half bridge modules 44 assigned to the respective electrolytic capacitors 12, 14, 62 is also provided here, as explained already in respect of FIG 3.

Contrary to FIG 3, provision is further made for chokes 74 to be connected in the connection of the electric coils 36, 38, 78 to the respective central terminals 110 of the half bridge modules 44. These are essentially not coupled magnetically to one another and also not to the transformer 76. That which was already cited with respect to the preceding exemplary embodiments applies to the electric coils 36, 38, 78. Furthermore, the second terminals of the electric coils 36, 38, 78 are connected in addition by means of capacitors 80, 82, 84 to the respectively positive electric potential of the assigned electrolytic capacitors 12, 14, 62. As apparent from FIG 5, it is also possible to achieve a multiple symmetry in this way. The resonance inductance can also use a series inductance instead of the scatter inductance of primary to secondary winding, which is currently realised by the chokes 74. However, the coupling of the electrolytic capacitors 12, 14, 62 to one another is hereby reduced. The total of the two capacitances 40, 80 and 42, 82 and also 72, 84 forms the respective resonance capacitance.

As in FIG 3, the generation of an auxiliary voltage 56 is also provided here again by means of an electric coil 22. Contrary to the embodiment according to FIG 3, the diodes are however replaced by MOSFETS 86, 88 which are actuated accordingly. As a result, the power loss can be reduced compared with the arrangement with diodes.

FIG 6 shows a further embodiment of a circuit arrangement according to the invention, which is based on the embodiment according to FIG 3. Reference is therefore also made here to the preceding embodiments.

Contrary to the embodiment according to FIG 3, there is provision for the generation of the auxiliary voltage with a winding 92 which is arranged on the transformer 34. A bridge rectifier 90 is connected to the electric coil 92, which for its part feeds the rectified voltage to the capacitor 54. The underlying functional principle corresponds to that which was mentioned previously. A high power with a compact winding can be reached by the bridge rectification with the bridge rectifier 90.

FIG 7 shows a further embodiment of a circuit arrangement according to the invention, which is based on the exemplary embodiment according to FIG 3, as a result of which reference is additionally made to the embodiments in this regard.

Contrary to the exemplary embodiment according to FIG 3, in this embodiment provision is made for a control transformer 96 to be provided, to which all semiconductor switches of all half bridge modules 44 are assigned by means of secondary-side windings assigned to the semiconductor switches. Only one single winding which is connected to a clock generator 94 is provided on the primary side. The clock generator 94 supplies a rectangular signal with a pulse duty factor of 1, as has already been explained above. The rectangular signal is provided on the primary-side winding and forwarded via the secondary-side coils to the respective semiconductor switches. Here the secondary-side coils are interconnected for the respective half bridge module 44 so that the two semiconductor switches of the half bridge module 44 are switched on or off alternately. Aside from an electrical isolation, this also simultaneously simplifies the clock generator, which only needs to provide a single clock signal.

FIG 8 shows a further embodiment of a circuit arrangement according to the invention, which in principle is based on the circuit arrangement according to FIG 6. Reference is therefore made in addition to the embodiments relating to this exemplary embodiment.

In addition to the embodiments according to FIG 6, in the embodiment according to FIG 8 provision is made for a current measuring unit 102 to be provided for each half bridge module 44. Here, the current measuring unit 102 consists of a series circuit of an electric resistor and a capacitor which is formed of a rectifier unit 98, which here has two diodes. These form the measuring circuit. The output of the rectifier unit 98 is connected with a resistance to a reference potential, here the negative electric potential of the intermediate circuit voltage 20. The measuring voltages supplied by the rectifier units 98 are fed to the clock generator 32 for evaluation and further processing, as a result of which the rectifier units 98 are connected to the clock generator 32. This embodiment avoids having to carry out a current measurement in the individual half bridge modules 44 by means of current shunts. The invention uses the voltage of the capacitors 40, 42, also known as resonance capacitors, for this purpose. A measuring voltage based on the voltage level of the clock generator 32 can be achieved by means of the capacitive voltage division.

FIG 9 shows another embodiment which is based on the embodiment according to FIG 3. Reference is therefore made in addition to the embodiments relating to this exemplary embodiment.

Contrary to the embodiment according to FIG 3, provision is made for a pair of half bridge modules 44 to be connected in parallel with each of the electrolytic capacitors 12, 14 in each case. The electric coils 36 or 38 are connected directly between the respective central terminals 110 of the half bridge modules 44. The two half bridge modules 44 connected in parallel are actuated complementarily with respect to their semiconductor switches so that the electric coils 36, 38 are each applied with the complete capacitor voltage of the electrolytic capacitors 12, 14.

The circuit according to FIG 9 therefore represents a full bridge operation, namely in the form of a full bridge push-pull converter, preferably with a pulse width modulation. For this purpose the clock generator 32 is actuated accordingly differently, so that it generates pulse-width modulated clock signals A, B which are connected to the corresponding semiconductor switches of the half bridge modules 44. As a result, a high performance can be achieved.

Moreover, the embodiment according to FIG 9 shows a throttle 104 and a diode 106 on the auxiliary voltage side, which is connected between the diodes 26, 28 and the capacitor 54. A regulated direct voltage can be generated as a result.

In principle the electrolytic capacitors 12, 14 can be discharged by the transformer 34 being operated in a controlled manner in the saturation and the energy of the electrolytic capacitors 12, 14 being reduced as losses by eddy currents in the transformer 34. This can be achieved by reducing the clock frequency and/or increasing a cut-off current limit, wherein for this purpose a saturation characteristic, of the transformer 34, in particular of its ferromagnetic core, should rather be soft so that a slow current increase can be reached when saturation occurs.

One important advantage in the balancing of electric voltages of capacitors connected in series by means of a transformer according to the invention lies in the circuit generating barely any power loss compared with a resistance balance both with the same and also with unbalanced leakage currents of the capacitors. Furthermore, the circuit arrangement of the invention can be used to easily realise an auxiliary voltage for supplying electricity to the clock generator or also further devices/loads. Furthermore, the invention enables provision of a monitoring of the circuit arrangement in order to be able to counteract interferences. For instance, the monitoring of a current of the semiconductor switches can be used so that with a very high imbalance of the electric voltage of the electrolytic capacitors the increases quickly within a very short time. As a result, the entire system could be switched off, for instance. If a resistance circuit were nevertheless also necessary, for instance in order to ensure a safe discharging of the electrolytic capacitors after switching off the intended operation or suchlike, this only needs to be used as a design criterion of the electric resistors.

The circuit topology places low demands on the electric strength of the components used. The topology of the circuit arrangement has a good degree of efficiency on account of the resonance operation, as a result of which a high output power and a good behaviour can be achieved with respect to electromagnetic compatibility. The degree of efficiency in particular with respect to the full bridge circuit is likewise suited to a high output power and has an acceptable degree of efficiency.

The description serves only to explain the invention and should not restrict this.

Patentkrav

1. Kredsløbsanordning (30,60,70) til symmetrering af elektriske spændinger ved elektriske kondensatorer (12,14) i en seriekobling, med hver især et halvbromodul (44), der er tilsluttet til hver af de elektriske kondensatorer (12, 14), og som tilvejebringer en midtertilslutning (110), og med en taktgiver (32, 94) til at drive alle halvbromoduler (44) i taktdrift, hvor der til hver midtertilslutning (110) af hvert halvbromodul (44) er tilsluttet en pågældende første tilslutning af en elektrisk spole (36,38,78), der er tilordnet individuelt til det pågældende halvbromodul (44), og en anden tilslutning af denne elektriske spole (36,38,78) tilsvarende er tilsluttet til en af to tilslutninger af kondensatoren (12, 14), der er tilsluttet parallelt til det tilsvarende halvbromodul (44), via en seriekondensator (40, 42, 72), hvor taktgiveren (32, 94) er indrettet til at drive halvbromodulet (44) synkront i taktdrift, og hvor de elektriske spoler (36,38,78) er koblet magnetisk på en sådan måde, at de magnetiske strømninger, der genereres af de elektriske spoler (36,38,78), adderes,
kendetegnet ved, at den pågældende seriekondensator (40, 42, 72) i drift af kredsløbsanordningen drives som resonanskondensator.

2. Kredsløbsanordning ifølge krav 1, **kendetegnet ved** en hjælpespole (22,92), der er koblet magnetisk med de elektriske spoler (36,38,78).

3. Kredsløbsanordning ifølge krav 2, **kendetegnet ved, at** hjælpespolen (22,92) omfatter en midtertapning.

4. Kredsløbsanordning ifølge et af kravene 1 til 3, **kendetegnet ved** en styretransformator (96) til kobling af halvbromodulerne (44) med taktgiveren (32,94) på styresiden.

5. Kredsløbsanordning ifølge et af kravene 1 til 4, **kendetegnet ved** strømmåleenheder til hver af halvbromodulerne (44), der hver især omfatter et målekredsløb (102), der er tilsluttet til seriekondensatorerne.

6. Kredsløbsanordning ifølge krav 5, **kendetegnet ved, at** målekredsløbet (102) omfatter en ensretterenhed (98).

7. Fremgangsmåde til symmetrering af elektriske spændinger ved elektriske kondensatorer (12,14) i en seriekobling, hvor et halvbromodul (44), der i hvert tilfælde er tilsluttet til hver af de elektriske kondensatorer (12, 14) og tilvejebringer en midtertilslutning (110), drives i taktdrift ved hjælp af en taktgiver (32,94) synkront med alle yderligere halvbromoduler (44), hvor der ved hjælp af elektriske spoler (36,38,78), der hver især er tilordnet individuelt til de elektriske kondensatorer (12,14) og er koblet magnetisk med hinanden, genereres magnetiske strømninger, og hvor de elektriske spoler (36,38,78) med hver især en første tilslutning er tilsluttet til midtertilslutninger (110) af de tilsvarende halvbromoduler (44) og med hver især en anden tilslutning er tilsluttet til de dertil i hvert tilfælde parallelkoblede elektriske kondensatorer (12,14) via en seriekondensator (40, 42, 72) på en sådan måde, at de magnetiske strømninger, der genereres af de elektriske spoler (36,38,78), adderes,
kendetegnet ved, at den pågældende seriekondensator (40, 42, 72) i drift af kredsløbsanordningen drives som resonanskondensator.

8. Fremgangsmåde ifølge krav 7, **kendetegnet ved, at** der ved hjælp af en hjælpespole (22,92) genereres en hjælpespænding (56).

9. Fremgangsmåde ifølge krav 7 eller 8, **kendetegnet ved, at** en værdi af hjælpespændingen (56) indstilles ved hjælp af en taktfrekvens af taktgiveren (32,94).

FIG 1

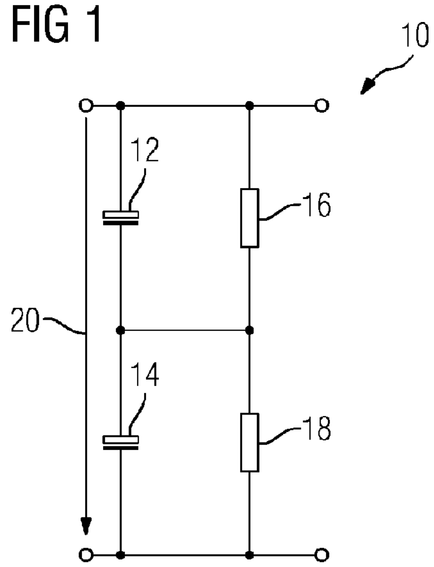
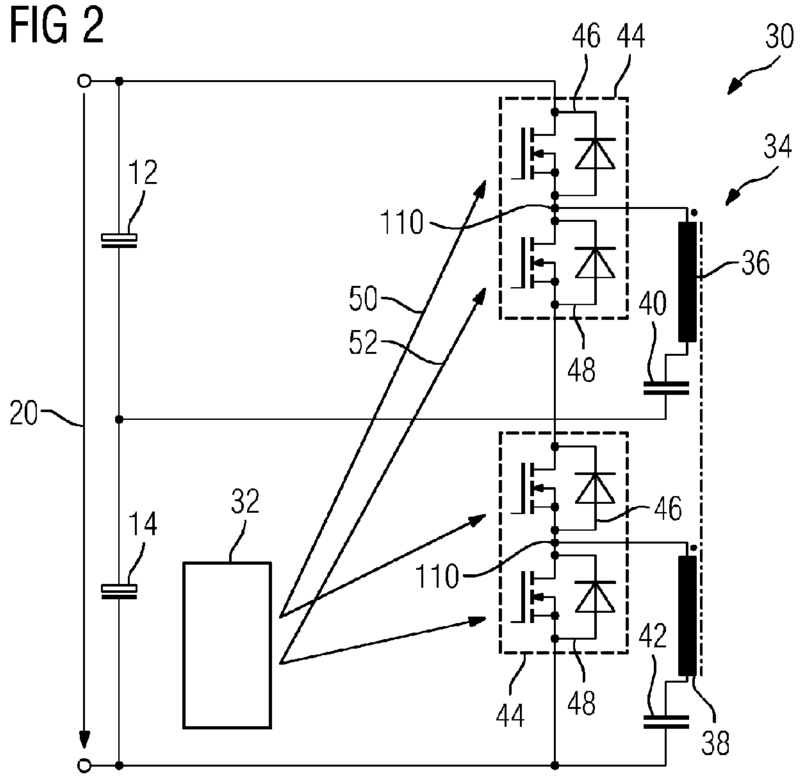

10
12
16
20
14
18

FIG 2


46
44
30
34
12
110
36
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40
52
48
20
46
32
14
110
42
44
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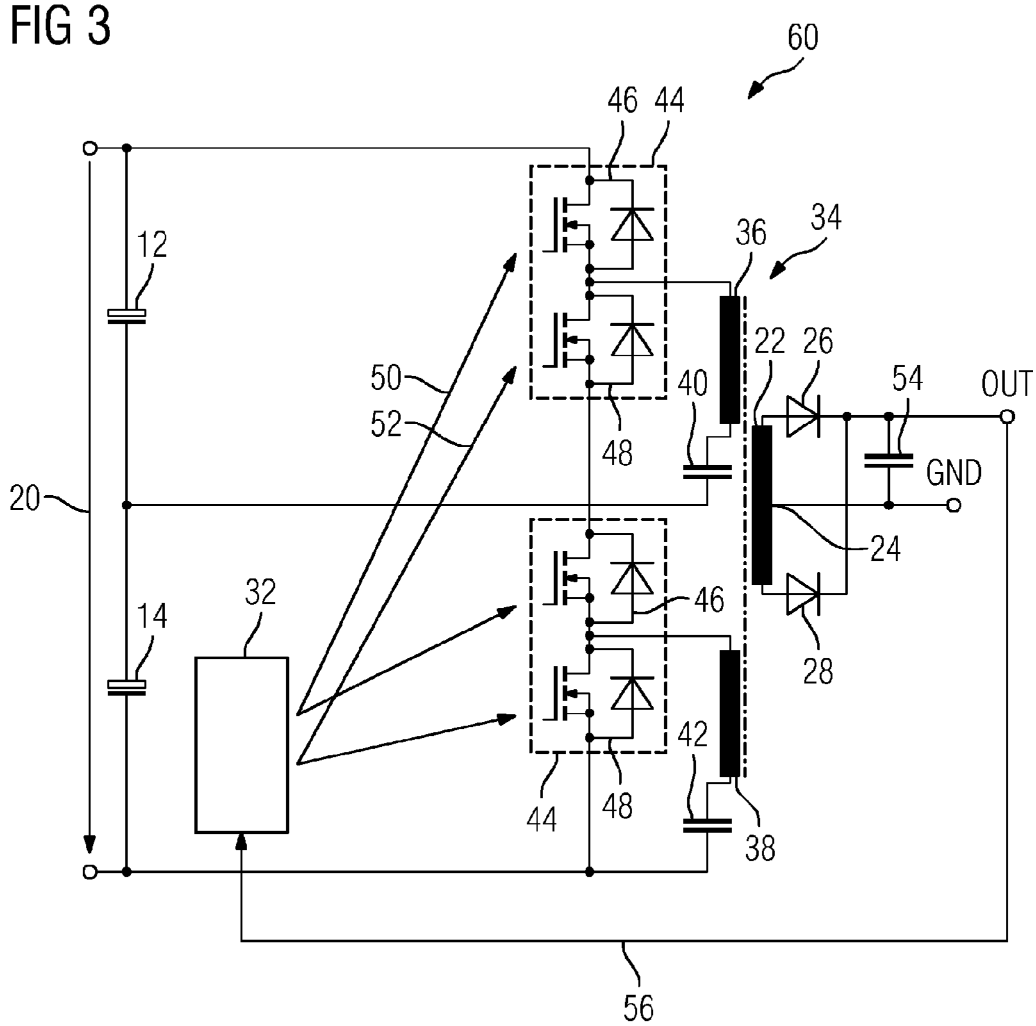
38

FIG 3


60
46
44
12
36
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22
26
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OUT
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48
GND
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24
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46
14
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44
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FIG 4

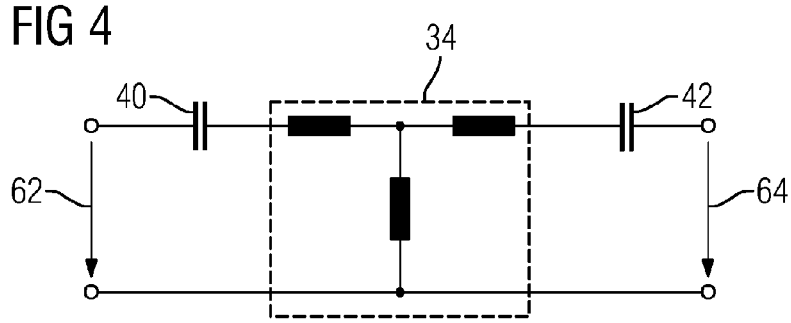
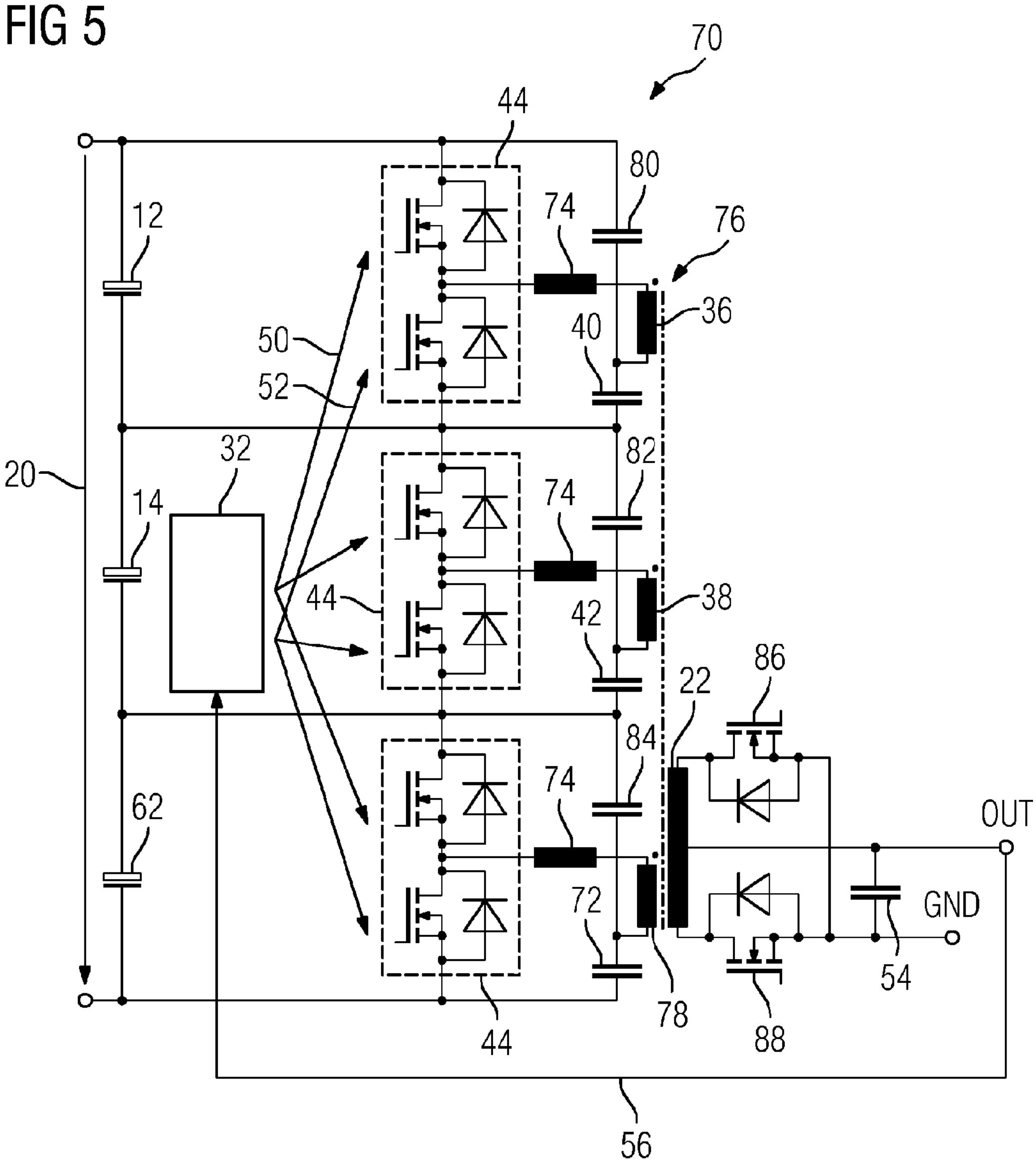

34
40
42
62
64

FIG 5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36
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40
52
20
32
82
14
74
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38
42
86
22
84
74
OUT
62
GND
72
54
78
44
88
56

FIG 6

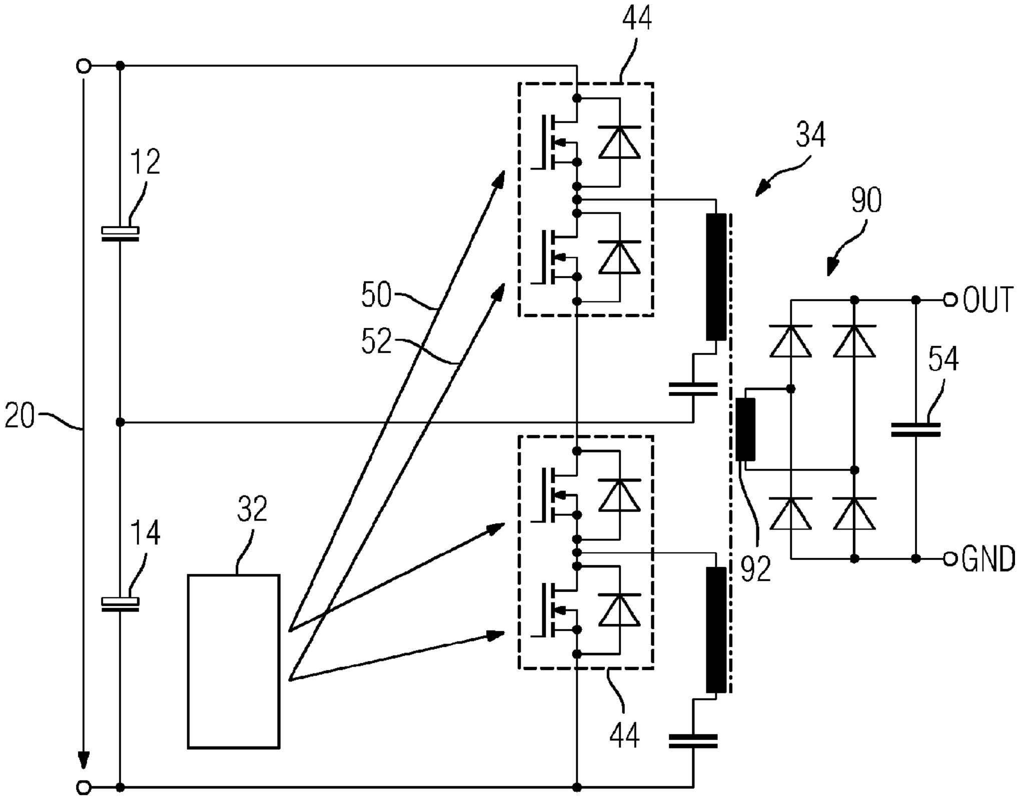

FIG 7

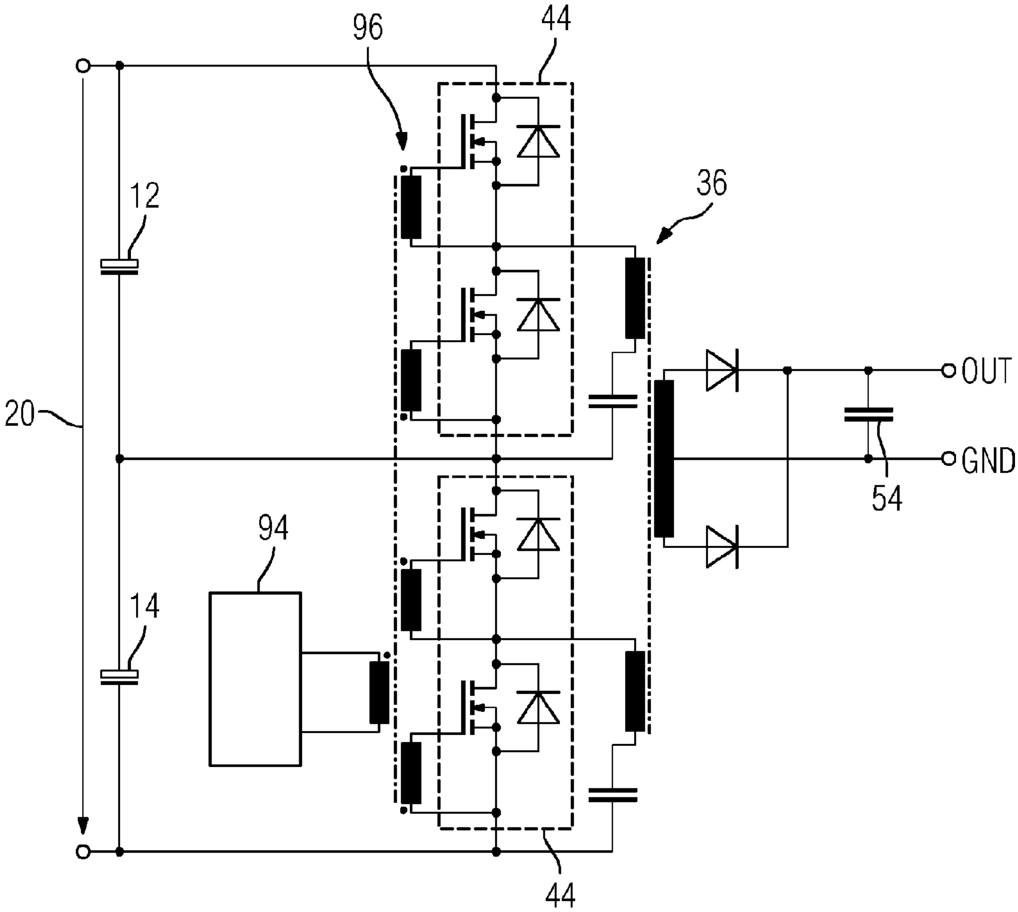

FIG 8

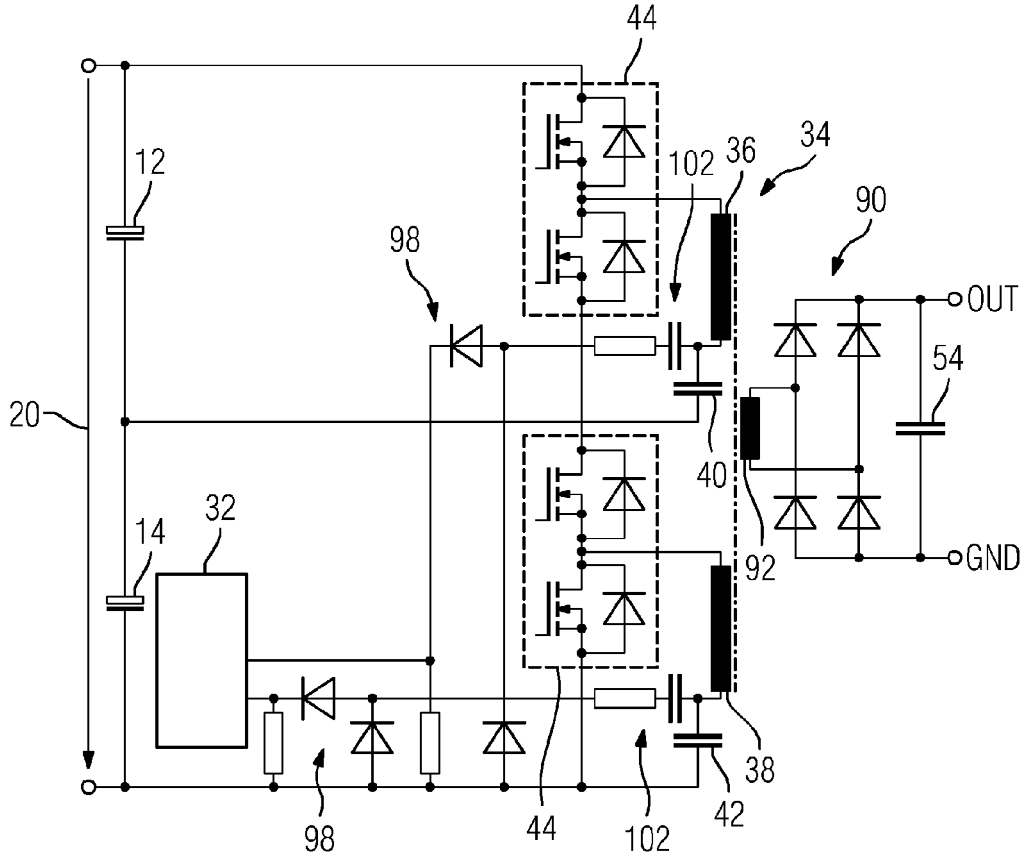

FIG 9