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(54) **Title:** SOLUTIONS INTEGRATED CIRCUIT INTEGRATION OF ALTERNATIVE ACTIVE AREA MATERIALS

(57) **Abstract:** Methods of forming areas of alternative material on crystalline semiconductor substrates, and structures formed thereby. Such areas of alternative material are suitable for use as active areas in MOSFETs or other electronic or opto-electronic devices.

SOLUTIONS FOR INTEGRATED CIRCUIT INTEGRATION OF ALTERNATIVE ACTIVE AREA MATERIALS

Related Applications

[0001] This application claims the benefit of U.S. Provisional Application 60/702,363 filed July 26, 2005, the entire disclosure of which is hereby incorporated by reference.

Field of the Invention

[0002] This invention relates to methods and materials for formation of structures including
5 alternative active area materials.

Background

[0003] As geometric scaling of Si-based MOSFET technology becomes more challenging, the heterointegration of alternate materials with Si becomes an attractive option for increasing the innate carrier mobility of MOSFET channels. Heterointegration of alternate materials has
10 thus far been limited to the addition of SiGe alloys of small Ge content for use as source-drain contact materials or heterojunction bipolar transistor base layers. Since such layers are only slightly lattice mismatched to Si, and since most modern Si MOSFET processes are compatible with these dilute SiGe alloys, few disruptions in the Si MOSFET integration sequence have been necessary. Unfortunately, the drive for increased carrier mobility (and concomitant device drive
15 current) will soon necessitate the use of other, more highly lattice-mismatched materials for historically Si-based devices, requiring more disruptive changes to the traditional device integration flow.

Summary

[0004] Heterointegration of alternative materials onto conventional and new substrates is
20 desirable for various electronic and optoelectronic applications. For example, the possibility of the heterointegration of III-V, II-VI materials and/or Ge with Si is an attractive path for increasing the functionality and performance of the CMOS platform. An economical solution to heterointegration could enable new fields of applications, such as replacing Si in CMOS transistors, particularly for critical path logic devices. This could significantly lower (a) channel
25 resistance, due to the ultra-high mobility and saturation velocity afforded by various non-Si semiconductors, and (b) source/drain resistance, due both to high mobility and to the narrower bandgap of many non-Si semiconductors, with the narrower bandgap leading to a lower electrical

resistance between the metal (or metal-alloy) contact and the semiconductor. Another new application could be the combination of Si CMOS logic with ultra-high speed RF devices, such as InP- or GaAs- based high electron mobility transistor (HEMT) or heterojunction bipolar transistor (HBT) devices similar to those utilized for high-frequency applications today. Yet another application could be the combination of Si CMOS logic with opto-electronic devices, since many non-Si semiconductors have light emission and detection performance superior to Si.

[0005] Selective epitaxy is an attractive path for hetero-materials integration for several reasons. First, it allows adding the non-Si semiconductor material only where it is needed, and so is only marginally disruptive to a Si CMOS process performed on the same wafer. Also, selective epitaxy may allow the combination of multiple new materials on a Si wafer, e.g., Ge for PMOS and InGaAs for NMOS. Furthermore, it is likely to be much more economical than key alternative paths, e.g., layer transfer of global hetero-epitaxial films, especially for integrating materials with large lattice mismatch.

[0006] Methods of forming areas of alternative material on crystalline semiconductor substrates are described. "Alternative" as used herein refers to either a non-Si semiconductor, or Si with a different surface or rotational orientation compared to an underlying Si substrate. Such areas are suitable for use as active area in MOSFETs or other electronic or opto-electronic devices. Also, designs for aspects of MOSFET devices utilizing such non-Si active areas are provided.

[0007] In an aspect, the invention features a method for forming a structure, including providing a substrate including a crystalline semiconductor material. A masking layer is formed over the substrate, and a window is defined in the masking layer. The window is filled with an active area material by selective epitaxy. A device is defined including at least a portion of the active area material.

[0008] The following feature may be included. A surface of the active area material is planarized such that the surface is substantially coplanar with a surface of the masking layer.

[0009] In another aspect, the invention features a method for forming a structure, including providing a substrate comprising a crystalline semiconductor material, and defining a first shallow trench isolation region in the semiconductor material. A thin dielectric layer is defined over the substrate, and a window is defined in the thin dielectric layer to expose a portion of the semiconductor material bound by the first shallow trench isolation region. The exposed portion of the semiconductor material is removed to define an opening. The opening is filled with an

active area material by selective epitaxy. The thin dielectric layer is selectively removed, and a device is defined including at least a portion of the active area material.

[0010] One or more of the following features may be included. A surface of the active area material is planarized such that the surface is substantially coplanar with a surface of the thin
5 dielectric layer. The substrate includes a layer including the crystalline semiconductor material bonded to a wafer. The crystalline semiconductor material has a first crystalline orientation and the active area material includes a second crystalline semiconductor material having a second crystalline orientation different from the first crystalline orientation.

[0011] A second shallow trench isolation region is defined in the semiconductor material. A
10 ratio of a width of the first shallow trench isolation region to a width of the second shallow trench isolation region is greater than 1, e.g., selected from a range of 1.2 to 3.

[0012] In another aspect, the invention features a method for forming a structure, the method including providing a substrate comprising a crystalline semiconductor material and defining a first shallow trench isolation region in the semiconductor material. A thin dielectric layer is
15 defined over the substrate. A window is defined in the thin dielectric layer to expose a portion of the first shallow trench isolation region. The exposed portion of the first shallow trench isolation region is removed to define an opening. The opening is filled with an active area material by selective epitaxy. The thin dielectric layer is selectively removed, and a device is defined including at least a portion of the active area material.

20 [0013] One or more of the following features may be included. A surface of the active area material may be planarized such that the surface is substantially coplanar with a surface of the thin dielectric layer. A second shallow trench isolation region is defined in the semiconductor material, such that a ratio of a width of a remaining portion of the first shallow trench isolation region to a width of the second shallow trench isolation region is greater than 1, e.g., selected
25 from a range of 1.2 to 3.

[0014] In another aspect, the invention features a structure that has a first active area including a first active area material and bound by a first shallow trench isolation region having a first width. A second active area includes a second active area material and is bound by a second shallow trench isolation region having a second width. A ratio of the first width to the second
30 width is greater than 1.

[0015] One or more of the following features may be included. The first active area material is a semiconductor such as Ge, SiGe, SiC, diamond, a III-V semiconductor, and/or a II-VI

semiconductor, and the second active area material includes Si. The first active area material has a first crystalline orientation and the second active area material has a second crystalline orientation different from the first crystalline orientation. The ratio of the first width to the second width is selected from a range of 1.2 to 3.

5 **[0016]** In another aspect, the invention features a method for forming a structure, the method including providing a substrate comprising a crystalline material and forming a first masking layer over the substrate. A first opening is defined in the first masking layer to expose a first portion of the substrate in a first region of the substrate. The first opening is filled with a first active area material by selective epitaxy. A second opening is defined in the first masking layer

10 to expose a second portion of the substrate in a second region of the substrate. The second opening is filled with a second active area material by selective epitaxy. A first device is defined that includes at least a portion of the first active area material, and a second device is defined that includes at least a portion of the second active area material.

[0017] One or more of the following features may be included. A second masking layer is

15 formed over the first region of the substrate before filling the second opening with the second active area material, and the second masking layer is removed after the second opening is filled with the second active area material. A surface of the first active area material and a surface of the second active area material is planarized after the removal of the second masking layer.

[0018] In another aspect, the invention features a structure including a first isolation region

20 and a first active area including a first semiconductor material and bound by the first isolation region. The structure also includes a second isolation region and a second active area including a second semiconductor material different from the first semiconductor material and bound by the second isolation region. A surface of the first semiconductor material, a surface of the second semiconductor material, a surface of the first isolation region, and a surface of the second

25 isolation region are all substantially coplanar.

[0019] One or more of the following features may be included. The first semiconductor material has a first crystalline orientation and the second semiconductor material has a second crystalline orientation different from the first crystalline orientation. The first semiconductor material includes Ge, InAs, InGaAs, InSb, AlSb, InAlSb, GaAs, or InP, and the second

30 semiconductor material includes Si and/or Ge.

[0020] In another aspect, the invention features a structure including an n-FET having a first channel comprising a first active area material, a first source, and a first drain region. A p-FET

has a second channel including a second active area material, a second source and a second drain region. The first source and drain regions and second source and drain regions include the same source/drain material.

[0021] One or more of the following features may be included. The first channel material is under tensile strain. The second channel material is under compressive strain. At least a portion of the source/drain material in the first source and first drain regions is disposed in a first and a second recess, at least a portion of the source/drain material in the second source and second drain regions is disposed in a third and a fourth recess, and a lattice constant of the source/drain material is smaller than a lattice constant of the first active area material and larger than a lattice constant of the second active area material.

[0022] At least a portion of the source/drain material in the first source and first drain regions is disposed in a first and a second recess, at least a portion of the source/drain material in the second source and second drain regions is disposed in a third and a fourth recess, and a lattice constant of the source/drain material is larger than a lattice constant of the first active area material and smaller than a lattice constant of the second active area material.

[0023] At least a portion of the source/drain material in the first source and first drain regions is disposed in a first and a second recess, the source/drain material in the second source and second drain regions is disposed on a top surface of the second active area material, and a lattice constant of the source/drain material is smaller than a lattice constant of the first active area material and smaller than a lattice constant of the second active area material. The source/drain material includes a group IV semiconductor.

[0024] The source/drain material in the first source and first drain regions is disposed on a top surface of the first active area material, at least a portion of the source/drain material in the second source and second drain regions is disposed in a third and a fourth recess, and a lattice constant of the source/drain material is larger than a lattice constant of the first active area material and larger than a lattice constant of the second active area material.

[0025] In another aspect, the invention features a method for forming a device, the method including providing a first active area material in a first region of a substrate and providing a second active area material in a second region of the substrate. A first source and a first drain are defined by the definition of a first and a second recess by removing a first portion and a second portion of the first active area material, and the deposition of a source/drain material into the first and second recesses. A second source and a second drain are defined by the definition of a third

and a fourth recess by removing a first portion and second portion of the second active area material, and the deposition of the source/drain material into the third and fourth recesses. A first device is defined having a channel disposed in the first active area material between the first source and first drain. A second device is defined having a channel disposed in the second active area material between the second source and second drain.

[0026] One or more of the following features may be included. The definition of the first, second, third, and fourth recesses includes a non-selective etch that removes the first and second active area materials at approximately the same rate. The definition of the first and second recesses in the first active material includes an etch that is highly selective with respect to the second active material. Defining the third and fourth recesses in the second active material includes an etch that is highly selective with respect to the first active material.

[0027] In another aspect, the invention features a method for forming a structure, the method including providing a substrate, providing a first active area material over a first portion of the substrate, and providing a second active area material over a second portion of the substrate. A thin layer is deposited over the first and second active area materials. A gate dielectric layer is formed over the thin layer. A first device, such as an n-FET, including the first active area material and a second device, such as a p-FET, including the second active area material are formed.

[0028] In another aspect, the invention features a structure including a first active area including a first active area material and a second active area including a second active area material different from the first active area material. A thin layer is disposed over the first active area material and the second active area material, and a gate dielectric layer is disposed over the thin layer.

[0029] One or more of the following features may be included. The first active area material and second active area material each include at least one of Ge, SiGe, SiC, diamond, III-V semiconductors, and II-VI semiconductors, and the thin layer includes Si. The gate dielectric layer includes at least one of SiO_2, SiON, Si_3N_4, and high-k dielectrics.

[0030] In another aspect, the invention features a method for forming a structure, the method including providing a substrate, providing a first active area material over a first portion of the substrate, and providing a second active area material over a second portion of the substrate. A first gate dielectric layer is formed over the first active area material, and a second gate dielectric layer is formed over the second active area material. A first electrode layer is deposited over the

first and second active area materials. A portion of the first electrode layer disposed over the second active area material is removed. A second electrode layer is deposited over the first and second active areas. The layers disposed over the substrate are planarized to define a co-planar surface including a surface of the first electrode layer disposed over the first active area material and a surface of the second electrode layer disposed over the second active area material. A first device including the first active area material and a second device including the second active area material are formed.

[0031] One or more of the following features may be included. The first device includes an n-FET. The first electrode layer includes at least one of indium, tantalum, zirconium, tungsten, molybdenum, chromium, tin, zinc, cobalt, nickel, rhenium, ruthenium, platinum, titanium, hafnium, silicon, and nitrogen. The second device includes a p-FET. The second electrode layer includes at least one of copper, molybdenum, chromium, tungsten, ruthenium, tantalum, zirconium, platinum, hafnium, titanium, cobalt, nickel, silicon, and nitrogen.

[0032] In another aspect, the invention features a structure including a first active area including a first active area material, and a second active area including a second active area material different from the first active area material. A first gate electrode material is disposed over the first active area material, and a second gate electrode material different from the first gate electrode material is disposed over the second active area material. The first gate electrode material includes at least one of indium, tantalum, zirconium, tungsten, molybdenum, chromium, tin, zinc, cobalt, nickel, rhenium, ruthenium, platinum, titanium, hafnium, silicon, and nitrogen, and the second gate electrode material includes at least one of copper, molybdenum, chromium, tungsten, ruthenium, tantalum, zirconium, platinum, hafnium, titanium, cobalt, nickel, silicon, and nitrogen.

[0033] In another aspect, the invention features a method for forming a structure, the method including providing a substrate comprising a crystalline semiconductor material, and forming a masking layer over the substrate. A window is defined in the masking layer. The window is at least partially filled with a first active area material by selective epitaxy. A second active area material is formed over the first active area material by selective epitaxy. A device including at least a portion of the second active area material is defined.

[0034] In another aspect, the invention features a method for forming a structure, the method including providing a substrate comprising a crystalline material, and forming a first masking layer over the substrate. A first opening is defined in the first masking layer to expose a first

portion of the substrate in a first region of the substrate. The first opening is filled with a first active area material by selective epitaxy. A first layer including a second active area material is formed over the first active area material by selective epitaxy. A second opening is defined in the first masking layer to expose a second portion of the substrate in a second region of the
5 substrate. The second opening is filled with a third active area material by selective epitaxy. A second layer including a fourth active area material is formed over the third active area material by selective epitaxy. A first device is defined, including at least a portion of the second active area material. A second device is defined, including at least a portion of the fourth active area material.

10 [0035] One or more of the following features may be included. The first device includes a first channel with a first strain, the second device includes a second channel with a second strain, a magnitude of the first strain is approximately equal to a magnitude of the second strain, and a sign of the first strain is opposite a sign of the second strain. The magnitude of the first strain is greater than approximately 1.5%. The first active area material is substantially the same as the
15 fourth active area material. The second active area material is substantially the same as the third active material.

[0036] In another aspect, the invention features a structure including a first active area material at least partially filling a window defined in a masking layer disposed over a semiconductor substrate. A second active area material is disposed over the first active area
20 material. A device includes at least a portion of the second active area material.

[0037] In another aspect, the invention features a first active area material disposed in a first opening defined in a first masking layer disposed over a crystalline substrate. A first layer comprising a second active area material is disposed over the first active area material. A third active area material is disposed in a second opening defined in the first masking layer. A second
25 layer comprising a fourth active area material disposed over the third active area material. A first device includes at least a portion of the second active area material. A second device includes at least a portion of the fourth active area material.

[0038] One or more of the following features may be included. The first and third active area materials are at least partially relaxed and the second and fourth active area materials are
30 substantially strained. The first and third active area materials are approximately fully relaxed. The first device is a transistor including a first source region and a first drain region disposed above the first active area material. The first source region and the first drain region are each

disposed within the first layer. The second device is a transistor including a second source region and a second drain region disposed above the third active area material. The second source region and the second drain region are each disposed within the second layer. The first device is an NMOS transistor and the second device is a PMOS transistor. The second active
5 area material includes a III-V semiconductor material and the fourth active area material includes a group IV semiconductor material. The second active area material includes at least one of InP, InAs, InSb, and InGaAs, and the fourth active area material comprises at least one of Si and Ge.

Brief Description of Drawings

10 [0039] Figures 1a – 1c, 2a – 2g, 3a – 3d, 4a – 4f, 5a – 5b, 6a – 6b, 7a – 7e, 8a – 8e, 9a – 9e, 10a – 10d, 11a – 11d, 12b – 12c, and 13a – 13g are schematic cross-sectional and top views illustrating the formation of alternative semiconductor structures; and

[0040] Figure 12a is a graph representing a correlation between band gap and mobility of several semiconductor materials.

15 [0041] Like-referenced features represent common features in corresponding drawings.

Detailed Description

[0042] Referring to Figures 1a – 1c and 2a – 2g, planar isolation regions may be utilized for the selective epitaxy of active area materials. Referring to Figures 1a, 2a, and 2b, a substrate 100
20 includes a crystalline semiconductor material. The substrate 100 may be, for example, a bulk silicon wafer, a bulk germanium wafer, a semiconductor-on-insulator (SOI) substrate, or a strained semiconductor-on-insulator (SSOI) substrate. A masking layer 110 is formed over the substrate 100. The masking layer 110 may be an insulator layer including, for example, silicon dioxide, aluminum oxide, silicon nitride, silicon carbide, or diamond, and may have a thickness
25 t_1 of, e.g., 50 – 1000 nanometers (nm). The masking layer 110 may be formed by a deposition method, such as chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), or a physical deposition method such as sputtering. Alternately, the masking layer 110 may be formed by thermal oxidation of the substrate.

30 [0043] A mask (not shown), such as a photoresist mask, is formed over the masking layer 110. The mask is patterned to expose at least a portion of the masking layer 110. The exposed portion of the masking layer 110 is removed by, e.g., reactive ion etching (RIE) to define a

window 120 to expose a region 130 of a top surface of the substrate 100. The window 120 may have a width w_1 of, e.g., 50 nm – 10 micrometers (μm) and a length l_1 of, e.g., 50 nm – 10 μm. The window has a height h_1 equal to the thickness t_1 of the masking layer 110. The window 120 corresponds to the active area of the electronic or opto-electronic device into which it will eventually be incorporated, and the dimensions are selected accordingly.

[0044] Referring to Figures 1b, 2c, and 2d, the window 120 is completely filled with an active area material 140 by selective epitaxy. Selective epitaxy may be performed by a deposition method such as LPCVD, atmospheric pressure CVD (APCVD), ultra-high vacuum CVD (UHCVD), reduced pressure CVD (RPCVD), metalorganic CVD (MOCVD), atomic layer deposition (ALD), or molecular beam epitaxy (MBE). The active area material 140 is formed selectively, i.e., it is formed on the crystalline semiconductor material of substrate 100 exposed by the window 120, but is not substantially formed on the masking layer 110. The active area material 140 is a crystalline semiconductor material, such as a group IV element or compound, a III-V compound, or a II-VI compound The group IV element may be carbon, germanium, or silicon, e.g., (110) silicon. The group IV compound may include silicon, germanium, tin, or carbon, e.g., silicon germanium (SiGe). The III-V compound may be, e.g., gallium arsenide (GaAs), indium arsenide (InAs), indium gallium arsenide (InGaAs), indium phosphide (InP), or indium antimonide (InSb), aluminum antimonide (AlSb), indium aluminum antimonide (InAlSb), or mixtures thereof. The II-VI compound may be, e.g., zinc telluride (ZnTe), cadmium selenide (CdSe), cadmium telluride (CdTe), zinc sulfide (ZnS), or zinc selenide (ZnSe), or mixtures thereof. In some embodiments, more than one active area material 140 can be formed in window 120, i.e., two or more layers of the active area material 140 can be formed by selective epitaxy. Defects may form at an interface between an active area material and the substrate 100. These defects may be trapped by sidewalls of the masking layer 110 defining the window 120, as described in U.S. Patent Application Serial Nos. 11/436,198 and 11/436,062, incorporated herein by reference.

[0045] After the window 120 is filled with the active area material 140, a portion 150 of the active area material 140 may extend above a top surface 160 of the masking layer 110 for various reasons, thereby forming a non-planar top surface. For instance, facets may form at a vertical interface between the semiconductor active area material and the insulator. Even without facets, a top surface of the active area material 140 may not be co-planar with a top surface of the insulator material, because of the difficulty of stopping reliably and repeatably the

selective epitaxy precisely at the point that the window 120 is filled with the active area material 140. A non-planar surface may present subsequent processing difficulties.

[0046] The portion of the active area material 140 extending above the masking layer 110 top surface may be removed by, for example, planarization, so that the active area material surface 170 is substantially coplanar with the top surface 160 of the masking layer 110, as depicted in Figure 1c. The active area material surface may be planarized by, for example, a chemical-mechanical polishing (CMP) step that is selective with respect to the masking layer 110.

[0047] Referring to Figures 2e – 2g, a device is formed including at least a portion of the active area material. The device may be a transistor 180, with a source 190, a drain 200, and a channel 210 disposed in the active area material. Subsequent processing steps may include the formation of a gate dielectric layer 220, the deposition of a gate electrode material, and the definition of a gate 230 by, e.g., dry etching. The source and drain regions may be defined by an ion implantation step. An interlayer dielectric may be formed over gate, source, and drain, and contact holes may be defined. A metal layer 235 may be deposited in the contact holes and over the structure. The resulting transistor 180 may be, for example, a field-effect transistor (FET), such as a complementary metal – oxide – semiconductor FET (CMOSFET) or a metal-semiconductor FET (MESFET). In an alternative embodiment, the device is a non-FET device such as a diode. The diode device could be a light detecting device (photodiode), or a light emitting device (either a light-emitting diode, or a laser diode). In an alternative application, the device is a bipolar junction transistor.

[0048] In an alternative embodiment, the active area material, such as a III-V or II-VI semiconductor alloy, or Ge, or a SiGe alloy, may be introduced only into selected active areas on a wafer, as follows.

[0049] Referring to Figures 3a – 3d, a first shallow trench isolation (STI) region 300 is defined in semiconductor substrate 100 in accordance with methods known to one of skill in the art. The STI region 300 includes a trench 310 filled with a dielectric material 320, such as silicon dioxide or silicon nitride. A thin dielectric layer 330 is formed over the substrate, including the first STI region. In an embodiment, the thin dielectric layer 330 includes the same material as the dielectric material 320. In an alternative embodiment, the thin dielectric layer 330 includes a material different from that of the dielectric material 320. The thin dielectric layer 330 may include Si_3N_4 and may have a thickness t_2 of, e.g., approximately 100 – 200 Å. If

the Si_3N_4 dielectric layer is too thick, it may damage the underlying material, such as silicon, by inducing stress. In an embodiment, the thin dielectric layer 330 includes an SiO_2 layer disposed under the Si_3N_4 layer. The SiO_2 layer alleviates the strain induced by the Si_3N_4 layer, and the thickness t_2 of the Si_3N_4 layer may be, for example, 1000 Å. The thickness of the SiO_2 layer may be, for example, 100 Å.

[0050] Referring to Figures 3a and 3b, a window 335 is defined in the thin dielectric layer 330 to expose a portion 340 of the substrate semiconductor material bound by the first STI region 300, while protecting other substrate portions. The window 335 may be defined by, e.g., a photoresist mask and a wet or a dry etch chemistry that selectively removes a portion of the thin dielectric layer 330 without attacking the underlying substrate semiconductor material. The exposed semiconductor material portion 340 is removed to define an opening 350. The semiconductor material portion 340 may be removed by a wet or dry etch chemistry that selectively removes the semiconductor material, e.g., Si, without attacking either the thin dielectric layer 330 or the STI trench fill material 320. For example, the semiconductor material portion 340 exposed by the window may be removed down to a level even with the bottom boundary of the first STI region 300. The sidewalls 360, 360' of the opening 350 are defined by the dielectric material used to line and/or fill the first STI region 300. In an embodiment, it may be preferable to remove semiconductor material portion 340 down to a level below that of the bottom boundary of the first STI region 300, and the removal process may even undercut first STI region 300, expanding opening 350 below first STI region 300. Such a profile for opening 350 may be advantageous for avoidance of facet formation or for reduction of defects in materials subsequently deposited in opening 350.

[0051] Referring to Figure 3c, the opening 350 is filled with active area material 140 by selective epitaxy. A top surface 370 of the active area material may be planarized such that the active area material is substantially coplanar with a top surface of the thin dielectric layer 330. The planarization may be performed by a CMP step, stopping at the top surface of the thin dielectric layer 330. In some embodiments, more than one active area material 140 can be formed in window 335, i.e., two or more layers of the active area material 140 can be formed by selective epitaxy.

[0052] As noted above, the thickness t_2 of the thin dielectric layer 330 may be small. An additional benefit of the small thickness t_2 is that the active area material extends only slightly above the semiconductor material of the substrate.

[0053] Referring to Figure 3d, the thin dielectric layer 330 is selectively removed, without substantially removing either the STI trench fill 320 or any underlying semiconductor material. For example, in an embodiment in which the thin dielectric layer 330 is Si_3N_4, it may be effectively removed with a heated solution comprising phosphoric acid. Optionally, a planarization step, such as CMP, may be used to fully planarize the surface of the structure including the active area material, after the removal of the thin dielectric layer 330, such that the active area material is substantially coplanar with the first STI region and the semiconductor material of the substrate. In the instance of a relatively thick dielectric layer 330, planarization after the removal of that layer may be preferable.

[0054] A device, such as a transistor, is defined, including at least a portion of the active area material 140.

[0055] Referring to Figures 4a – 4f, the crystalline semiconductor material of the substrate may have a first crystalline orientation, and the active area material may include a second crystalline semiconductor material having a second crystalline orientation different from the first crystalline orientation. Referring to Figure 4a, substrate 100 may include a first layer 400 having a first crystalline orientation, and a bonded layer 410 on the first layer 400 may include a second crystalline material having a second crystalline orientation, with a bonded interface 412 disposed between the two layers. In an embodiment, the first crystalline material of the substrate and the second crystalline material may include the same material having different orientations. For example, the first layer 400 may be (100) Si and the bonded layer may be (110) Si. In an embodiment, substantially all of substrate 100 disposed below bonded layer 410 may consist of first layer 400. For example, first layer 400 may be a (100) Si wafer and bonded layer 410 may be (110) Si.

[0056] Referring to Figure 4b, first STI region 300 is defined in the bonded layer 410, extending to the first layer 400. In an embodiment, first STI region 300 may extend into first layer 400. The first STI region 300 bounds a portion 415 of the second crystalline semiconductor material.

[0057] Referring to Figure 4c, a masking overlayer 420 is defined over the substrate 100. The masking overlayer 420 may be, for example, a thin low-stress Si_3N_4 layer with a thickness t_3 of, e.g., approximately 100 – 200 Å. A window 430 is defined in the masking overlayer 420 to expose the second crystalline semiconductor material portion 415 bound by the first STI region 300.

[0058] Referring to Figure 4d, the exposed second crystalline semiconductor material may be removed by a dry or a wet etch to define an opening 440. This removal can be via a non-selective wet or dry etch that is timed to stop after a surface 450 of the first layer 400 is exposed. Alternately, this removal can be selective, via a wet etch that preferentially removes semiconductor material of a given crystalline orientation. For example, a solution of tetramethyl-ammonium-hydroxide (TMAH) at 25% concentration and 70°C will etch (110) Si very quickly, at about 0.5 µm/min. Since this solution etches (100) Si at only 0.27 µm/min and (111) Si at only 0.009 µm/min, the solution can be used to easily remove (110) Si above a layer of (100) or (111) Si.

[0059] Referring to Figure 4e, the opening 440 is filled by the first crystalline material by selective epitaxy. A top surface of the selective epitaxial material 460 may be planarized such that it is substantially coplanar with the top surface of bonded layer 410. The planarization may be performed by a CMP step, stopping, for example, at a top surface 470 of the masking overlayer 420.

[0060] Referring to Figure 4f, the masking layer is removed, and devices are formed, having active areas comprising the first crystalline material and the second crystalline material, the two crystalline materials having different crystalline orientations.

[0061] In an embodiment, the active area 480 of an n-FET is bound by the first STI region 300, and the active area 490 of a p-FET is bound by a second STI region 300' formed in parallel to the formation of the first STI region 300. (110) surface Si has much higher hole mobility than the (100) surface, but the electron mobility of the (110) surface is poorer. It may be advantageous, therefore, to provide (100) Si in the area bound by the first STI region 300 for use as the active area 480 of an n-FET, and to provide (110) Si in the area 490 bound by the second STI region 300' for use as the active area of a p-FET.

[0062] In an alternative embodiment, the bonded layer 410 includes (100) Si and is bonded to a wafer including (110) Si. After the STI region 300, 300' formation, the (100) Si is removed from the area bound by the second STI region 300'. (110) Si is selectively grown in the area bound by the second STI region for use as the active area of a p-FET, and planarized. (100) Si bound by the first STI region is used as the active area of an n-FET.

[0063] In another alternative embodiment, the bonded layer 410 is (100) strained silicon, transferred from a graded buffer on a second substrate and bonded to a (110) Si wafer. After STI formation, the (100) strained silicon is removed from the area bound by the second STI region

300'. (110) Si is selectively grown in the area bound by the second STI region 300' for use as the active area of a p-FET, and planarized. (100) strained Si bound by the first STI region is used as the active area of an n-FET.

[0064] As discussed above, an overlayer masking material, such as masking overlayer 420 or thin dielectric layer 330 may be used to cover certain regions, e.g., p-FET regions, during the selective growth of alternative active area material on uncovered regions, e.g., n-FET regions. Defining the edge of the overlayer masking material is a challenge, because the lithographic step used to define the edge requires a very fine alignment to the STI region. For example, the alignment may need to be within ± 10nm. If the STI region to which the edge is aligned is too narrow in comparison to an alignment tolerance of the lithographic step, misalignment may result.

[0065] Referring to Figures 5a – 5b, the first STI region 300 that bounds a region in which an active area will be defined is wider than the second STI region 300' formed on the same substrate 100. For example, STI region 300 may have a width w_2 selected from a range of 40 nm to 400 nm, and the second STI region 300' may have a width w_3 selected from a range of 20 nm to 200 nm. A ratio of the width of STI region 300 to the width of the second STI region may be greater than 1, preferably selected from the range of 1.2 to 3. The ratio may also be greater than 3, but this may create an excessive area penalty.

[0066] As discussed above with reference to Figures 3a – 3d, thin dielectric layer 330 is formed and a window is defined. The wider STI region 300 facilitates the alignment of the photoresist mask, such that edges 500 of the thin dielectric layer 330 are more reliably defined over the STI region 300. The substrate semiconductor material 510 exposed by the window is removed to define an opening (not shown). The opening is filled with active area material (not shown) by selective epitaxy. A top surface of the active area material may be planarized such that the active area material is substantially coplanar with a top surface of the thin dielectric layer 330. The planarization may be performed before and/or after the removal of the thin dielectric layer 330. In the instance of a relatively thick dielectric layer 330, planarization after the removal of that layer may be preferable. In some embodiments, more than one active area material can be formed in the opening, i.e., two or more layers of the active area material can be formed by selective epitaxy.

[0067] Referring to Figures 6a – 6b, in an alternative embodiment, first STI region 300 that is wider than an active area is defined in substrate 100 comprising a crystalline semiconductor

material. Thin dielectric layer 330 is formed over the substrate, and a window 600 is defined in the thin dielectric layer 330 to expose a portion of the first STI region 300. The exposed portion of the first STI region is removed by, e.g., a dry etch which will not substantially etch silicon, comprising, e.g., HCl and/or HBr, to define an opening 610. The opening 610 is filled with an active area material (not shown) by selective epitaxy. A top surface of the active area material may be planarized such that the active area material is substantially coplanar with a top surface of the thin dielectric layer 330. The planarization may be performed before and/or after the removal of the thin dielectric layer 330. In some embodiments, more than one active area material can be formed in the opening 610, i.e., two or more layers of the active area material can be formed by selective epitaxy.

[0068] The remaining insulator strips 620 around the periphery of the opening will function as isolation structures. A ratio of the width of these strips to a width of a second STI region 300' may be greater than 1.

[0069] The thin dielectric layer is removed 330, and a device is defined including at least a portion of the active area material.

[0070] The first STI region 300 has a width w_4 of, e.g., the sum of the equivalent of the active area (typically a minimum of ten times the gate length) and two times a trench width (each typically two times a gate length). Thus, for a subsequently formed device with a gate length of 45 nm, the first STI region 300 may have a width of 630 nm.

[0071] Referring to Figures 7a – 7e, two or more different active area materials may be selectively grown on a single substrate. A masking layer 110 is formed over substrate 100, which includes a crystalline material as described above. The masking layer 110 includes a non-crystalline material, such as a dielectric, e.g., SiO_2 or Si_3N_4. The masking layer 110 may act as an isolation region. A first opening 710 is defined in the first masking layer to expose a first portion of the substrate in a first region 720 of the substrate. The first opening 710 may be defined by a wet or a dry selective etch.

[0072] The first opening is filled with a first active area material 730 by selective epitaxy, such that the first active area material forms in the first opening 710, but is not substantially formed on the masking layer 110. In some embodiments, more than one active area material can be formed in the first opening 710, i.e., two or more layers of the active area material can be formed by selective epitaxy.

[0073] A second masking layer 740 may be formed over the substrate such that the first

region of the substrate is covered. The second masking layer 740 includes a non-crystalline material, such as a dielectric. A second opening 750 is defined in the second and first masking layer to expose a second portion of the substrate in a second region 760 of the substrate. The second opening is filled with a second active area material 770 by selective epitaxy. The second
5 masking layer 740 prevents the second active area material 770 from forming by selective epitaxy on the crystalline first active area material 730. The second masking layer may be removed by, e.g., a selective wet etch, after the second opening is filled with the second active area material. In some embodiments, more than one active area material can be formed in the second opening 750, i.e., two or more layers of the active area material can be formed by
10 selective epitaxy.

[0074] Thus, the structure may include first isolation region 110', first active area comprising a first active area material 730 and bound by the first isolation region 110', second isolation region 110'', and second active area comprising a second active area material 770 different from the first active area material and bound by the second isolation region 110''.
15 Preferably, a surface of the first active area material 730, a surface of the second active area material 770, a surface of the first isolation region 110', and a surface of the second isolation region 110'' are all substantially coplanar.

[0075] Each of the first and second active area materials 730, 770 may be formed in the manner discussed above with respect to active area material 140, and may include any of the
20 listed materials. In an embodiment, the first active area material has a first crystalline orientation and the second active area material has a second crystalline orientation different from the first crystalline orientation. In some embodiments, the first active area material may include at least one of a group IV element or compound, such as Si or Ge or SiGe, or a III-V compound, such as InAs, InGaAs, InSb, AlSb, InAlSb, GaAs, and InP, and the second active area material may
25 include at least one of a group IV element or compound, such as Si or Ge or SiGe, or a III-V compound, such as InAs, InGaAs, InSb, AlSb, InAlSb, GaAs, and InP.

[0076] After the removal of the second masking layer, a surface of the first active area material and a surface of the second active area material may be planarized by, e.g., CMP. This CMP step enables the non-selective polishing of two different materials by polishing both the
30 first active area material and the second active area material at the same rate.

[0077] By further processing, a first device including the first active area is formed, and a second device including the second active area is formed.

[0078] In this way, two types of alternative active area materials may be formed on a substrate for use in electronic or opto-electronic devices. For example, a first active area material may be suitable for use as the active area of an n-FET, e.g., InGaAs, and the second active area material may be suitable for use as the active area of a p-FET, e.g., Si, Ge, or SiGe.

5 [0079] Referring also to Figures 8a–8e, in an embodiment, no second masking layer 740 is formed prior to the formation of the second active area material. Thus, after the filling of the first opening with the first active area material 730, the second opening 750 in the first masking layer 110 is defined and filled with the second active area material 770. The second active area material 770 is formed by selective epitaxy, which results in the second active area material

10 being formed on all exposed crystalline surfaces, including a top surface of the first active area material. After formation of the second active area material 770, the structure may be planarized by, e.g., CMP.

[0080] Referring to Figure 9a – 9e, different transistors in a CMOS circuit may have different active area materials. The design and processing challenges of the incorporation of two

15 types of active area materials in a single substrate may be reduced by the use of a single source/drain material for both n- and p-FET. Moreover, the described structure allows a CMOS circuit to include an n-FET with a channel having a first type of stress and a p-FET with a channel having a second type of stress, which may be beneficial for various channel material combinations.

20 [0081] As explained above, in some instances, two different active area materials may be preferable for the formation of different types of devices on a single substrate. For example, a CMOS device 900 may include (i) a n-FET 905 that has a first channel 910 disposed in a first active area material 915, such as Ge, GaAs, InAs, InSb, or InGaAs, a first source region 920, and a first drain region 925; and (ii) an p-FET 930 may have a second channel 940 disposed in a

25 second active area material 935, such as SiGe, Ge, Si with a (110) surface, or InSb, a second source region 945, and a second drain region 950.

[0082] The CMOS device 900 may be formed as follows. The first active area material 915, suitable for use as first channel 910 of the n-FET 905, is provided in a first region 955 of semiconductor substrate 100. The second active area material 935, suitable for use as second

30 channel 940 of the p-FET 930, is provided in a second region 960 of semiconductor substrate 100.

[0083] Referring to Figures 9c and 9d, the first source and the first drain regions 920, 925 are

defined by first defining a first and a second recess 965, 970 by removing a first portion and a second portion of the first active area material 915, and then depositing a source/drain material into the first and second recesses. Subsequently or, preferably in parallel, the second source and the second drain regions 945, 950 are defined by first defining a third and a fourth recess 980, 985 by removing a first portion and a second portion of the second active area material 935, and then depositing a source/drain material into the third and fourth recesses.

[0084] The recesses may be formed by a suitable wet or dry etch. For example, the first, second, third, and fourth recesses 965, 970, 980, 985 may be formed by a non-selective etch that removes the first and second active area materials at approximately the same rate. For example, a dry etch with a 45% SF_6/ 55% O_2 chemistry [with total gas pressure of 100 milliTorr (mTorr), RF power of 50 Watts, and total gas flow rate of 30 standard cubic centimeters per minute (sccm)] may be used to etch active areas that include Si and Ge at approximately the same rate of 200 nm/min. (*See* A. Campo, et al., "Comparison of Etching Processes of Silicon and Germanium in SF_6-O_2 Radio-Frequency Plasma," *J. Vac. Sci. Technol. B*, Vol. 13, No. 2, p. 235, 1995, incorporated herein by reference.) Alternatively, the first and second recesses 965, 970 in the first active material may be defined by an etch that is highly selective with respect to the second active material. Similarly, the third and fourth recesses 980, 985 may be removed by an etch that is highly selective with respect to the first active material. For example, if the first active area material is Si and the second active area material is Ge, the first and second recesses 965, 970 in the Si material may be created with a SF_6/H_2/CF_4 etch chemistry. Gas flows of 35 sccm for SF_6, 65 sccm for H_2, and 80 sccm for CF_4, a pressure of 150 mTorr and RF power of 50 Watts enable this chemistry to etch Si at approximately 10 nm/min with complete selectivity to Ge. (*See* G. S. Oehrlein, et al., "Studies of the Reactive Ion Etching of SiGe alloys," *J. Vac. Sci. Technol. A*, Vol. 9, No. 3, p. 768, 1991, incorporated herein by reference.) The third and fourth recesses 980, 985 may then be created with an HCl etch chemistry, at a total pressure of 20 Torr and an HCl partial pressure of 208 mTorr (in H_2 carrier gas). At an etch temperature of 500 – 600 °C, this chemistry etches Ge at 10 – 20 nm/min with complete selectivity to Si. (*See* Y. Bogumilowicz, et al., "Chemical Vapour Etching of Si, SiGe and Ge with HCl; Applications to the Formation of Thin Relaxed SiGe Buffers and to the Revelation of Threading Dislocations," *Semicond. Sci. Technol.*, Vol. 20, p. 127, 2005, incorporated herein by reference.)

[0085] The source/drain material deposited into the first source and drain regions 920, 925 is the same as the source/drain material deposited into the second source and drain regions 945,

950. By selecting source/drain materials with appropriate lattice constants, desired types of stress may be induced in the active area materials. For example, the first active area material may be under tensile strain, and/or the second active area material may be under compressive strain. In an embodiment, the channel 940 of the p-FET 930 is compressively strained and the channel 910 of the n-FET 905 is tensilely strained; thus, for the case of channel materials comprising, for example, Si, SiGe, or Ge the carrier mobilities of both devices are enhanced. Here, the source/drain material has a lattice constant that is smaller than a lattice constant of the first active area material of the n-FET channel. Hence, the n-FET channel is tensilely strained. The lattice constant of the source/drain material is larger than a lattice constant of the second active area material of the p-FET channel. Hence, the p-FET channel is compressively strained. More particularly, the first active area material may be Ge, the second active area material may be Si, and the source/drain material may be SiGe.

[0086] In another embodiment, the first active area material may be under compressive strain, and/or the second active area material may be under tensile strain. Therefore, the channel 940 of the p-FET 930 is tensilely strained and the channel 910 of the n-FET 905 is compressively strained. Here, the source/drain material has a lattice constant that is larger than a lattice constant of the first active area material of the n-FET channel. Hence, the n-FET channel 910 is compressively strained. The lattice constant of the source/drain material is smaller than a lattice constant of the second active area material of the p-FET channel 940. Hence, the p-FET channel 940 is tensilely strained. More particularly, the first active area material may be Si, the second active area material may be Ge, and the source/drain material may be SiGe.

[0087] The type of strain that may be beneficial for device performance may be determined from piezoresistance coefficients. A relatively large positive piezoresistance coefficient is an indicator that compressive strain will enhance carrier mobilities. A relatively large negative piezoresistance coefficient is an indicator that tensile strain will enhance carrier mobilities. For example, the piezoresistance coefficient for <110> Si for p-type devices is 71.8, as measured in parallel to current flow. Hence compressive strain will help increase carrier mobilities in p-type devices having <110>-oriented Si channels. The piezoresistance coefficient for <110> Ge for n-type devices is -72, as measured in parallel to current flow. Hence, tensile strain will help increase carrier mobilities in n-type devices having <110>-oriented Ge channels. In an embodiment, CMOS device 900 includes n-FET 905 having a <110>-oriented Ge tensilely strained channel 910, and p-FET 930 with a <110>-oriented Si compressively strained channel

940, and a source/drain material of Si_xGe_y.

[0088] In an embodiment, at least a portion of the source/drain material in the first source and first drain regions 920, 925 is disposed in a first and a second recess 965, 970, at least a portion of the source/drain material in the second source and second drain regions 945, 950 is disposed in a third and a fourth recess 980, 985, and a lattice constant of the source/drain material is smaller than a lattice constant of the first active area material 915 and larger than a lattice constant of the second active area material 935. In another embodiment, a lattice constant of the source/drain material is larger than a lattice constant of the first active area material 915 and smaller than a lattice constant of the second active area material 935.

[0089] Alternatively, at least a portion of the source/drain material in the first source and first drain regions 920, 925 is disposed in a first and a second recess 965, 970, the source/drain material in the second source and second drain regions 945, 950 is disposed on a top surface of the second active area material, and a lattice constant of the source/drain material is smaller than a lattice constant of the first active area material 915 and smaller than a lattice constant of the second active area material 935. In this case, third and fourth recesses 980, 985 are not formed before deposition of the source/drain material because additional strain on p-FET 930 is not desired or may even deleteriously affect performance of p-FET 930. The source/drain material may include a group IV semiconductor, such as Si, Ge, SiGe, or SiC.

[0090] In yet another embodiment, the source/drain material in the first source and first drain regions 920, 925 is disposed on a top surface of the first active area material, at least a portion of the source/drain material in the second source and second drain regions 945, 950 is disposed in a third and a fourth recess 980, 985, and a lattice constant of the source/drain material is larger than a lattice constant of the first active area material 915 and larger than a lattice constant of the second active area material 935. In this case, first and second recesses 965, 970 are not formed before deposition of the source/drain material because additional strain on n-FET 905 is not desired or may even deleteriously affect performance of n-FET 905.

[0091] With subsequent processing, a first device, such as n-FET 905, is defined, having a channel 910 disposed in the first active area material between the first source 920 and the first drain 925. Also, a second device, such as a p-FET 930, is defined, having a channel 940 disposed in the second active area material between the second source 945 and the second drain 950.

[0092] The design and fabrication of CMOS devices having different n- and p- active areas

may be simplified by the use of a single gate dielectric material for both n- and p-type devices.

[0093] Referring to Figures 10a – 10d, first active area material 730 is provided over a first portion 1000 of substrate 100, and second active area material 770 is provided over a second portion 1010 of substrate 100, as discussed above with reference to Figures 7a – 7e. The first and second active area materials may each include, for example, at least one of Ge, SiGe, SiC, diamond, III-V semiconductors, and II-VI semiconductors.

[0094] A very thin layer 1020, .e.g., of thickness t = 5 – 20Å is deposited over both the first and the second active area materials so that a top surface of each active material includes the same material. This deposition may be selective, i.e., such that deposition occurs on the active area materials, but not on the surface of the isolation regions surrounding the active areas. This thin layer 1020 may include, e.g., Si, Ge, or another material selected for its high quality interface properties with a particular gate dielectric. This thin layer 1020 may be deposited by, e.g., a method such as ALD, that allows for very fine thickness control. A gate dielectric layer 1030 is thereafter formed over the thin layer 1020. In an embodiment, the thin layer 1020 includes Si and the gate dielectric layer 1030 includes thermally grown SiO_2. Alternatively, the gate dielectric layer 1030 may include SiON, Si_3N_4, or a deposited high-k dielectric, such as hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), or zirconium oxide (ZrO_2).

[0095] A first device 1040 is formed including the first active area material 730 and a second device 1050 is formed including the second active area material 770. For example, the first device 1040 may be an n-FET and the second device 1050 may be a p-FET.

[0096] The performance, design and fabrication of CMOS devices having different n- and p-active areas may be improved by the use of different gate electrode materials for the n- and p-type devices, selected, e.g., in view of work-function considerations.

[0097] Referring to Figures 11a – 11d, first active area material 730 is provided over a first portion 720 of substrate 100, and second active area material 770 is provided over a second portion 760 of substrate 100, as discussed above with reference to Figures 7a – 7e. Gate dielectric layer 1030 is formed over the substrate 100, either directly over both of the first and second active areas, or by first forming the thin layer 1020 as described above with reference to Figures 10a – 10c. In an embodiment, a first gate dielectric layer is formed over the first active area material 730 and a second gate dielectric layer is formed over the second active area material 770. For example, the second active area material may be masked by a dielectric masking layer such as SiO_2 or Si_3N_4, and the first gate dielectric layer is formed over only

exposed first active area material 730 by a method such as oxidation, nitridation, or atomic layer deposition. Either before or after deposition of a gate electrode material on the first active area (described below), the masking material may be removed from the second active area and applied to the first active area. The second gate dielectric layer may then be formed over only 5 exposed second active area material 770 by a method such as oxidation, nitridation, or atomic layer deposition. The masking material may then be removed. In an embodiment, the first and second gate dielectric layers are formed from the same material and are formed in a single step.

[0098] A first gate electrode material 1100 is deposited over the substrate 100, including over the first active area material 730. The first gate electrode material 1100 may be suitable for 10 use as a gate of an n-FET device, and may include, for example, indium (In), tantalum (Ta), zirconium (Zr), tungsten (W), molybdenum (Mo), chromium (Cr), tin (Sn), zinc (Zn), cobalt (Co), nickel (Ni), rhenium (Re), ruthenium (Ru), platinum (Pt), titanium (Ti), hafnium (Hf), alloys of one or more of the aforementioned materials, and alloys of one or more of the aforementioned materials with Si and/or nitrogen. Referring to Figure 11b, the first gate 15 electrode material 1100 disposed over the second active area material 770 may be removed, e.g., by a wet or dry etch highly selective to the underlying gate dielectric layer. A suitable dry etch may be XeF_2 at 2.6 mTorr, which will etch Ti, Ta, Mo, and W but is very selective to most oxides. (*See* K. R. Williams, et al., "Etch Rates for Micromachining Processing—Part II," *J. Micromechanical Systems,* Vol. 12, No. 6, p. 761, 2003, incorporated herein by reference.)

20 **[0099]** Referring to Figure 11c, a second gate electrode material 1110 is deposited over the substrate 100, including over the second active area material 770. The second gate electrode material 1110 may be suitable for use as a gate of a p-FET device, and may include, for example, copper (Cu), Mo, Cr, W, Ru, Ta, Zr, Pt, Hf, Ti, Co, Ni, alloys of one or more of the aforementioned materials, and alloys of one or more of the aforementioned materials with Si 25 and/or nitrogen. The second gate electrode material 1110 disposed over the first active area material 730 may be removed, e.g., by a wet or dry etch highly selective to the underlying first gate electrode material. For example, for the case of a first gate electrode material of tungsten (W) and a second gate electrode material of titanium (Ti), a room-temperature wet etch solution of 10:1 H_2O:HF can be used to remove the Ti at a rate of approximately 1100 nm/minute, while 30 stopping selectively on the W that is etched at a rate at least 100 times slower. (*See* K.R. Williams et al., "Etch rates for micromachining processes" *J. Microelectromech. Syst.* 5, p256-269, 1996, incorporated herein by reference). Alternatively, the second gate electrode material

1110 disposed over the first active area material 730 may be removed by a planarization step, such as CMP.

[0100] Referring to Figure 11d, the first and second gate electrode layers 1100, 1110 disposed over the substrate 100 are planarized to define a co-planar surface 1130 including a surface of the first electrode layer 1100 disposed over the first active area material 730 and a surface of the second electrode layer 1110 disposed over the second active area material 770. In an embodiment, the first gate electrode material 1100 may be used as a CMP stop for the second gate electrode material.

[0101] A first gate may be defined over the first active area material and a second gate may be defined over the second active area material. A first device, such as an n-FET is defined, including the first active area material, and a second device, such as a p-FET is defined, including the second active area material.

[0102] Referring to Figures 12a–12c, two different materials may be deposited in a single active area region to improve device characteristics. Referring to Figure 12a, certain channel materials, e.g., InSb or InAs, may enable high carrier mobility but may also have low band gaps that may cause high source or drain diode leakage. Referring to Figure 12b, a transistor 1200 having an active area including a channel material with a relatively low band gap may be susceptible to high source and/or drain 1202, 1204 leakage. Improved results may be achieved by defining an active area by the selective epitaxy of two active area materials.

[0103] Referring to Figure 12c, using a selective epitaxy process analogous to the processes described with reference to Figures 1a–1c and 2a–2g, a bi-layer structure is defined by the selective epitaxy of a lower active area material layer 1210 in a window 120 defined in the masking layer 110. The lower active area material layer 1210 may include a first semiconductor material 1215 (S1) having a relatively high band gap, such as GaSb, AlSb, CdSe, ZnTe, InAlAs, CdTe, or InAlSb. A thickness t_4 of the first active area material 1210 may be equal to depth d_1 of the window 120. Thickness t_4 and depth d_1 may be, for example, selected from a range of, e.g., 200 nm to 500 nm. A planarization step (e.g., CMP) to planarize lower active area material layer 1210 may be performed, so that the top surface of lower active area material layer 1210 and the top surface of masking layer 110 are co-planar. Subsequently, an upper active area material layer 1220 may be formed over the lower active area material layer 1210. The upper active area material layer may include a second semiconductor material 1225 (S2) that provides a high carrier mobility, but may have a low bandgap, such as InAs or InSb. A thickness t_5 of the upper

active material layer may be, for example, selected from a range of 5 nm to 100 nm. In an embodiment, the lower active area material may be substantially uniform, e.g., ungraded, in composition.

[0104] In a preferred embodiment, a lattice mismatch between the first material S1 1215 and
5 the second material S2 1225 is sufficiently small to reduce the formation of defects. The lattice mismatch is preferably less than about 2%. Some possible material combinations are given below in Table 1:

S2	S1	S1 E_g (eV)
InAs	GaSb	0.8
InAs	AlSb	1.7
InAs	CdSe	1.8
InAs	ZnTe	2.4
InAs	InAlAs	0.8-1.0
InSb	CdTe	1.5
InSb	InAlSb	0.8

Table 1: S1 and S2 material combinations

10 **[0105]** A device 1250, such as a transistor, may be formed including the lower and upper active area layers 1210, 1220. Bottom portions of source and drain regions 1260, 1265 may be disposed in the lower active area layer 1210, and upper portions of the source and drain regions 1260, 1265 may be disposed in the upper active area layer 1220. Leakage current is thereby reduced while high carrier mobility is provided.

15 **[0106]** Defects 1230 may form at an interface between the substrate and the semiconducting material S1, due to lattice constant mismatch. These defects may be trapped by sidewalls of the masking layer 110 defining the window 120, as described in U.S. Patent Application Serial No.11/436,198 and 11/436,062,

[0107] Referring to Figures 13a–13e, in some embodiments, selective epitaxy of active area
20 materials may be used to provide channel regions with high strain levels, e.g., ≥1.5%, that may be used in both NMOS and PMOS devices. Masking layer 110 is formed over substrate 100, which includes a crystalline material as described above. The masking layer 110 includes a non-crystalline material, such as a dielectric, e.g., SiO_2 or Si_3N_4. First opening 710 is defined in the masking layer 110, exposing a first portion 1300 of the substrate 100. First active area material

730, such as Si, is grown by selective epitaxy within the first opening 710. A top portion of the first active area material 730 extending above a top surface of the masking layer 110 may be planarized by, e.g., CMP. Thereafter, a first layer 1310 including second active area material 770 is selectively grown over the first active area material 730. The second active area material 770 may be lattice mismatched to the first active area material 730. For example, $Si_{1-x}Ge_x$ may be formed over relaxed Si, with $x \geq 0.35$. A thickness t_6 of the second active area material 770 is preferably less than a thickness leading to gross relaxation. In compressive layers, such as $Si_{1-x}Ge_x$ formed over Si, this relaxation thickness is approximately three to four times a critical thickness h_c, i.e., a thickness at which misfit dislocations may start to appear. For example, for $x = 0.35$ the critical thickness at which misfit dislocations may start to appear is approximately 65 nm, so thickness t_6 is preferably less than approximately 260 nm.

[0108] Each of the first and second active area materials 730, 770 may be formed in the manner discussed above with respect to active area material 140, and may include any of the listed materials. In some embodiments, the first active area material may include at least one of a group IV element or compound, such as Si or Ge or SiGe, or a III-V compound, such as InAs, InGaAs, InSb, AlSb, InAlSb, GaAs, and InP, and the second active area material may include at least one of a group IV element or compound, such as Si or Ge or SiGe, or a III-V compound, such as InAs, InGaAs, InSb, AlSb, InAlSb, GaAs, and InP.

[0109] The first portion of the substrate, including first and second active area materials 730, 770, is covered with second masking layer 740. The second masking layer 740 includes a non-crystalline material, such as a dielectric, e.g., SiO_2 or Si_3N_4. Second opening 750 is defined in the masking layer 110. The second opening 750 is filled with a third active area material 1315, e.g., $Si_{1-x}Ge_x$ with $x \geq 0.35$. A thickness of the third active area material 1315 is preferably greater than a thickness that leads to gross relaxation, such that the third active area material is relaxed. In compressive layers, such as $Si_{1-x}Ge_x$ formed over a Si substrate, this relaxation thickness is approximately three to four times a critical thickness h_c, i.e., a thickness at which misfit dislocations may start to appear. For example, for $x = 0.35$ the critical thickness at which misfit dislocations may start to appear is approximately 65 nm, so the thickness of the third active material 1315 is preferably greater than approximately 260 nm. Defects may form at an interface between the second active area material 770 and the substrate 100. These defects may be trapped by sidewalls of the masking material 110 defining the opening 750, as described in U.S. Patent Application Serial Nos. 11/436,198 and 11/436,062. A top portion of the third active

area material 1315 extending above the top surface of the masking layer 110 may be planarized by, e.g., CMP. Thereafter, a second layer 1320 comprising a fourth active area material 1317, e.g., Si, is selectively grown over the third active area material 1315. A thickness t_7 of the fourth active area material 1317 is preferably less than a thickness that leads to gross relaxation. For
5 tensilely strained layers, such as Si disposed over relaxed $Si_{1-x}Ge_x$, the thickness t_7 is less than about 10 times the critical thickness h_c. For example, for $x = 0.35$, the critical thickness at which misfit dislocations may start to appear is approximately 65 nm, so thickness t_7 is preferably less than approximately 650 nm. The second masking layer 740 is removed by, e.g., a selective wet etch.

10 **[0110]** Each of the third and fourth active area materials 1315, 1317 may be formed in the manner discussed above with respect to active area material 140, and may include any of the listed materials. In some embodiments, the third active area material may include at least one of a group IV element or compound, such as Si or Ge or SiGe, or a III-V compound, such as InAs, InGaAs, InSb, AlSb, InAlSb, GaAs, and InP, and the fourth active area material may include at
15 least one of a group IV element or compound, such as Si or Ge or SiGe, or a III-V compound, such as InAs, InGaAs, InSb, AlSb, InAlSb, GaAs, and InP.

[0111] In an embodiment, the first and second active area materials 730, 770 deposited in the first opening 710 may be the same as the fourth and third active area materials 1317, 1315, respectively, deposited in the second opening 750. This will result in equivalent strain levels for,
20 e.g., NMOS and PMOS devices incorporating these active areas. That is, an NMOS and a PMOS device will incorporate strains substantially identical in magnitude but opposite in sign. In a preferred embodiment, Si on SiGe is used for the NMOS regions, and SiGe on Si is used for the PMOS regions, thus providing the beneficial sign of strain for both NMOS and PMOS regions. Other combinations of materials are possible. Based on the observation that tensile
25 strain typically helps electron mobility (be it in Si, SiGe, and perhaps even SiC) and compressive strain (in the direction of current flow) typically helps PMOS mobility (be it in Si or SiGe), a guideline for material selection may be that for the NMOS case the natural lattice constant of the channel material is preferably smaller than the semiconductor below, and vice versa for PMOS. Prefeably, for both the NMOS and PMOS cases, the lower active area material is substantially
30 relaxed, such that the upper active area material is strained.

[0112] Referring to Figure 13e, a resulting structure 1355 includes first and second active areas 1360, 1370. The first active area 1360 may be suitable for formation of a PMOS device. It

may include second active area material 770, e.g., highly compressively strained $Si_{1-x}Ge_x$, disposed over first active area material 730, e.g., Si. The highly compressively strained material may enhance PMOS device performance by providing high hole mobility. The second active area 1370 may be suitable for formation of an NMOS device. It may include fourth active area material 1317, e.g., highly tensilely strained Si, disposed over third active area material 1315, e.g., relaxed $Si_{1-x}Ge_x$. The highly tensilely strained material may enhance NMOS device performance by providing high electron mobility.

[0113] Referring to Figure 13f, PMOS and NMOS transistors 1380, 1385 are formed over first and second active areas 1360, 1370 of the structure 1355. In an embodiment, the PMOS and NMOS transistors may have shallow source and drain regions 1390, 1390', 1395, 1395' disposed entirely in the upper active area materials, i.e., second active area material 770 and fourth active area material 1317, respectively. Thus, the source and drain regions do not intersect an interface between two epitaxial layers, that may include misfit dislocations that may lead to severe, unacceptable leakage.

[0114] Referring to Figure 13g, the source and drain regions 1390, 1390', 1395, 1395' may include silicide material, thereby enhancing source and drain contacts. The source and drain regions may be thickened by selective epitaxy. In an embodiment, the PMOS source and drain regions may include $Si_{1-x}Ge_x$ and the NMOS source and drain regions may include Si, thereby enhancing the respective device performances.

[0115] In all of the structures and devices discussed above, a non-uniform doping profile may be formed during the epitaxy of the layers. This doping profile may preferably have a lower concentration of dopants in a top portion of the layer(s).

[0116] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the invention described herein. Scope of the invention is thus indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

What is claimed is:

1 1. A method for forming a structure, the method comprising:
2 providing a substrate comprising a crystalline semiconductor material;
3 forming a masking layer over the substrate;
4 defining a window in the masking layer;
5 filling the window with an active area material by selective epitaxy; and
6 defining a device including at least a portion of the active area material.

1 2. The method of claim 1, further comprising planarizing a surface of the active area
2 material such that the surface is substantially coplanar with a surface of the masking layer.

1 3. A method for forming a structure, the method comprising:
2 providing a substrate comprising a crystalline semiconductor material;
3 defining a first shallow trench isolation region in the semiconductor material;
4 defining a thin dielectric layer over the substrate;
5 defining a window in the thin dielectric layer to expose a portion of the semiconductor
6 material bound by the first shallow trench isolation region;
7 removing the exposed portion of the semiconductor material to define an opening;
8 filling the opening with an active area material by selective epitaxy;
9 selectively removing the thin dielectric layer; and
10 defining a device including at least a portion of the active area material.

1 4. The method of claim 3, further comprising planarizing a surface of the active area
2 material such that the surface is substantially coplanar with a surface of the thin dielectric layer.

1 5. The method of claim 3, wherein the substrate includes a layer bonded to a wafer and the
2 layer comprises the crystalline semiconductor material.

1 6. The method of claim 5, wherein the crystalline semiconductor material has a first
2 crystalline orientation and the active area material comprises a second crystalline semiconductor
3 material having a second crystalline orientation different from the first crystalline orientation.

1 7. The method of claim 3, further comprising defining a second shallow trench isolation
2 region in the semiconductor material.

1 8. The method of claim 7, wherein a ratio of a width of the first shallow trench isolation
2 region to a width of the second shallow trench isolation region is greater than 1.

1 9. The method of claim 8, wherein the ratio of widths is selected from a range of 1.2 to 3.

1 10. A method for forming a structure, the method comprising:
2 providing a substrate comprising a crystalline semiconductor material;
3 defining a first shallow trench isolation region in the semiconductor material;
4 defining a thin dielectric layer over the substrate;
5 defining a window in the thin dielectric layer to expose a portion of the first shallow
6 trench isolation region;
7 removing the exposed portion of the first shallow trench isolation region to define an
8 opening;
9 filling the opening with an active area material by selective epitaxy;
10 selectively removing the thin dielectric layer; and
11 defining a device including at least a portion of the active area material.

1 11. The method of claim 10, further comprising planarizing a surface of the active area
2 material such that the surface is substantially coplanar with a surface of the thin dielectric layer.
1 12. The method of claim 10, further comprising defining a second shallow trench isolation
2 region in the semiconductor material, wherein a ratio of a width of a remaining portion of the
3 first shallow trench isolation region to a width of the second shallow trench isolation region is
4 greater than 1.
1 13. The method of claim 12, wherein the ratio is selected from a range of 1.2 to 3.
1 14. A structure comprising:
2 a first active area comprising a first active area material and bound by a first shallow
3 trench isolation region having a first width; and
4 a second active area comprising a second active area material and bound by a second
5 shallow trench isolation region having a second width,
6 wherein a ratio of the first width to the second width is greater than 1.
1 15. The structure of claim 14, wherein the first active area material is a semiconductor
2 selected from the group consisting of Ge, SiGe, SiC, diamond, III-V semiconductors, and II-VI
3 semiconductors, and the second active area material comprises Si.
1 16. The structure of claim 14, wherein the first active area material has a first crystalline
2 orientation and the second active area material has a second crystalline orientation different from
3 the first crystalline orientation.
1 17. The structure of claim 14, wherein the ratio of the first width to the second width is

2 selected from a range of 1.2 to 3.

1 18. A method for forming a structure, the method comprising:

2 providing a substrate comprising a crystalline material;

3 forming a first masking layer over the substrate;

4 defining a first opening in the first masking layer to expose a first portion of the substrate

5 in a first region of the substrate;

6 filling the first opening with a first active area material by selective epitaxy;

7 defining a second opening in the first masking layer to expose a second portion of the

8 substrate in a second region of the substrate;

9 filling the second opening with a second active area material by selective epitaxy;

10 defining a first device including at least a portion of the first active area material; and

11 defining a second device including at least a portion of the second active area material.

1 19. The method of claim 18, further comprising:

2 forming a second masking layer over the first region of the substrate before filling the

3 second opening with the second active area material; and

4 removing the second masking layer after filling the second opening with the second

5 active area material.

1 20. The method of claim 19, further comprising planarizing a surface of the first active area

2 material and a surface of the second active area material after the removal of the second masking

3 layer.

1 21. A structure comprising:

2 a first isolation region;

3 a first active area comprising a first semiconductor material and bound by the first

4 isolation region;

5 a second isolation region; and

6 a second active area comprising a second semiconductor material different from the first

7 semiconductor material and bound by the second isolation region,

8 wherein a surface of the first semiconductor material, a surface of the second

9 semiconductor material, a surface of the first isolation region, and a surface of the second

10 isolation region are all substantially coplanar.

1 22. The structure of claim 21, wherein the first semiconductor material has a first crystalline

2 orientation and the second semiconductor material has a second crystalline orientation different

3 from the first crystalline orientation.

1 23. The structure of claim 21, wherein the first semiconductor material is selected from the
2 group consisting of Ge, InAs, InGaAs, InSb, GaAs, and InP, and the second semiconductor
3 material comprises at least one of Si and Ge.

1 24. A structure comprising:
2 an n-FET having
3 a first channel comprising a first active area material, and
4 a first source and a first drain region; and
5 a p-FET having
6 a second channel comprising a second active area material, and
7 a second source and a second drain region,
8 wherein the first source and drain regions and second source and drain regions comprise
9 the same source/drain material.

1 25. The structure of claim 24, wherein the first channel is under tensile strain.

1 26. The structure of claim 24, wherein the second channel is under compressive strain.

1 27. The structure of claim 24, wherein at least a portion of the source/drain material in the
2 first source and first drain regions is disposed in a first and a second recess, at least a portion of
3 the source/drain material in the second source and second drain regions is disposed in a third and
4 a fourth recess, and a lattice constant of the source/drain material is smaller than a lattice
5 constant of the first active area material and larger than a lattice constant of the second active
6 area material.

1 28. The structure of claim 24, wherein at least a portion of the source/drain material in the
2 first source and first drain regions is disposed in a first and a second recess, at least a portion of
3 the source/drain material in the second source and second drain regions is disposed in a third and
4 a fourth recess, and a lattice constant of the source/drain material is larger than a lattice constant
5 of the first active area material and smaller than a lattice constant of the second active area
6 material.

1 29. The structure of claim 24, wherein at least a portion of the source/drain material in the
2 first source and first drain regions is disposed in a first and a second recess, the source/drain
3 material in the second source and second drain regions is disposed on a top surface of the second
4 active area material, and a lattice constant of the source/drain material is smaller than a lattice
5 constant of the first active area material and smaller than a lattice constant of the second active

6 area material.

1 30. The structure of claim 29, wherein the source/drain material comprises a group IV
2 semiconductor.

1 31. The structure of claim 24, wherein the source/drain material in the first source and first
2 drain regions is disposed on a top surface of the first active area material, at least a portion of the
3 source/drain material in the second source and second drain regions is disposed in a third and a
4 fourth recess, and a lattice constant of the source/drain material is larger than a lattice constant of
5 the first active area material and larger than a lattice constant of the second active area material.

1 32. A method for forming a device, the method comprising:
2 providing a first active area material in a first region of a substrate;
3 providing a second active area material in a second region of the substrate;
4 defining a first source and a first drain by
5 defining a first and a second recess by removing a first portion and a second
6 portion of the first active area material, and
7 depositing a source/drain material into the first and second recesses;
8 defining a second source and a second drain by
9 defining a third and a fourth recess by removing a first portion and second portion
10 of the second active area material, and
11 depositing the source/drain material into the third and fourth recesses;
12 defining a first device having a channel disposed in the first active area material between
13 the first source and first drain; and
14 defining a second device having a channel disposed in the second active area material
15 between the second source and second drain.

1 33. The method of claim 32, wherein defining the first, second, third, and fourth recesses
2 comprises a non-selective etch that removes the first and second active area materials at
3 approximately the same rate.

1 34. The method of claim 32, wherein defining the first and second recesses in the first active
2 material comprises an etch that is highly selective with respect to the second active material.

1 35. The method of claim 32, wherein defining the third and fourth recesses in the second
2 active material comprises an etch that is highly selective with respect to the first active material.

1 36. A method for forming a structure, the method comprising:
2 providing a substrate;

3 providing a first active area material over a first portion of the substrate;
4 providing a second active area material over a second portion of the substrate;
5 depositing a thin layer over the first and second active area materials;
6 forming a gate dielectric layer over the thin layer;
7 forming a first device comprising the first active area material; and
8 forming a second device comprising the second active area material.

1 37. The method of claim 36, wherein the first device comprises an n-FET and the second
2 device comprises a p-FET.

1 38. A structure comprising:
2 a first active area comprising a first active area material;
3 a second active area comprising a second active area material different from the first
4 active area material;
5 a thin layer disposed over the first active area material and the second active area
6 material; and
7 a gate dielectric layer disposed over the thin layer.

1 39. The structure of claim 38, wherein the first active area material and second active area
2 material are each selected from the group consisting of Ge, SiGe, SiC, diamond, III-V
3 semiconductors, and II-VI semiconductors, and the thin layer comprises Si.

1 40. The structure of claim 38, wherein the gate dielectric layer is selected from the group
2 consisting of SiO_2, SiON, Si_3N_4, and high-k dielectrics.

1 41. A method for forming a structure, the method comprising:
2 providing a substrate;
3 providing a first active area material over a first portion of the substrate;
4 providing a second active area material over a second portion of the substrate;
5 forming a first gate dielectric layer over the first active area material;
6 forming a second gate dielectric layer over the second active area material;
7 depositing a first electrode layer over the first and second active area materials;
8 removing a portion of the first electrode layer disposed over the second active area
9 material;
10 depositing a second electrode layer over the first and second active areas;
11 planarizing the layers disposed over the substrate to define a co-planar surface including
12 a surface of the first electrode layer disposed over the first active area material and a surface of

13 the second electrode layer disposed over the second active area material;
14 forming a first device comprising the first active area material; and
15 forming a second device comprising the second active area material.
1 42. The method of claim 41, wherein the first device comprises an n-FET.
1 43. The method of claim 42, wherein the first electrode layer comprises at least one material
2 selected from the group consisting of indium, tantalum, zirconium, tungsten, molybdenum,
3 chromium, tin, zinc, cobalt, nickel, rhenium, ruthenium, platinum, titanium, hafnium, silicon,
4 and nitrogen.
1 44. The method of claim 41, wherein the second device comprises a p-FET.
1 45. The method of claim 44, wherein the second electrode layer comprises at least one
2 material selected from the group consisting of copper, molybdenum, chromium, tungsten,
3 ruthenium, tantalum, zirconium, platinum, hafnium, titanium, cobalt, nickel, silicon, and nitrogen.
1 46. A structure comprising:
2 a first active area comprising a first active area material;
3 a second active area comprising a second active area material different from the first
4 active area material;
5 a first gate electrode material disposed over the first active area material; and
6 a second gate electrode material different from the first gate electrode material disposed
7 over the second active area material,
8 wherein the first gate electrode material comprises at least one material selected from the
9 group consisting of indium, tantalum, zirconium, tungsten, molybdenum, chromium, tin, zinc,
10 cobalt, nickel, rhenium, ruthenium, platinum, titanium, hafnium, silicon, and nitrogen and the
11 second gate electrode material comprises at least one material selected from the group consisting
12 of copper, molybdenum, chromium, tungsten, ruthenium, tantalum, zirconium, platinum,
13 hafnium, titanium, cobalt, nickel, silicon, and nitrogen.
1 47. A method for forming a structure, the method comprising:
2 providing a substrate comprising a crystalline semiconductor material;
3 forming a masking layer over the substrate;
4 defining a window in the masking layer;
5 at least partially filling the window with a first active area material by selective epitaxy;
6 forming a second active area material over the first active area material by selective
7 epitaxy; and

8 defining a device including at least a portion of the second active area material.

1 48. A method for forming a structure, the method comprising:
2 providing a substrate comprising a crystalline material;
3 forming a first masking layer over the substrate;
4 defining a first opening in the first masking layer to expose a first portion of the substrate
5 in a first region of the substrate;
6 filling the first opening with a first active area material by selective epitaxy;
7 forming a first layer comprising a second active area material over the first active area
8 material by selective epitaxy;
9 defining a second opening in the first masking layer to expose a second portion of the
10 substrate in a second region of the substrate;
11 filling the second opening with a third active area material by selective epitaxy;
12 forming a second layer comprising a fourth active area material over the second active
13 area material by selective epitaxy;
14 defining a first device including at least a portion of the second active area material; and
15 defining a second device including at least a portion of the fourth active area material.

1 49. The method of claim 48, wherein the first device comprises a first channel with a first
2 strain, the second device comprises a second channel with a second strain, a magnitude of the
3 first strain is approximately equal to a magnitude of the second strain, and a sign of the first
4 strain is opposite a sign of the second strain.

1 50. The method of claim 49, wherein the magnitude of the first strain is greater than
2 approximately 1.5%.

1 51. The method of claim 48, wherein the first active area material is substantially the same as
2 the fourth active area material.

1 52. The method of claim 51, wherein the second active area material is substantially the same
2 as the third active material.

1 53. The method of claim 48, wherein the second active area material is substantially the same
2 as the third active material.

1 54. A structure comprising:
2 a first active area material at least partially filling a window defined in a masking layer
3 disposed over a semiconductor substrate;
4 a second active area material disposed over the first active area material; and

5 a device including at least a portion of the second active area material.

1 55. A structure comprising:

2 a first active area material disposed in a first opening defined in a first masking layer
3 disposed over a crystalline substrate;

4 a first layer comprising a second active area material disposed over the first active area
5 material;

6 a third active area material disposed in a second opening defined in the first masking
7 layer;

8 a second layer comprising a fourth active area material disposed over the third active area
9 material;

10 a first device including at least a portion of the second active area material; and

11 a second device including at least a portion of the fourth active area material.

1 56. The structure of claim 55, wherein the first and third active area materials are at least
2 partially relaxed and the second and fourth active area materials are substantially strained.

1 57. The structure of claim 56, wherein the first and third active area materials are
2 approximately fully relaxed.

1 58. The structure of claim 55, wherein the first device is a transistor comprising a first source
2 region and a first drain region disposed above the first active area material.

1 59. The structure of claim 58, wherein the first source region and the first drain region are
2 each disposed within the first layer.

1 60. The structure of claim 58, wherein the second device is a transistor comprising a second
2 source region and a second drain region disposed above the third active area material.

1 61. The structure of claim 60, wherein the second source region and the second drain region
2 are each disposed within the second layer.

1 62. The structure of claim 60, wherein the first device is an NMOS transistor and the second
2 device is a PMOS transistor.

1 63. The structure of claim 55, wherein the second active area material comprises a III-V
2 semiconductor material and the fourth active area material comprises a group IV semiconductor
3 material.

1 64. The structure of claim 63, wherein the second active area material comprises at least one
2 of InP, InAs, InSb, and InGaAs and the fourth active area material comprises at least one of Si
3 and Ge.

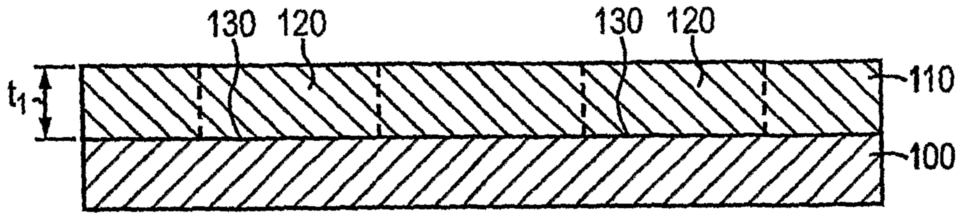

FIG. 1A

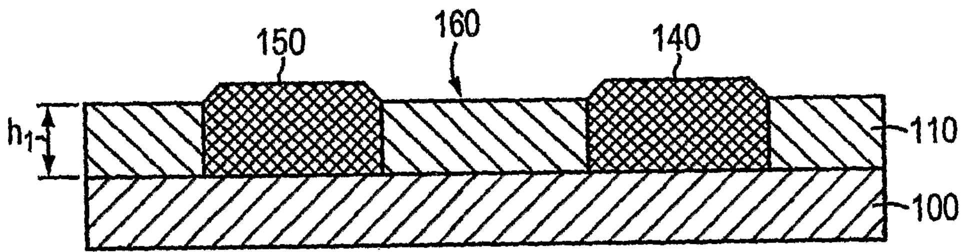

FIG. 1B

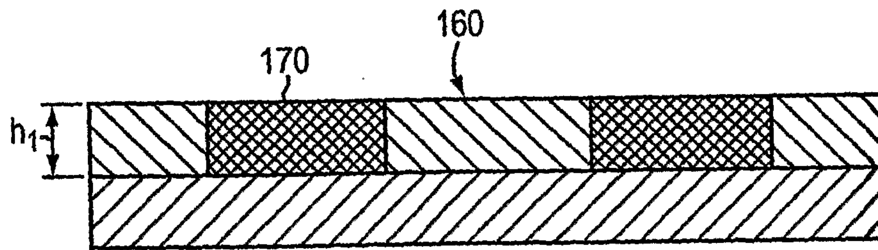

FIG. 1C

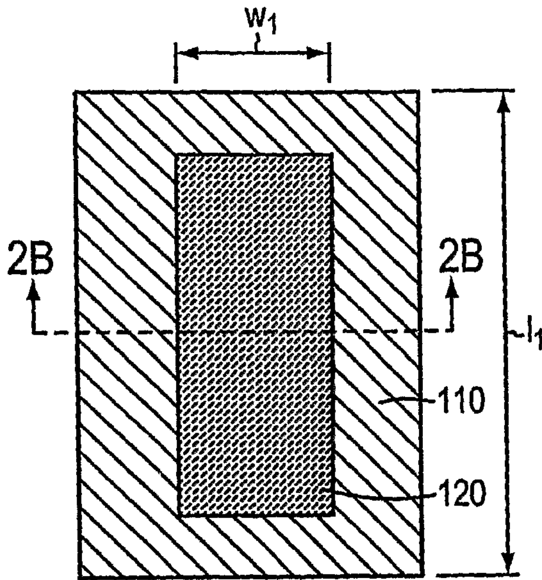

FIG. 2A

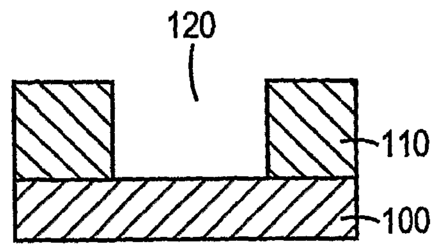

FIG. 2B

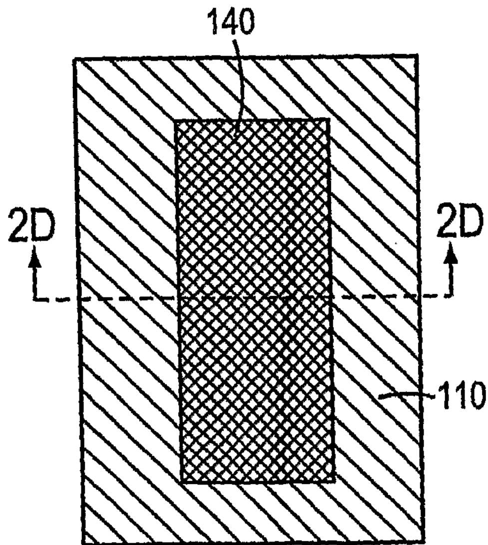

FIG. 2C

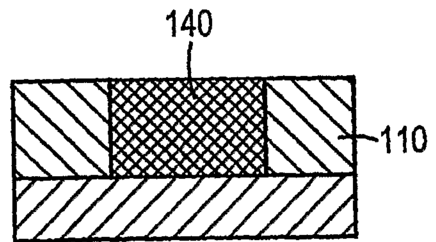

FIG. 2D

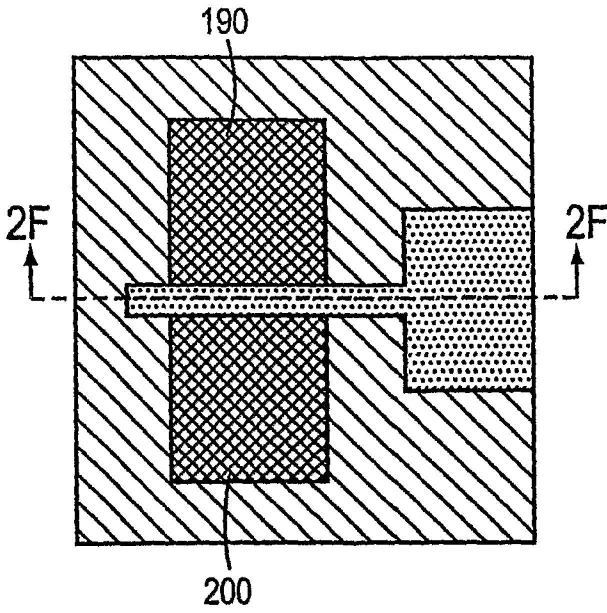

FIG. 2E

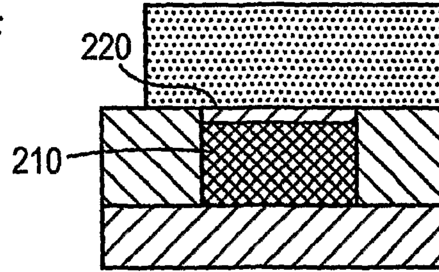

FIG. 2F

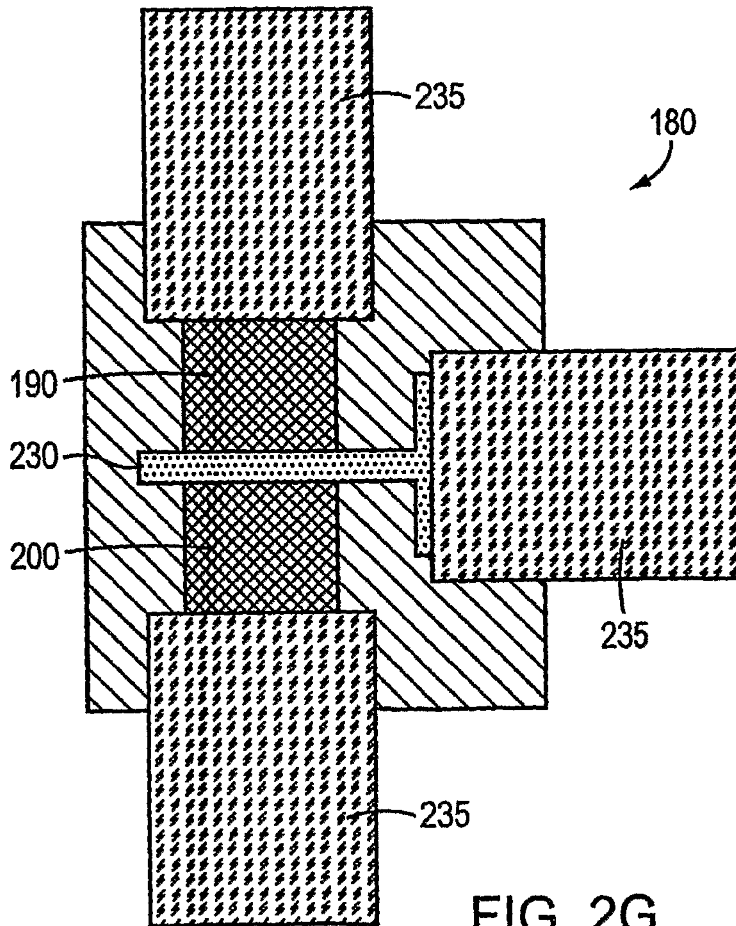

FIG. 2G

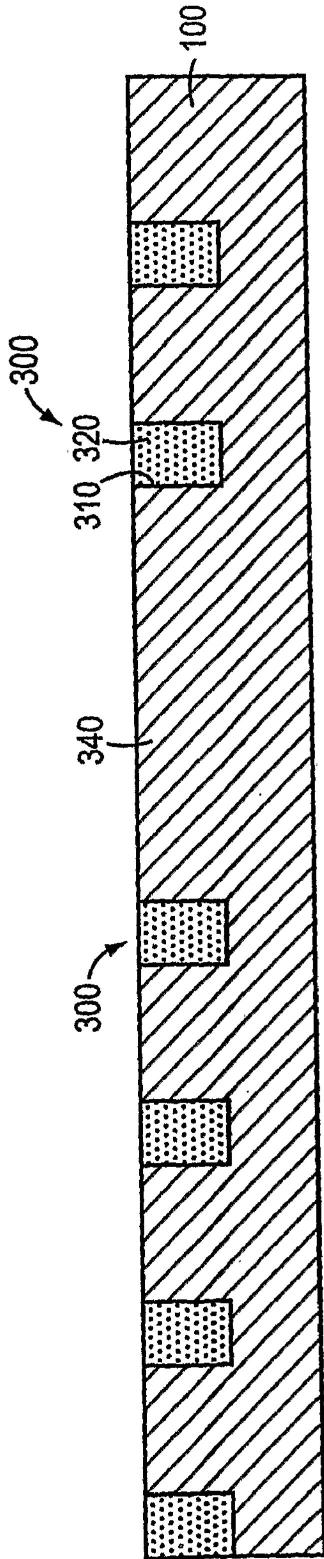

FIG. 3A

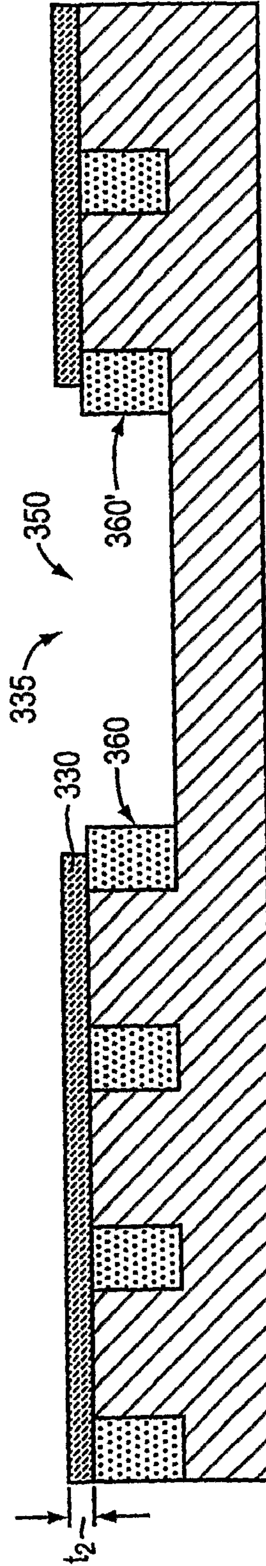

FIG. 3B

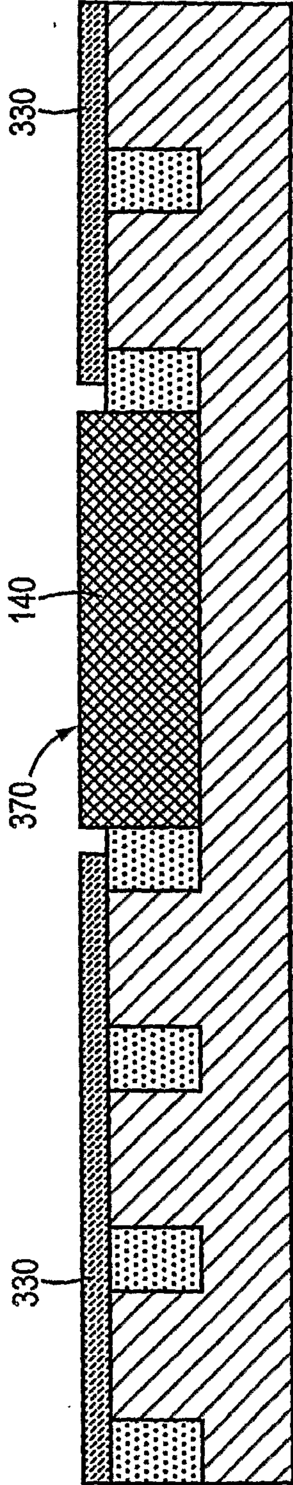

FIG. 3C

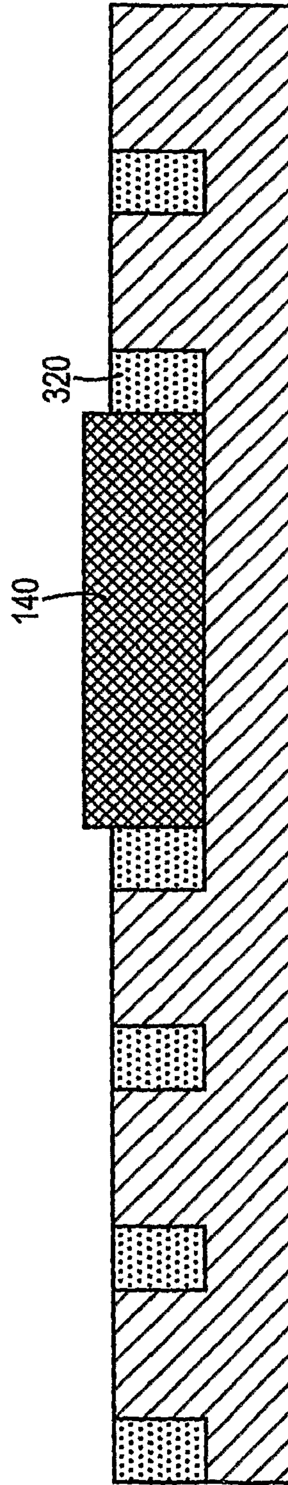

FIG. 3D

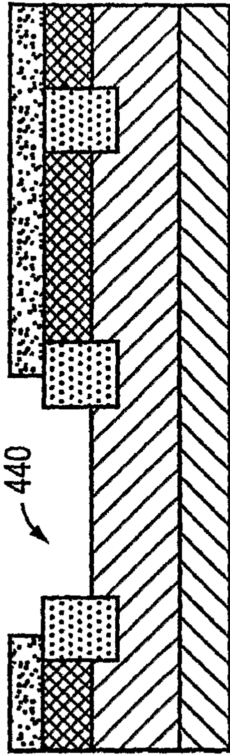

FIG. 4D

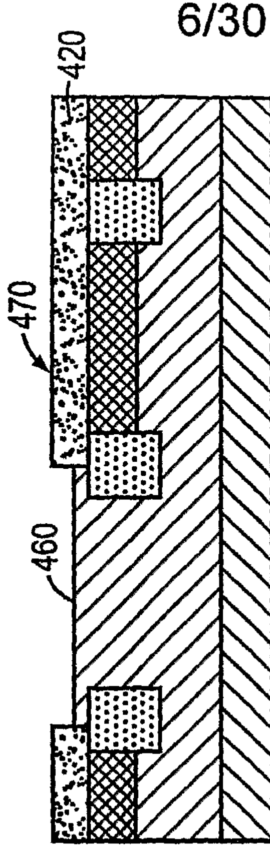

FIG. 4E

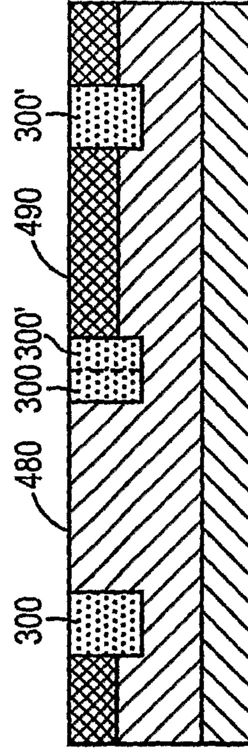

FIG. 4F

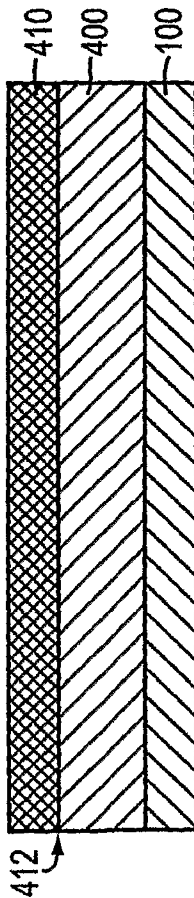

FIG. 4A

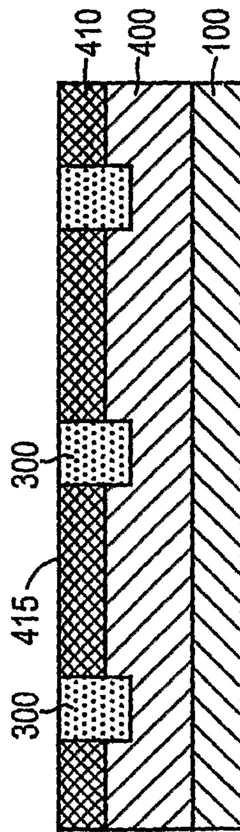

FIG. 4B

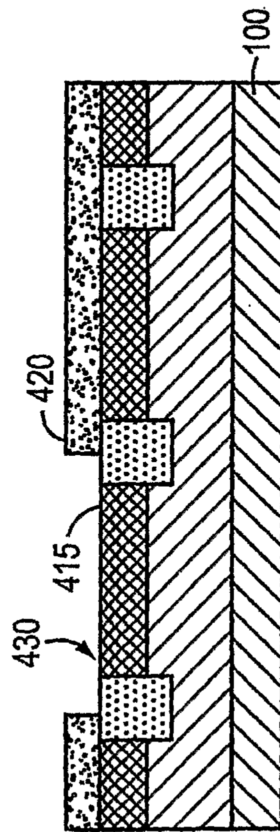

FIG. 4C

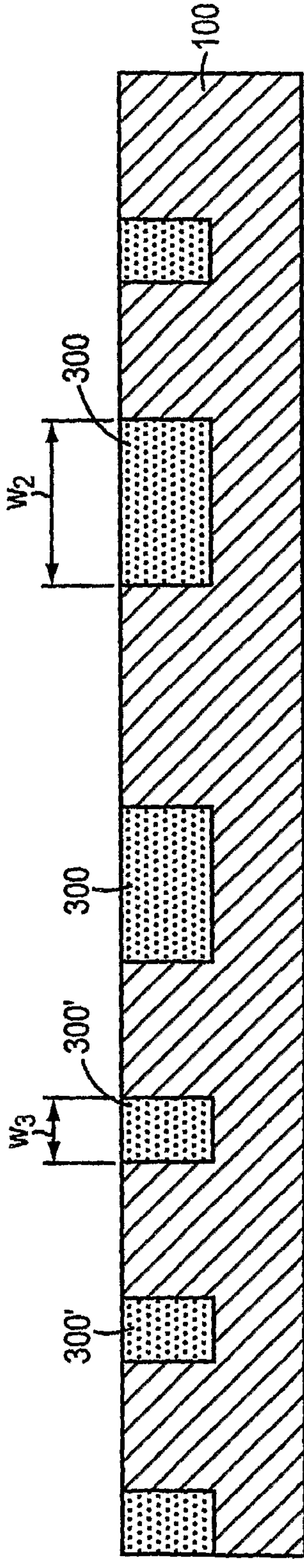

FIG. 5A

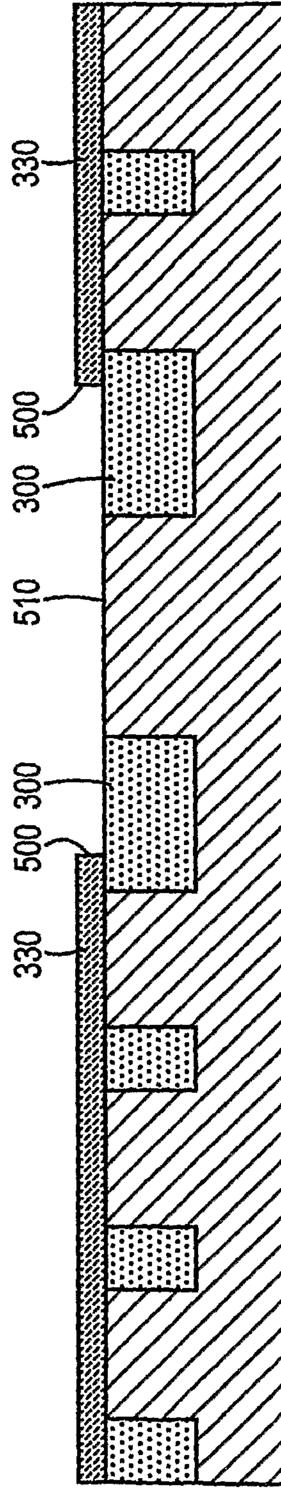

FIG. 5B

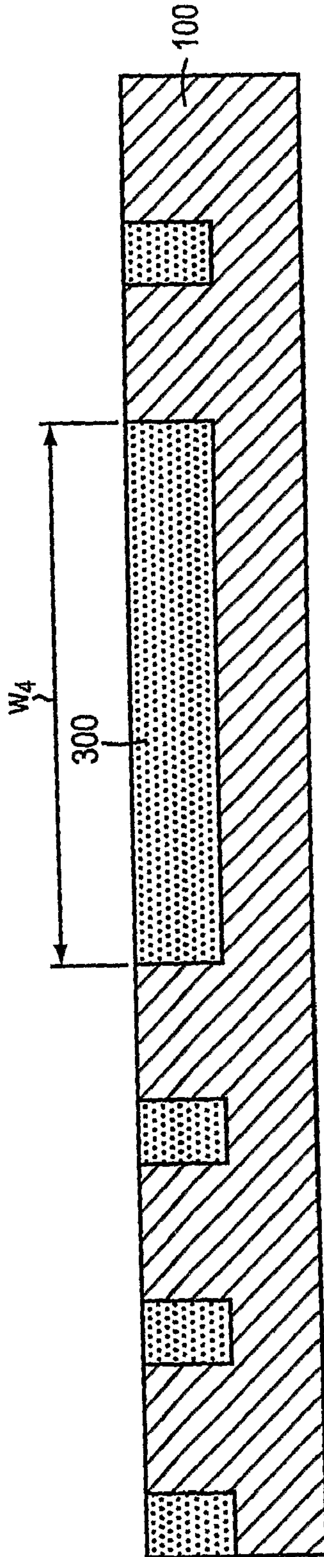

FIG. 6A

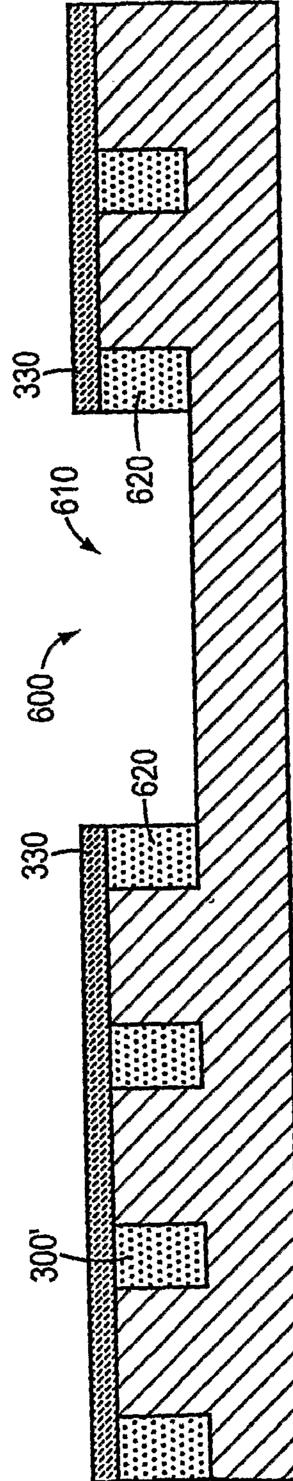

FIG. 6B

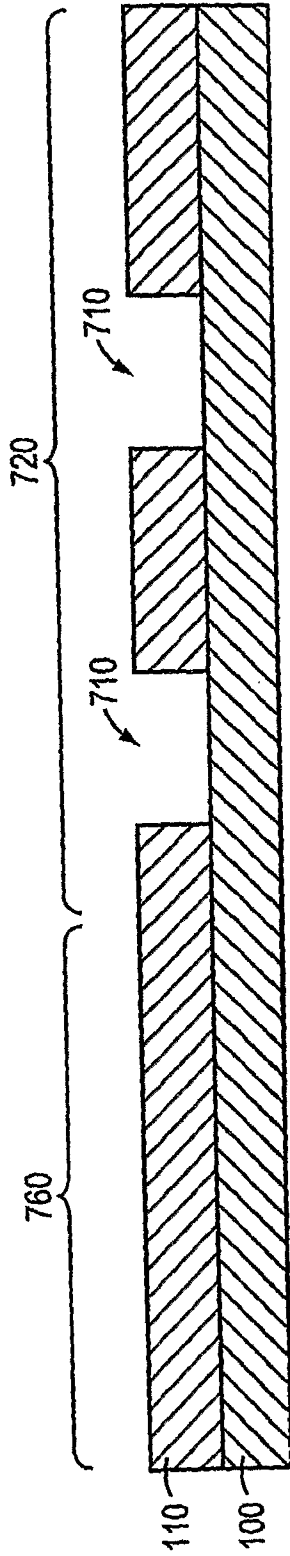

FIG. 7A

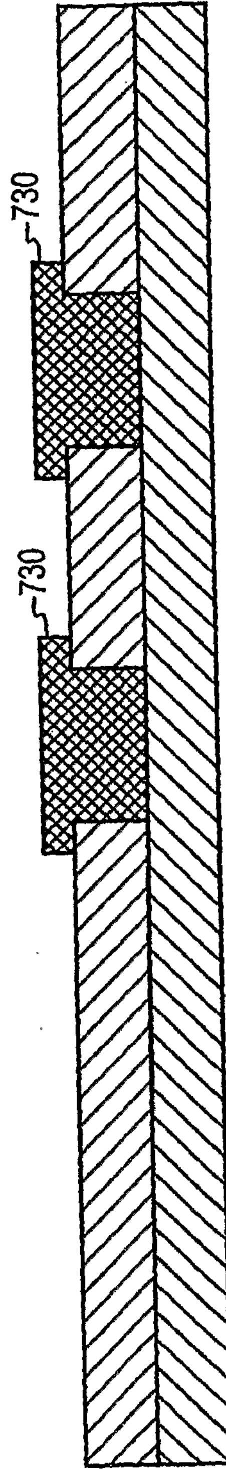

FIG. 7B

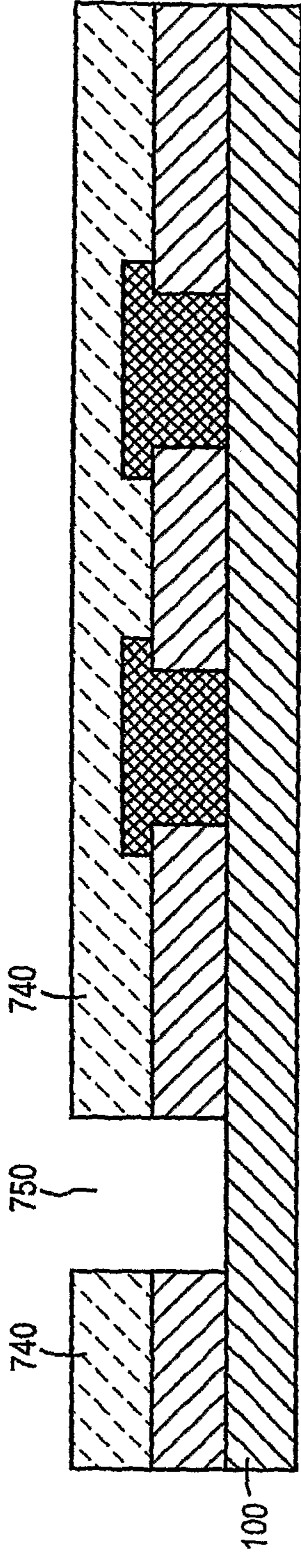

FIG. 7C

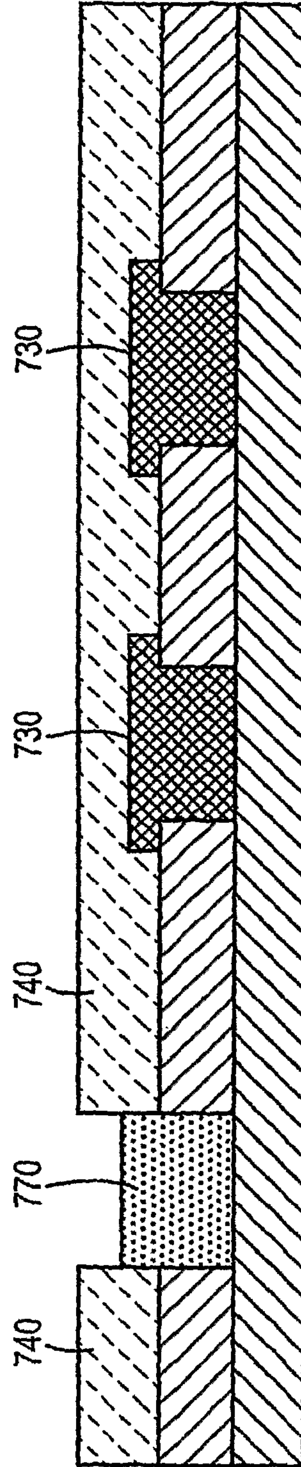

FIG. 7D

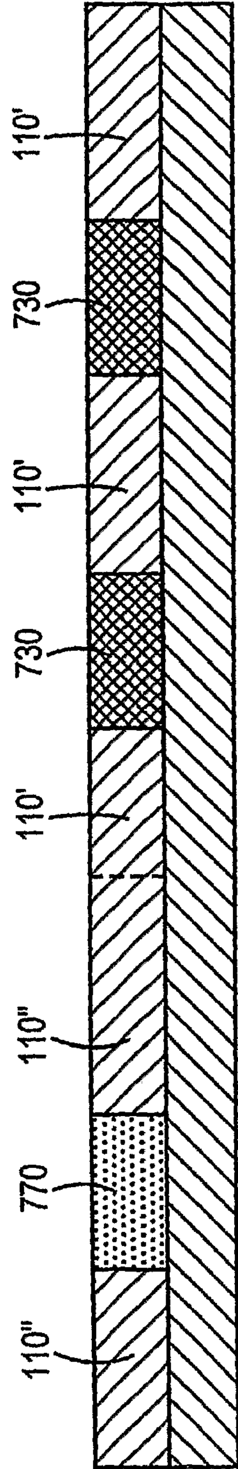

FIG. 7E

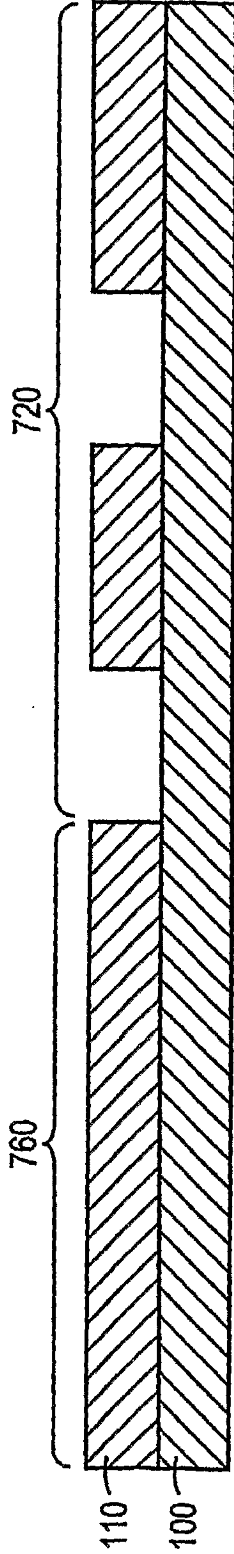

FIG. 8A

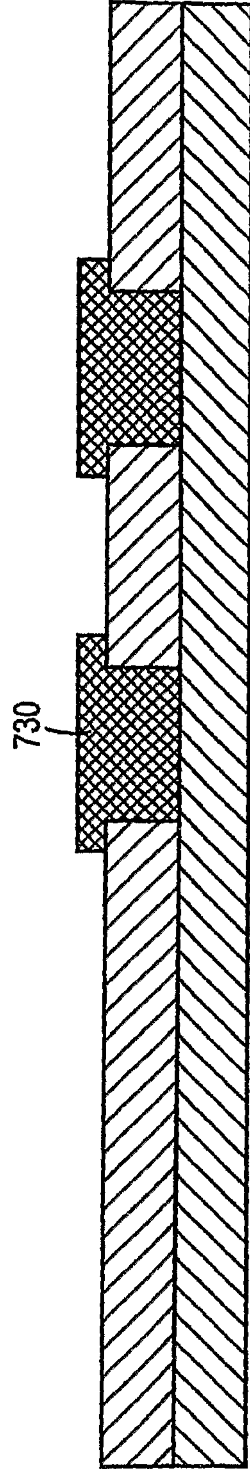

FIG. 8B

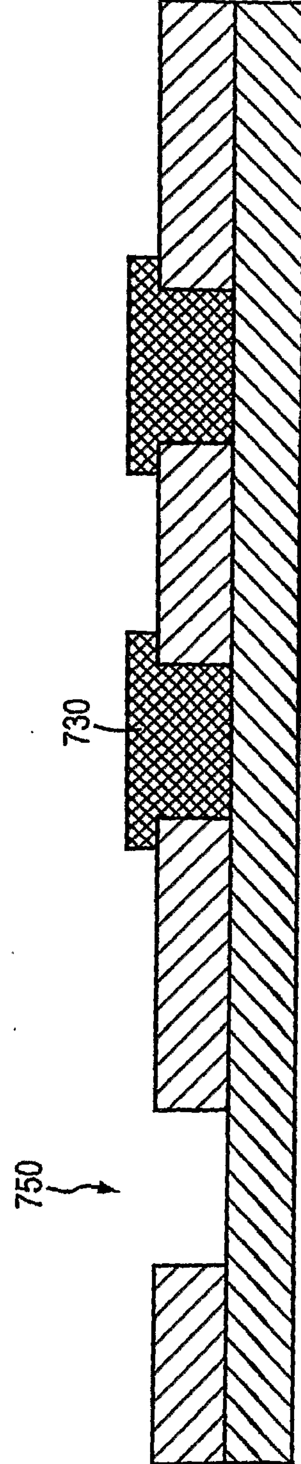

FIG. 8C

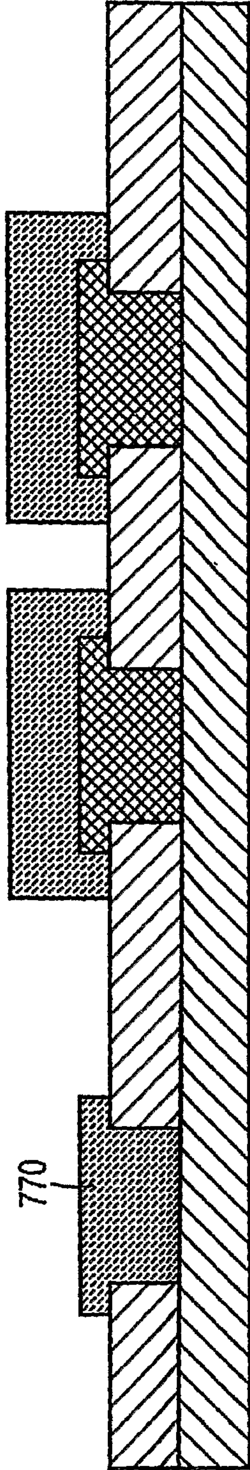

FIG. 8D

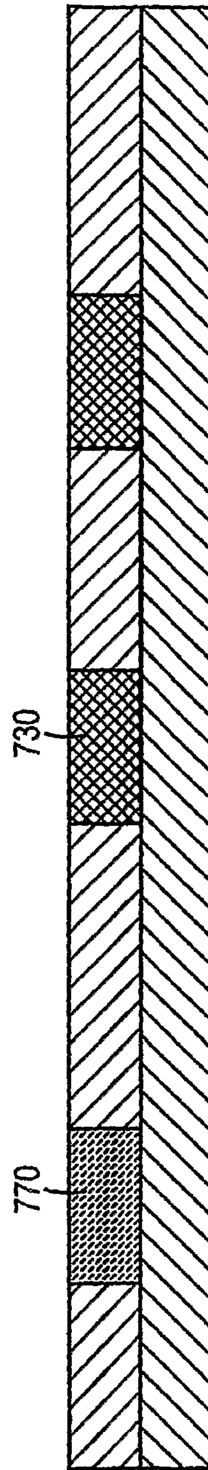

FIG. 8E

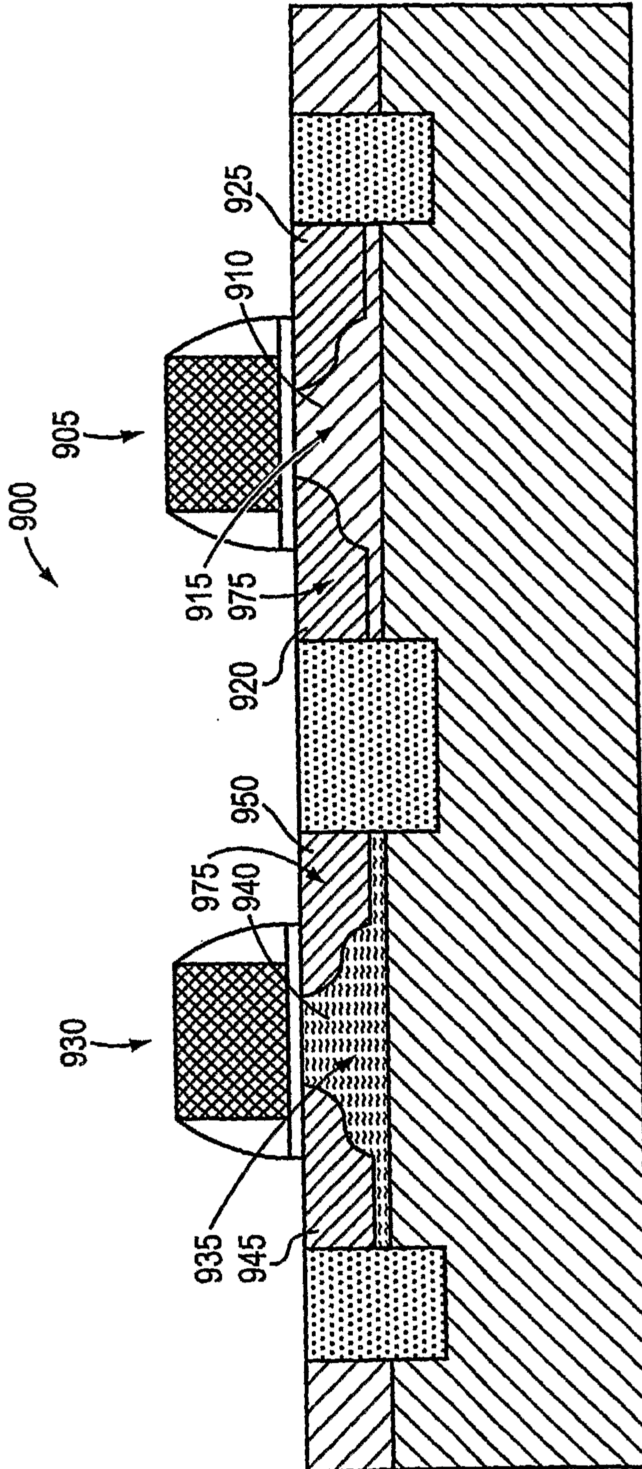

FIG. 9A

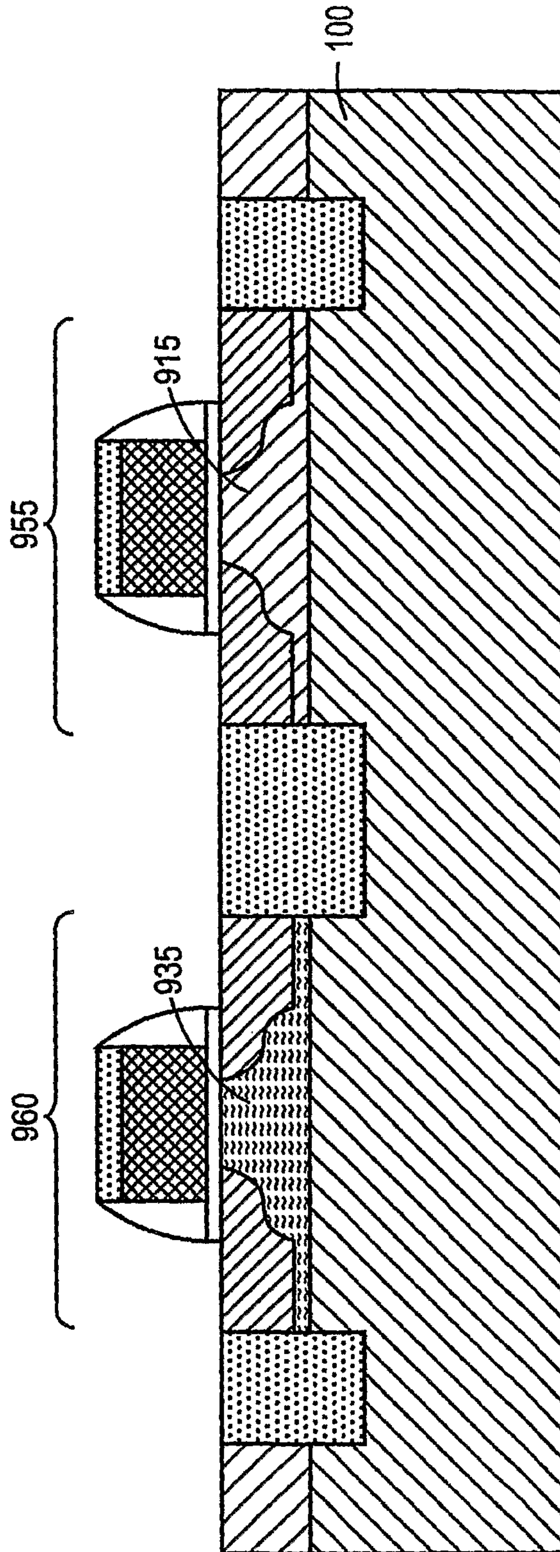

FIG. 9B

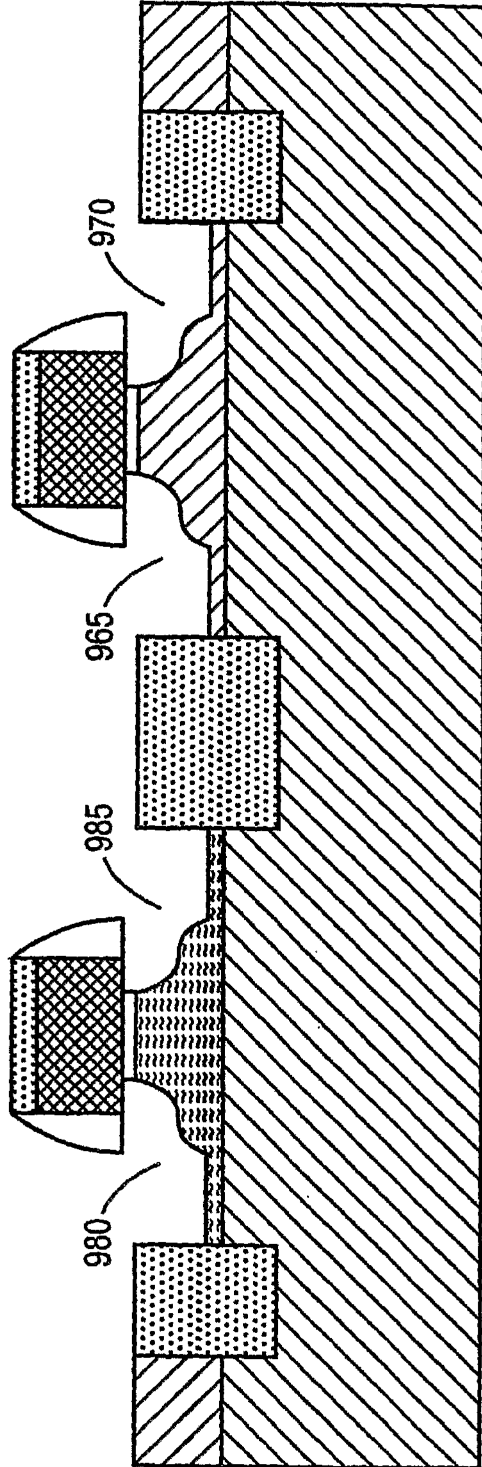

FIG. 9C

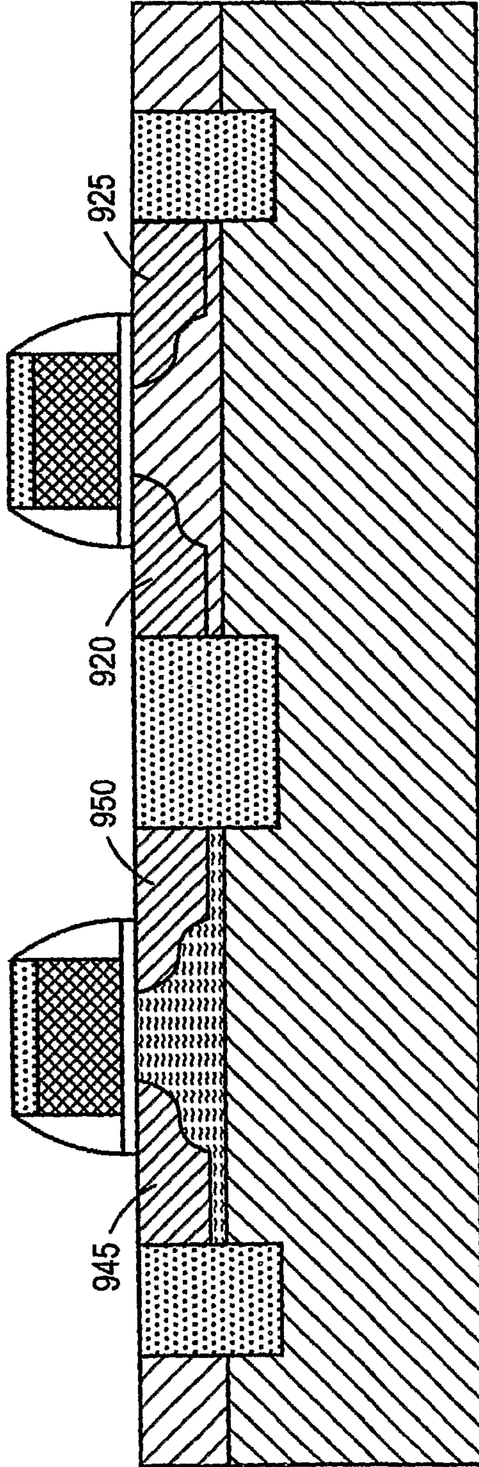

FIG. 9D

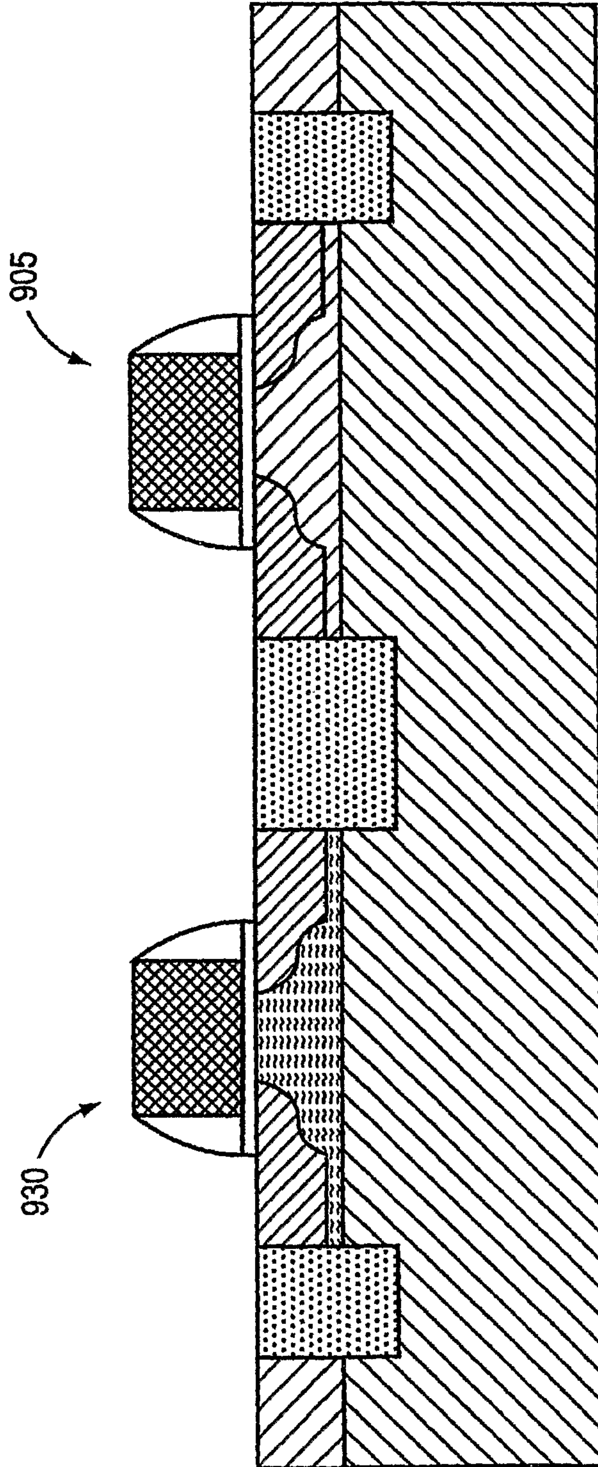

FIG. 9E

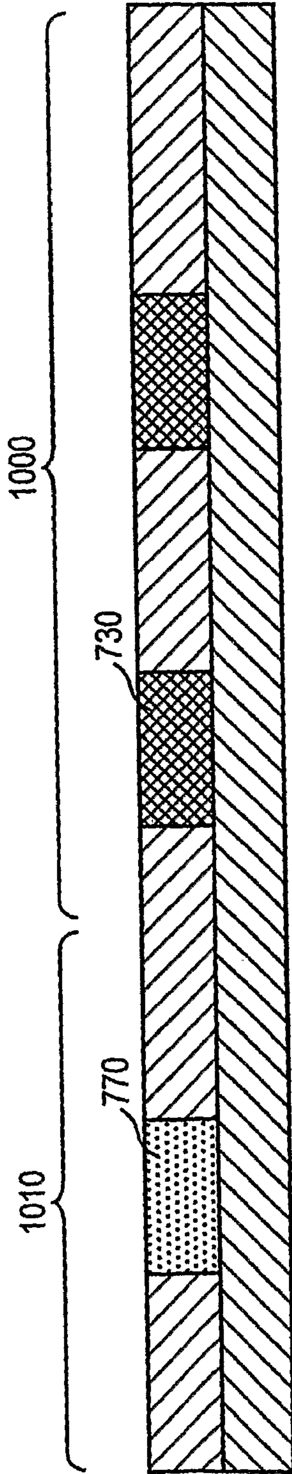

FIG. 10A

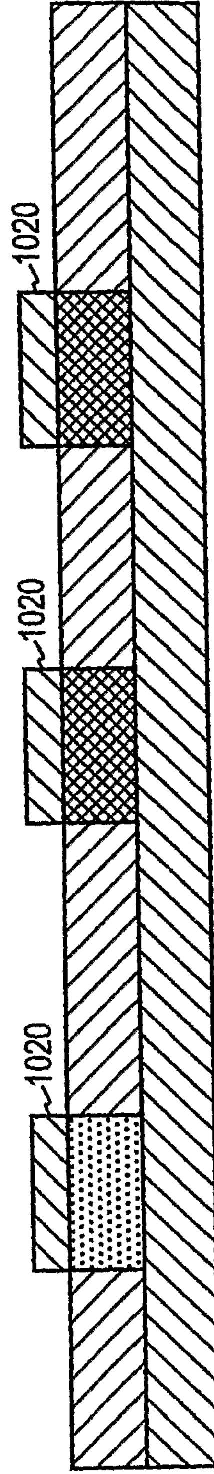

FIG. 10B

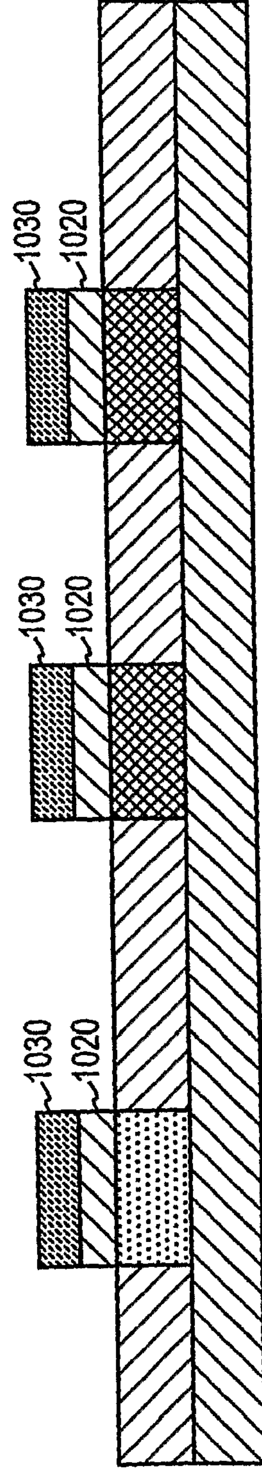

FIG. 10C

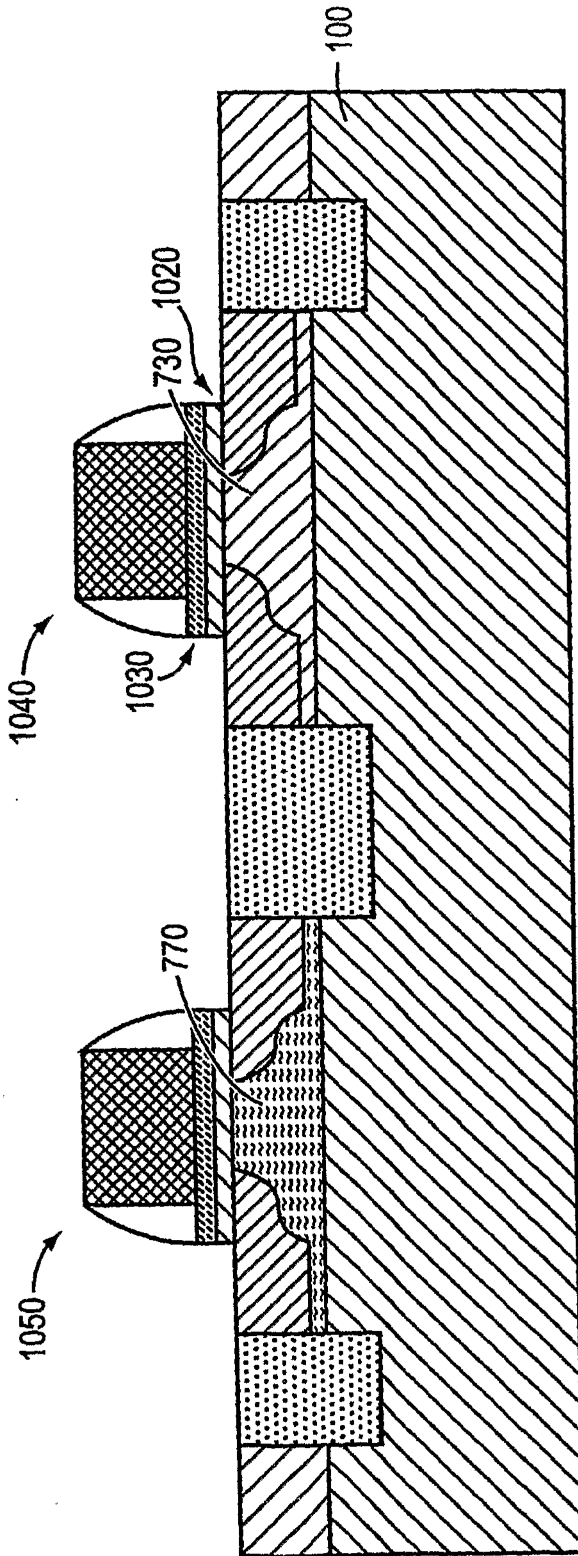

FIG. 10D

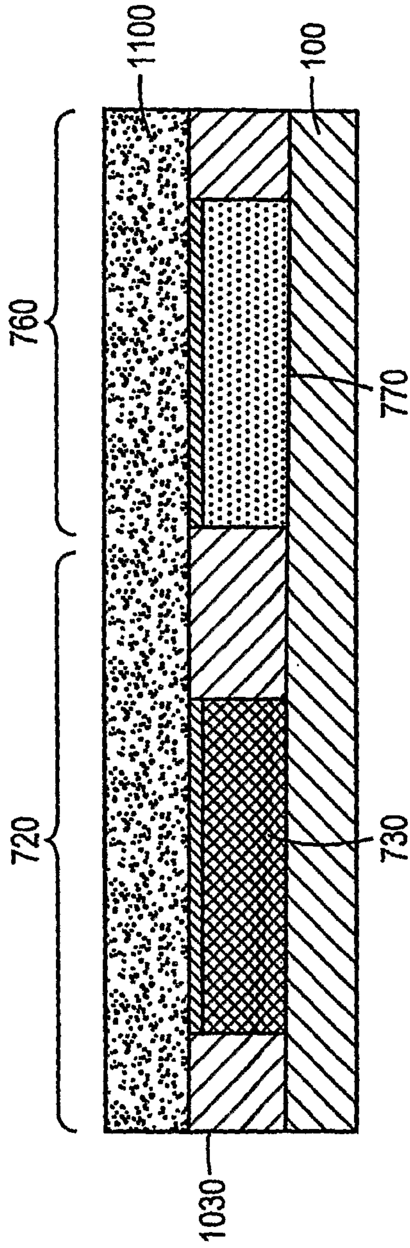

FIG. 11A

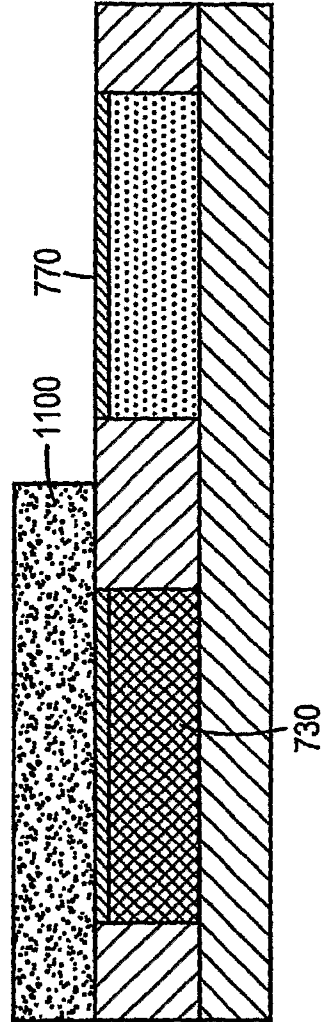

FIG. 11B

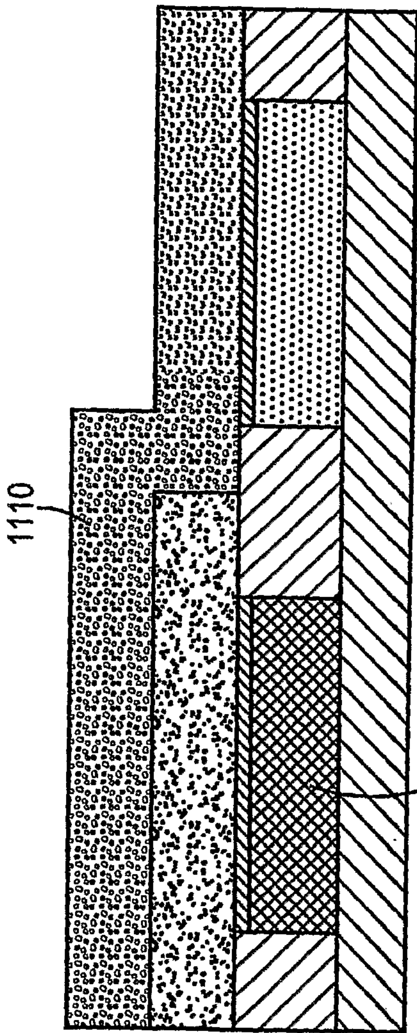

FIG. 11C

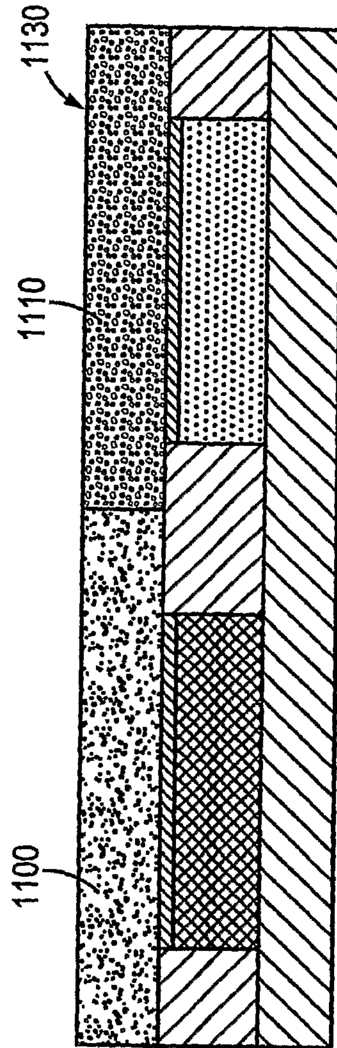

FIG. 11D

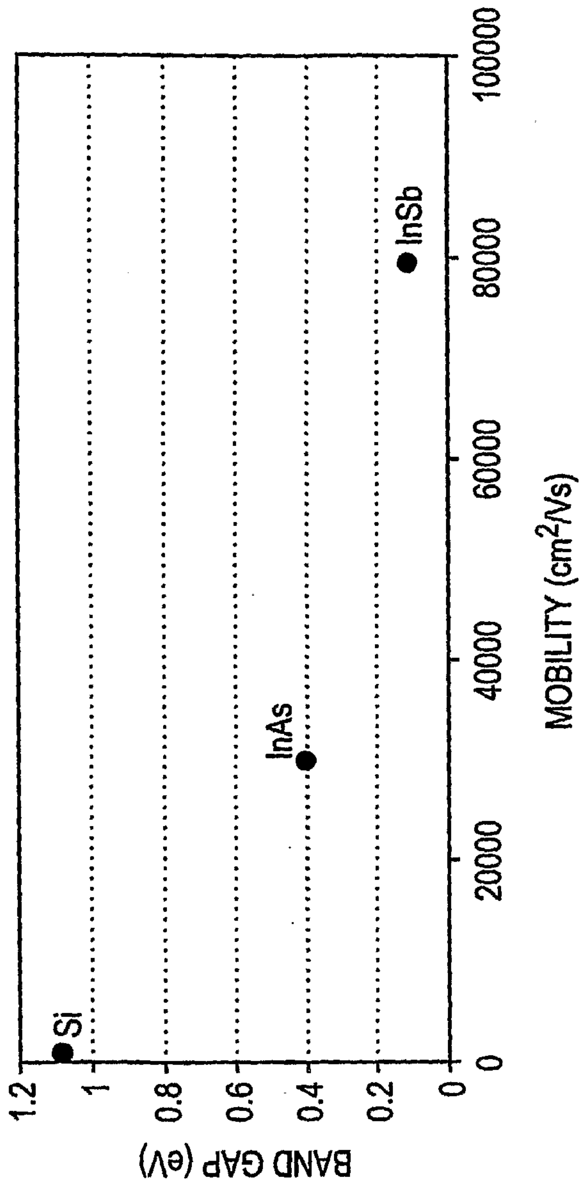

FIG. 12A

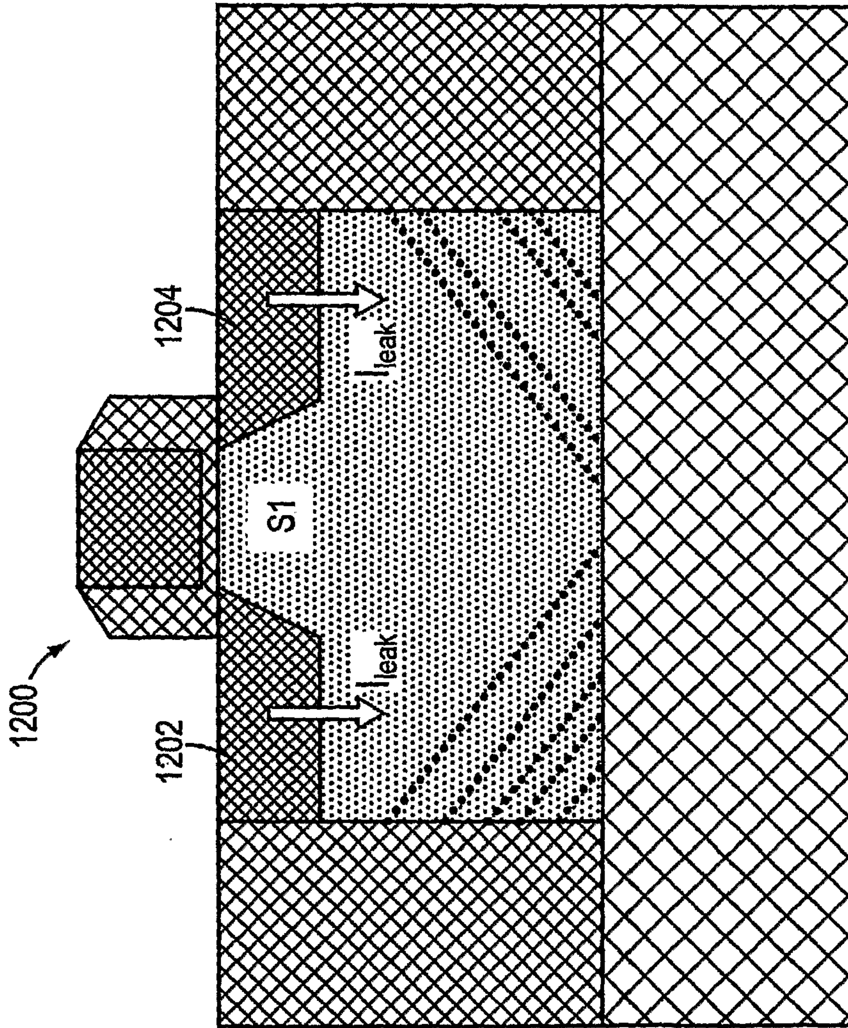

FIG. 12B

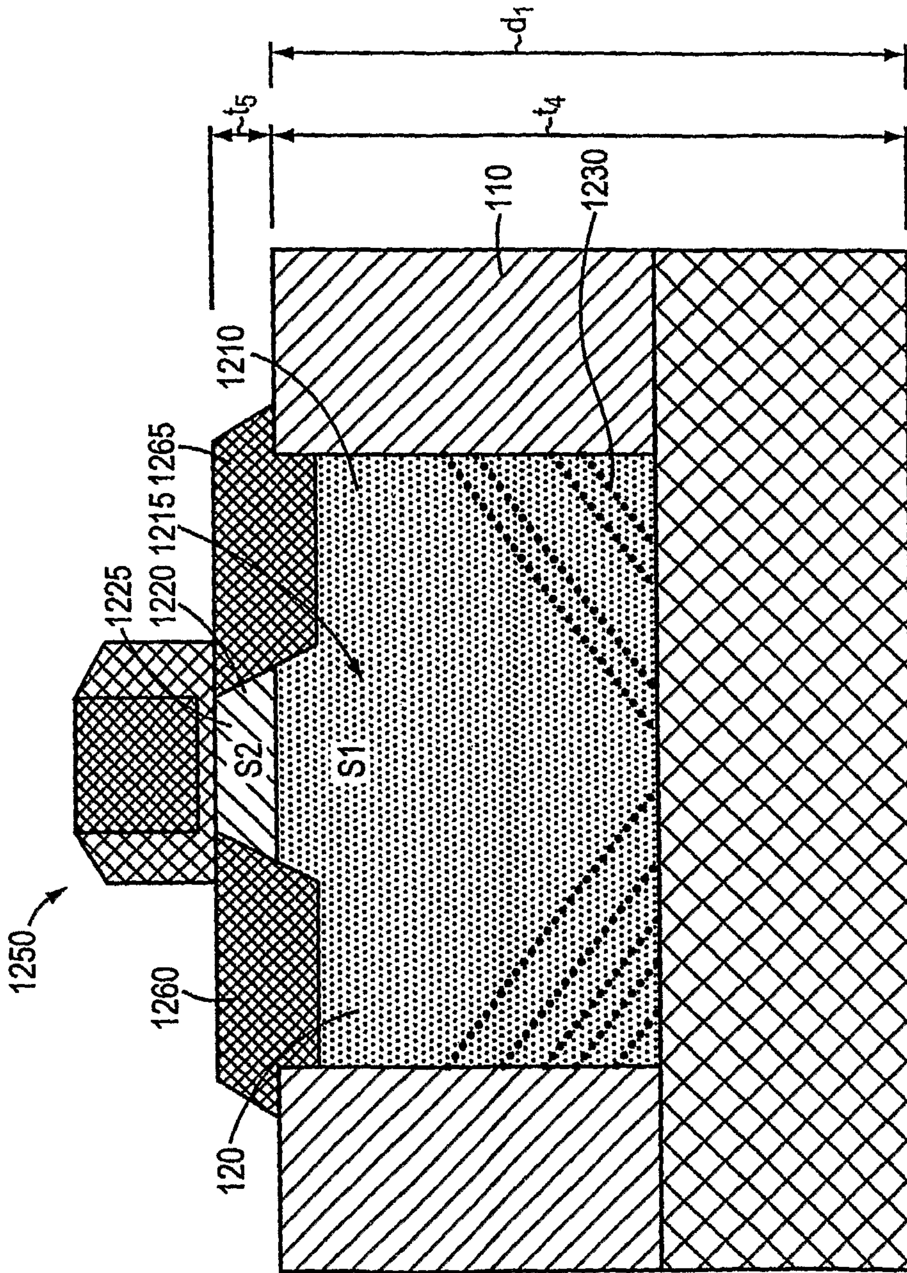

FIG. 12C

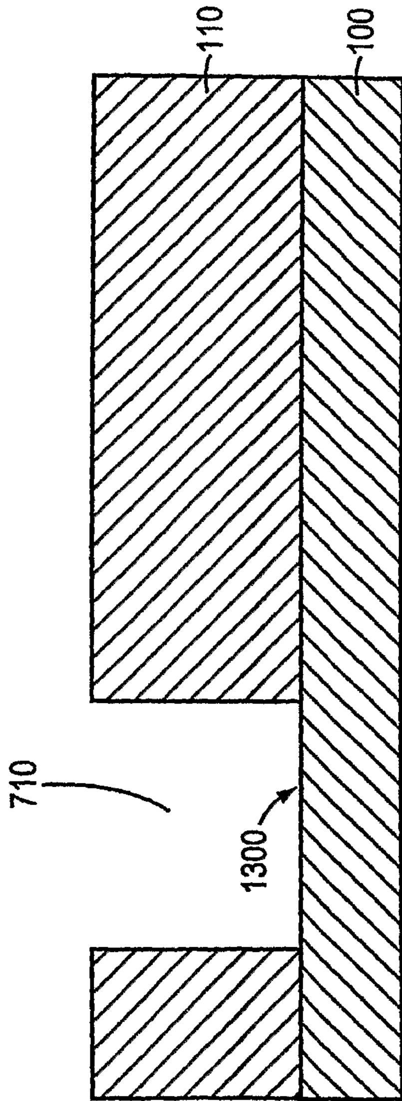

FIG. 13A

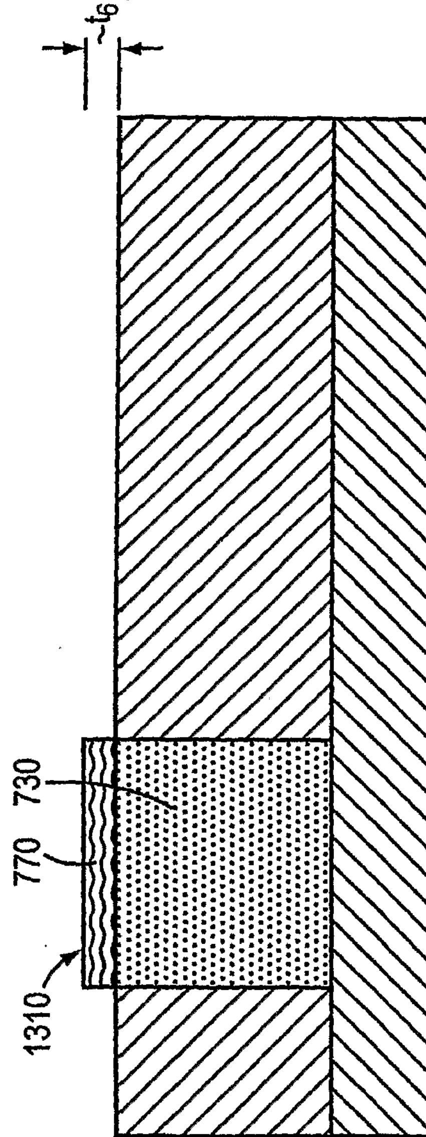

FIG. 13B

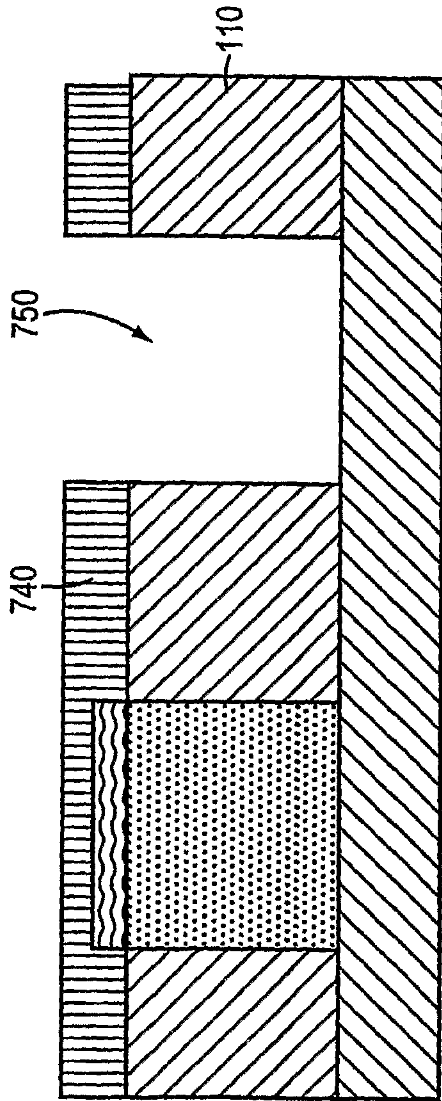

FIG. 13C

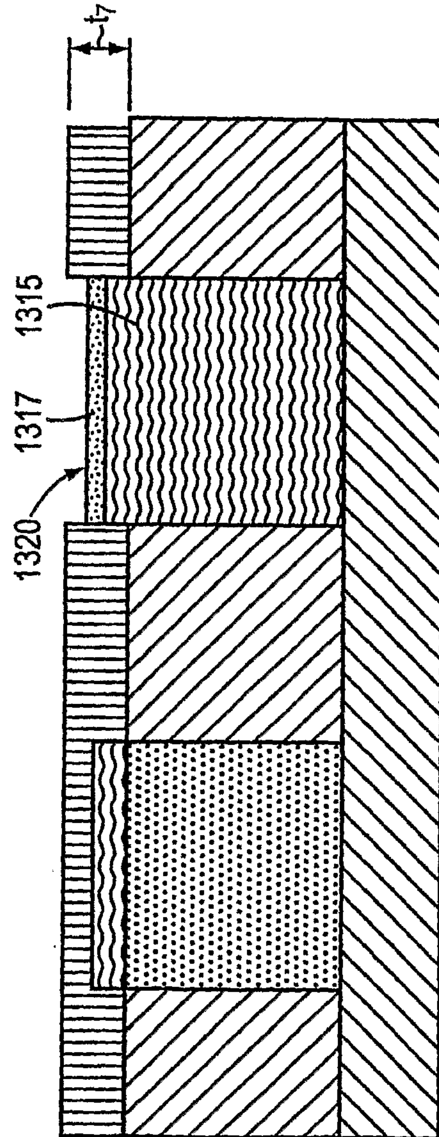

FIG. 13D

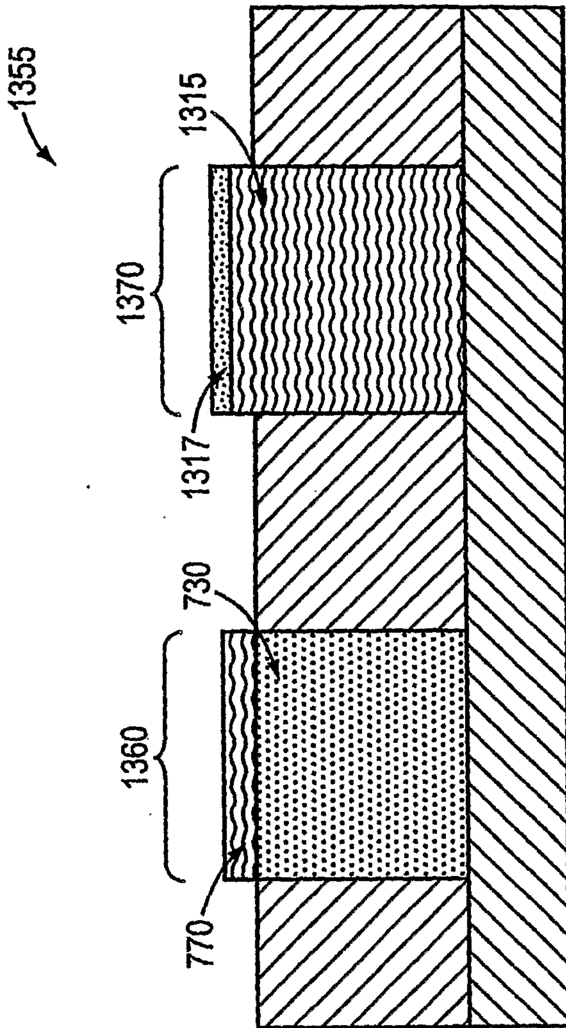

FIG. 13E

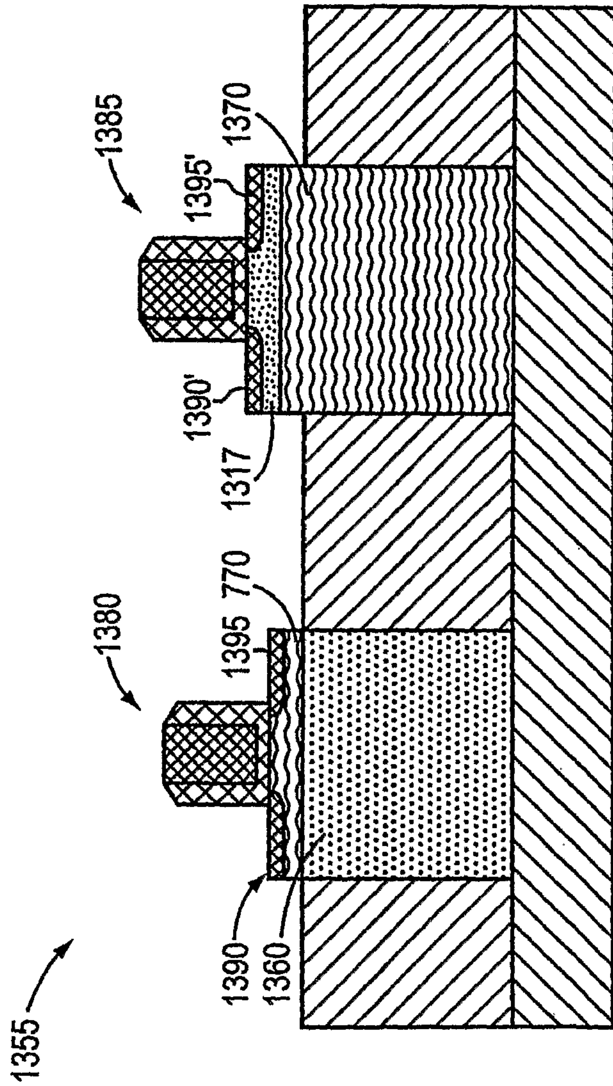

FIG. 13F

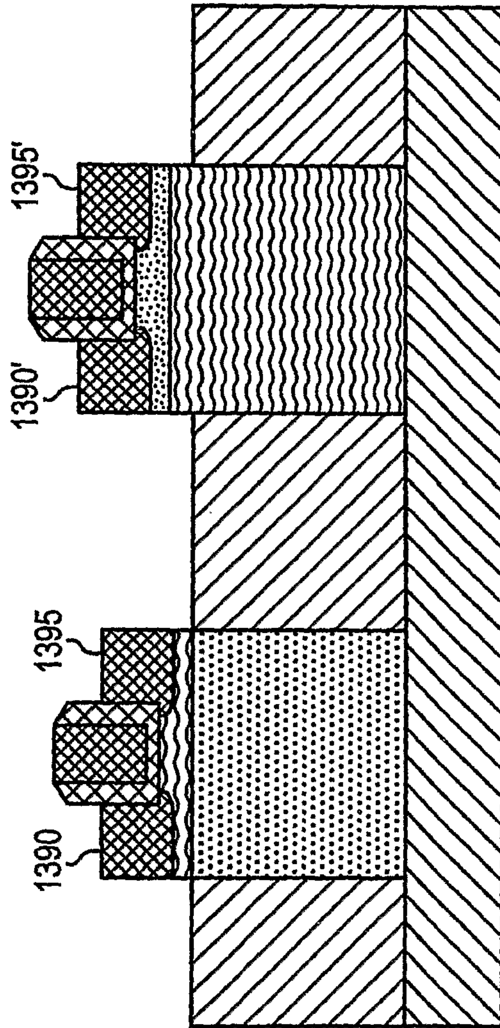

FIG. 13G