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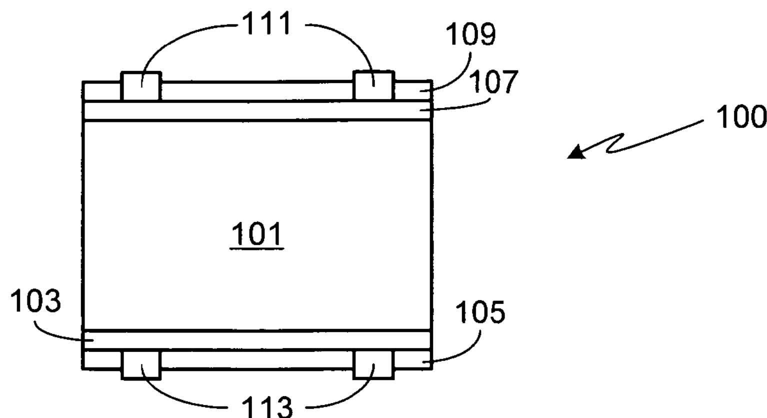


FIG. 1

(57) Abstract: A simplified manufacturing process and the resultant bifacial solar cell (BSC) are provided, the simplified manufacturing process reducing manufacturing costs. The BSC includes an active region (107) located on the front surface of the substrate (101), formed for example by a phosphorous diffusion step. The back surface includes a doped region (103), the doped region having the same conductivity as the substrate but with a higher doping level. Contact grids (111/113) are formed, for example by screen printing. Front junction isolation is accomplished using a laser scribe.

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# BIFACIAL SOLAR CELLS WITH BACK SURFACE DOPING

## FIELD OF THE INVENTION

[001] The present invention relates generally to solar cells and, in particular, to an improved structure and manufacturing process for a bifacial solar cell.

## BACKGROUND OF THE INVENTION

[002] Bifacial solar cells (BSC) may use any of a variety of different designs to achieve higher efficiencies than those typically obtained by a conventional, monofacial solar cell. One such design is shown in U.S. Patent No. 5,665,175 which discloses a BSC configuration with first and second active regions formed on the front and back surfaces of the BSC, respectively, the two regions separated by a distance λ. The distance λ allows a leakage current to flow between the first and second active regions, thus allowing a solar cell panel utilizing such bifacial cells to continue to operate even if one or more individual solar cells become shaded or defective.

[003] U.S. Patent No. 7,495,167 discloses an $n^+pp^+$ structure and a method of producing the same. In the disclosed structure, the $p^+$ layer, formed by boron diffusion, exhibits a lifetime close to that of the initial level of the substrate. In order to achieve this lifetime, the '167 patent teaches that after phosphorous gettering, the cell must be annealed at a temperature of 600° C or less for one hour or more. In order to retain the lifetime recovered by the phosphorous and low-temperature born gettering steps, the cell then undergoes a final heat treatment step in which the cell is fired at a temperature of around 700° C or less for one minute or less.

[004] U.S. Patent Application Publication No. 2005/0056312 discloses an alternative technique for achieving two or more p-n junctions in a single solar cell, the disclosed technique using transparent substrates (e.g., glass or quartz substrates). In one disclosed embodiment, the BSC includes two thin-film polycrystalline or amorphous cells formed on opposing sides of a transparent substrate. Due to the design of the cell, the high temperature deposition of the absorber layers can be completed before the low temperature deposition of the window layers, thus avoiding degradation or destruction of the p-n junctions.

[005] Although there are a variety of BSC designs and techniques for fabricating the same, these designs and techniques tend to be relatively complex, and thus expensive. Accordingly, what is needed is a solar cell design that achieves the benefits associated

with bifacial solar cells while retaining the manufacturing simplicity of a monofacial solar cell. The present invention provides such a design.

## SUMMARY OF THE INVENTION

[006] The present invention provides a simplified manufacturing process and the resultant bifacial solar cell (BSC), the simplified manufacturing process reducing manufacturing costs. In at least one embodiment of the invention, a manufacturing method is provided that is comprised of the steps of depositing a boron doped layer onto the back surface of a p-type silicon substrate, depositing a back surface dielectric over the boron doped layer, diffusing phosphorous onto the front surface of the silicon substrate to form an $n^+$ layer and a front surface junction, removing the phosphor-silicate glass formed during the diffusion step (e.g., by etching with HF), depositing a front surface passivation and AR dielectric layer onto the $n^+$ layer, applying front and back surface contact grids, firing the front and back surface contact grids, and isolating the front surface junction, for example using a laser scriber. The front and back surface contact grid firing steps may be performed simultaneously. Alternately, the back surface contact grid applying and firing steps may be performed prior to, or after, the front surface contact grid applying and firing steps. The boron doped layer depositing step can be formed by depositing a boron doped silicon dioxide layer using CVD, depositing a boron doped polysilicon layer using CVD, depositing a boron doped amorphous silicon layer using PE-CVD, spray coating a boric acid solution onto the back surface of the substrate, spray/wipe coating a boron-doped spin-on glass onto the back surface of the substrate, or by other means. The phosphorous diffusing step may be performed at a temperature in the range of 825° C to 890° C for a duration of approximately 10 to 20 minutes.

[007] In at least one embodiment of the invention, a bifacial solar cell (BSC) is provided that is comprised of a silicon substrate of a first conductivity type with a front surface active region of a second conductivity type and a back surface doped region of the first conductivity type, dielectric layers deposited on the front surface active region and on the back surface doped region, a front surface contact grid applied to the front surface passivation and AR dielectric layer which alloys through the front surface dielectric to the active region during firing, a back surface contact grid applied to the back surface dielectric layer which alloys through the back surface dielectric to the back surface doped region during firing, and a groove on the front surface of the silicon substrate, the groove isolating the front surface junction. The silicon substrate may be comprised of p-type

silicon, the active region may be comprised of $n^+$ material resulting from a phosphorous diffusion step, and the doped region may be comprised of a boron dopant. The silicon substrate may be comprised of n-type silicon, the active region may be comprised of $p^+$ material resulting from a boron diffusion step, and the doped region may be comprised of a phosphorous dopant.

[008] A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

[009] Fig. 1 illustrates a preferred embodiment of a BSC in accordance with the invention;

[0010] Fig. 2 illustrates the process flow for the BSC of Fig. 1; and

[0011] Fig. 3 illustrates an alternate process flow for the BSC of Fig. 1.

## DESCRIPTION OF THE SPECIFIC EMBODIMENTS

[0012] Fig. 1 illustrates a cross-sectional view of a preferred bifacial solar cell (BSC) structure fabricated in accordance with the procedure described in Figs. 2 and 3. Silicon substrate 101 may be of either p- or n-type. In the exemplary device and process illustrated in Figs. 1-3, a p-type substrate is used.

[0013] Initially, substrate 101 is prepared using any of a variety of well-known substrate preparatory processes (step 201). In general, during step 201 saw and handling induced damage is removed via an etching process, for example using a nitric and hydrofluoric (HF) acid mixture. After substrate preparation, the bottom surface of substrate 101 is doped, thereby forming a back surface doped region 103 (step 203). Region 103 is doped with the same doping type as substrate 101. Increasing the doping level of region 103, compared to substrate 101, lowers the contact resistance. Additionally, doped region 103 reduces back surface recombination and the effects of a positive potential in the back surface insulator to attract minority carriers to the back surface and thus away from the front surface collecting junction.

[0014] Region 103 can be formed using any of a variety of techniques. Exemplary techniques include, but are not limited to, chemical vapor deposition (CVD), plasma enhanced CVD (PE-CVD), spray coating, and spin coating. Accordingly, and assuming a p-type substrate, region 103 can be formed by depositing a boron doped

polysilicon layer using CVD; depositing a boron doped silicon dioxide or amorphous silicon layer using PE-CVD; spray/spin coating a boric acid solution or doped spin-on glass onto the back surface of substrate 101; or by other means.

[0015] After formation of region 103, a dielectric layer 105 is deposited on the back surface of substrate 101, specifically on top of doped region 103 as shown (step 205). Preferably layer 105 is comprised of either silicon nitride or silicon dioxide, preferably deposited at a temperature of 300° C to 400° C, and has a thickness of approximately 76 nanometers for silicon nitride or 100 nanometers for silicon dioxide. In an alternate embodiment, layer 105 is comprised of silicon oxynitride. In another alternate embodiment, layer 105 is comprised of a dielectric stack, for example 70 nanometers of silicon nitride on 10 nanometers of silicon dioxide or aluminum oxide.

[0016] After deposition of dielectric layer 105, phosphorous is diffused onto the front surface of substrate 101, creating $n^+$ layer 107 and a p-n junction at the interface of substrate 101 and $n^+$ layer 107 (step 207). Preferably $n^+$ layer 107 is formed using phosphoryl chloride ($POCl_3$), where the diffusion is performed at a diffusion temperature in the range of 825° C to 890° C, preferably at a temperature of approximately 850° C, for 10 to 20 minutes in a nitrogen atmosphere (step 207). It will be appreciated that during the phosphorous diffusion step 207, boron from region 103 is diffused into the back surface of substrate 101 to form a back surface field (BSF). The phosphor-silicate glass (PSG) formed during diffusion step 207 is then etched away, for example using a hydrofluoric (HF) etch at or near room temperature for 1 to 5 minutes (step 209). In the preferred embodiment, the front side junction has a depth of 0.3 to 0.6 microns and a surface doping concentration of about $8x10^{21}/cm^3$.

[0017] In step 211, a front surface passivation and anti-reflection (AR) dielectric layer 109 is deposited, layer 109 preferably being approximately 76 nanometers thick. In the exemplary embodiment, layer 109 is comprised of silicon nitride or silicon oxynitride. Preferably, layer 109 is deposited at a temperature of 300° C to 400° C.

[0018] After deposition of the dielectric layer 109, contact grids are applied to the front and back surfaces of BSC 100 (step 213), for example using a screen printing process. In the exemplary embodiment, front contact grid 111 is comprised of silver while back contact grid 113 is comprised of an aluminum-silver mixture. In the preferred embodiment, both the front and back contact grids are aligned and use the same contact size and spacing, with electrodes being approximately 100 microns wide, 15 microns

thick and spaced approximately 2.5 millimeters apart. In at least one alternate embodiment, the back contact grid uses a finer spacing in order to lessen resistance losses from lateral current flow in the substrate. Next, a contact firing step 213 is performed, preferably at a peak temperature of 750° C for 3 seconds in air. As a result of this process, contacts 111 alloy through passivation and AR dielectric coating 109 to $n^+$ layer 107. Similarly, contacts 113 alloy through dielectric coating 105 to layer 103. Lastly, the front junction is isolated, for example using a laser scriber to form a groove on the front cell surface around the periphery of the cell (step 217).

**[0019]** Fig. 3 illustrates an alternate process for fabricating cell 100. As illustrated, this process is identical to that shown in Fig. 2, except that the front surface and back surface contact grids are applied and fired separately, thereby allowing different firing conditions to be used for each grid. Preferably contact grid 113 is applied (step 301) and fired (step 303) first, followed by the application (step 305) and firing (step 307) of front contact grid 111.

**[0020]** As previously noted, an n-type substrate may also be used with the invention. In such an embodiment, an n-type dopant, such as phosphorous, is used for region 103 while a p-type material, such as boron, is diffused into the front surface to form the p-n junction at the interface of substrate 101 and diffused region 107.

**[0021]** As will be understood by those familiar with the art, the present invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. Accordingly, the disclosures and descriptions herein are intended to be illustrative, but not limiting, of the scope of the invention.

WHAT IS CLAIMED IS:

1. A method of fabricating a bifacial solar cell, the method comprising the steps of:

depositing a boron doped layer on a back surface of a p-type silicon substrate;

depositing a back surface dielectric onto said boron doped layer;

diffusing phosphorous onto a front surface of said silicon substrate to form an $n^+$ layer and a front surface junction;

removing a phosphor-silicate glass (PSG) formed during said phosphorous diffusing step;

depositing a front surface passivation and anti-reflection (AR) dielectric layer onto said $n^+$ layer;

applying printing a back surface contact grid;

applying printing a front surface contact grid;

firing said back surface contact grid;

firing said front surface contact grid; and

isolating said front surface junction.

2. The method of claim 1, wherein said step of applying said back surface contact grid further comprises the step of screen printing said back surface contact grid, and wherein said step of applying said front surface contact grid further comprises the step of screen printing said front surface contact grid.

3. The method of claim 1, wherein said front surface junction isolating step further comprises the step of forming a groove on the front surface of the BSC with a laser scriber.

4. The method of claim 1, wherein said steps of firing said back and front surface contact grids are performed simultaneously.

5. The method of claim 1, wherein said step of firing said back surface contact grid is performed prior to said step of applying said front surface contact grid.

6. The method of claim 1, wherein said boron doped layer depositing step further comprises the step of depositing a boron doped silicon dioxide layer using chemical vapor deposition.

7. The method of claim 1, wherein said boron doped layer depositing step further comprises the step of depositing a boron doped silicon layer using chemical vapor deposition.

8. The method of claim 1, wherein said boron doped layer depositing step further comprises the step of depositing a boron doped amorphous silicon layer using plasma enhanced chemical vapor deposition.

9. The method of claim 1, wherein said boron doped layer depositing step further comprises the step of spraying a boric acid solution onto said back surface of said silicon substrate.

10. The method of claim 1, wherein said boron doped layer depositing step further comprises the step of spraying a boron doped spin-on glass onto said back surface of said silicon substrate.

11. The method of claim 1, wherein said PSG removing step further comprises the step of etching said front surface with a hydrofluoric etch.

12. The method of claim 1, further comprising the step of selecting said dielectric from the group consisting of silicon nitride, silicon dioxide and silicon oxynitride.

13. The method of claim 1, wherein said step of depositing said back surface dielectric onto said boron doped layer further comprises the step of depositing a dielectric stack onto said boron doped layer.

14. The method of claim 12, further comprising the step of selecting materials for said dielectric stack from the group consisting of silicon nitride, silicon dioxide and aluminum oxide.

15. The method of claim 1, wherein said phosphorous diffusing step is performed at a temperature of approximately 850° C for a duration of approximately 10 to 20 minutes.

16. The method of claim 1, further comprising the step of selecting said front surface passivation and AR dielectric layer from the group consisting of silicon nitride and silicon oxynitride.

17. A bifacial solar cell, comprising:

a silicon substrate of a first conductivity type with a front surface and a back surface;

a doped region of said first conductivity type located on said back surface of said silicon substrate;

a dielectric layer deposited on said doped region;

an active region of a second conductivity type located on said front surface of said silicon substrate;

a passivation and AR dielectric layer deposited on said active region;

a first contact grid applied to said dielectric layer, said first contact grid comprised of a first metal, wherein after a firing step said first contact grid is alloyed through said dielectric layer to said doped region located on said back surface of said silicon substrate;

a second contact grid applied to said passivation and AR dielectric layer, said second contact grid comprised of a second metal, wherein after said firing step said second contact grid is alloyed through said passivation and AR dielectric layer to said active region; and

a groove on said front surface of said silicon substrate, said groove isolating a front surface p-n junction formed by said active region and said silicon substrate.

18. The bifacial solar cell of claim 17, wherein said silicon substrate is comprised of a p-type silicon, said active region is comprised of $n^+$ material resulting from a phosphorous diffusion step, and said doped region is comprised of a boron dopant.

19. The bifacial solar cell of claim 18, wherein said dielectric layer is comprised of a material selected from the group consisting of silicon nitride and silicon

dioxide, and wherein said passivation and AR dielectric layer silicon substrate is comprised of a material selected from the group consisting of silicon nitride and silicon oxynitride.

20. The bifacial solar cell of claim 17, wherein said silicon substrate is comprised of an n-type silicon, said active region is comprised of $p^+$ material resulting from a boron diffusion step, and said doped region is comprised of a phosphorous dopant.

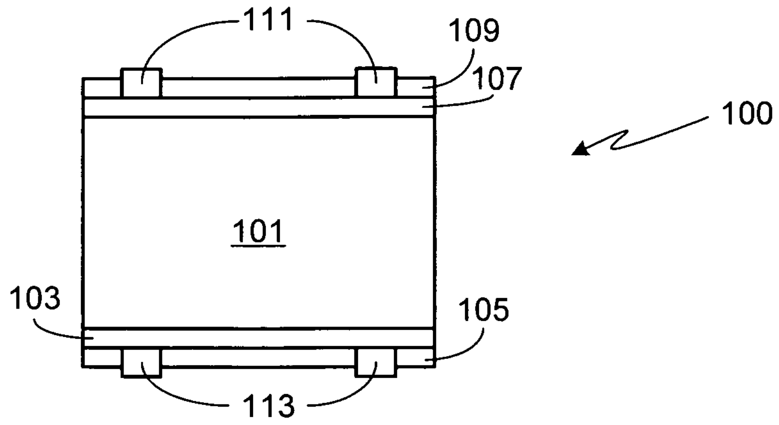


FIG. 1

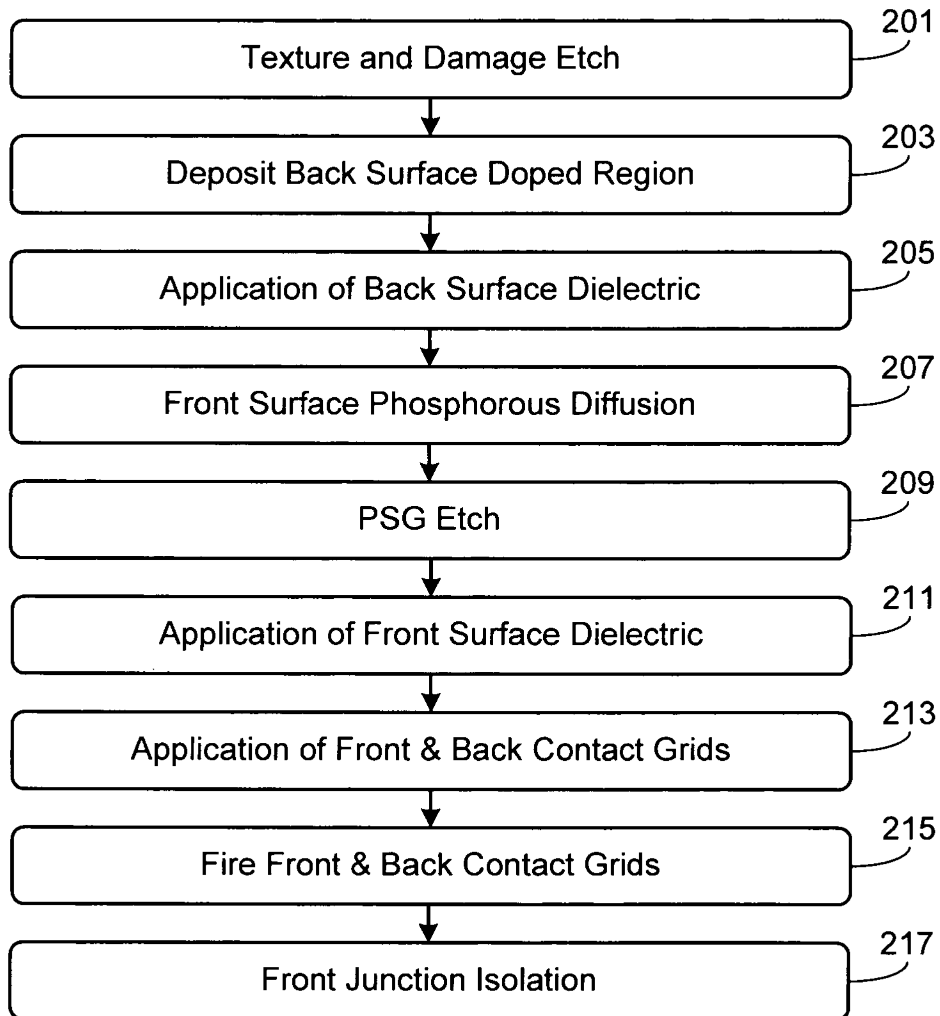


FIG. 2

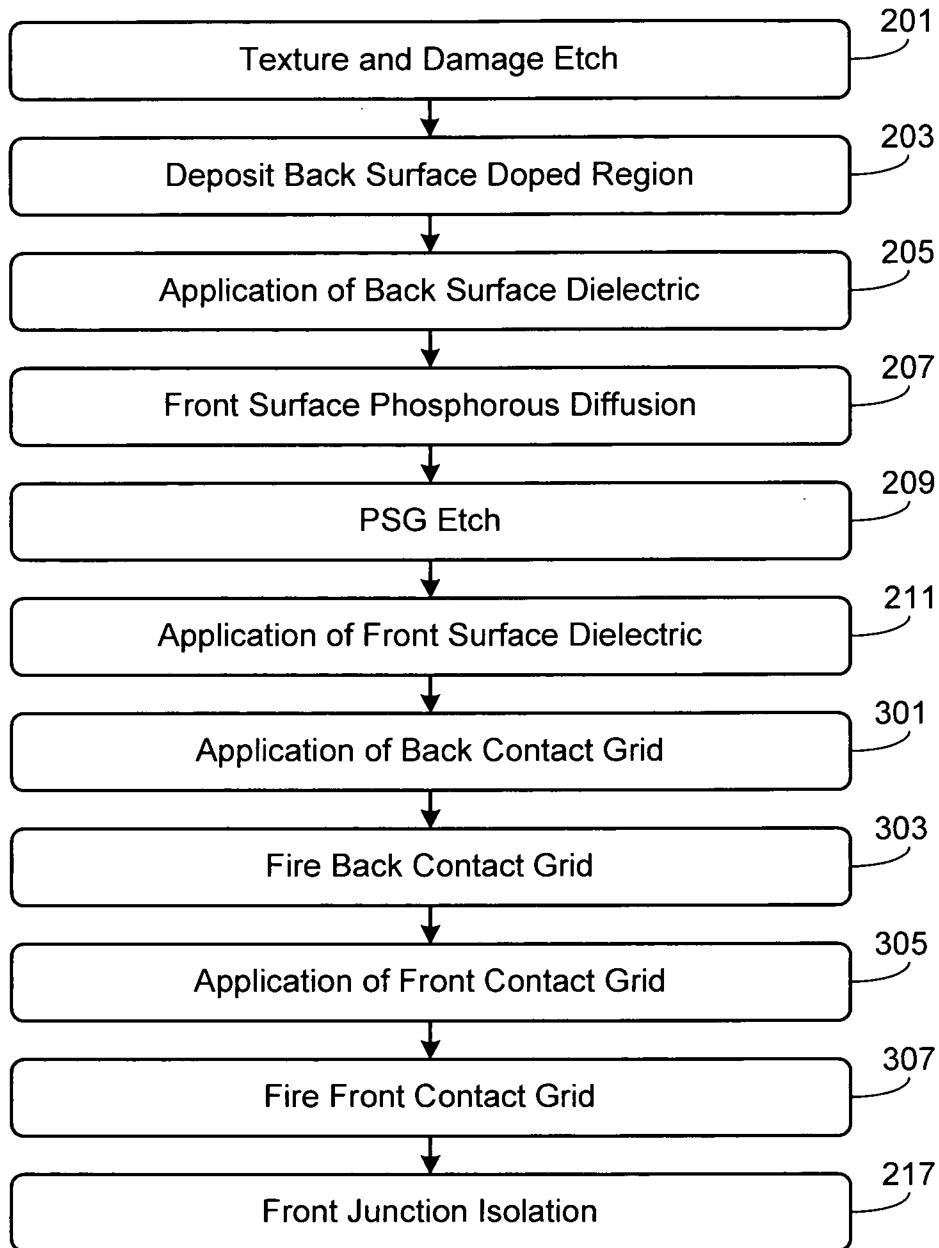


FIG. 3