

[54] REGISTER OVERFLOW WARNING DEVICE

[75] Inventors: **Shigeharu Bekki**, Yokohama;
Akihiro Yamataka, Funabashi;
Takashi Mikami; **Juji Kishimoto**,
 both of Tokyo, all of Japan

[73] Assignee: **Canon Kabushiki Kaisha**, Tokyo,
 Japan

[22] Filed: **Sept. 13, 1972**

[21] Appl. No.: **288,739**

[30] Foreign Application Priority Data

Sept. 17, 1971 Japan..... 46-84504
 Sept. 17, 1971 Japan..... 46-84505

[52] U.S. Cl..... **340/248 R**, 235/92 EA, 340/324 R,
 340/331, 340/253 B, 235/92 PL

[51] Int. Cl. **G08b 5/00**

[58] Field of Search 235/92 PL, 92 R, 92 MP,
 235/92 EA, 92 WT; 340/266, 324 R, 331,
 248 R, 253 B

[56] References Cited

UNITED STATES PATENTS

3,065,356 11/1962 Blake et al. 325/61.11 E
 3,478,248 11/1969 Ivec 340/331 X
 3,488,558 1/1970 Grafton..... 340/331

3,560,769 2/1971 Shimizu et al. 340/331 X
 3,585,629 6/1971 Baynard..... 340/331 X
 3,653,015 6/1970 Rock..... 235/92 PL X
 3,739,344 6/1973 Serracchioli et al. 340/172.5

OTHER PUBLICATIONS

Manual, DPM Series 200A, 200B, -Copies made in
 Group 230-Newport Labs., 1968, 5 sheets.

Schematic Diagram, 4000 Count DPM, Newport
 Labs., 7/71, Copies made in Group 230.

Brochure, Series 400A Digital Panel Meters, Newport
 Labs., 7/71, 2 sheet, Copies made in Group 230.

Primary Examiner—Thomas J. Sloyan

Attorney, Agent, or Firm—Fitzpatrick, Cella, Harper
 & Scinto

[57] ABSTRACT

In an electronic desk top calculator, when numerical
 informations such as entry information and arithmetic
 results overflow from the predetermined digits of the
 register, a plurality of digit indicator elements are con-
 trolled to be turned on and off simultaneously or in
 sequence in order to warn operator of the calculator
 of the overflow. For this purpose, the plurality of digit
 indicator elements are used as overflow indication
 lamps.

8 Claims, 4 Drawing Figures

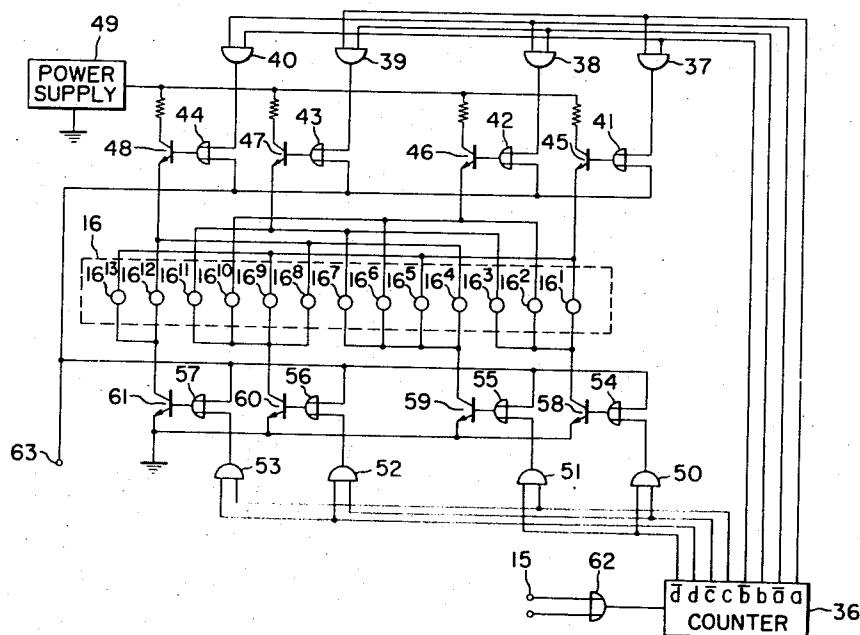


FIG. 1

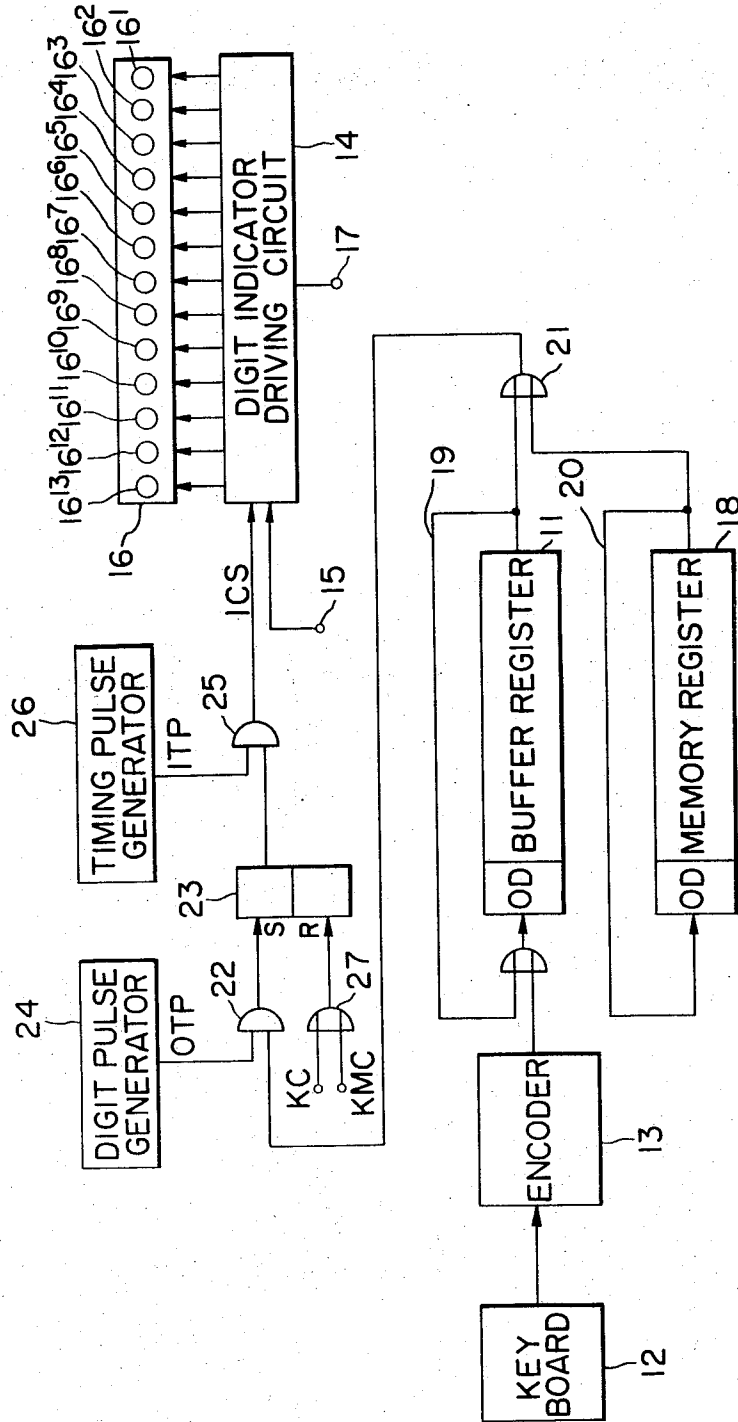


FIG. 2

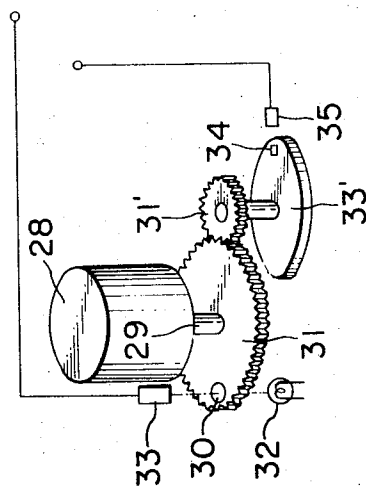
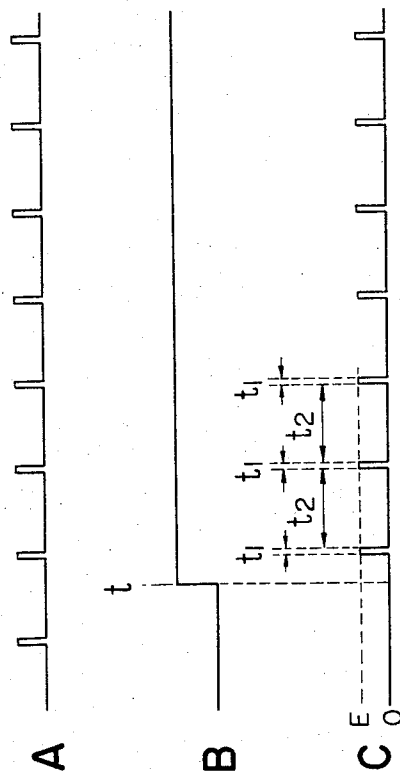
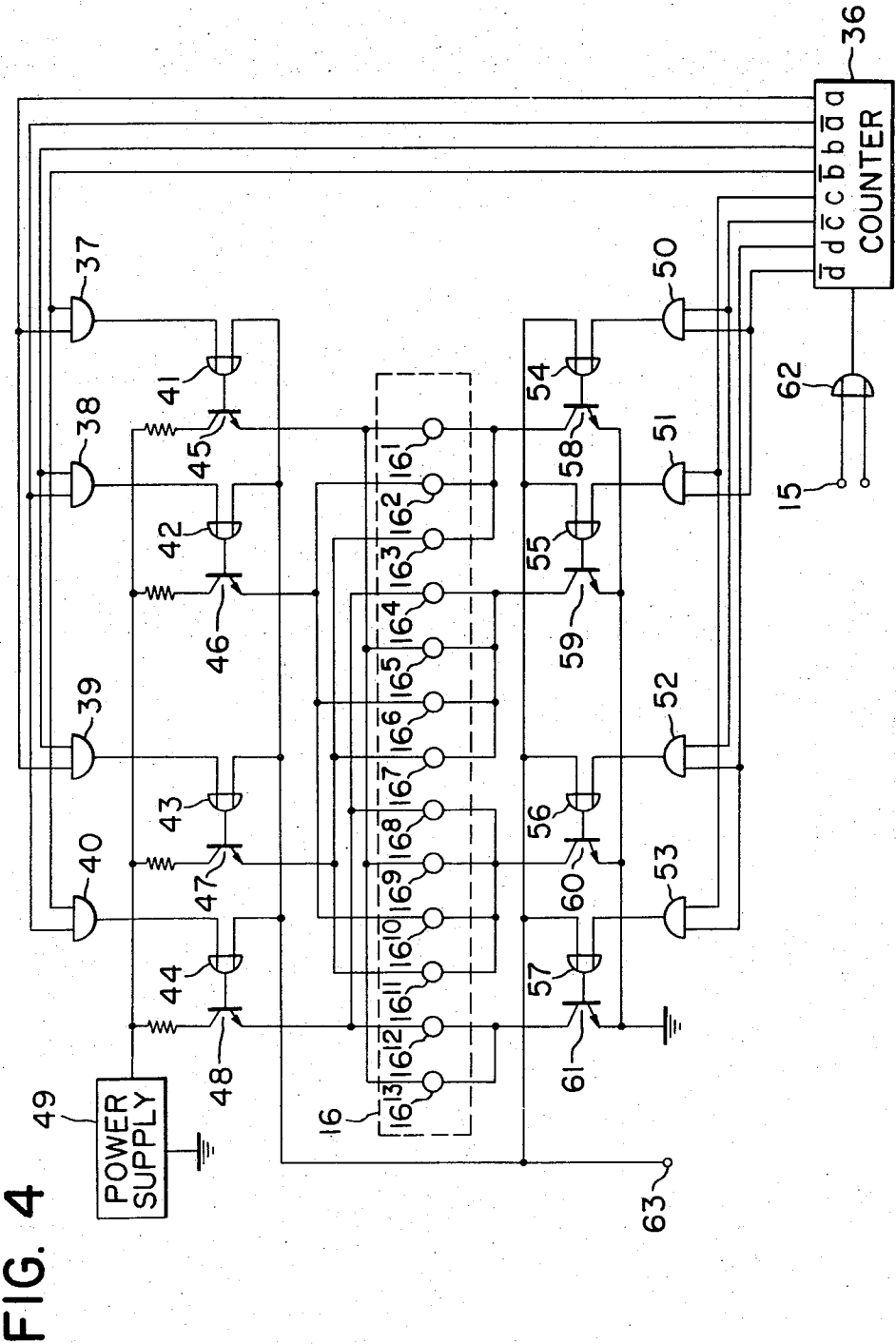


FIG. 3





REGISTER OVERFLOW WARNING DEVICE**BACKGROUND OF THE INVENTION****1. Field of the Invention**

This invention relates to an overflow warning device 5 for electronic calculators.

2. Description of the Prior Art

An electronic desk top calculator with a printer is constructed such that printing is not effected upon every registration of a numeral having a digit or digits. 10 Instead, numerical input information is stored in a register and, after completion of such registration, the information contained in the register is printed out all together upon depression of a function key.

When a numeral having a plurality of digits is registered, it is impossible during the course of registration to confirm what number of digits of a given numeral has been entered into the register. It is therefore common practice to provide a separate confirmation means for such registration of digits.

The confirmation means for this registration of digit comprises digit indicator elements such as lamps whose number corresponds to possible registration digits. These elements are provided in a row in a given portion of the calculator; and the digit indicator element corresponding to digit numbers previously registered turns on with each new registration of a digit.

Additionally, an overflow warning lamp is provided to indicate the overflow of entry information, arithmetic result and the like from the predetermined digits of the register; and this lamp turns on at the time of overflow.

However, a single lamp is normally used as an overflow lamp; and it is difficult to attract the operator's attention thereto, with the result that the operator may often overlook the overflow condition even when the overflow lamp is turned on. This not only interferes with operation but also causes the calculation to miss.

SUMMARY OF THE INVENTION

An object of the invention is to remove the drawbacks inherent in the prior art and to arouse operator's attention by using the digit indicator itself as an overflow lamp and by driving the digit indicators at the time of overflow in a manner different from that the manner in which they are driven during usual registration times.

It is another object of this invention to provide a more noticeable warning to the operator of an overflow condition by flashing the digit indicator lamp instead of keeping them turned on during the overflow period.

Still another object of this invention is to provide a more noticeable warning to the operator of an overflow condition by turning on and off a plurality of digit indicator lamps in sequence at the time of overflow.

A still further object of this invention is to provide a more noticeable warning to the operator of an overflow condition by simultaneously flashing all of a plurality of the digit indicator lamps at the time of overflow.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an overflow warning device according to the present invention;

FIG. 2 is a schematic view illustrating an indication timing pulse generator used in the device of FIG. 1;

FIG. 3 is a chart showing signal waveforms in which A represent and indication timing pulse signal, B repre-

sents an overflow signal and C represents an indication control signal; and

FIG. 4 is a circuit diagram showing in more detail a digit indicator driving circuit and an indicator used in the device of FIG. 1.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The present invention will be described with reference to the embodiment shown in the drawings. Referring particularly to FIG. 1 showing the block diagram of the overflow warning device according to the present invention, the reference numeral 11 designates a buffer register capable of storing information of, for example, 13 digits. Numerical information is supplied to a key board 12 and is converted to a binary code in an encoder 13 and then is entered in sequence into the buffer register 11 where it is stored. Each single pulse produced by operation of a keyboard entry key is at the same time applied to a terminal 15 of a digit indicator driving circuit 14; and the single pulse produced by the key board for a digit number to be registered, is counted in the digit indicator driving circuit 14. A indicator 16 having a digit number capacity equal to that of the buffer register 11 is also provided. The digit indicator 16 includes digit indicator elements 16¹ - 16¹³, and the particular elements corresponding to the counted digit number are selectively energized. The digit indicator driving circuit 14 is arranged such that resetting is effected by applying a reset signal to a reset terminal 17 by means of a function key; and the energization of the digit indicator elements 16¹ to 16¹³ which have been selectively energized is stopped, thereby extinguishing the indication of the indicator 16.

Accordingly, if the number of three digits, for example, 123 is supplied from the key board 12, the digit indicator element 16¹ will light upon entry of the first digit "1", the digit indicator element 16² will light upon entry of the second digit "2" and the digit indicator element 16³ will light upon entry of the digit "3." It is to be noted that such lighting condition of the digit indicator elements is maintained until the following entry of the digit or operation of a function key. The numerical information thus supplied from the key board 12 is stored successively in the buffer register 11; and the operation of function key (that is operation of pushing the function key of $\div$) which follows such entry prints out the information stored in the buffer register (mechanism thereof is not shown in the drawing). At the same time, a reset signal is applied to the reset terminal 17 of said digit indicator driving circuit 14 by depression of the function key thereby extinguishing the indication of the digit indicator.

The buffer register 11, and a memory register 18, each has a 14 digit memory capacity which includes 13 digits plus a single overflow digit OD (a decimal point digit and sign digit are actually included but are omitted for simplicity). The registers 11 and 18 retain their stored information by means of recirculating loops 19 and 20; and they read out a part of the information via an OR gate 21. The output of the OR gate 21 is applied to a set input of a flip-flop 23 through an AND gate 22 while an overflow timing pulse (OTP) from indication timing pulse generator 24 is applied to the AND gate 22 as another AND input. Thus overflow is detected by means of the AND gate 22.

It may be assumed that either of the registers 11 and 18 will overflow. When this occurs, digit information will exist at the 14th digit of the overflowed register; and the digit pulse corresponding to this 14th digit (which is a signal with a pulse width corresponding to the one digit period starting when the 14th digit comes to LSD of the register and ending when the same is read out) is applied to the AND gate 22 along with an overflow timing pulse (OTP) from the digit pulse generator circuit 24. This enables an output to be delivered from the AND gate 22 only when there is information other than zero in the overflow digit.

The set output of the flip-flop 23 is further applied to the digit indicator driving circuit 14 through an AND gate 25 while indication timing pulses (ITP) from an indication timing pulse generator 26 are continuously applied to another input terminal of the AND gate 25. Therefore, an output can be obtained from the AND gate 25 whenever the indication timing pulse is of high level. It will be possible to control the intermittent lighting of the digit indicator elements 16¹ to 16¹³ by applying the output of the AND gate 25 to the digit indicator driving circuit 14 as an indication control signal.

Accordingly, the operator recognizes the overflow of the calculator and pushes a key to produce a clear signal KC or a clear memory signal KMC. Such clear signal, however, is applied to the reset terminal of the flip-flop 23 through an OR gate 27 to reset the flip-flop so that an indication control signal cannot be obtained from the AND gate 25; and the energization of the digit indicator 16¹ to 16¹³ is thereby stopped.

It should be noted that while two kinds of registers 11 and 18 are used in the embodiment of FIG. 1, a read out output may be applied to the OR gate 21 even in the case where other registers than those shown in the drawings are used.

It is necessary that the timing pulse delivered from the indication timing pulse generator 26 be of rather low frequency, because lighting of the digit indicator cannot be visually confirmed for timing pulses having considerably high frequency. This may be achieved, for example, in the device shown in FIG. 2.

In FIG. 2, reference numeral 28 designates a motor for driving a printer of an electric desk top calculator; and the motor always rotates during usage time of the calculator. Fixedly mounted on a rotary shaft 29 of the motor 28 is a gear 31 provided with a hole 30. A light emissive element 32, such as lamp, and a sensor 33. During the rotation of the motor 28, pulses of a fixed rate can be obtained from the sensor 33 as shown in FIG. 3A. It is noted that the frequency of the pulses is determined by rotational speed of the motor. With the rotation of the motor being three revolutions per second, for example, a pulse whose period is in the order of 300 m.sec. can be obtained. If it is desired to have higher frequency pulses, it is suggested that the holes of the gear 31 should be increased alternately, a smaller gear 31' engaging with the gear 31 may be provided along with a disc 33' arranged coaxially with the gear 31' to rotate therewith. A magnet 34 is positioned on the disc 33' and a magnetic sensor 35 is fixedly positioned to sense the rotating magnet 34. Thus pulses of higher frequency than the sensor above referred to can be obtained.

Explanation will be made in more detail of an indication control signal (ICS) coming from the AND gate

25. The pulse signal as shown in FIG. 3A is applied to the AND gate 25 continuously from the indication timing pulse generator 26; and the signal as shown in FIG. 3B is also applied to the AND gate 25 from the set output of the flip-flop 23 (it is set at t). The output of the AND gate 25 will thus be an indication control signal ICS having no output before the time t but consisting of a pulse signal after the time t, as shown in FIG. 3C.

The indicator 16 can be controlled by controlling the digit indicator driving circuit 14 by means of such indication control signal, thereby to effect the warning of overflow. There is thus provided means for control of flashing of all the digit indicator elements 16¹ to 16¹³ simultaneously or successively at the time of overflow. For a more detailed explanation of such flashing control, the digit indicator driving circuit 14 and the indicator 16 will now be discussed with reference to FIG. 4.

Reference numeral 36 designates a four bit hexadecimal counter with a a, $\bar{a}$ and b, $\bar{b}$ bit outputs connected to AND gates 37 to 40, the outputs of which are applied, respectively, to the base electrodes of transistors 45 to 48 (first switching elements) through corresponding OR gates 41 to 44, for ON-OFF control of these transistors. Emitter electrodes of the transistors 45 to 48 are selectively connected with the digit indicator elements 16¹ to 16¹³ in such a manner that one electrode of the digit indicator elements is selected in sequence correspondingly to the contents of the counter 36. Collectors of the transistors 45 to 48 are connected in common to a power supply 49.

The c, $\bar{c}$ and d, $\bar{d}$ bit outputs of the counter 36 are connected to AND gates 50 to 53, the outputs of which are applied, respectively, to the base electrodes of transistors 58 to 61 (second switching elements) through corresponding OR gates 54 to 57, for ON-OFF control of these transistors.

Collectors of the transistors 58 to 61 are selectively connected with the digit indicator elements 16¹ to 16¹³ in such a manner that other electrodes of the digit indicator elements are selected in sequence correspondingly to the contents of the counter 36. Emitters of the transistors are connected in common to the ground of the power supply 49.

Accordingly, in response to the contents of the counter 36, one of the digit indicator elements 16¹ to 16¹³ is selectively lit.

The circuit of FIG. 4 is so arranged that a signal is applied in common to the OR gates 41 to 44 and 54 to 57. Inputs to the counter 36 are applied through the OR gate 62. By applying entry signals to the input terminal 15 of the OR gate 62, the indicator elements 16¹ to 16¹³ will operate as an ordinary digit indicator for entry information.

Upon application of a certain numeral at the time of registration, a single pulse signal produced by the entry is applied to the OR gate 62 through the terminal 15. The counter 36 will then count "1" and have indication of 0001. In this condition, however, only the AND gates 37 and 50 have outputs and the transistors 45 and 58 will be turned ON, with the result that only the digit indicator element 16¹ is lit while the other digit indicator elements remain extinguished.

The digit indicator element 16¹ is held in its lighted condition; and, when a numeral of one digit is further entered following the previous entry, the counter will count "2" and have the contents being 0010. Under

this condition, the AND gates 38 and 50 will only have outputs and the transistors 46 and 58 will be turned ON. As a result, the digit indicator element 16¹ which has been lighted extinguishes while only the indicator element 16² begins to light up.

The digit indicator elements 16¹ to 16¹³ light successively in response to the entry of each digit; and they are extinguished only when a reset signal, produced by depression of a function key, is applied to the terminal 17.

The digit indicator can operate as an ordinary digit indicator by arranging the device such that the entry key signal is applied to the terminal 15 of the OR gate 62. If the indication control signal as above referred to is applied to the terminal 63 as an input the, flashing of each of digit indicator element of the indicator 16 can be simultaneously controlled at a constant rate.

Because the indication control signal (ICS) is a pulse signal having a constant rate as shown in FIG. 3C, such a pulse train is continuously applied to the counter 36 at the time of overflow. More particularly, at the time t_1 of FIG. 3, all of the transistors 45 to 48 and 58 to 61 are rendered conductive all at once upon application of a pulse of E level thereto with the result that all of the digit indicator elements 16¹ to 16¹³ are turned on. During the period t_2 following the period of t_1 , the indication control signal is of 0 level and thus all of the transistors 45 to 48 and 58 to 61 are rendered nonconductive, with the result that all of the digit indicator elements 16¹ to 16¹³ are turned off. For example, it is assumed that the pulse rate is 300 m sec. the indicator 16 will turn on every 300 m sec. so as to warn of overflow.

Such indication has an advantageous effect in that all of the digit indicator elements (13 in the embodiment) are used for overflow and simultaneously controlled for flashing.

It is also possible in another embodiment to arrange the digit indicator elements 16¹ to 16¹³ in such a manner that they may turn on in sequence. For this purpose, arrangement is so made that the indication control signal is applied to the OR gate of the input circuit of the counter 36 as above mentioned. In this case, however, the indication timing pulses should be of higher frequency than that in the embodiment as above described.

With this arrangement, a series of pulses which provide the indication control signal, are continuously applied to the counter 36 at the time of overflow.

In this way, the contents of the counter will change whenever pulses occur and in response to this, the lighting indication of the indicator 16 will be also changed.

For example, it is assumed that pulse rate is 25 m sec. lighting of the digit indicator elements 16¹ to 16¹³ will move in sequence from the side of the digit indicator element 16¹ to the indicator element 16¹³ at time interval of 25 m sec. Once the digit indicator element 16¹³ turns on, the counter 36 rests for the period of three pulses (3×25 m sec.), as the same is hexadecimal counter; and thereafter, returning to the digit indicator element 16¹, lighting will again start therefrom in order.

Thus, if the indication control signal caused by the overflow signal is fed to the counter where entered digit is counted, the digit indicator element 16¹ to 16¹³ will act to light and extinguish intermittently in sequence at the time of overflow. This is very effective to attract operator's attention.

We claim:

1. An overflow warning device comprising:
 - input means for entering digital information;
 - a register having a predetermined storage capacity for storing the information entered by said input means;
 - a plurality of digit indicators each having a first and a second electrode for indicating the digit of the information entered in said register;
 - means for detecting the overflow of the information entered in said register beyond the predetermined storage capacity of said register;
 - means for producing indication controlling signals by which a flashing period of said indicators is determined;
 - a plurality of first switching means connected to selected ones of said first electrodes of said digit indicators;
 - a plurality of second switching means connected to selected one of said second electrodes of said digit indicators;
 - counting means having a plurality of bit outputs for counting the indication controlling signals;
 - means for applying some bit outputs of said counting means to said first switching means to control the operation of said first switching means;
 - means for applying other bits outputs of said counting means to said second switching means to control the operation of said second switching means; and
 - means for supplying power to said digit indicators through said first and second switching means whereby the digit indicators will light and extinguish intermittently and in sequence upon the occurrence of said overflow.
2. An overflow warning device according to claim 1, wherein said indication controlling signal producing means comprises a motor and means for generating signals in response to the rotation of said motor.
3. An overflow warning device according to claim 1, wherein said first and second switching means comprise transistors.
4. An overflow warning device according to claim 1, wherein said counting means is connected to an OR gate having two inputs to one of which the indication controlling signals are applied and to the other of which is applied a pulse generated when the digital information is entered by said input means.
5. An overflow warning device according to claim 1, wherein said overflow detecting means comprises an AND gate to which is applied the information entered in said register and a digit signal corresponding to the overflow digit of said register and a flip-flop to which is applied an output of said AND gate.
6. An overflow warning device according to claim 5, wherein said flip-flop has clear signal applying means for reversing a condition of said flip-flop in which the output of said AND gate is applied thereto.
7. An overflow warning device comprising:
 - input means for entering digital information;
 - a register having a predetermined storage capacity for storing the information entered by said input means;
 - a plurality of digit indicators each having a first and a second electrode for indicating the digit of the information entered in said register;

means for detecting the overflow of the information entered in said register beyond the predetermined storage capacity of said register;
 means for producing indication controlling signals by which a flashing period of said indicators is determined; 5
 a plurality of first switching means connected to selected ones of said first electrodes of said digit indicators;
 a plurality of second switching means connected to selected ones of said second electrodes of said digit indicators; 10
 counting means having a plurality of bit outputs for counting the indication controlling signals;
 means for applying a plurality of bit outputs of said counting means to said first switching means through first AND gates to control the operation of said first switching means; 15
 means for applying a plurality of other bit outputs of said counting means to said second switching means through second AND gates to control the operation of said second switching means; and 20
 means for supplying power to said digit indicators through said first and second switching means whereby the digit indicators will light and extinguish intermittently and in sequence upon the occurrence of said overflow. 25

8. An overflow warning device comprising:
 input means for entering digital information;
 a register having a predetermined storage capacity 30
 and an overflow digit stage which stores information beyond a given storage capacity for storing the information entered by said input means;

a plurality of digit indicators each having a first and a second electrode for indicating the digit of the information entered in said register;
 an AND gate to which is applied information entered in said register and a digit signal corresponding to the overflow digit stage of said register;
 a flip-flop to which is applied an output of said AND gate;
 means for generating indication controlling signals in response to the rotation of a motor to determine a flashing period of said digit indicators;
 a plurality of first switching means being connected to selected ones of said first electrodes of said digit indicators;
 a plurality of second switching means being connected to selected ones of said second electrodes of said digit indicators;
 counting means having a plurality of bit outputs for counting the indication controlling signals;
 means for applying some bit outputs of said counting means to said first switching means to control the operation of said first switching means;
 means for applying other bit outputs of said counting means to said second switching means to control the operation of said second switching means; and
 means for supplying power to said digit indicators through said first and second switching means whereby the digit indicators will light and extinguish intermittently and in sequence upon the occurrence of said digit signal corresponding to the overflow digit stage of said register.

* * * * *

35

40

45

50

55

60

65

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,864,677 Dated February 4, 1975

Inventor(s) SHIGEHARU BEKKI, ET AL.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 2, line 17, "is" (second occurrence) to read -- in --;

Column 3, line 49, after the numeral "33" insert the following phrase --are arranged on opposite sides of the gear 31--.

Signed and sealed this 22nd day of April 1975.

(SEAL)
Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents
and Trademarks