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(54) **SUBMICRON METALLIZATION USING ELECTROCHEMICAL DEPOSITION**

SUBMIKRONE METALLISIERUNG UNTER VERWENDUNG ELEKTROCHEMISCHER
BESCHICHTUNG

METALLISATION SUBMICRONIQUE PAR DEPOT ELECTROCHIMIQUE

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Description

[0001] This invention relates to the deposition of metal on microelectronic workpieces. It relates particularly to such deposition into a micro-recessed structure in the workpiece surface.

[0002] An integrated circuit is an interconnected ensemble of devices formed within a semiconductor material and within a dielectric material that overlies a surface of the semiconductor material. Devices which may be formed within the semiconductor material include MOS transistors, bipolar transistors, diodes and diffused resistors. Devices which may be formed within the dielectric include thin-film resistors and capacitors. Typically, more than 100 integrated circuit die (IC chips) are constructed on a single 8 inch diameter silicon wafer. The devices utilized in each dice are interconnected by conductor paths formed within the dielectric.

[0003] Typically, two or more levels of conductor paths, with successive levels separated by a dielectric layer, are employed as interconnections. In current practice, an aluminum alloy and silicon oxide are typically used for, respectively, the conductor and dielectric.

[0004] Delays in propagation of electrical signals between devices on a single dice limit the performance of integrated circuits. More particularly, these delays limit the speed at which an integrated circuit may process these electrical signals. Larger propagation delays reduce the speed at which the integrated circuit may process the electrical signals, while smaller propagation delays increase this speed. Accordingly, integrated circuit manufacturers seek ways in which to reduce the propagation delays.

[0005] For each interconnect path, signal propagation delay may be characterized by a time delay T . See E.H. Stevens, Interconnect Technology, QMC, Inc., July 1993. An approximate expression for the time delay, T , as it relates to the transmission of a signal between transistors on an integrated circuit is given by the equation:

$$\tau = RC[1 + (V_{SAT}/RI_{SAT})]$$

[0006] In this equation, R and C are, respectively, an equivalent resistance and capacitance for the interconnect path, and I_{SAT} and V_{SAT} are, respectively, the saturation (maximum) current and the drain-to-source potential at the onset of current saturation for the transistor that applies a signal to the interconnect path. The path resistance is proportional to the resistivity, ρ , of the conductor material.

[0007] The path capacitance is proportional to the relative dielectric permittivity, K_e , of the dielectric material. A small value of T requires that the interconnect line carry a current density sufficiently large to make the ratio V_{SAT}/RI_{SAT} small. It follows, therefore, that a low- ρ conductor which can carry a high current density and a low-

Ke dielectric should be utilized in the manufacture of high-performance integrated circuits.

[0008] To meet the foregoing criterion, copper interconnect lines within a low-Ke dielectric will likely replace aluminum-alloy lines within a silicon oxide dielectric as the most preferred interconnect structure. See "Copper Goes Mainstream: Low-k to Follow", Semiconductor International, November 1997, pp. 67-70. Resistivities of copper films are in the range of 1.7 to 2.0 $\mu\Omega\text{cm}$. while resistivities of aluminum-alloy films are higher in the range of 3.0 to 3.5 $\mu\Omega\text{cm}$.

[0009] Despite the advantageous properties of copper, several problems must be addressed for copper interconnects to become viable in large-scale manufacturing processes.

[0010] Diffusion of copper is one such problem. Under the influence of an electric field, and at only moderately elevated temperatures, copper moves rapidly through silicon oxide. It is believed that copper also moves rapidly through low-Ke dielectrics. Such copper diffusion causes failure of devices formed within the silicon.

[0011] Another problem is the propensity of copper to oxidize rapidly when immersed in aqueous solutions or when exposed to an oxygen-containing atmosphere. Oxidized surfaces of the copper are rendered non-conductive and thereby limit the current carrying capability of a given conductor path when compared to a similarly dimensioned non-oxidized copper path.

[0012] A still further problem with using copper in integrated circuits is that it is difficult to use copper in a multi-layer, integrated circuit structure with dielectric materials. Using traditional methods of copper deposition, copper adheres only weakly to dielectric materials.

[0013] Finally, because copper does not form volatile halide compounds, direct plasma etching of copper cannot be employed in fine-line patterning of copper. As such, copper is difficult to use in the increasingly small geometries required for advanced integrated circuit devices.

[0014] The semiconductor industry has addressed some of the foregoing problems and has adopted a generally standard interconnect architecture for copper interconnects. To this end, the industry has found that fine-line patterning of copper can be accomplished by etching trenches and vias in a dielectric, filling the trenches and vias with a deposition of copper, and removing copper from above the top surface of the dielectric by chemical-mechanical polishing (CMP). An interconnect architecture called dual damascene can be employed to implement such an architecture and thereby form copper lines within a dielectric. Fig. 1 illustrates the process steps generally required for implementing the dual damascene architecture.

[0015] Deposition of thin, uniform barrier and seed layers into high aspect ratio (depth/ diameter) vias and high aspect ratio (depth/width) trenches is difficult. The upper portions of such trenches and vias tend to pinch-off before the respective trench and/or via is completely filled

or layered with the desired material.

[0016] Electrodeposition of the copper metallization has been found to be the most efficient way to deposit copper into the trenches and vias. This method has been found to impart the best electromigration resistance performance to the resulting interconnect. However, this method of depositing the copper is not without problems of its own. For example, acid copper plating solutions for copper interconnect often contain organic additives to provide improved throwing power, enhanced leveling effect, and proper deposit characteristics. Since these additives play a significant role in copper plating, the concentrations of these additives in the plating bath need to be tightly controlled to ensure consistent trench fill and film properties. The present inventors have recognized that it would be desirable to use an additive-free plating solution to improve bath control, thereby eliminate the need to monitor the concentrations of the additives. Further, they have recognized that, even in the presence of such additives, certain plating parameters must be optimized.

[0017] The present inventors have found that application of metallization, particularly copper metallization, using low current density plating waveforms provides better trench and via filling results when compared to high current density plating waveforms. This is particularly true when additive-free plating solutions are used. However, such low current density plating waveforms are often quite slow in producing metal films of the requisite thickness. Accordingly, a low current density plating waveform is used during initial plating operations while a high current density plating waveform is used to decrease the fill time and, if desired, provide a different film morphology, some time after the initial plating operations are complete.

[0018] The present invention is directed at a method for depositing a metal into a micro-recessed structure in the surface of a microelectronic workpiece. According to the invention, the method comprises:

- a) making contact between the surface of the workpiece and an electroplating solution in an electroplating cell, the cell including an anode disposed in electrical contact with the solution, and the workpiece surface forming a cathode;
- b) in a first phase, depositing an initial film of metal into the micro-recessed structure using at least a first electroplating waveform having a first current density; and
- c) in a second phase, substantially completing filling of the micro-recessed structure using at least a second electroplating waveform having a second current density.

The first and second phases are normally separate, with the second phase commencing only after expiry of the first. The second current density is normally substantially higher than the first.

[0019] In accordance with one embodiment of the present invention, the waveshape and its frequency are used to influence the surface morphology of the copper metallization deposit. Further, high metal concentrations in the additive-free plating solutions are used to provide more effective filling of the trench and via structures.

[0020] With respect to plating solutions that include additives, the present inventors have found that the plating process may be optimized by employing low metal concentration plating solutions. Such solutions produce higher quality filling of the trenches and vias when compared with copper metallization deposited using solutions having high metal concentrations.

[0021] The methods are suitable for use in connection with additive free as well as additive containing electroplating solutions. In accordance with one embodiment, the method includes making contact between the surface of the microelectronic workpiece and an electroplating solution in an electroplating cell that includes a cathode formed by the surface of the microelectronic workpiece and an anode disposed in electrical contact with the electroplating solution. Next, an initial film of the metal is deposited into the micro-recessed structure using at least a first electroplating waveform having a first current density. The first current density of the first electroplating waveform is provided to enhance the deposition of the metal at a bottom of the micro-recessed structure. After this initial plating, deposition of the metal is continued using at least a second electroplating waveform having a second current density. The second current density of the second electroplating waveform is provided to assist in reducing the time required to substantially complete filling of the micro-recessed structure.

[0022] Further details of the invention will be apparent from the following description of embodiments thereof, given by way of example. Reference will be made to the accompanying drawings wherein:

Figure 1 is a scanning electron microscope ("SEM") photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was deposited using a plating bath without organic additives and using a low-current plating waveform.

Figure 2 is a SEM photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was deposited using a plating bath without organic additives and using a high current density plating waveform.

Figures 3(a) - (d) are SEM photographs showing cross-sections of metallization layers plated exterior to respective semiconductor substrates wherein the metallization layers were deposited using incremental depositions at different current densities and thicknesses.

Figure 4 is a SEM photograph showing a cross-section of a metallization layer plated exterior to a sem-

iconductor substrate wherein the metallization layer was deposited using a pulse reverse waveform.

Figure 5 is a SEM photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was deposited using a two-step waveform comprised of an initial waveform having a low-current density followed by a further waveform having high-current density.

Figure 6 is a SEM photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was plated using the two-step waveform used to plate the metallization layer of Figure 5, but wherein plating solution had a high copper concentration.

Figures 7 and 8 are SEM photographs showing cross-sections of metallization layers plated exterior to respective semiconductor substrates wherein the layers were deposited using a one-step waveform in a plating bath having organic additives.

Figure 9 is a SEM photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was plated using the one-step waveform used in the metallization process of Figures 7 and 8, but wherein the copper concentration of the plating solution has been reduced.

Figures 10(a) - 10(c) are FIB photographs showing cross-sections of metallization layers plated exterior to respective semiconductor substrates wherein the metallization layers were plated using a plating bath having organic additives, and wherein the photographs illustrate the effect of seed layer quality on the plating process.

[0023] The present invention can be understood with reference to the experiments disclosed herein. Although the experiments were performed in connection with the plating of a metal comprising copper, it will be recognized that the teachings disclosed herein are so applicable to the electroplating of other metals. All the experiments were performed on 200mm wafers using a plating tool, such as a plating tool available from Semitool, Inc., of Kalispell, Montana. Three plating baths were examined. The first one, bath 1 (either 24g/L or 36g/L copper) had no organic additives. The bath 2 (Additive A) and the bath 2 (Additive B) contain organic additives from different vendors.

[0024] Good trench fill was obtained at low current density of 4mA/cm² for copper concentrations from 15 to 36 g/L. It is believed that the high micro-throwing power at low current density due to low concentration polarization is responsible for such trench fill at high copper concentrations. Figure 1 presents a scanning electron microscope ("SEM") cross-section obtained from bath 1 with 24g/L copper. Void-free fill was obtained for 0.5μ wide, 2:1 aspect ratio trench. The waveshape used was a forward pulse with 1 ms on and 1 ms off (WF1). It was found

that the waveshape was not significant for fill as long as the current density was low. As seen from Figure 1, rough surface or large grains were observed with 4mA/cm², implying that grain growth was the principal mechanism for the deposition as opposed to the formation of new nuclei. The copper deposit becomes smoother with high current density (40 mA/cm²) as shown in Figure 2. However, the fill at this higher current is not as good and seam voids were seen in the trench.

[0025] In view of the characteristics of the low current density and high current density waveforms, the present inventors have found that such waveforms can be combined during a single electroplating process whereby the advantages associated with each waveform are exploited to provide a sub-micron electroplating process that meets the process characteristics (void filling and time for filling) required to make it commercially viable. To this end, an electroplating waveform having low current density is used during the initial phases of the trench and/or via filling stage of the process. At some time subsequent to such initial filling, the electroplating waveform transitions to a higher current density waveform to complete the electroplating process and reduce the total time required for the process.

[0026] To understand how the copper was deposited inside trench and via features, incremental deposition at different current densities and thicknesses, represented as Ampere-minutes (A-min), was conducted. The results are compared in Figures 3(a) - (d). At low current density, large grains were seen (Figures 3(a) and (b)). As the thickness increased from 1.26 to 3.78 A-min, enhanced growth at the bottom of the trench is achieved, probably explaining why good fill was obtained in Figure 1 at low current density. As such, the low-current density value should be chosen to provide enhanced growth of the copper metallization layer at the lower portions of the feature into which the copper metallization is deposited. At high current density (40mA/cm², Figures 3(c) and (d)), the deposit is smooth and very conformal. Compared to Figure 2, where seam voids are observed, conformal plating is not sufficient to guarantee void-free fill because the top part of the trench is often pinched off first leaving voids inside.

[0027] It is believed that the seam voids illustrated in these Figures resulted from the overplating of copper deposit at the top of the feature due to its high current distribution. It is expected that the overplated copper will be preferentially removed if a reverse pulse is included in the waveshape. However, the addition of reverse pulses did not improve the trench fill as shown in Figure 4 where seam voids were still observed even with a pulse reverse waveshape.

[0028] Therefore, an initial low current density approach is necessary for gap fill if no-additive bath is used. In addition to good trench fill, initial low current is helpful to improve the contact to the seed layer, particularly when the seed layer is very thin. However, the drawback of low current is its long processing time. To circumvent this, a

plating recipe with multiple steps is preferred in which a low current plating waveform is used to fill the small feature and, possibly, to enhance the seed layer, and then a high current plating waveform is used to finish the process and to provide smooth surface for one or more subsequent CMP processes.

[0029] Figure 5 shows a cross-section obtained with a two-step waveform of 4mA/cm² followed by 32mA/cm². An improvement in gap fill was observed. Using the same two-step waveform, an increase in the copper concentration (36g/L) provided significant improvement of the fill process as illustrated in Figure 6.

[0030] The effect of copper concentration on the gap fill for acidic baths with additives was examined using bath 2 disclosed above. Figure 7 illustrates a metallization way are plated from such a bath using a 1-step waveform at 20 mA/cm². Figure 8 is a cross-section obtained at 20mA/cm² with 20g/L copper in the solution. Although the surface of the deposit was smooth, similar to bath 3, voids were observed in the trench at this copper concentration. As the copper concentration decreased from 20 to 10g/L, void-free fill was obtained as in Figure 9. The better gap fill at lower copper concentration in the presence of organic additives is different from that obtained for additive-free bath in which high copper provided better gap fill. This implies a different controlling mechanism for copper growth in the presence of additives. Similar to those obtained from additive-free bath, pulse reverse was found to produce voids and rough surface in this bath with additives.

[0031] Figures 10(a) - (c) illustrates the effect of seed layer on the gap fill. The center voids (Figure 10a) are formed when the top of the feature is pinched off before the filling is completed. The overhanging of the seed layer at the top of the feature, due to the line-of-sight deposition inherent in the PVD process, is often the main reason for the center voids and the insufficient suppressor of copper growth at the top of the trench during the plating is the other one. The former needs the optimization of the PVD process to deposit a conformal layer and may possibly require a combination of PVD process and other techniques such as CVD or electrochemical deposition for small features. The latter calls for the optimization of the plating process by changing the bath composition and plating waveform.

[0032] The bottom and sidewall voids (Figure 10(b)) are mainly attributed to the insufficient coverage of the seed layer. Copper oxide is always formed on the seed layer prior to the plating when the wafer is exposed to air. This oxide is readily removed, and the underlying copper can be chemically etched when the wafer is in contact with the acidic plating solution. This may lead to the exposure of the barrier layer to the solution and result in the formation of bottom or sidewall voids. There are ways to eliminate these voids either by having a thick layer in the feature or using less aggressive plating solutions for the copper plating. By optimizing the seed layer, void-free gap fill was achieved as in Fig. 10(c).

Claims

1. A method for depositing a metal into a micro-recessed structure in the surface of a microelectronic workpiece, which method comprises:
 - a) making contact between the surface of the workpiece and an electroplating solution in an electroplating cell, the cell including an anode disposed in electrical contact with the solution, and the workpiece surface forming a cathode;
 - b) in a first phase, depositing an initial film of metal into the micro-recessed structure using a first electroplating waveform having a first current density; and
 - c) in a second phase, substantially completing filling of the micro-recessed structure with the same metal using a second electroplating waveform having a second, higher, current density.
2. A method according to Claim 1 wherein the first phase continues for a first predetermined period of time, and the second phase commences after expiry of said period.
3. A method according to any preceding Claim wherein the micro-recessed structure is a semiconductor wafer.
4. A method according to any preceding Claim wherein the electroplating solution is substantially free of organic additives and has a first predetermined concentration of the metal that is to be electroplated that is higher than a second predetermined concentration suitable for use in a plating bath including organic additives.
5. A method according to Claim 4 wherein the electroplating solution comprises a concentration of the metal that is between about 15g/L and 36g/L.
6. A method according to any of Claims 1 to 3 wherein the metal that is to be plated comprises copper.
7. A method according to any of Claims 1 to 3 wherein the ratio between the first current density and the second current density is about 1:10.
8. A method according to any of Claims 1 to 3 wherein the ratio between the first current density and the second current density is about 1:8.
9. A method according to any of Claims 1 to 3 wherein the first predetermined period of time is on the order of 30 seconds.
10. A method according to any preceding Claim wherein the first electroplating waveform is a pulsed wave-

form.

11. A method according to any preceding Claim wherein the micro-recessed structure has a width of approximately 0.5 microns.
12. A method according to any preceding Claim wherein the micro-recessed structure has an aspect ratio of 2:1.
13. A method according to any preceding Claim wherein the initial film of metal deposited using the first electroplating waveform has a first morphology, and the second metal deposited using the second electroplating waveform has a second morphology that is different than the first morphology.
14. A method according to any preceding Claim including the step of depositing a thin seed layer on the microelectronic workpiece prior to deposition of the initial film, deposition of the initial film enhancing the thin seed layer.
15. A method according to any preceding Claim including, after processing the micro-recessed structure with the second electroplating waveform, the step of processing the micro-recessed structure using a third electroplating waveform including a reverse current pulse to remove overflow.

Patentansprüche

1. Verfahren zur Abscheidung eines Metalls in eine Mikrovertiefungen aufweisende Struktur in der Oberfläche eines mikroelektronischen Werkstücks, wobei das Verfahren aufweist:
 - a) Herstellen eines Kontaktes zwischen der Oberfläche des Werkstücks und einer Lösung zur elektrochemischen Abscheidung in einer Zelle zur elektrochemischen Abscheidung, wobei die Zelle eine Anode aufweist, die in elektrischem Kontakt mit der Lösung angeordnet ist, und die Werkstückoberfläche eine Kathode bildet,
 - b) in einer ersten Phase Abscheiden einer anfänglichen Schicht von Metall in die Mikrovertiefungen aufweisende Struktur unter Verwendung einer ersten Wellenform zur elektrochemischen Abscheidung mit einer ersten Stromdichte und
 - c) in einer zweiten Phase im Wesentlichen Vervollständigen des Füllens der Mikrovertiefungen aufweisenden Struktur mit demselben Metall unter Verwendung einer zweiten Wellenform zur elektrochemischen Abscheidung mit einer zweiten, höheren Stromdichte.

2. Verfahren nach Anspruch 1, bei dem die erste Phase für eine erste vorbestimmte Zeitdauer andauert und die zweite Phase nach Beendigung der ersten Zeitdauer anfängt.
3. Verfahren nach einem der vorhergehenden Ansprüche, bei dem die Mikrovertiefungen aufweisende Struktur ein Halbleiterwafer ist.
4. Verfahren nach einem der vorhergehenden Ansprüche, bei dem die Lösung zur elektrochemischen Abscheidung im Wesentlichen frei von organischen Zusatzstoffen ist und eine erste vorbestimmte Konzentration des Metalls aufweist, das elektrochemisch abgeschieden werden soll, die höher als eine zweite vorbestimmte Konzentration ist, die zur Verwendung in einer Lösung zur elektrochemischen Abscheidung geeignet ist, die organische Zusatzstoffe enthält.
5. Verfahren nach Anspruch 4, bei dem die Lösung zur elektrochemischen Abscheidung eine Konzentration des Metalls aufweist, die zwischen ungefähr 15 g/L und 36 g/L beträgt.
6. Verfahren nach einem der Ansprüche 1 bis 3, bei dem das Metall, das abgeschieden werden soll, Kupfer aufweist.
7. Verfahren nach einem der Ansprüche 1 bis 3, bei dem das Verhältnis zwischen der ersten Stromdichte und der zweiten Stromdichte ungefähr 1:10 beträgt.
8. Verfahren nach einem der Ansprüche 1 bis 3, bei dem das Verhältnis zwischen der ersten Stromdichte und der zweiten Stromdichte ungefähr 1:8 beträgt.
9. Verfahren nach einem der Ansprüche 1 bis 3, bei dem die erste vorbestimmte Zeitdauer in der Größenordnung von 30 Sekunden liegt.
10. Verfahren nach einem der vorhergehenden Ansprüche, bei dem die erste Wellenform zur elektrochemischen Abscheidung eine gepulste Wellenform ist.
11. Verfahren nach einem der vorhergehenden Ansprüche, bei dem die Mikrovertiefungen aufweisende Struktur eine Breite von ungefähr 0,5 μm hat.
12. Verfahren nach einem der vorhergehenden Ansprüche, bei dem die Mikrovertiefungen aufweisende Struktur ein Geometrieverhältnis von 2:1 aufweist.
13. Verfahren nach einem der vorhergehenden Ansprüche, bei dem die anfängliche Schicht von Metall, die unter Verwendung der ersten Wellenform zur elektrochemischen Abscheidung abgeschieden wird, eine erste Morphologie aufweist und das zweite Metall,

das unter Verwendung der zweiten Wellenform zur elektrochemischen Abscheidung abgeschieden wird, eine zweite Morphologie aufweist, die anders als die erste Morphologie ist.

14. Verfahren nach einem der vorhergehenden Ansprüche, das den Schritt aufweist, vor der Abscheidung der anfänglichen Schicht eine dünne Keimschicht auf dem mikroelektronischen Werkstück abzuscheiden, wobei die Abscheidung der anfänglichen Schicht die dünne Keimschicht verbessert.
15. Verfahren nach einem der vorhergehenden Ansprüche, das nach der Bearbeitung der Mikrovertiefungen aufweisenden Struktur mit der zweiten Wellenform zur elektrochemischen Abscheidung den Schritt aufweist, die Mikrovertiefungen aufweisende Struktur unter Verwendung einer dritten Wellenform zur elektrochemischen Abscheidung zu bearbeiten, die einen Gegenstromimpuls aufweist, um Überfüllung zu entfernen.

Revendications

1. - Procédé de dépôt d'un métal dans une structure à micro-cavités dans la surface d'une pièce à travailler micro-électronique, lequel procédé comprend :
- a) faire contact entre la surface de la pièce à travailler et une solution d'électroplacage dans une cellule d'électroplacage, la cellule comprenant une anode placée en contact électrique avec la solution, et la surface de la pièce à travailler formant une cathode ;
- b) dans une première phase, déposer un film initial de métal dans la structure à micro-cavités à l'aide d'une première forme d'onde d'électroplacage ayant une première densité de courant ; et
- c) dans une seconde phase, compléter de façon substantielle le remplissage de la structure à micro-cavités avec le même métal à l'aide d'une seconde forme d'onde d'électroplacage ayant une seconde densité de courant, supérieure.
2. - Procédé selon la revendication 1, dans lequel la première phase se poursuit pendant une première période de temps prédéterminée, et la seconde phase commence après l'expiration de ladite période.
3. - Procédé selon l'une quelconque des revendications précédentes, dans lequel la structure à micro-cavités est une tranche de semi-conducteur.
4. - Procédé selon l'une quelconque des revendications précédentes, dans lequel la solution d'électroplacage est sensiblement exempte d'additifs orga-

niques et a une première concentration prédéterminée du métal devant être électroplacé qui est supérieure à une seconde concentration prédéterminée appropriée pour une utilisation dans un bain de placage comprenant des additifs organiques.

5. - Procédé selon la revendication 4, dans lequel la solution d'électroplacage comprend une concentration du métal qui est entre environ 15 g/L et 36 g/L.
6. - Procédé selon l'une quelconque des revendications 1 à 3, dans lequel le métal devant être plaqué comprend le cuivre.
7. - Procédé selon l'une quelconque des revendications 1 à 3, dans lequel le rapport entre la première densité de courant et la seconde densité de courant est d'environ 1:10.
8. - Procédé selon l'une quelconque des revendications 1 à 3, dans lequel le rapport entre la première densité de courant et la seconde densité de courant est d'environ 1:8.
9. - Procédé selon l'une quelconque des revendications 1 à 3, dans lequel la première période de temps prédéterminée est de l'ordre de 30 secondes.
10. - Procédé selon l'une quelconque des revendications précédentes, dans lequel la première forme d'onde d'électroplacage est une forme d'onde pulsée.
11. - Procédé selon l'une quelconque des revendications précédentes, dans lequel la structure à micro-cavités a une largeur d'approximativement 0,5 micron.
12. - Procédé selon l'une quelconque des revendications précédentes, dans lequel la structure à micro-cavités a un rapport d'allongement de 2:1.
13. - Procédé selon l'une quelconque des revendications précédentes, dans lequel le film initial de métal déposé à l'aide de la première forme d'onde d'électroplacage a une première morphologie, et le second métal déposé à l'aide de la seconde forme d'onde d'électroplacage a une seconde morphologie qui est différente de la première morphologie.
14. - Procédé selon l'une quelconque des revendications précédentes, comprenant l'étape consistant à déposer une fine couche d'ensemencement sur la pièce à travailler microélectronique avant le dépôt du film initial, le dépôt du film initial renforçant la fine couche d'ensemencement.

15. - Procédé selon l'une quelconque des revendications précédentes, comprenant, après le traitement de la structure à micro-cavités par la seconde forme d'onde d'électroplacage, l'étape consistant à traiter la structure à micro-cavités à l'aide d'une troisième forme d'onde d'électroplacage comprenant une impulsion de courant inverse pour enlever le trop-plein.

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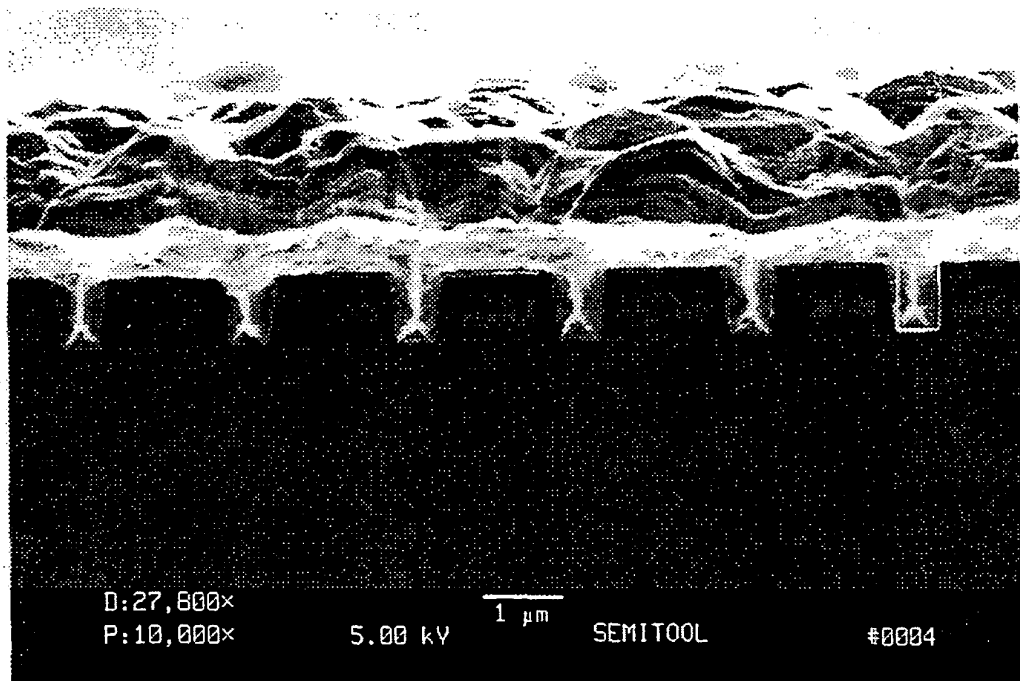


FIG. 1

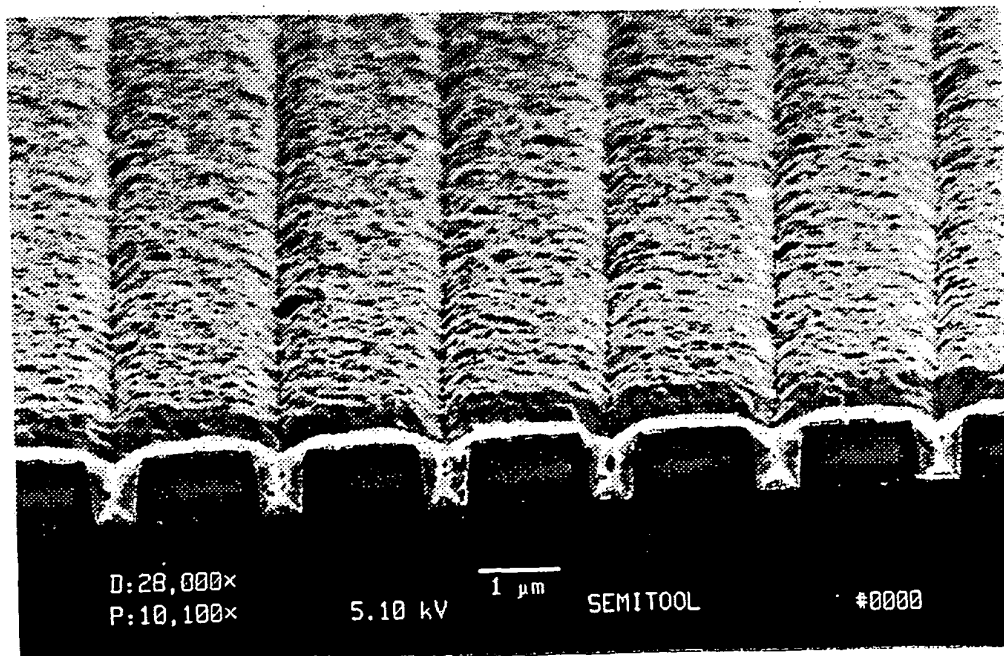


FIG. 2

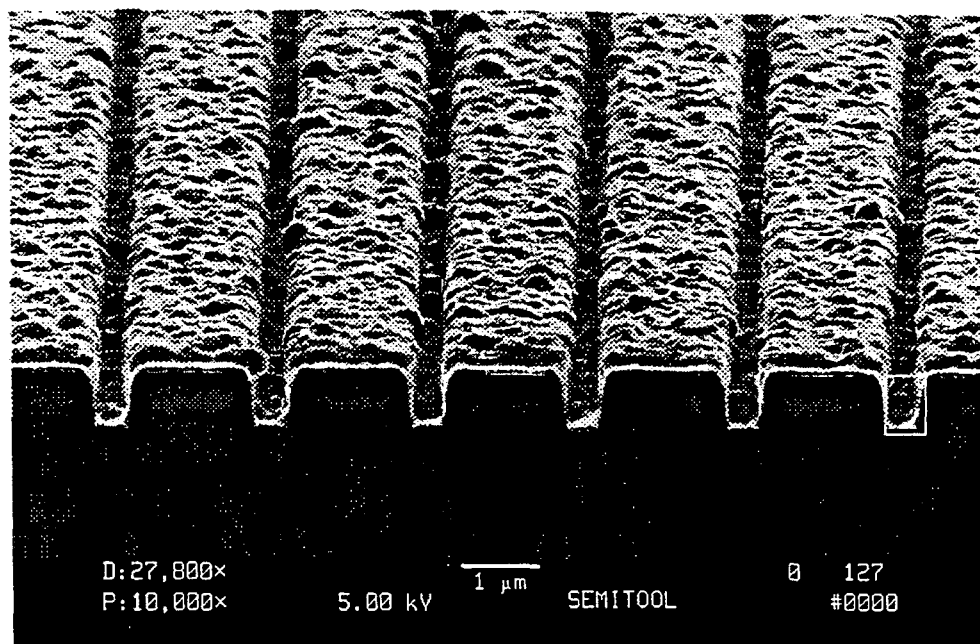


FIG. 3(a)

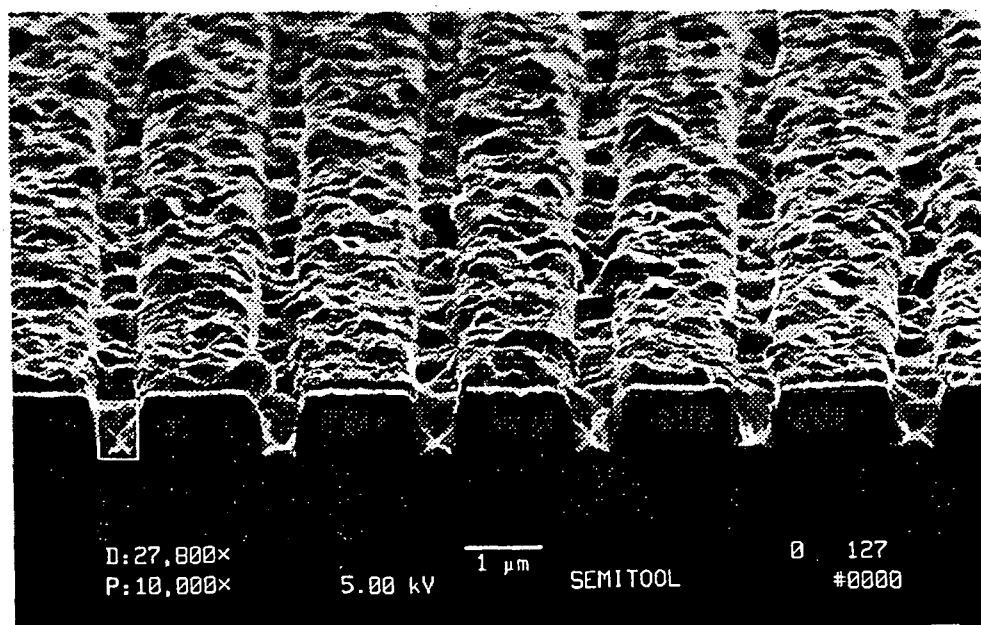


FIG. 3(b)

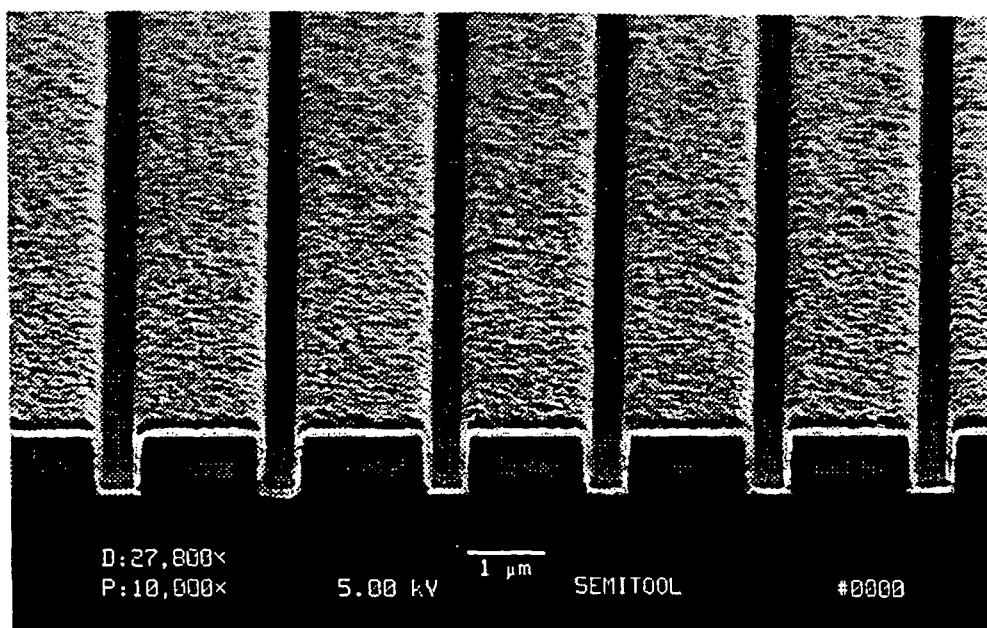


FIG. 3(c)

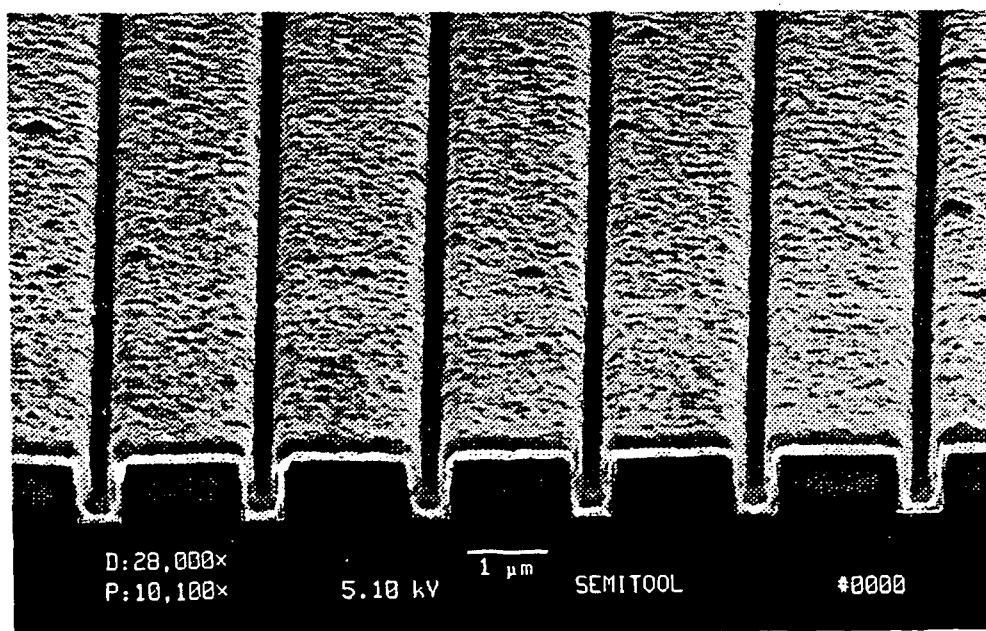


FIG. 3(d)

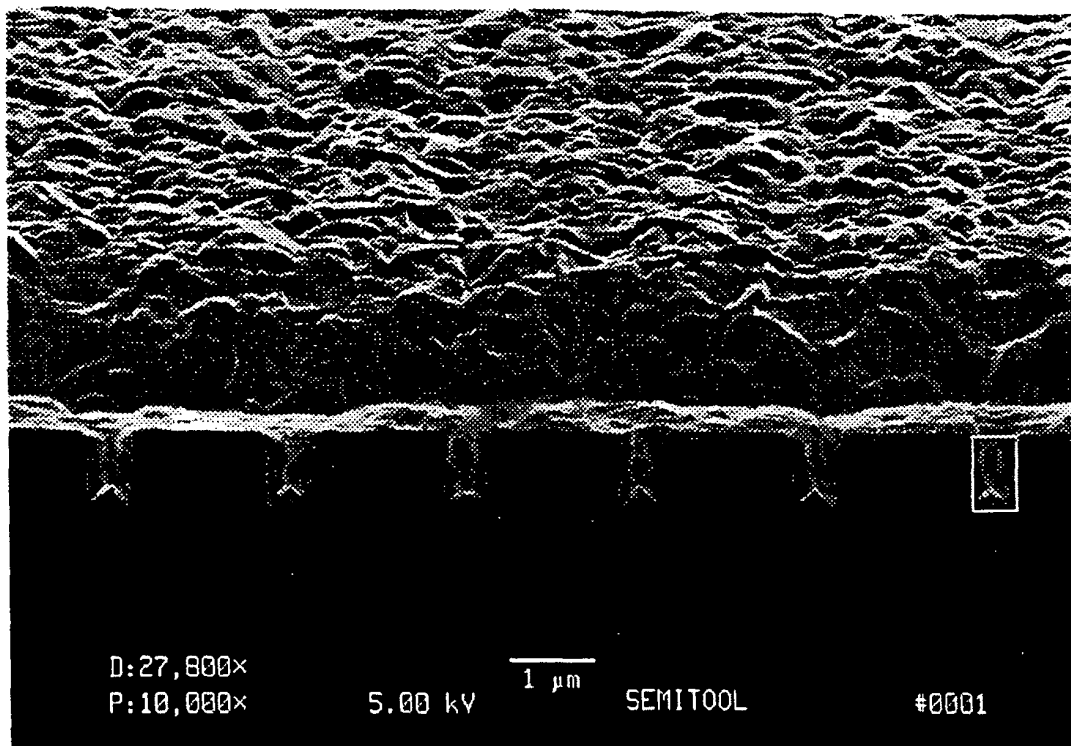


FIG. 4

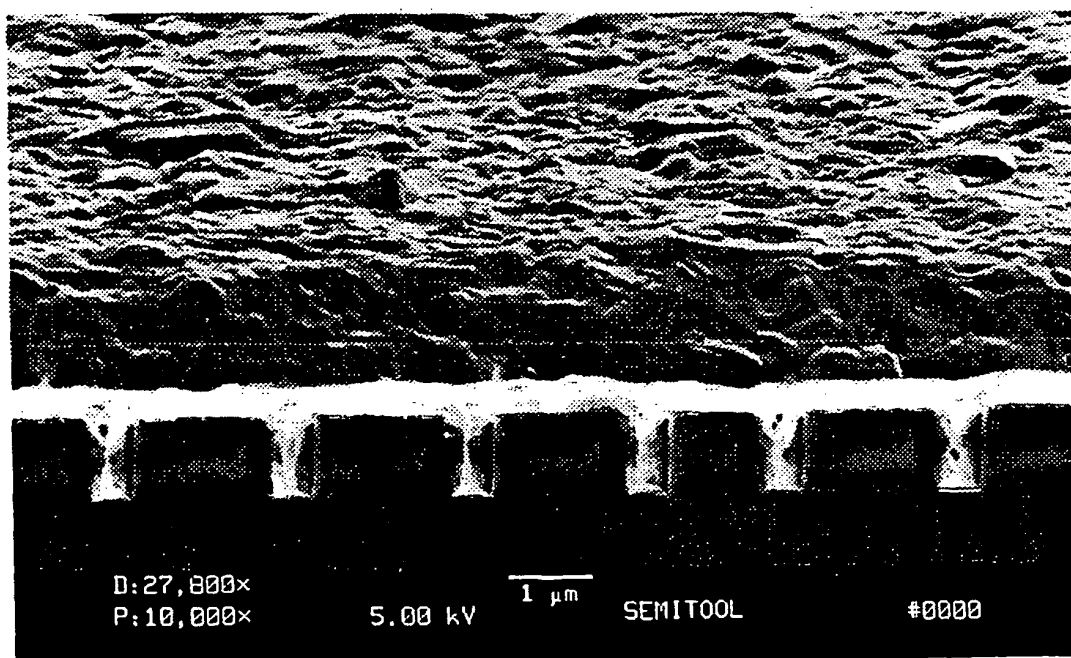


FIG. 5

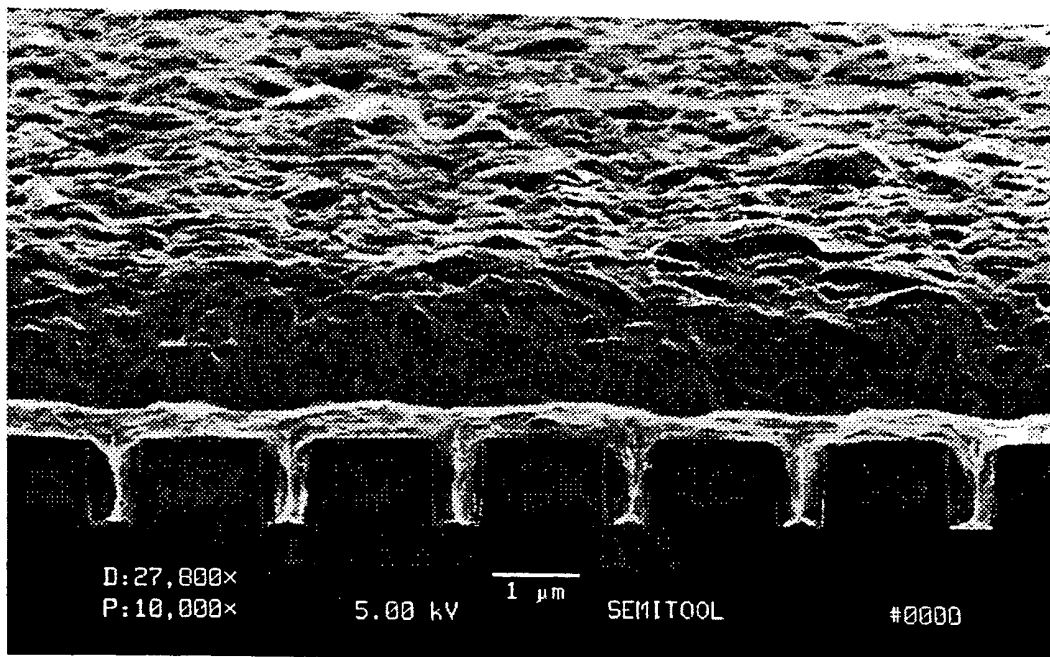


FIG. 6

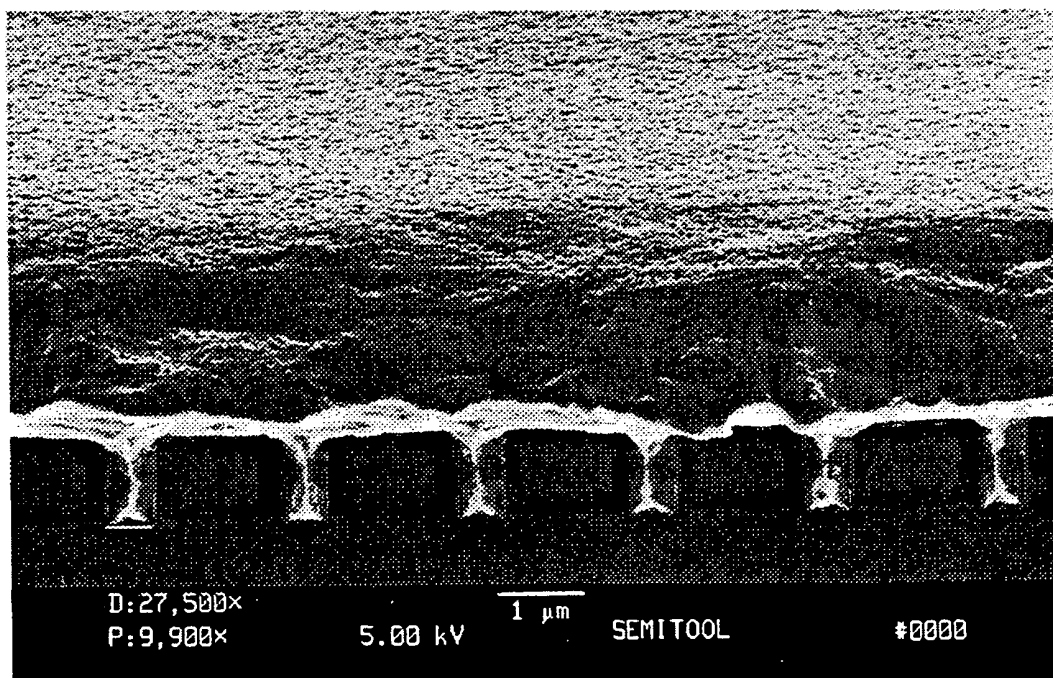


FIG. 7

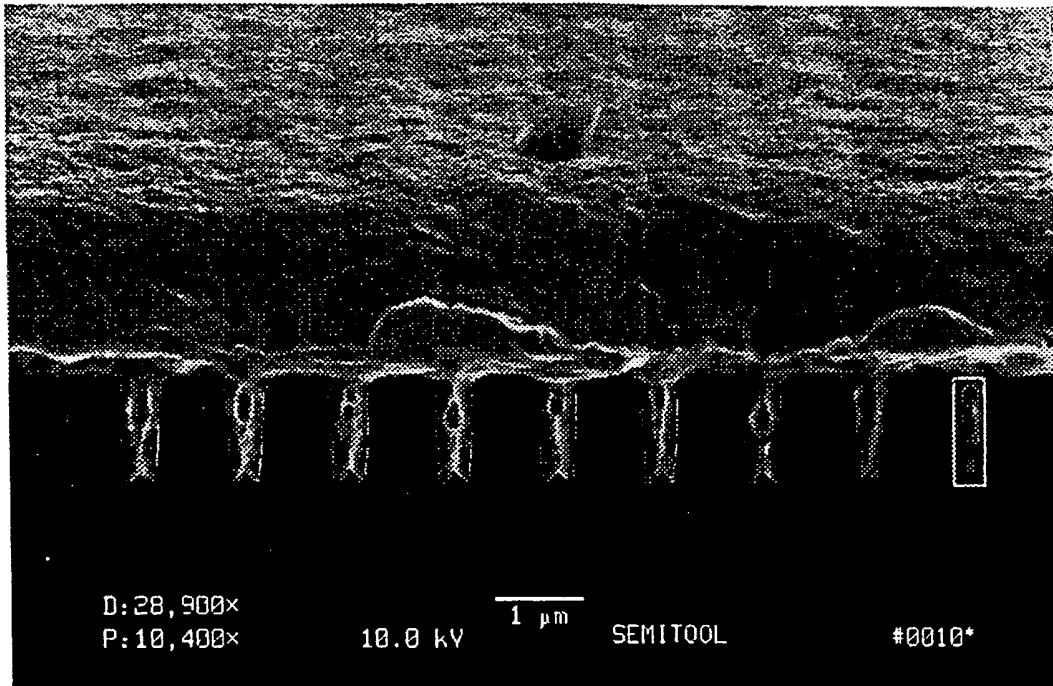


FIG. 8

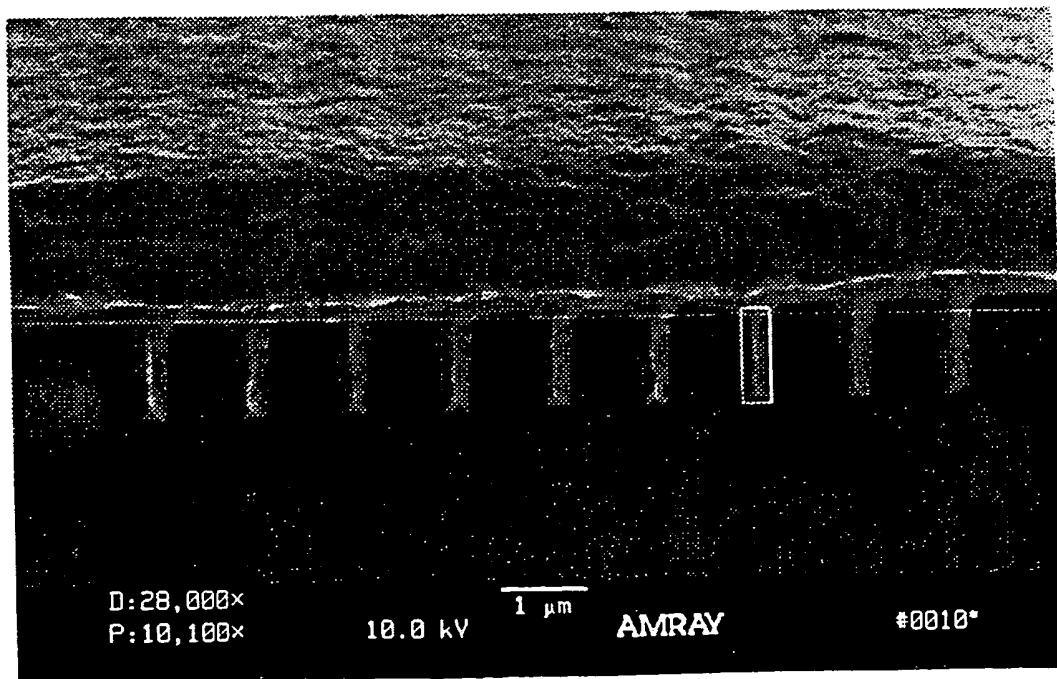


FIG. 9

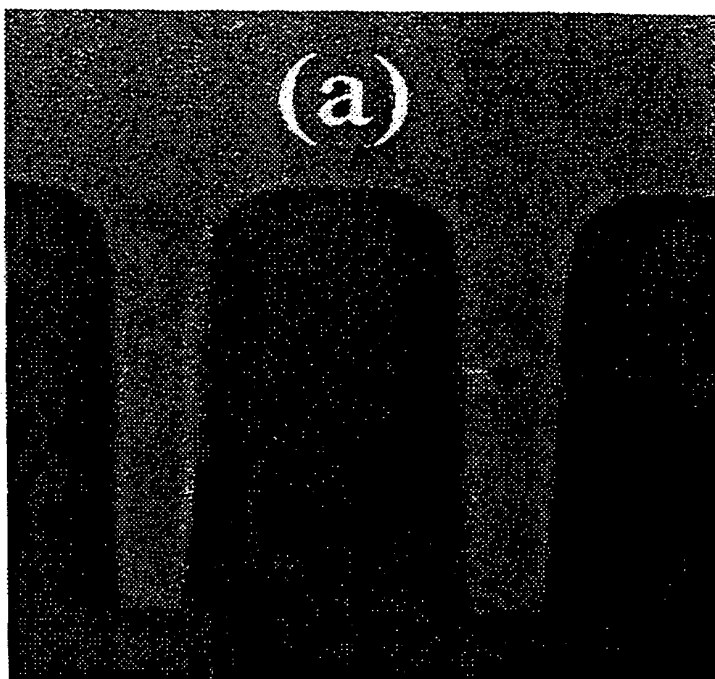


FIG. 10(a)

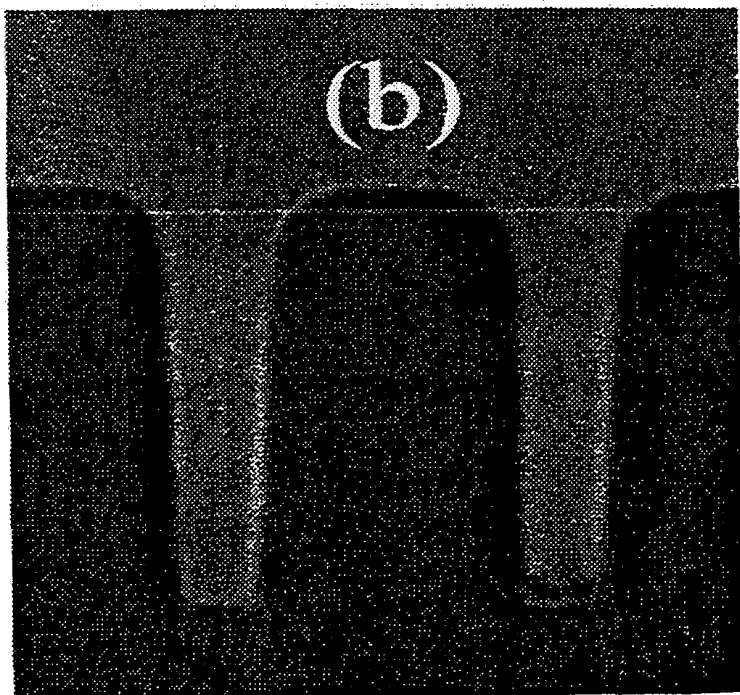


FIG. 10(b)

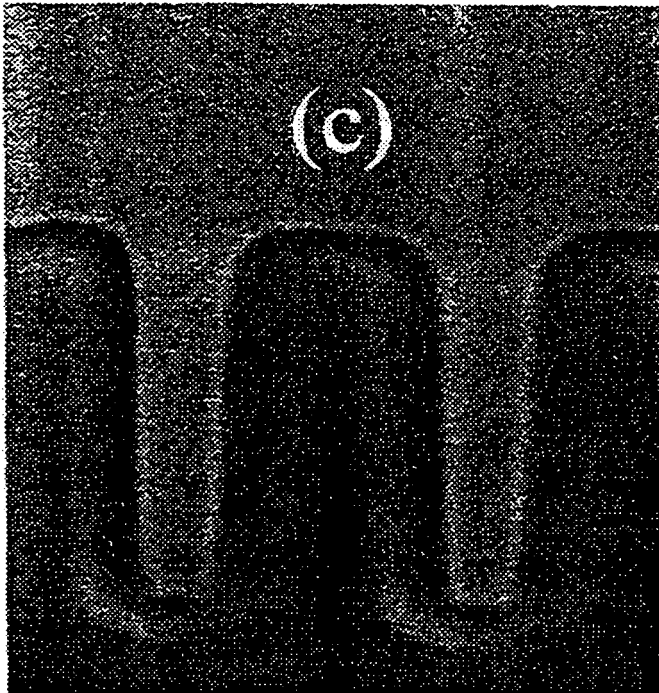


FIG. 10(c)

REFERENCES CITED IN THE DESCRIPTION

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