ABSTRACT

A timing pulse generator, which produces a plurality of timing pulses, is controlled by a series connected arrangement of a monostable-multivibrator and a clock pulse generator. The monostable multivibrator or delay is triggered by an output from the timing pulse generator, so as to render the clock pulse generator disabled for a predetermined period of time, whereby both clock pulses and timing pulses will be inhibited for the predetermined period of time.

9 Claims, 6 Drawing Figures
Fig. 4

MONOSTABLE CIRCUIT

CLOCK PULSE OSCILLATOR

Fig. 5A

CLOCK PULSES

CP1

CP2

t1'

t2'

t3'

t4'

BIT TIMING PULSES

T11

T12

T1

DIGIT TIMING PULSES

TA

TB

STEP TIMING PULSES

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Fig. 5 B

SE
SS
CLOCK PULSES
CP1
CP2
t1'
t2'
t3'
t4'

BIT TIMING PULSES
t1
T11 T11A
T12

DIGIT TIMING PULSES
T12A
T1B

STEP TIMING PULSES
TA
TB

TA
TB
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APPARATUS FOR CONTROLLING CLOCK PULSES

This is a Continuation-in-Part Application of U.S. Pat. Application Ser. No. 829,589, filed on June 2, 1969 now abandoned.

The present invention relates to an apparatus for controlling clock pulses and more specifically to an apparatus for controlling clock pulses for the purpose of stabilizing the operation of a device, the operation of which progresses in accordance with clock pulses, such as dynamic type calculators.

The operation of calculators, for example, a dynamic type is controlled in accordance with the progress of steps, each covering a certain number of clock pulses. Conventionally, successive clock pulses have been utilized in the operation and a change to another state of operation has been made by means of a gate at the time of switching of steps. In such an apparatus described as above, however, a delay in the operation of the gate arises, resulting in the disadvantage that a given number of the clock pulses can not be utilized in the subsequent step. Such delay also can be the cause of improper operation of the apparatus.

In order to avoid such an erroneous operation, it has been proposed to provide a time interval between one step and the next subsequent step, so that clock pulses can not be fed during the time interval. Though a special register may be provided for the purpose of producing such a time interval, there are disadvantages in that the apparatus is complicated and is expensive.

Furthermore, it has been contemplated to extend the pulse width of the bit timing pulses. However, if the pulse width is extended, there will arise the disadvantage in that the time of operation of the device is lengthened.

An object of the present invention is to avoid the erroneous operation of an apparatus operating in accordance with clock pulses by means of a comparatively simple and economical means. According to the present invention, therefore, an output terminal of a clock pulse generator is blocked for the purpose of stopping the generation of the clock pulses for a certain time period at the time of a change of operation of the apparatus operating in accordance with the clock pulses and to maintain the duration of the first bit timing pulse of the first digit of the subsequent step for a certain time as will last until the apparatus continues to the next step.

Another object of the present invention is to provide such an apparatus as can adjust the time interval during which the generation of clock pulses is stopped by blocking the output of the clock pulse generator at the time of the change of the operation. Thus, a stabilized and errorless operation is possible even in case of high speed clock pulses and a slow speed gate circuit.

According to the present invention, in addition to the clock pulse generator and the timing signal generating means for generating step pulses, namely, for generating step timing pulses, digit timing pulses and bit timing pulses, in accordance with the clock pulses means, are provided for producing an output for a certain time period, based upon a step terminating signal supplied from the timing signal generating means and a switching means for blocking or cutting off the clock pulse generating means during the presence of the output of the means for producing the output.

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A further detailed description will be made in conjunction with a preferred embodiment of the present invention with reference to the accompanying drawings, in which;

FIG. 1 illustrates a block diagram of an embodiment of the present invention,

FIG. 2 illustrates a circuit diagram showing the connection between a monostable multivibrator circuit and a clock pulse generator, and

FIG. 3 illustrates the wave form of the output obtained from the principal part of the apparatus in accordance with the present invention.

FIG. 4 is a block diagram showing the details of FIG. 1.

FIG. 5A is a time chart showing the operation of a conventional device, the operation of which progresses in accordance with clock pulses and

FIG. 5B is a time chart showing the operation of the device shown in FIG. 4.

Referring to FIG. 1, 1 denotes a generator for generating clock pulses CP, 2 denotes a timing signal generator for generating step pulses SP, namely, for generating step timing pulses TA, TB, etc., digit timing pulses T1, T2, etc., and bit timing pulses r1, r2, etc., as shown in FIG. 4, based upon the clock pulses CP and

3 denotes a monostable multivibrator for generating the output S5 for a certain time period and at the same time stopping the generation of clock pulses of the generator 1, based upon a step terminating signal SE generated by the timing generator 2 at the time of a change of steps.

Referring to FIG. 2, the collector of a transistor 10 is connected by means of a lead wire 12 through a resistor 11 to the positive terminal 13 of a DC source, while the emitter of the transistor 10 is connected by means of a lead wire 14 to the negative terminal 15 of the DC source. The collector of another terminal 16 is connected by means of the wire 12 through a resistor 17 to the positive terminal 13 of the source, while the emitter of the transistor 16 is connected by means of the wire 14 to the negative terminal 15. The base of the transistor 16 is connected through a variable capacitor 18 to the collector of the transistor 10 and also connected to the positive terminal of a variable resistor 11' and by means of the lead wire 12, and the collector of the transistor 16 is connected through a resistor 20 shunted by a capacitor 19 to the base of the transistor 10.

The monostable multivibrator 3 is constituted of the transistors 10 and 16 and the transistor 16 supplies an output for a certain time period when the step terminating signal SE generated from the timing signal generator 2 of FIG. 1 at the end of every step is supplied to the transistor 10. The collector of the transistor 16 is connected through a resistor 21 to the base of a switching transistor 22. The emitter of the transistor 22 is connected by means of the wire 14 to the negative terminal 15 and the collector is connected to the base of another transistor 24 constituting the clock pulse generator 1 which will be explained afterwards. The clock pulse generator 1 is constituted of transistors 23 and 24; each collector thereof being connected by means of the lead wire 12 through resistors 25 and 26 respectively to the positive terminal 13 of the source, each emitter thereof being connected by means of the lead wire 14 to the negative terminal 15 and each base being connected by way of resistors 27 and 28 and by
means of the wire 12 to the positive terminal 13 of the source. A capacitor 29 is connected between the collector of the transistor 23 and the base of the transistor 24, while a capacitor 30 is connected between the base of the transistor 23 and the collector of the transistor 24. The collector of the switching transistor 22 is connected to the base of one of the transistors constituting the generator 1.

Now referring to both FIG. 1 and FIG. 3, the clock pulses CP are generated by the generator 1 and are fed to the timing signal generator 2. Then the step pulses SP are generated by the timing signal generator 2 in accordance to the clock pulses CP as is conventional and the step terminating signal SE is generated at the time of the change of operation as is also conventional. The step terminating signal SE is supplied to the base of the transistor 10 constituting the monostable multivibrator 3, resulting in an output of the transistor 16 for a certain time period, during which the switching transistors 22 becomes conducting. The base of the transistor 24 constituting the generator 1 is grounded by means of the transistor 22 and the transistor 24 remains blocked in a non-conducting state, resulting in cut off of the generator 1, while the transistor 22 is in the conducting state.

Referring to FIG. 3, the step terminating signal SE is fed from the timing signal generator 2 to the monostable multivibrator 3 when each step ends at a time $t_i$. The monostable multivibrator 3 generates, in accordance with the signal SE, the output SS for a certain time period up to a time $t_{o}$, during which the generator 1 is cut off. At the time $t_o$, however, the output SS of the monostable multivibrator 3 becomes zero and the transistor 22 becomes non-conducting, and releases grounding of the base of the transistor 24, i.e., removes therefrom the grounding connection. Accordingly, the generator 1 begins to generate again its signal and the clock pulses CP for the subsequent step are fed to the timing signal generator 2.

The operation hereinabove mentioned will be fully described with reference to FIG. 4 and FIG. 5B. In FIG. 4, the timing pulse generator 2 shown in FIG. 1 comprises the bit timing pulse generating circuit 31, the digit timing pulse generating circuit 32 and the step timing pulse generating circuit 33. In a conventional electronic desktop calculator, as shown in FIG. 5B, bit timing pulses (for example, $t_{1}, t_{2}, t_{3}, t_{4}$ and $t_{5}$), digit timing pulses (for example, $T_1$ to $T_{12}$ in case of 12 digits) and step timing pulses (TA and TB) are generated by clock pulses CP, and CP, from the circuit 31, the circuit 32 and the circuit 33, respectively, to effect various operations. As shown in FIG. 5B, according to the present invention, when one step TA has been changed over to the following step TB, the generation of the clock pulses CP, and CP, can be stopped for a period between $t_1$ to $t_2$. Accordingly, during this period between $t_1$ to $t_2$, a signal $(t_{1} \cdot T_B)$ representative of the first bit of the first digit (T_B) during the step TB can be maintained without any change. In other words, the duration of this signal $(t_{1} \cdot T_B)$ can be lengthened.

On the contrary thereto, according to the conventional calculator of a similar type, in the event that the step timing pulse TB is distorted at the starting portion as indicated by the dotted line in FIG. 5A at the time of change-over of the steps, the logical product between the bit timing pulse $t_{1} \cdot B$ and the step timing pulse TB which should have been "1" has a tendency to become "0", resulting in that the calculator is often erroneously operated. However, according to the present invention, as indicated by the dotted line in FIG. 5B, even if the starting portion of the step timing pulse TB is distorted at the time of change-over of the steps, the logical product between TB and $t_{1} \cdot B$ can be ensured to be "1" since the duration of the first signal $(t_{1} \cdot B)$ can be lengthened as hereinbefore described. Thus, no erroneous operation occurs. Subsequently, after the time $t_o$, the generation of the clock pulses can be restarted and, therefore, the bit timing pulses can be transferred from $t_{2} \cdot B$, $t_{3} \cdot B$, $t_{4} \cdot B$, in the order so that the normal operation of the device commences.

Thus, the generation of clock pulses is stopped for a time $t_2 - t_1$ when one step has been changed over to the following step whereby the duration of the first bit timing pulse of the first digit of the next subsequent step is maintained for a certain time as will last until the apparatus continues to the next step. The time duration $t_2 - t_1$ can be adjusted to an arbitrary value by changing, for example, the pulse width of the pulse obtained from the monostable multivibrator 3. Even in case of high speed clock pulses and a low speed gate circuit, the erroneous operation can be avoided by properly choosing, by way of the variable condenser 18 and the variable resistor 11, the output time of the multivibrator 3 so as to maintain the duration of the first bit timing pulse of the first digit of a new step.

What is claimed is:

1. An apparatus for controlling clock pulses in a device, the operation of which progresses in accordance with clock pulses and timing pulses, and said apparatus comprises a clock pulse generator means operable to generate clock pulses and a timing signal generator means for generating step timing pulses, digit timing pulses and bit timing pulses in accordance with the clock pulses fed thereto, characterized in that said apparatus comprises further means for providing an output for a certain time period by a step terminating signal obtained from said timing signal generator means at the time of change in step to maintain the duration of the first timing pulse of the first digit of each new step, and a switching means for stopping the generation of the clock pulses in said clock pulse generator means during the presence of the output from said further means.

2. An apparatus according to claim 1, characterized in that the further means comprises a monostable multivibrator including two transistors each having an emitter, a collector and a base, with the base of one transistor being cross-connected to the collector of the other transistor and the base of the other transistor being cross-connected to the collector of the other transistor, while the emitters of each transistor are connected to a source of common reference potential.

3. An apparatus for controlling the generation of clock pulses comprising:
   a clock pulse generator for generating respective series of clock pulses;
   first means, responsive to the output of said clock pulse generator, for generating bit timing pulses, digit timing pulses and step timing pulses, the respective durations of which correspond to preselected intervals of time from clock pulses received thereby; and
   second means, responsive to the termination of one of said step timing pulses, for lengthening the dura-
tion of the bit timing pulse generated coincident
with a subsequent step timing pulse, by preventing
the application of the output of said clock pulse
generator to said first means for a predetermined
period of time.

4. An apparatus according to claim 3, wherein said
second means comprises a monostable multivibrator
including two transistors each having an emitter, a col-
lector and a base, with the base of one transistor being
cross-connected to the collector of the other transistor
and the base of the other transistor being cross con-
ected to the collector of the one transistor, while the
emitters of each transistor are connected to a source of
common reference potential.

5. An apparatus according to claim 4, wherein said
second means comprises a transistor switching circuit
connected to the output of said monostable multivibrator
and the input to said clock pulse generator.

6. An apparatus for controlling the generation of
clock pulse comprising:
a clock pulse generator for generating respective se-
ries of clock pulses;
first means, responsive to the output of said clock
pulse generator, for generating bit timing pulses,
digit timing pulses and step timing pulses, the re-
spective durations of which correspond to prese-
lected intervals of time, from clock pulses received
thereby;
a monostable multivibrator, responsive to the termi-
ation of one of said step timing pulses, for generating
a lengthened pulse of a predetermined duration
longer than the spacing between successive clock
pulses; and
second means, responsive to the output of said mono-
stable multivibrator, for disabling said clock pulse
generator for the duration of said lengthened pulse.

7. An apparatus according to claim 6, wherein the
sum of the durations of said bit timing pulses, in one cy-
cle, corresponds to the duration of one digit timing
pulse, and wherein the sum of the duration of said digit
timing pulses, for one cycle, corresponds to the dura-
tion of a step timing pulse.

8. An apparatus according to claim 7, wherein said
monostable multivibrator includes two transistors each
having an emitter, a collector and a base, with the base
of one transistor being cross-connected to the collector
of the other transistor and the base of the other transis-
tor being cross connected to the collector of the one
transistor, while the emitters of each transistor are con-
ected to a source of common reference potential.

9. An apparatus according to claim 8, wherein said
second means comprises a transistor switching circuit
connected to the output of said monostable multivibra-
tor and the input to said clock pulse generator.

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