

(19) World Intellectual Property Organization  
International Bureau(43) International Publication Date  
24 August 2006 (24.08.2006)

PCT

(10) International Publication Number  
**WO 2006/088320 A1**(51) International Patent Classification:  
**H04N 7/015** (2006.01)(21) International Application Number:  
PCT/KR2006/000538(22) International Filing Date:  
16 February 2006 (16.02.2006)

(25) Filing Language: Korean

(26) Publication Language: English

(30) Priority Data:  
10-2005-0012814  
16 February 2005 (16.02.2005) KR(71) Applicant (for all designated States except US): **ELECTRONICS AND TELECOMMUNICATIONS RESEARCH INSTITUTE** [KR/KR]; 161, Gajeong-dong, Yuseong-gu, Daejeon 305-350 (KR).

(71) Applicant and

(72) Inventor: **AHN, Chie-teuk** [KR/KR]; #208-603 Expoapt., Jeonmin-dong, Yuseong-gu, Daejeon 305-761 (KR).

(72) Inventors; and

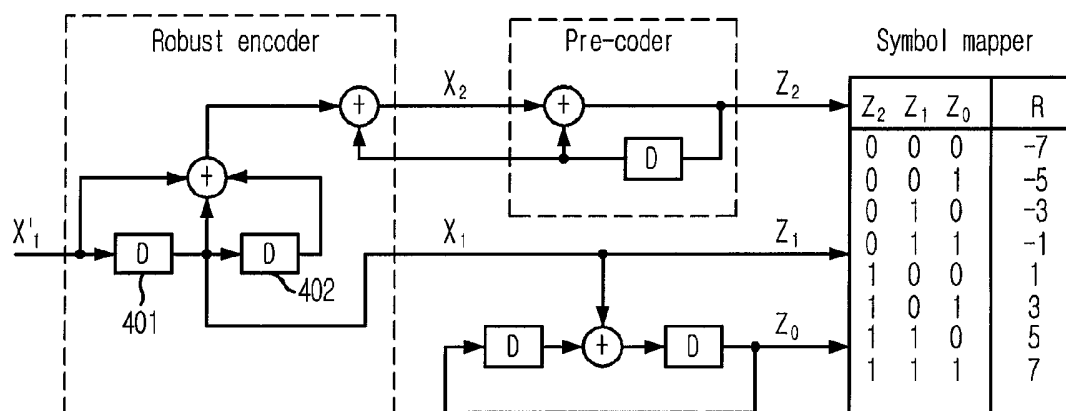
(75) Inventors/Applicants (for US only): **JI, Kum-ran** [KR/KR]; 167, Manyeon-ri, Hwasun-eup, Hwasun-gun, Jeollanam-do 519-806 (KR). **KIM, Sung-hoon** [KR/KR]; #210-206 Samsung Narmae Apt., Gajang-dong, Seo-gu, Daejeon 302-726 (KR). **LEE, Jae-young** [KR/KR]; #514-201 Jugong Apt., 27, Jamsil 5-dong, Songpa-gu,Seoul 138-916 (KR). **KIM, Seung-won** [KR/KR]; #105-202 Guwha Dongseong Apt., Samcheon-dong, Seo-gu, Daejeon 302-222 (KR). **LEE, Soo-in** [KR/KR]; #106-606 Clover Apt., Dunsan-dong, Seo-gu, Daejeon 302-120 (KR). **KIM, Jae-bum** [KR/KR]; #5-202 Information & Communication, University Dormitory, Hwaam-dong, Yuseong-gu, Daejeon 305-732 (KR). **PARK, Hyun-cheol** [KR/KR]; #409-901 Expoapt., Jeonmin-dong, Yuseong-gu, Daejeon 305-762 (KR).(74) Agent: **SHINSUNG PATENT FIRM**; 2-3f, Line Bldg., 823-30, Yeoksam-dong, Kangnam-ku, Seoul 135-080 (KR).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: IMPROVED ENCODER OF E-8VSB FORWARD ERROR CORRECTION FOR DIGITAL TELEVISION SYSTEM OF ATSC



(57) Abstract: Provided is an error correcting encoder and, more particularly, to an error correcting encoder used for an improved transmission method of the Advanced Television System Committee (ATSC), and a method thereof. The error correcting encoder for digital television broadcasting, which is suggested in the present research, includes a robust encoder for encoding a one-bit input into robust encoded data; a pre-coding block for receiving the robust encoded data and performing pre-coding to thereby produce a pre-coded signal; and a trellis encoding block for performing trellis encoding on the robust encoded data and the pre-coded signal.



**Published:**

— *with international search report*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

IMPROVED ENCODER OF E-8VSB FORWARD ERROR CORRECTION FOR  
DIGITAL TELEVISION SYSTEM OF ATSC

Description

Technical Field

5

The present invention relates to an error correcting code encoder; and, more particularly, to an apparatus for encoding error correcting codes which are used in an advanced transmission method of a terrestrial digital television broadcasting system based on the Advanced Television System Committee (ATSC), and a method thereof.

Background Art

15

Rapid development in digital technology also affects a broadcasting field, and it stimulates the combination between a broadcasting network and the Internet. However, the conventional terrestrial television (TV) broadcasting method of the Advanced Television System Committee (ATSC) has a problem that the broadcasting cannot be received in mobile and portable terminals and even if it is received, the reception performance is poor. Detailed description on the ATSC DTV standards and the A/53 is presented at <http://www.atsc.org>.

25

Fig. 1 is a block diagram showing a conventional digital television (DTV) transmitting block. As illustrated in the drawing, data inputted into the transmitting block 100 are serial data streams each of which includes 188-byte MPEG-compatible data packets including a synch byte and 187-byte payload data. The inputted data are randomized in a data randomizer 101, and each packet is encoded to include 20-byte parity information for Forward Error Correction (FEC), Reed Solomon (RS) coding, and 1/6 data field interleaving, and 2/3 trellis coding. According to the Advanced Television

System Committee (ATSC), the data randomizer 101 performs XOR on all payload data bytes inputted to a pseudo random binary sequence (PRBS) having the maximum length of 16 bits, which is initialized at the starting point of a data field.

5       The RS encoder 103 receives the randomized data and generates data of a total of 207 bytes per data segment by adding 20 RS parity bytes for FEC to the 187-byte data.

      Among the inputted packet data, the randomization and FEC are not performed onto sync data which correspond to a  
10       segment sync signal.

      Subsequently, data packets included in sequential segments of each data field are interleaved in a data interleaver 105, and the interleaved data packets are interleaved again and encoded in a trellis encoder 107.  
15       The trellis encoder 107 generates a stream of a data symbol expressed in three bits by using additional two bits inputted thereto. One bit of the inputted two bits is pre-coded and the other bit goes through a 4-state trellis encoding to be reduced into two bits. The outputted three  
20       bits are mapped to an 8-level symbol. The trellis encoder 107 includes 12 parallel trellis encoders and some pre-coders to generate 12 interleaved and encoded data sequences.

      An 8-level symbols is combined with a segment sync  
25       and field sync bit sequences 117 which are transmitted from a synchronization unit (not shown) to thereby generate data frames for transmission. Subsequently, a pilot signal is added in a pilot adder 111. A symbol stream goes through Vestigial Side Band (VSB) suppressed-carrier modulation in  
30       a VSB modulator 113. An 8-level symbol stream of a baseband is finally transformed into a radio frequency signal in a Radio Frequency (RF) signal converter 115.

      Error correction codes of the ATSC digital terrestrial TV broadcasting use RS codes as external codes  
35       and use concatenated codes formed of 2/3 trellis codes as

internal codes.

Fig. 2 is a block diagram describing a structure of the trellis encoder of Fig. 1. The Fig. 2 shows a structure of the trellis encoder used in an internal error  
5 correcting encoder of the ATSC digital terrestrial TV broadcasting and it shows 8-VSB modulation symbol allocation based on the output of the trellis encoder.

Referring to Fig. 2, the trellis encoder 107 includes a pre-coding block and a 2/3 trellis encoding block. Two  
10 bits  $X_1$  and  $X_2$  from the data interleaver 105 are inputted into the trellis encoding block whose encoding rate is 2/3 to thereby produce three output bits  $z_0$ ,  $z_1$  and  $z_2$ . The output bits  $z_0$ ,  $z_1$  and  $z_2$  are allocated with 8 symbols and they go through 8-VSB modulation in the VSB modulator 113.  
15 The number of memories of the trellis encoder 107 is two and thus, the number of trellis states becomes 4 during decoding.

However, conventional 8-VSB transceivers provide distorted signals in indoor and mobile channel environments  
20 due to variable channel and multipath phenomenon and, for this reason, signal reception performance is poor in receivers. To solve the problem, researchers are studying to develop an advanced transmission scheme having a strong error correction function, and it is called for to develop  
25 an excellent error correcting encoder suitable for the advanced transmission scheme, and an encoding method thereof.

### Disclosure

#### 30 Technical Problem

It is, therefore, an object of the present invention, which is devised to overcome the shortcoming of conventional technologies, to provide an error correcting  
35 encoder for digital television (TV) broadcasting and a

method thereof.

It is another object of the present invention to an error correcting encoder which is improved from the conventional Advanced Television System Committee (ATSC) suitably for an error correction of a dual stream transmission method.

The other objects and advantages of the present invention will be understood by those skilled in the art of the present invention from the drawing, detailed description, and claims of the present invention.

#### Technical Solution

In accordance with one aspect of the present invention, there is provided an error correcting encoder for digital television broadcasting, which includes: a robust encoder for encoding a one-bit input into robust encoded data; a pre-coding block for receiving the robust encoded data and performing pre-coding to thereby produce a pre-coded signal; and a trellis encoding block for performing trellis encoding on the robust encoded data and the pre-coded signal.

In accordance with another aspect of the present invention, there is provided an error-correction encoding method for digital television broadcasting, which includes the steps of: a) encoding a one-bit input into robust encoded data by using shift registers and XOR operation units; b) receiving the robust encoded data and performing pre-coding to thereby produce a pre-coded signal; and c) performing trellis encoding on the robust encoded data and the pre-coded signal.

#### Advantageous Effects

The technology of the present invention can improve

error correction performance by reducing the encoding rate from 2/3 to 1/3 and increasing the number of memories from two to four in an error correcting encoder. Although the final encoding rate is changed from 2/3 to 1/3, the error  
5 correcting encoder still remains compatible with a conventional system using 8-Vestigial Side Band (VSB) scheme by outputting 8 symbols. Therefore, the present invention can provide an internal error correcting encoder suitable for dual stream transmission.

10

#### Description of Drawings

The above and other objects and features of the present invention will become apparent from the following  
15 description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a conventional DTV transmitting block;

Fig. 2 shows a trellis encoder of Fig. 1;

20 Fig. 3 is a block diagram illustrating a structure of an internal error correcting encoder in accordance with an embodiment of the present invention;

Fig. 4 is a block diagram describing the internal error correcting encoder in detail in accordance with an  
25 embodiment of the present invention; and

Fig. 5 is a graph presenting Bit Error Rate (BER) performance curves with respect to a Signal-to-Noise Ratio (SNR) in a conventional encoder and the error correcting encoder of the present invention.

30

#### Best Mode for the Invention

Other objects and aspects of the invention will become apparent from the following description of the embodiments  
35 with reference to the accompanying drawings, which is set

forth hereinafter. Also, when it is considered that detailed description on a related art may obscure the points of the present invention, the description will not be provided herein. Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings.

Fig. 3 is a block diagram illustrating a structure of an internal error correcting encoder in accordance with an embodiment of the present invention. The internal error correcting encoder of Fig. 3 can be applied to an improved transmission method of digital terrestrial television (TV) broadcasting.

Referring to Fig. 3, the internal error correcting encoder includes a robust encoder 10, a pre-coding block 20, and a trellis encoding block 30. The robust encoder 10 receives a one-bit input signal  $X_1'$  from an interleaver (not shown) and outputs  $X_1$  and  $X_2$  which correspond to input data of a conventional internal error correcting encoder. The pre-coding block 20 receives the  $X_2$  and outputs a  $Z_2$  symbol. The trellis encoding block 30 receives  $X_1$  and  $X_2$  and outputs  $Z_0$  and  $Z_1$  symbols at an encoding rate of  $2/3$ . The internal error correcting encoder of the present invention further includes the robust encoder 10 in addition to the conventional encoder. A trellis encoder which is formed of the pre-coding block 20 and the trellis encoding block 30 follows structure defined in the Advanced Television System Committee (A/53) Standards. Thus, each of the pre-coding block and the trellis encoding block includes a register (D) for storing a bit delay value, for example, 12-bit delay value. The internal error correcting encoder finally outputs  $Z_0$ ,  $Z_1$  and  $Z_2$  and the encoding rate becomes  $1/3$ . Although the final encoding rate is  $1/3$ , the internal error correcting encoder can maintain the compatibility with devices of conventional transmission schemes by outputting 8 symbols.

Fig. 4 is a block diagram describing the internal error correcting encoder in detail in accordance with an embodiment of the present invention.

Referring to Fig. 4, bits  $X_1(k)$  and  $X_2(k)$  corresponding to the input of a conventional encoder which receives an input bit  $X'_1(k)$  at time  $k$  are outputted as shown in the following equations.

$$\begin{aligned} X_1(k) &= X'_1(k-1) \\ X_2(k) &= Z_2(k-1) \oplus \{X'_1(k) \oplus X'_1(k-1) \oplus X'_1(k-2)\} \end{aligned} \quad \text{Eq. 1}$$

where  $\oplus$  denotes an exclusive-or (XOR) operation; and  $X(k-d)$  denotes a bit signal of  $X$  delayed by  $d$  at time  $k$ .

15

Referring to Fig. 4 and the Equation 1, the error correcting encoder of the present invention encodes input signals by using a total of four memories, i.e., two memories in a standard trellis encoder and two memories 401 and 402 in the robust encoder 10.

20

Output signals based on the input of the internal error correcting encoder presented according to the Equation 1 and the state thereof are as shown in Tables 1 and 2.

25

Table 1

|   | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | -7 | -5 | -7 | -5 | 1  | 3  | 1  | 3  | -3 | -1 | -3 | -1 | 5  | 7  | 5  | 7  |
| 1 | 1  | 3  | 1  | 3  | -7 | -5 | -7 | -5 | 5  | 7  | 5  | 7  | -3 | -1 | -3 | -1 |

Table 2

|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|--|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
|--|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|

|   |    |    |    |    |    |    |    |    |   |    |   |    |   |    |   |    |
|---|----|----|----|----|----|----|----|----|---|----|---|----|---|----|---|----|
| 0 | 0  | 2  | 1  | 3  | 0  | 2  | 1  | 3  | 5 | 7  | 4 | 6  | 5 | 7  | 4 | 6  |
| 1 | 12 | 14 | 13 | 15 | 12 | 14 | 13 | 15 | 9 | 11 | 8 | 10 | 9 | 11 | 8 | 10 |

Since the robust encoder 10 has two memories, the total number of memories of the internal error correcting encoder becomes four. Thus, the number of trellis states becomes 16 after decoding.

In the specification of the present invention, the robust encoded data are the output signals  $X_1$  and  $X_2$  of the robust encoder 10.

When internal error-correction encoding is carried out as described in the embodiment, a receiving part can improve the performance of its receiver by performing trellis decoding with reference to the Tables 1 and 2. To be specific, the receiving part converts a receiving signal into a baseband signal, performs equalization for determining the symbol level of the receiving signal, and decodes the determined symbol level into a data symbol such that the symbol level and the state corresponding thereto are as shown in the Tables 1 and 2. Detailed description on the receiving part is presented in Korean Patent Publication No. 2004-64306.

#### <Experimental result>

Computer simulation results on the performance of the conventional encoder shown in Fig. 1 and the internal error correcting encoder of Fig. 4 will be described herein. Fig. 5 is a graph showing Bit Error Rate (BER) performance curves with respect to a Signal-to-Noise Ratio (SNR) in the conventional encoder and the error correcting encoder of the present invention. Herein, an Additive White Gaussian Noise (AWGN) model was used as a noise channel, an error rate was computed by using a Monte Carlo simulation method and dividing the entire errors by transmitted data.

The result was that the internal error correcting

encoder of the present invention had power gain of about 7dB compared to the conventional encoder, with respect to a bit error rate  $10^{-5}$ .

5       The method of the present invention is realized as a program and stored in a computer-readable recording medium, such as CD-ROM, RAM, ROM, floppy disks, hard disks, and magneto-optical disk and the like. Since this process can be easily implemented by those of ordinary skill in the art, detailed description on it will not be provided herein.

10       While the present invention has been described with respect to certain preferred embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.

What is claimed is:

1. An error correcting encoder for digital television broadcasting, comprising:

5 a robust encoder for encoding a one-bit input into robust encoded data;

a pre-coding block for receiving the robust encoded data and performing pre-coding to thereby produce a pre-coded signal; and

10 a trellis encoding block for performing trellis encoding on the robust encoded data and the pre-coded signal.

2. The error correcting encoder as recited in claim 15 1, wherein the robust encoder performs robust encoding based on equations:

$$X_1(k) = X_1'(k-1)$$

$$X_2(k) = Z_2(k-1) \oplus \{X_1'(k) \oplus X_1'(k-1) \oplus X_1'(k-2)\}$$

20 where  $\oplus$  denotes an exclusive-or (XOR) operation; and  $X(k-d)$  denotes a bit signal of X delayed by d at time k.

3. The error correcting encoder as recited in claim 25 1, wherein a one-bit data symbol is encoded such that an output symbol level of the trellis encoder and a state corresponding thereto are as shown in Tables 1 and 2:

Table 1

|   | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | -7 | -5 | -7 | -5 | 1  | 3  | 1  | 3  | -3 | -1 | -3 | -1 | 5  | 7  | 5  | 7  |
| 1 | 1  | 3  | 1  | 3  | -7 | -5 | -7 | -5 | 5  | 7  | 5  | 7  | -3 | -1 | -3 | -1 |

Table 2

|   | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8 | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| 0 | 0  | 2  | 1  | 3  | 0  | 2  | 1  | 3  | 5 | 7  | 4  | 6  | 5  | 7  | 4  | 6  |
| 1 | 12 | 14 | 13 | 15 | 12 | 14 | 13 | 15 | 9 | 11 | 8  | 10 | 9  | 11 | 8  | 10 |

4. The error correcting encoder as recited in claim 1, wherein the robust encoder generates robust encoded data  $X_1$  and  $X_2$  by using two shift registers and two X-OR operation units.

5. An error-correction encoding method for digital television broadcasting, comprising the steps of:

10 a) encoding a one-bit input into robust encoded data by using shift registers and XOR operation units;

b) receiving the robust encoded data and performing pre-coding to thereby produce a pre-coded signal; and

15 c) performing trellis encoding on the robust encoded data and the pre-coded signal.

6. The method as recited in claim 5, wherein, in the step a), the robust encoding is performed based on equations:

20 
$$X_1(k) = X_1'(k-1)$$

$$X_2(k) = Z_2(k-1) \oplus \{X_1'(k) \oplus X_1'(k-1) \oplus X_1'(k-2)\}$$

where  $\oplus$  denotes an exclusive-or (XOR) operation; and

25  $X(k-d)$  denotes a bit signal of X delayed by d at time k.

7. The error correcting encoder as recited in claim 5, wherein, in the step c), a one-bit data symbol is encoded such that an output symbol level of the trellis encoding and a state corresponding thereto are as shown in

30

Tables 1 and 2:

Table 1

|   | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | -7 | -5 | -7 | -5 | 1  | 3  | 1  | 3  | -3 | -1 | -3 | -1 | 5  | 7  | 5  | 7  |
| 1 | 1  | 3  | 1  | 3  | -7 | -5 | -7 | -5 | 5  | 7  | 5  | 7  | -3 | -1 | -3 | -1 |

5 Table 2

|   | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8 | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| 0 | 0  | 2  | 1  | 3  | 0  | 2  | 1  | 3  | 5 | 7  | 4  | 6  | 5  | 7  | 4  | 6  |
| 1 | 12 | 14 | 13 | 15 | 12 | 14 | 13 | 15 | 9 | 11 | 8  | 10 | 9  | 11 | 8  | 10 |

8. An error correcting decoder for digital television broadcasting, comprising:

a receiving means for converting a receiving signal  
10 into a baseband signal;

an equalizing means for determining a symbol level of the receiving signal; and

a decoding means for decoding the symbol level into a data symbol such that a symbol level and a state  
15 corresponding thereto are as shown in Tables 1 and 2:

Table 1

|   | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | -7 | -5 | -7 | -5 | 1  | 3  | 1  | 3  | -3 | -1 | -3 | -1 | 5  | 7  | 5  | 7  |
| 1 | 1  | 3  | 1  | 3  | -7 | -5 | -7 | -5 | 5  | 7  | 5  | 7  | -3 | -1 | -3 | -1 |

Table 2

|   | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8 | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| 0 | 0  | 2  | 1  | 3  | 0  | 2  | 1  | 3  | 5 | 7  | 4  | 6  | 5  | 7  | 4  | 6  |
| 1 | 12 | 14 | 13 | 15 | 12 | 14 | 13 | 15 | 9 | 11 | 8  | 10 | 9  | 11 | 8  | 10 |

9. An error-correcting decoding method for digital television broadcasting, comprising the steps of:

5 a) converting a receiving signal into a baseband signal;

b) determining a symbol level of the receiving signal; and

10 c) decoding the symbol level into a data symbol such that a symbol level and a state corresponding thereto are as shown in Tables 1 and 2:

Table 1

|   | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | -7 | -5 | -7 | -5 | 1  | 3  | 1  | 3  | -3 | -1 | -3 | -1 | 5  | 7  | 5  | 7  |
| 1 | 1  | 3  | 1  | 3  | -7 | -5 | -7 | -5 | 5  | 7  | 5  | 7  | -3 | -1 | -3 | -1 |

Table 2

|   | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8 | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| 0 | 0  | 2  | 1  | 3  | 0  | 2  | 1  | 3  | 5 | 7  | 4  | 6  | 5  | 7  | 4  | 6  |
| 1 | 12 | 14 | 13 | 15 | 12 | 14 | 13 | 15 | 9 | 11 | 8  | 10 | 9  | 11 | 8  | 10 |

15

1/3

FIG. 1

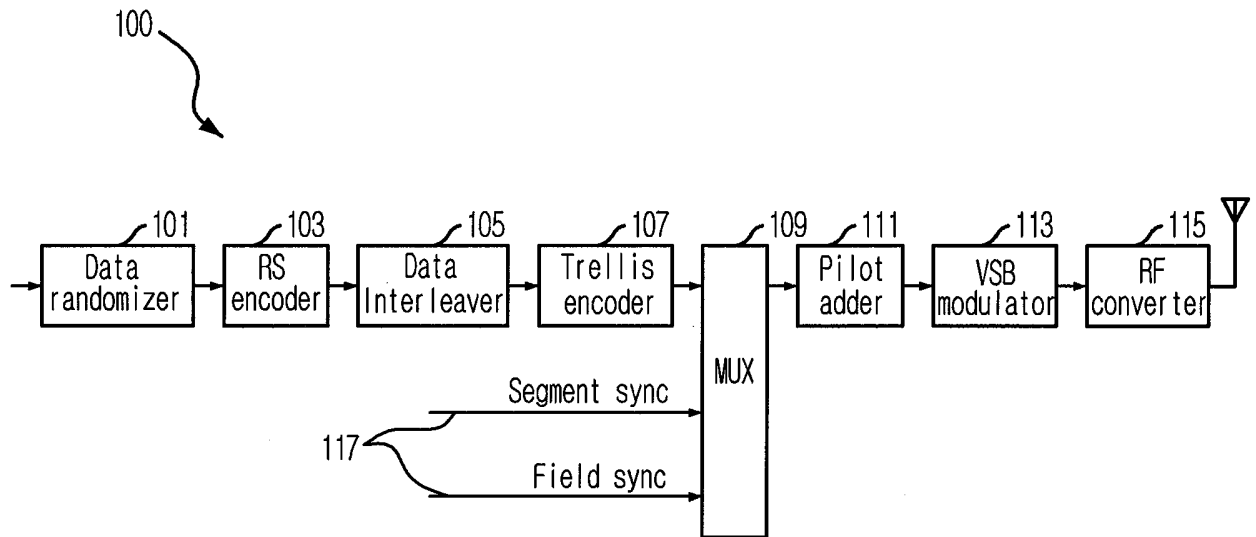


FIG. 2

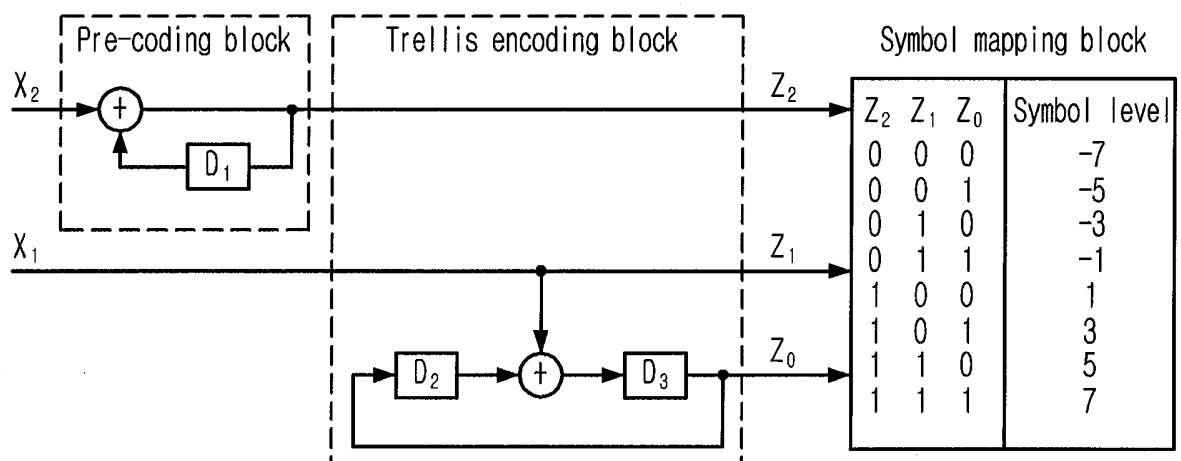


FIG. 3

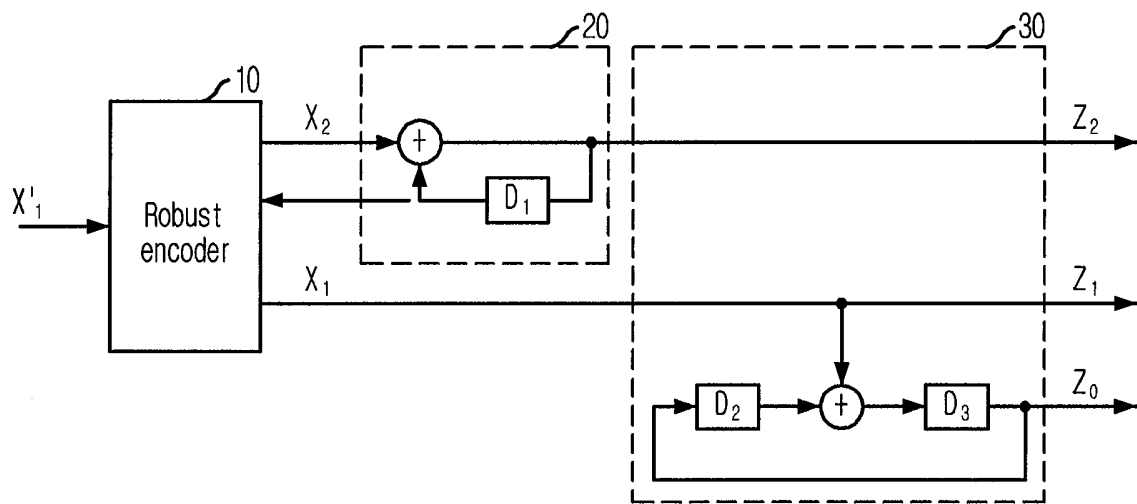


FIG. 4

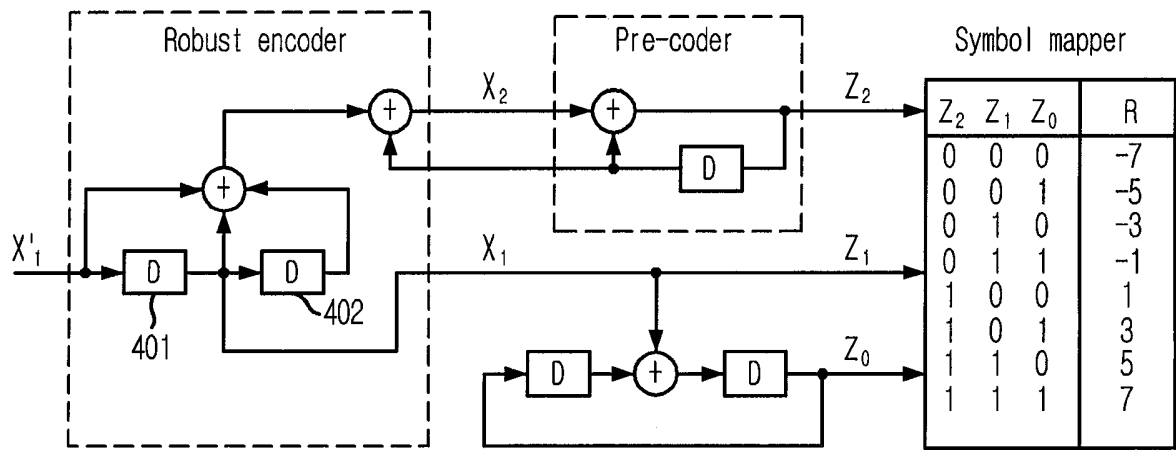
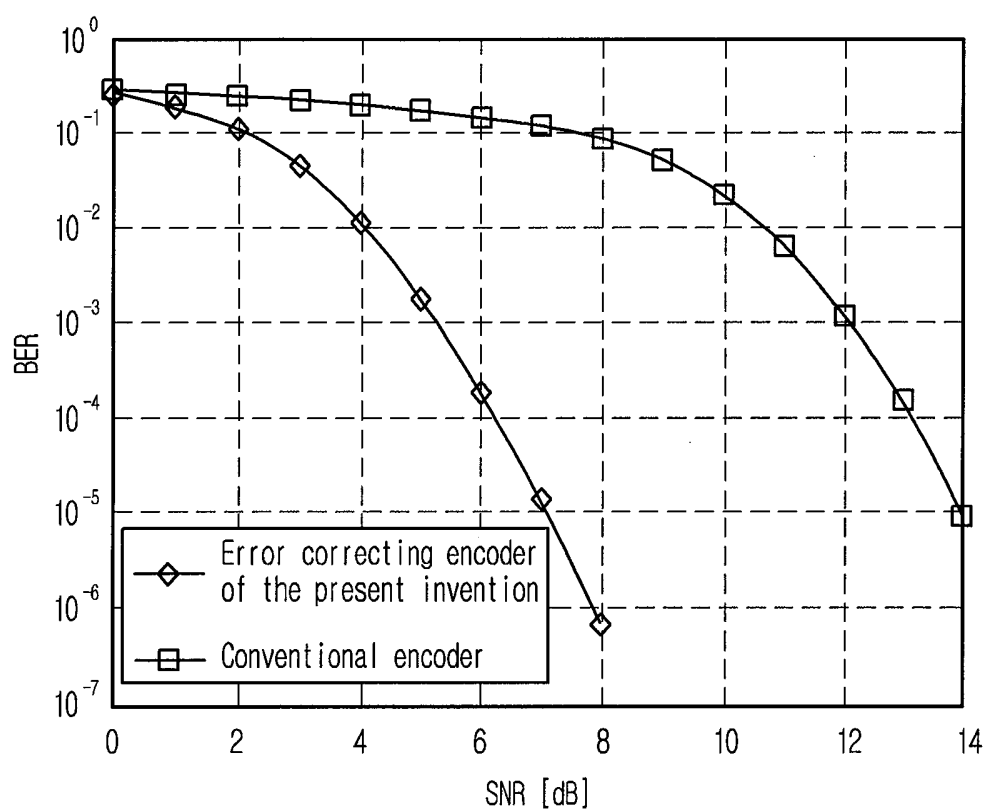


FIG. 5



## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/KR2006/000538**A. CLASSIFICATION OF SUBJECT MATTER****H04N 7/015(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC8 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Patents and applications for inventions since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS " coding, encoding, encrypt, decoding, error correct,

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|-----------|------------------------------------------------------------------------------------|-----------------------|
| A         | US2002041608A1(LG ELECTRONICS) 2002-04-11<br>SEE THE WHOLE PAPER                   | 1-9                   |
| A         | US2002041634A1(LG ELECTRONICS) 2002-04-11<br>SEE THE WHOLE PAPE                    | 1-9                   |
| A         | US2002172277A1(LG ELECTRONICS) 2002-11-21<br>SEE THE WHOLE PAPE                    | 1-9                   |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

25 MAY 2006 (25.05.2006)

Date of mailing of the international search report

**25 MAY 2006 (25.05.2006)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office  
920 Dunsan-dong, Seo-gu, Daejeon 302-701,  
Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

JANG, Hyun Geun

Telephone No. 82-42-481-5775



**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

PCT/KR2006/000538

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s)                                                                              | Publication<br>date                                                                            |
|-------------------------------------------|---------------------|---------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|
| US2002041608A1                            | 11.04.2002          | CN1186932C<br>CN1346212A<br>KR1020020024697A                                                            | 26.01.2005<br>24.04.2002<br>01.04.2002                                                         |
| US2002041634A1                            | 11.04.2002          | CN1163037C<br>CN1349335A<br>KR1020020026624                                                             | 18.08.2004<br>15.05.2002<br>12.04.2002                                                         |
| US2002172277A1                            | 21.11.2002          | BR200112186A<br>CA2410783A1<br>CN1231056C<br>CN1437825A<br>MXPA02012327A<br>US6947487BB<br>W002085014A1 | 20.05.2003<br>24.10.2002<br>07.12.2005<br>20.08.2003<br>06.09.2004<br>20.09.2005<br>24.10.2002 |