Title: SEMICONDUCTOR PRODUCT WITH A SILVER AND GOLD ALLOY

Abstract: A semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy forms an outside layer of the product. Moreover, the present invention pertains to a semiconductor substrate comprising a silver and gold alloy layer, wherein the silver and gold alloy forms an outside layer of the semiconductor substrate. The present invention has a particular application in having a silver and gold alloy form the outside layer of various items, including a lead frame, a board grid array, a header, a printed circuit board, a Reed switch, and a connector.
This application is related to and claims priority to Korean Patent Application No. 10-2000-0048799, filed August 23, 2000, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates to a semiconductor product comprising a silver and gold alloy layer, wherein the silver and gold alloy forms an outside layer of the product. Moreover, the present invention pertains to a semiconductor substrate comprising a silver and gold alloy layer, wherein the silver and gold alloy forms an outside layer of the semiconductor substrate. The present invention has a particular application in having a silver and gold alloy form the outside layer of various items, including a lead frame, a ball grid array, a header, a printed circuit board, a Reed switch, and a connector.
2. Description of the Related Art

Generally, substrates for a semiconductor device make electrical interconnections between electrical and electronic devices, which includes such devices as a semiconductor chip and a printed circuit board ("PCB"). Moreover, the characteristics of a good substrate material include bondability to connecting wires, durability from corrosion, adhesion to the mold resin (which typically act as a cover), and ductility for manipulation.

To achieve such characteristics, conventional substrates for a semiconductor device have used an outermost layer of Sn-Pb in a multi-plated layer structure also including a copper layer and a nickel layer. However, lead is widely considered to be a health hazard. Lead is toxic to human individuals and it has a long history of documented adverse impact on humans and the environment. Thus, the U.S. Congress and the Environmental Protection Agency have been concerned about the use of lead in the electrical and electronic industries.

Conventionally, alternatives to the Sn-Pb layer have been a palladium layer or a gold layer as the outermost layer. However, a palladium layer or a gold layer has manifested problems in wire bondability, adhesion to the mold resin, and attachment characteristics for a PCB. Additionally, the costs of palladium and of gold have traditionally been fairly high.
SUMMARY OF THE INVENTION

An object of the present invention is to provide semiconductor devices that are lead-free and thus environmentally friendly, while at the same, providing the desired characteristics of improved bondability, corrosion durability, adhesion to mold resin, ductility, and cost effectiveness.

In one embodiment of the present invention, a semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product.

In another embodiment of the present invention, a semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product, and wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight.

In another embodiment of the present invention, a semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches.

In another embodiment of the present invention, a semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches.

In another embodiment of the present invention, a semiconductor product
comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches.

In another embodiment of the present invention, a semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches.

In another embodiment of the present invention, a semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product, and further comprises a nickel layer positioned beneath said silver and gold alloy.

In another embodiment of the present invention, a semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further
comprises a nickel layer positioned beneath the silver and gold alloy, wherein a
thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a semiconductor product
comprises a silver and gold alloy layer, wherein the silver and gold alloy layer
forms an outside layer of the semiconductor product, and wherein a thickness of
the silver and gold alloy layer ranges from 3 to 160 microinches, and further
comprises a nickel layer positioned beneath the silver and gold alloy, wherein a
thickness of the nickel layer ranges from 20 to 100 microinches.

In another embodiment of the present invention, a semiconductor product
comprises a silver and gold alloy layer, wherein the silver and gold alloy layer
forms an outside layer of the semiconductor product, and wherein a thickness of
the silver and gold alloy layer ranges from 5 to 20 microinches, and further
comprises a nickel layer positioned beneath the silver and gold alloy, wherein a
thickness of the nickel layer ranges from 20 to 100 microinches.

In another embodiment of the present invention, a semiconductor product
comprises a silver and gold alloy layer, wherein the silver and gold alloy layer
forms an outside layer of the semiconductor product, wherein a gold composition
of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a
thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and
further comprises a nickel layer positioned beneath the silver and gold alloy,
wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a semiconductor product
comprises a silver and gold alloy layer, wherein the silver and gold alloy layer
forms an outside layer of the semiconductor product, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 20 to 100 microinches.

In another embodiment of the present invention, a semiconductor product comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the semiconductor product, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 20 to 100 microinches.

For each one of the above-described embodiments, the semiconductor product may more specifically comprise a substrate, a lead frame, a ball grid array ("BGA"), or a header. Furthermore, the above embodiments may also apply to a PCB, a Reed switch, or a connector. Moreover, the silver and gold
alloy may further comprise 1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium. Also, present invention may be applicable to other types of semiconductor or electrical devices.

Thus, in another embodiment of the present invention, the semiconductor product may comprise a substrate, and the substrate may comprise a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, and wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver
and gold alloy layer ranges from 3 to 160 microinches.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, and further comprises a nickel layer positioned beneath said silver and gold alloy.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a substrate comprises a
silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 20 to 100 microinches.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 20 to 100 microinches.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a
nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 20 to 100 microinches.

In another embodiment of the present invention, a substrate comprises a silver and gold alloy layer, wherein the silver and gold alloy layer forms an outside layer of the substrate, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 20 to 100 microinches.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements (generally ball-shaped), a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver
and gold layer.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microns.
of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches.
In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and further comprises a nickel layer positioned beneath said silver and gold alloy.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one
of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 20 to 100 microinches.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and
further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 20 to 100 microinches.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20
microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 10 to 300 microinches.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 20 to 100 microinches.

In another embodiment of the present invention, a semiconductor product comprises a ball grid array comprising a plurality of soldering elements, a plurality of ball pad areas, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements, a pad area for receiving a semiconductor chip, and a plurality of lead areas, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight,
and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer ranges from 20 to 100 microinches.

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BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned aspects and other features of the invention will be explained in the following description, taken in conjunction with the accompanying drawings wherein:

Fig. 1 is a diagram illustrating an embodiment of the present invention;

Fig. 2 is a diagram illustrating another embodiment of the present invention;

Fig. 3 is a diagram illustrating another embodiment of the present invention;

Fig. 4a is a diagram illustrating another embodiment of the present invention;

Fig. 4b is a diagram illustrating another embodiment of the present invention;

Fig. 5a is a diagram illustrating another embodiment of the present invention;

Fig. 5b is a diagram illustrating another embodiment of the present invention;
Fig. 6a is a diagram illustrating another embodiment of the present invention;
Fig. 6b is a diagram illustrating another embodiment of the present invention;
Fig. 6a and 6c is a diagram illustrating another embodiment of the present invention;
Fig. 7a is a diagram illustrating another embodiment of the present invention;
Fig. 7b is a diagram illustrating another embodiment of the present invention;
Fig. 8a is a diagram illustrating another embodiment of the present invention;
Fig. 8b is a diagram illustrating another embodiment of the present invention;
Fig. 8c is a diagram illustrating another embodiment of the present invention;
Fig. 9a is a diagram illustrating another embodiment of the present invention;
Fig. 9b is a diagram illustrating another embodiment of the present invention;
Fig. 9c is a diagram illustrating another embodiment of the present invention;
Fig. 10a is a diagram illustrating another embodiment of the present invention;
invention; and

Fig. 10b is a diagram illustrating another embodiment of the present invention;

DETAILED DESCRIPTION

The present invention will be described in detail, with reference to the accompanying drawings.

Fig. 1 shows an embodiment according to the present invention. A semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10. Also, there may be additional layers, such as a nickel layer 12 beneath the silver and gold layer 11 and a copper layer 13 beneath the nickel layer. The semiconductor product, as will be discussed below, can be a variety of items including, but not limited to, a substrate, a lead frame, a BGA, and a header.

In another embodiment of the present invention, also illustrated by Fig. 1, a semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10, and wherein a gold composition of the silver and gold alloy layer 11 ranges from 5 to 50% by weight.

In another embodiment of the present invention, as also illustrated by Fig. 1, a semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor
product 10, and wherein a thickness of the silver and gold alloy layer 11 ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10, and wherein a thickness of the silver and gold alloy layer 11 ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10, wherein a gold composition of the silver and gold alloy layer 11 ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 11 ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10, wherein a gold composition of the silver and gold alloy layer 11 ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 11 ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10, and further comprises a nickel layer 12 positioned beneath the silver and gold
alloy 11. Also, a copper layer may also lie under the nickel layer 12.

In another embodiment of the present invention, also illustrated by Fig. 1, a semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10, and wherein a thickness of the silver and gold alloy layer 11 ranges from 3 to 160 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 12 ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10, and wherein a thickness of the silver and gold alloy layer 11 ranges from 5 to 20 microinches, and further comprises a nickel layer positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 12 ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10, and wherein a thickness of the silver and gold alloy layer 11 ranges from 3 to 160 microinches, and further comprises a nickel layer 12 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 12 ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a
semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the
silver and gold alloy layer 11 forms an outside layer of the semiconductor product
10, and wherein a thickness of the silver and gold alloy layer 11 ranges from 5 to
20 microinches, and further comprises a nickel layer 12 positioned beneath the
silver and gold alloy, wherein a thickness of the nickel layer 12 ranges from 20 to
100 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a
semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the
silver and gold alloy layer 11 forms an outside layer of the semiconductor product
10, wherein a gold composition of the silver and gold alloy layer 11 ranges from
5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 11
ranges from 3 to 160 microinches, and further comprises a nickel layer 12
positioned beneath the silver and gold alloy, wherein a thickness of the nickel
layer 12 ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a
semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the
silver and gold alloy layer 11 forms an outside layer of the semiconductor product
10, wherein a gold composition of the silver and gold alloy layer 11 ranges from
5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 11
ranges from 5 to 20 microinches, and further comprises a nickel layer 12
positioned beneath the silver and gold alloy, wherein a thickness of the nickel
layer 12 ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a
semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10, wherein a gold composition of the silver and gold alloy layer 11 ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 11 ranges from 3 to 160 microinches, and further comprises a nickel layer 12 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 12 ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated by Fig. 1, a semiconductor product 10 comprises a silver and gold alloy layer 11, wherein the silver and gold alloy layer 11 forms an outside layer of the semiconductor product 10, wherein a gold composition of the silver and gold alloy layer 11 ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 11 ranges from 5 to 20 microinches, and further comprises a nickel layer 12 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 12 ranges from 20 to 100 microinches.

In the present invention, the silver and gold layer as the outermost layer improves bondability, prevents oxidation of the lower layers, improves adhesion between the different layers, and improves the adhesion to the mold resin. Silver, when used alone, adsorbs moisture from the air and causes problems in the molding process. Moreover, use of the silver and gold alloy layer avoids having to use Sn-Pb, with its concomitant health and environmental problems with lead.

In the present invention, the nickel layer prevents the diffusion of copper from the copper layer, improves the attachment of semiconductor chip package
on the printed circuit board, improves solderability, and bondability when a gold wire makes the interconnection of a substrate to a semiconductor chip.

In another embodiment of the present invention, as illustrated in Fig. 2, the semiconductor product comprises a substrate 20. The substrate 20 may comprise a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20. Also, there may additional layers, such as a nickel layer 22 beneath the silver and gold layer 21 and a copper layer 23 beneath the nickel layer.

In another embodiment of the present invention, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, and wherein a gold composition of the silver and gold alloy layer 21 ranges from 5 to 50% by weight.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, and wherein a thickness of the silver and gold alloy layer 21 ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, and wherein a thickness of the silver and gold alloy layer 21 ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, wherein a gold
composition of the silver and gold alloy layer 21 ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 21 ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, wherein a gold composition of the silver and gold alloy layer 21 ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 21 ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, and further comprises a nickel layer 22 positioned beneath said silver and gold alloy.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, and wherein a thickness of the silver and gold alloy layer 21 ranges from 3 to 160 microinches, and further comprises a nickel layer 22 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 22 ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, and wherein a
thickness of the silver and gold alloy layer 21 ranges from 5 to 20 microinches, and further comprises a nickel layer 22 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 22 ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, and wherein a thickness of the silver and gold alloy layer 21 ranges from 3 to 160 microinches, and further comprises a nickel layer 22 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 22 ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, and wherein a thickness of the silver and gold alloy layer 21 ranges from 5 to 20 microinches, and further comprises a nickel layer 22 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 22 ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, wherein a gold composition of the silver and gold alloy layer 21 ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 21 ranges from 3 to 160
microinches, and further comprises a nickel layer 22 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 22 ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, wherein a gold composition of the silver and gold alloy layer 21 ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 21 ranges from 5 to 20 microinches, and further comprises a nickel layer 22 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 22 ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, wherein a gold composition of the silver and gold alloy layer 21 ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 21 ranges from 3 to 160 microinches, and further comprises a nickel layer 22 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 22 ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 2, a substrate 20 comprises a silver and gold alloy layer 21, wherein the silver and gold alloy layer 21 forms an outside layer of the substrate 20, wherein a gold composition of the silver and gold alloy layer 21 ranges from 5 to 50% by weight,
and wherein a thickness of the silver and gold alloy layer 21 ranges from 5 to 20 microinches, and further comprises a nickel layer 22 positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 22 ranges from 20 to 100 microinches.

In another embodiment of the present invention, as illustrated in Figs. 3 and 4b, the semiconductor product comprises a lead frame 30. The lead frame 30 may comprise a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30.

As illustrated in Fig. 3, a lead frame 30 generally includes a ball pad area 32 and a plurality of leads 33. The present invention’s silver and gold alloy layer 31b forms an outside layer of at least one of the ball pad area 32 and a lead 33, which is shown in Fig. 4b as a cross-section of either a ball pad area or a lead.

Furthermore, in a conventional lead frame 30a, as shown in Fig. 4a, the outer layer 31a is a layer of Sn-Pb, a palladium layer, or a gold layer. Moreover, the outer layer 31a may lie over a layer of nickel 34a, which may in turn lie over a layer of copper 35a.

In the present embodiment, as illustrated in Fig. 4b, the outside layer comprises a silver and gold alloy layer 31b, thereby avoiding the environmental and health problems associated with an Sn-Pb layer, and the performance and cost problems associated with a palladium layer and with a gold layer.

As illustrated in Fig. 4b, the silver and gold alloy layer 31b may lie over a nickel layer 34b, and the nickel layer 34b may lie over a copper layer 35b.

In another embodiment of the present invention, also illustrated in Fig. 4b,
a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, and wherein a gold composition of the silver and gold alloy layer 31b ranges from 5 to 50% by weight.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, and wherein a thickness of the silver and gold alloy layer 31b ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, and wherein a thickness of the silver and gold alloy layer 31b ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, wherein a gold composition of the silver and gold alloy layer 31b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 31b ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, wherein a
gold composition of the silver and gold alloy layer 31b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 31b ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, and further comprises a nickel layer 34b positioned beneath said silver and gold alloy.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, and wherein a thickness of the silver and gold alloy layer 31b ranges from 3 to 160 microinches, and further comprises a nickel layer 34b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 34b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, and wherein a thickness of the silver and gold alloy layer 31b ranges from 5 to 20 microinches, and further comprises a nickel layer 34b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 34b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver
and gold alloy layer 31b forms an outside layer of the lead frame 30b, and wherein a thickness of the silver and gold alloy layer 31b ranges from 3 to 160 microinches, and further comprises a nickel layer 34b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 34b ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, and wherein a thickness of the silver and gold alloy layer 31b ranges from 5 to 20 microinches, and further comprises a nickel layer 34b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 34b ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, wherein a gold composition of the silver and gold alloy layer 31b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 31b ranges from 3 to 160 microinches, and further comprises a nickel layer 34b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 34b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, wherein a
gold composition of the silver and gold alloy layer 31b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 31b ranges from 5 to 20 microinches, and further comprises a nickel layer 34b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 34b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, wherein a gold composition of the silver and gold alloy layer 31b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 31b ranges from 3 to 160 microinches, and further comprises a nickel layer 34b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 34b ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 4b, a lead frame 30b comprises a silver and gold alloy layer 31b, wherein the silver and gold alloy layer 31b forms an outside layer of the lead frame 30b, wherein a gold composition of the silver and gold alloy layer 31b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 31b ranges from 5 to 20 microinches, and further comprises a nickel layer 34b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 34b ranges from 20 to 100 microinches.

In another embodiment of the present invention, as illustrated in Fig. 10b, the lead frame is disclosed with greater specificity. The lead frame 100b thus
further comprises a semiconductor chip 102b and a plurality of wires 103b, wherein a first end of each of one of the plurality of wires 103b is bonded onto the semiconductor chip 102b, and a second end of each one of the plurality of wires 103b is bonded onto the silver and gold layer 101b. This more detailed embodiment can be combined and applied with all of the above described other lead frame embodiments.

Also, a mold resin 106b covers the assembly as shown in Fig. 10b, and a nickel layer 107b may lie beneath the silver and gold layer 101b, with a copper layer 105b under the nickel layer 107b.

In a conventional lead frame 100a, as shown in Fig. 10a, the layer 101a may be silver and the layer 104a may be Sn-Pb.

In the present embodiment, as illustrated in Fig. 10b, the outside layer comprises a silver and gold alloy layer 101b, thereby avoiding the environmental and health problems associated with lead.

In another embodiment of the present invention, as illustrated in Figs. 5b, the semiconductor product comprises a ball grid array 50b. The ball grid array 50b may comprise a silver and gold alloy layer 51b, wherein the silver and gold alloy layer 51b forms an outside layer of the ball grid array 50b.

Generally, as illustrated in Figs. 5a, a BGA comprises a plurality of soldering elements 58a, a plurality of ball pad areas defined by layers 51a and 57a, wherein each one of the plurality of ball pad areas 51a and 57a receives a respective one of the plurality of soldering elements 58a, a pad area 59a for receiving a semiconductor chip, and a plurality of lead areas defined by layers.
51a, 54a, and 55a. A semiconductor chip 52a may then be placed on top of a pad area 59a and be connected to another lead area via a wire 53a (which may be formed from Au/Al). The arrangement may then be covered with a mold resin (not shown). The soldering elements are generally ball-shaped, but of course, other shapes are possible (including, but not limited to, a bump or half-ball-shaped elements).

In a conventional ball grid array 50a, as shown in Fig. 5a, the outer layer 51a of the ball pad areas, pad area, and the lead areas may be a gold layer. Moreover, the outer layer 51a may lie over a layer of nickel 54a, which may in turn lie over a layer of copper 55a. The layers are surrounded by a material 56a made out of typically, PI film, ceramic, or plastic.

In the present embodiment, as illustrated in Fig. 5b, the outside layer comprises a silver and gold alloy layer 51b, thereby avoiding the performance and cost problems associated with a gold layer.

As illustrated in Fig. 5b, the silver and gold alloy layer 51b may lie over a nickel layer 54b, and the nickel layer 54b may lie over a copper layer 55b.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for
receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Fig. 5b,
a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and
57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and further comprises a nickel layer 54b positioned beneath said silver and gold alloy.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a
semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer 54b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 54b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer 54b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 54b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one
of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer 54b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 54b ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer 54b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 54b ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and
57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer 54b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 54b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer 54b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 54b ranges from 10 to 300 microinches.
In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer ranges from 3 to 160 microinches, and further comprises a nickel layer 54b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 54b ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 5b, a semiconductor product comprises a ball grid array 50b comprising a plurality of soldering elements 58b, a plurality of ball pad areas defined by layers 51b and 57b, wherein each one of the plurality of ball pad areas receives a respective one of the plurality of soldering elements 58b, a pad area 59b for receiving a semiconductor chip, and a plurality of lead areas defined by layers 51b, 54b, and 55b, wherein at least one of the plurality of ball pad areas, a pad area for receiving a semiconductor chip, and the plurality of lead areas comprise the silver and gold layer, wherein a gold composition of the silver and gold alloy layer ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold
alloy layer ranges from 5 to 20 microinches, and further comprises a nickel layer 54b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 54b ranges from 20 to 100 microinches.

In another embodiment of the present invention, as illustrated in Figs. 6a and 6c, the semiconductor product comprises a header 60a. The header 60a may comprise a glass top portion 62a with a plurality of leads 63a, wherein the silver and gold alloy layer 61c forms an outside layer of the plurality of leads 63a (as shown in cross-section in Fig. 6a and 6c).

In a conventional lead for a header, as shown in Fig. 6b, the outer layer 61b of may be a gold layer. Moreover, the outer layer 61b may lie over a layer of nickel 64b, which may in turn lie over a layer of copper 65b.

Again, as noted above, in the present embodiment, as illustrated in Fig. 6a and 6c, the outside layer comprises a silver and gold alloy layer 61c, thereby avoiding the performance and cost problems associated with a gold layer.

As illustrated in Fig. 61c, the silver and gold alloy layer 61c may lie over a nickel layer 64c, and the nickel layer 64c may lie over a copper layer 65c.

In another embodiment of the present invention, also illustrated in Fig. 6a and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of the plurality of leads 63a of header 60a, and wherein a gold composition of the silver and gold alloy layer 61c ranges from 5 to 50% by weight.

In another embodiment of the present invention, also illustrated in Fig. 6a and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy
layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of
the plurality of leads 63a of header 60a, and wherein a thickness of the silver and
gold alloy layer 61c ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Fig. 6a
and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy
layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of
the plurality of leads 63a of header 60a, and wherein a thickness of the silver and
gold alloy layer 61c ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Fig. 6a
and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy
layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of
the plurality of leads 63a of header 60a, wherein a gold composition of the silver
and gold alloy layer 61c ranges from 5 to 50% by weight, and wherein a
thickness of the silver and gold alloy layer 61c ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Fig. 6a
and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy
layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of
the plurality of leads 63a of header 60a, wherein a gold composition of the silver
and gold alloy layer 61c ranges from 5 to 50% by weight, and wherein a
thickness of the silver and gold alloy layer 61c ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Fig. 6a
and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy
layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of
the plurality of leads 63a of header 60a, and further comprises a nickel layer 64c positioned beneath said silver and gold alloy.

In another embodiment of the present invention, also illustrated in Fig. 6a and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of the plurality of leads 63a of header 60a, and wherein a thickness of the silver and gold alloy layer 61c ranges from 3 to 160 microinches, and further comprises a nickel layer 64c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 64c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 6a and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of the plurality of leads 63a of header 60a, and wherein a thickness of the silver and gold alloy layer 61c ranges from 5 to 20 microinches, and further comprises a nickel layer 64c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 64c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 6a and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of the plurality of leads 63a of header 60a, and wherein a thickness of the silver and gold alloy layer 61c ranges from 3 to 160 microinches, and further comprises a nickel layer 64c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 64c ranges from 20 to 100 microinches.
In another embodiment of the present invention, also illustrated in Fig. 6a and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of the plurality of leads 63a of header 60a, and wherein a thickness of the silver and gold alloy layer 61c ranges from 5 to 20 microinches, and further comprises a nickel layer 64c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 64c ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 6a and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of the plurality of leads 63a of header 60a, wherein a gold composition of the silver and gold alloy layer 61c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 61c ranges from 3 to 160 microinches, and further comprises a nickel layer 64c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 64c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 6a and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of the plurality of leads 63a of header 60a, wherein a gold composition of the silver and gold alloy layer 61c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 61c ranges from 5 to 20 microinches, and further comprises a nickel layer 64c positioned beneath the silver and gold
alloy, wherein a thickness of the nickel layer 64c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 6a and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of the plurality of leads 63a of header 60a, wherein a gold composition of the silver and gold alloy layer 61c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 61c ranges from 3 to 160 microinches, and further comprises a nickel layer 64c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 64c ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 6a and 6c, a plurality of leads 63a of header 60a comprises a silver and gold alloy layer 61c, wherein the silver and gold alloy layer 61c forms an outside layer of the plurality of leads 63a of header 60a, wherein a gold composition of the silver and gold alloy layer 61c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 61c ranges from 5 to 20 microinches, and further comprises a nickel layer 64c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 64c ranges from 20 to 100 microinches.

In another embodiment of the present invention, as illustrated in Figs. 7b, a printed circuit board 70b comprises a silver and gold layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the board 70b.
The PCB 70b may comprise solder mask portions 74b surrounding multilayer portions with a silver and gold layer 71b, a nickel layer 72b, and a copper layer 73b. Under this arrangement is a material 75b which may be formed from BT resin or FR-4. Material 75b in turn surrounds another multilayer portion with silver and gold layer 71b over a nickel layer 72b.

In a conventional PCB, as shown in Fig. 7a, the outer layer 71a of may be a gold layer. Moreover, the outer layer 71a may lie over a layer of nickel 72a, which may in turn lie over a layer of copper 74a.

Again, as noted above, in the present embodiment, as illustrated in Fig. 7b, the outside layer comprises a silver and gold alloy layer 71b, thereby avoiding the performance and cost problems associated with a gold layer.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, and wherein a gold composition of the silver and gold alloy layer 71b ranges from 5 to 50% by weight.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, and wherein a thickness of the silver and gold alloy layer 71b ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein
the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, and wherein a thickness of the silver and gold alloy layer 71b ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, wherein a gold composition of the silver and gold alloy layer 71b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 71b ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, wherein a gold composition of the silver and gold alloy layer 71b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 71b ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, and further comprises a nickel layer 72b positioned beneath said silver and gold alloy.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit
board 70b, and wherein a thickness of the silver and gold alloy layer 71b ranges from 3 to 160 microinches, and further comprises a nickel layer 72b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 72b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, and wherein a thickness of the silver and gold alloy layer 71b ranges from 5 to 20 microinches, and further comprises a nickel layer 72b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 72b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, and wherein a thickness of the silver and gold alloy layer 71b ranges from 3 to 160 microinches, and further comprises a nickel layer 72b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 72b ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, and wherein a thickness of the silver and gold alloy layer 71b ranges from 5 to 20 microinches, and further comprises a nickel layer 72b positioned
beneath the silver and gold alloy, wherein a thickness of the nickel layer 72b ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, wherein a gold composition of the silver and gold alloy layer 71b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 71b ranges from 3 to 160 microinches, and further comprises a nickel layer 72b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 72b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, wherein a gold composition of the silver and gold alloy layer 71b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 71b ranges from 5 to 20 microinches, and further comprises a nickel layer 72b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 72b ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, wherein a gold composition of the silver and gold alloy layer 71b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold
alloy layer 71b ranges from 3 to 160 microinches, and further comprises a nickel layer 72b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 72b ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Fig. 7b, a printed circuit board 70b comprises a silver and gold alloy layer 71b, wherein the silver and gold alloy layer 71b forms an outside layer of the printed circuit board 70b, wherein a gold composition of the silver and gold alloy layer 71b ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 71b ranges from 5 to 20 microinches, and further comprises a nickel layer 72b positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 72b ranges from 20 to 100 microinches.

In another embodiment of the present invention, as illustrated in Figs. 8a and 8c, a Reed switch 80a comprises a reed portion 82a, a glass envelope 84a, a gap 85a, and a glass to metal hermetic seal 83a, wherein a silver and gold layer 81c forms an outside layer of the reed portion 82a. Under the silver and gold layer 81c is a layer of nickel 86c and under 86c is a copper layer 87c.

In a conventional Reed switch, the reed portion, however, as shown in Fig. 8b, the outer layer 81b may be a gold layer. The outer layer 81b may lie over a layer of nickel 86b, which may in turn lie over a layer of copper 87b.

Again, as noted above, in the present embodiment, as illustrated in Figs. 8a and 8c, the outside layer comprises a silver and gold alloy layer 81c, thereby avoiding the performance and cost problems associated with a gold layer.

In another embodiment of the present invention, also illustrated in Figs. 8a
and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, and wherein a gold composition of the silver and gold alloy layer 81c ranges from 5 to 50% by weight.

5 In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, and wherein a thickness of the silver and gold alloy layer 81c ranges from 3 to 160 microinches.

10 In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, and wherein a thickness of the silver and gold alloy layer 81c ranges from 5 to 20 microinches.

15 In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, wherein a gold composition of the silver and gold alloy layer 81c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 81c ranges from 3 to 160 microinches.

20 In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a,
wherein a gold composition of the silver and gold alloy layer 81c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 81c ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, and further comprises a nickel layer 86c positioned beneath said silver and gold alloy.

In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, and wherein a thickness of the silver and gold alloy layer 81c ranges from 3 to 160 microinches, and further comprises a nickel layer 86c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 86c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, and wherein a thickness of the silver and gold alloy layer 81c ranges from 5 to 20 microinches, and further comprises a nickel layer 86c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 86c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Figs. 8a
and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, and wherein a thickness of the silver and gold alloy layer 81c ranges from 3 to 160 microinches, and further comprises a nickel layer 86c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 86c ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, and wherein a thickness of the silver and gold alloy layer 81c ranges from 5 to 20 microinches, and further comprises a nickel layer 86c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 86c ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, wherein a gold composition of the silver and gold alloy layer 81c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 81c ranges from 3 to 160 microinches, and further comprises a nickel layer 86c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 86c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein
the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, wherein a gold composition of the silver and gold alloy layer 81c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 81c ranges from 5 to 20 microinches, and further comprises a nickel layer 86c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 86c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, wherein a gold composition of the silver and gold alloy layer 81c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 81c ranges from 3 to 160 microinches, and further comprises a nickel layer 86c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 86c ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Figs. 8a and 8c, a reed portion 82a comprises a silver and gold alloy layer 81c, wherein the silver and gold alloy layer 81c forms an outside layer of the reed portion 82a, wherein a gold composition of the silver and gold alloy layer 81c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 81c ranges from 5 to 20 microinches, and further comprises a nickel layer 86c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 86c ranges from 20 to 100 microinches.

In another embodiment of the present invention, as illustrated in Figs. 9a
and 9c, an electrical connector 90a comprises a connecting portion 93a, and a lead 92a, wherein a silver and gold layer 91c forms an outside layer of the lead 92a. Under the silver and gold layer 91c is a layer of nickel 94c and under 94c is a copper layer 95c.

In a conventional electrical connector, the outer layer of the lead, as shown in Fig. 9b, may be a gold layer. The outer layer 91b may lie over a layer of nickel 94b, which may in turn lie over a layer of copper 95b.

Again, as noted above, in the present embodiment, as illustrated in Figs. 9a and 9c, the outside layer comprises a silver and gold alloy layer 91c, thereby avoiding the performance and cost problems associated with a gold layer.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, and wherein a gold composition of the silver and gold alloy layer 91c ranges from 5 to 50% by weight.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, and wherein a thickness of the silver and gold alloy layer 91c ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, and wherein a thickness of the silver and gold alloy layer 91c ranges from 5 to 20 microinches.
In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, wherein a gold composition of the silver and gold alloy layer 91c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 91c ranges from 3 to 160 microinches.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, wherein a gold composition of the silver and gold alloy layer 91c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 91c ranges from 5 to 20 microinches.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, and further comprises a nickel layer 94c positioned beneath said silver and gold alloy.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, and wherein a thickness of the silver and gold alloy layer 91c ranges from 3 to 160 microinches, and further comprises a nickel layer 94c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 94c ranges from 10 to 300 microinches.
In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, and wherein a thickness of the silver and gold alloy layer 91c ranges from 5 to 20 microinches, and further comprises a nickel layer 94c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 94c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, and wherein a thickness of the silver and gold alloy layer 91c ranges from 3 to 160 microinches, and further comprises a nickel layer 94c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 94c ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, and wherein a thickness of the silver and gold alloy layer 91c ranges from 5 to 20 microinches, and further comprises a nickel layer 94c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 94c ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver
and gold alloy layer 91c forms an outside layer of the lead 92a, wherein a gold composition of the silver and gold alloy layer 91c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 91c ranges from 3 to 160 microinches, and further comprises a nickel layer 94c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 94c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, wherein a gold composition of the silver and gold alloy layer 91c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 91c ranges from 5 to 20 microinches, and further comprises a nickel layer 94c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 94c ranges from 10 to 300 microinches.

In another embodiment of the present invention, also illustrated in Figs. 9a and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, wherein a gold composition of the silver and gold alloy layer 91c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 91c ranges from 3 to 160 microinches, and further comprises a nickel layer 94c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 94c ranges from 20 to 100 microinches.

In another embodiment of the present invention, also illustrated in Figs. 9a
and 9c, a lead 92a comprises a silver and gold alloy layer 91c, wherein the silver and gold alloy layer 91c forms an outside layer of the lead 92a, wherein a gold composition of the silver and gold alloy layer 91c ranges from 5 to 50% by weight, and wherein a thickness of the silver and gold alloy layer 94c ranges from 5 to 20 microinches, and further comprises a nickel layer 94c positioned beneath the silver and gold alloy, wherein a thickness of the nickel layer 94c ranges from 20 to 100 microinches.

For all of the above described embodiments and accompanying drawings, the silver and gold alloy may further comprise 1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium. The addition of the element aids in refining grain morphology and decreasing the porosity of a deposited metal.

As noted above, the use of the silver and gold alloy and nickel in the present invention achieves improved characteristics. An electroplating method may be used to create the present invention, as well as, electroless plating, and vapor deposition methods.

The present invention has been tested as detailed below (although results are shown with respect to silver and gold alloy, similar results were obtained for silver and gold plus one element alloy).

The Preparation of the Sample

The surface of copper or copper alloy coil was degreased and activated by acid. The Ni and Au/Ag alloy or Au or Ag are electroplated orderly on the entire surface of copper or copper alloy base material.
Test for Evaluation of Bondability

After wire binding was conducted by using a wire-bonding machine, the tensile strength was measured by using a bonding pull tester.

Test for Evaluation of Solder Wettability

After heat treatment at 175°C for 7 hours and half, the sample was aged forcibly at 95°C under 95% relative humidity for 8 hours. And, then test for evaluation of solder wettability was conducted, referring to MIL-STD-883D.

Test for evaluation of Adhesion to Mold Resin

After the sample was sealed up with a mold resin at molding temperature 170°C for 90 seconds and treated for 6 hours at 175°C by heat, the adhesion between substrate for semiconductor device and mold resin was evaluated by using SAT(Scanning Acoustic Tomograph) referring to MRT(Moisture Resistance Test). But, the range of temperature was -55°C to 125°C, and before SAT was performed, the sample was cured at 125°C for 24 hours.

The results of the each evaluation test are shown in tables 1,2,3. In the tables, the conditions prepared for each example are marked as symbol "•". The order of multi-plated layer is always nickel layer deposited on a copper or copper alloy substrate as a first intermediate layer and Au/Ag alloy deposited on the nickel-plated layer (as an outermost layer). Au/Ag alloy layer is deposited as an outermost layer from example 1 to example 12, and Au or Ag layer as an outermost is
deposited between example 13 to example 24.

Table 1.

<table>
<thead>
<tr>
<th>Laminate structure</th>
<th>Ni</th>
<th>Au</th>
<th>Ag</th>
<th>Composition (weight %)</th>
<th>Evaluation test on bondability Pull strength in wire bonding(g)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness (μm)</td>
<td>30</td>
<td>50</td>
<td>70</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Example 1</td>
<td>•</td>
<td>•</td>
<td>•</td>
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<td>Example 2</td>
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<td>Example 3</td>
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<td>Example 4</td>
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<td>Example 5</td>
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<td>Example 6</td>
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<td>Example 7</td>
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<td>Example 8</td>
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<td>Example 9</td>
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<td>Example 10</td>
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<td>Example 11</td>
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<td>Example 12</td>
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<td>Example 13</td>
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<td>Example 14</td>
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<td>Example 15</td>
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<td>Example 16</td>
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<td>Example 17</td>
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<td>Example 18</td>
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<td>Example 19</td>
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<td>Example 20</td>
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<td>Example 21</td>
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<td>Example 22</td>
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<td>Example 23</td>
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<td>Example 24</td>
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</tr>
</tbody>
</table>

According to the result of table 1, examples having an outermost layer of Au/Ag alloy show higher values in the pull strength of wire bonding than examples having outermost layer of Au. Also, when only Ag existed as an outermost layer, a gold wire could not be bonded on surface of Ag layer.
Table 2.

<table>
<thead>
<tr>
<th>Laminate structure</th>
<th>Ni</th>
<th>Au/Ag</th>
<th>Composition (weight %)</th>
<th>Evaluation on Solder Wettability Covered Amount(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness (μin)</td>
<td>30</td>
<td>50</td>
<td>70 5 10 15</td>
<td></td>
</tr>
<tr>
<td>Example 1</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:11, Ag:89</td>
</tr>
<tr>
<td>Example 2</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:16, Ag:84</td>
</tr>
<tr>
<td>Example 3</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:22, Ag:78</td>
</tr>
<tr>
<td>Example 4</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:27, Ag:73</td>
</tr>
<tr>
<td>Example 5</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:30, Ag:70</td>
</tr>
<tr>
<td>Example 6</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:35, Ag:65</td>
</tr>
<tr>
<td>Example 7</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:30, Ag:70</td>
</tr>
<tr>
<td>Example 8</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:33, Ag:67</td>
</tr>
<tr>
<td>Example 9</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:32, Ag:68</td>
</tr>
<tr>
<td>Example 10</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:34, Ag:66</td>
</tr>
<tr>
<td>Example 11</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:31, Ag:69</td>
</tr>
<tr>
<td>Example 12</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>Au:31, Ag:69</td>
</tr>
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<td>Example 13</td>
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<td>Cu:3 Ni:5 Ag:92</td>
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<td>Example 14</td>
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<td>Cu:2 Ni:4 Ag:94</td>
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<tr>
<td>Example 15</td>
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<td>Example 16</td>
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<td>•</td>
<td>•</td>
<td>Cu:4 Ni:3 Ag:93</td>
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<tr>
<td>Example 17</td>
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<td>•</td>
<td>•</td>
<td>Cu:2 Ni:4 Ag:94</td>
</tr>
<tr>
<td>Example 18</td>
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<td>•</td>
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<td>Cu:1 Ni:4 Ag:95</td>
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<tr>
<td>Example 19</td>
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<td>Cu:2 Ni:5 Ag:93</td>
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<td>Example 20</td>
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<td>Example 21</td>
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<td>Example 23</td>
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<td>Cu:1 Ni:4 Ag:95</td>
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<td>Example 24</td>
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<td>•</td>
<td>Cu:1 Ni:1</td>
<td>Au:98</td>
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</table>

According to the result of table 2, on surface of outermost layer of Au or Ag of between examples 13 and examples 24, Ni and Cu are detected by Energy Disperse Spectroscopy. Also, covered amount (%) of solder in an evaluation on solder wettability could not reach over 95% the limit of pass. As a result, the diffusion of Ni or Cu made the substrates deteriorate in solder wettability. On the other hand, the examples having an outermost layer of Au/Ag alloy which were not contaminated by the diffusion of Ni or Cu all passed in an evaluation on solder wettability showing over 99%.
Table 3

<table>
<thead>
<tr>
<th>Laminate structure</th>
<th>Ni</th>
<th>30</th>
<th>50</th>
<th>70</th>
<th>5</th>
<th>10</th>
<th>15</th>
<th>Composition (weight %)</th>
<th>Evaluation on adhesion of mold resin</th>
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<tr>
<td>Thickness (μm)</td>
<td></td>
<td></td>
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<td>Au:11, Ag:89</td>
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<td>Example 1</td>
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<td>Example 3</td>
<td>●</td>
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<td></td>
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<td></td>
<td>Au:27, Ag:73</td>
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<td>●</td>
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<td></td>
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<td>Au:30, Ag:70</td>
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<td>Au:35, Ag:65</td>
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<td>Example 9</td>
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<td>Au:34, Ag:66</td>
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<td>●</td>
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<td>Au:31, Ag:69</td>
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<td>Example 12</td>
<td>●</td>
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<td>Example 13</td>
<td>●</td>
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<td>Example 15</td>
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<td>Ag:100</td>
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<td>Example 16</td>
<td>●</td>
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<td>Example 17</td>
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<tr>
<td>Example 23</td>
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<tr>
<td>Example 24</td>
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</table>

According to the result of table 3, the examples of Au or Au/Ag alloy deposited as an outermost layer on Ni plated layer attain better adhesion of mold resin than the examples of only Ag deposited as outermost layer on nickel plated layer. If SAT system detected voids or gaps between the substrates and mold resin,
the sample failed.

It is understood that while the various particular embodiments set forth herein have been described in detail, the description has been illustrated purposes only, and it is to be understood that changes and variables may be made without departing from the spirit or scope of the following claims.
What is claimed is:

1. A semiconductor product comprising:
   a silver and gold alloy layer, wherein said silver and gold alloy layer forms an outside layer of said product.

2. A semiconductor product according to claim 1, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

3. A semiconductor product according to claim 1, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

4. A semiconductor product according to claim 1, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

5. A semiconductor product according to claim 2, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

6. A semiconductor product according to claim 2, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

7. A semiconductor product according to claim 1, further comprising a nickel layer positioned beneath said silver and gold alloy.
8. A semiconductor product according to claim 3, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

9. A semiconductor product according to claim 4, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

10. A semiconductor product according to claim 3, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

11. A semiconductor product according to claim 4, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

12. A semiconductor product according to claim 8, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

13. A semiconductor product according to claim 9, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.
14. A semiconductor product according to claim 10, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

15. A semiconductor product according to claim 11, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

16. A semiconductor product according to claim 1, wherein said product comprises a substrate and said layer comprises an outside layer of said substrate.

17. A semiconductor product according to claim 16, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

18. A semiconductor product according to claim 16, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

19. A semiconductor product according to claim 16, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

20. A semiconductor product according to claim 17, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

21. A semiconductor product according to claim 17, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.
22. A semiconductor product according to claim 16, further comprising a nickel layer positioned beneath said silver and gold alloy.

23. A semiconductor product according to claim 18, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

24. A semiconductor product according to claim 19, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

25. A semiconductor product according to claim 18, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

26. A semiconductor product according to claim 19, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

27. A semiconductor product according to claim 23, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.
28. A semiconductor product according to claim 24, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

29. A semiconductor product according to claim 25, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

30. A semiconductor product according to claim 26, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

31. A semiconductor product according to claim 1, wherein said product comprises a lead frame and said layer comprises an outside layer of said lead frame.

32. A semiconductor product according to claim 31, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

33. A semiconductor product according to claim 31, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

34. A semiconductor product according to claim 31, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

35. A semiconductor product according to claim 32, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.
36. A semiconductor product according to claim 32, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

37. A semiconductor product according to claim 31, further comprising a nickel layer positioned beneath said silver and gold alloy.

38. A semiconductor product according to claim 33, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

39. A semiconductor product according to claim 34, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

40. A semiconductor product according to claim 33, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

41. A semiconductor product according to claim 34, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.
42. A semiconductor product according to claim 38, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

43. A semiconductor product according to claim 39, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

44. A semiconductor product according to claim 40, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

45. A semiconductor product according to claim 41, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

46. A semiconductor product according to claim 1, further comprising:
   a ball grid array comprising a plurality of soldering elements;
   a plurality of ball pad areas, wherein each one of said plurality of ball pad areas receives a respective one of said plurality of soldering elements;
   a pad area for receiving a semiconductor chip; and
   a plurality of lead areas;
   wherein at least one of said plurality of ball pad areas, said pad area for receiving a semiconductor chip, and said plurality of lead areas comprises said silver and gold alloy layer.

47. A semiconductor product according to claim 46, wherein a gold composition of
said silver and gold alloy layer ranges from 5 to 50 % by weight.

48. A semiconductor product according to claim 46, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

49. A semiconductor product according to claim 46, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

50. A semiconductor product according to claim 47, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

51. A semiconductor product according to claim 47, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

52. A semiconductor product according to claim 46, further comprising a nickel layer positioned beneath said silver and gold alloy.

53. A semiconductor product according to claim 48, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

54. A semiconductor product according to claim 49, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said
nickel layer ranges from 10 to 300 microinches.

55. A semiconductor product according to claim 48, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

56. A semiconductor product according to claim 49, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

57. A semiconductor product according to claim 53, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

58. A semiconductor product according to claim 54, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

59. A semiconductor product according to claim 55, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

60. A semiconductor product according to claim 56, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

61. A semiconductor product according to claim 1, wherein said product comprises
a header comprising a plurality of leads, wherein said layer comprises an outside layer of said plurality of leads.

62. A semiconductor product according to claim 61, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

63. A semiconductor product according to claim 61, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

64. A semiconductor product according to claim 61, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

65. A semiconductor product according to claim 62, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

66. A semiconductor product according to claim 62, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

67. A semiconductor product according to claim 61, further comprising a nickel layer positioned beneath said silver and gold alloy.

68. A semiconductor product according to claim 63, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said
nickel layer ranges from 10 to 300 microinches.

69. A semiconductor product according to claim 64, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

70. A semiconductor product according to claim 63, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

71. A semiconductor product according to claim 64, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

72. A semiconductor product according to claim 68, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

73. A semiconductor product according to claim 69, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

74. A semiconductor product according to claim 70, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.
75. A semiconductor product according to claim 71, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

76. A printed circuit board, comprising:

a silver and gold alloy layer, wherein said silver and gold alloy layer forms an outside layer of said board.

77. A semiconductor product according to claim 76, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

78. A semiconductor product according to claim 76, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

79. A semiconductor product according to claim 76, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

80. A semiconductor product according to claim 77, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

81. A semiconductor product according to claim 77, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

82. A semiconductor product according to claim 76, further comprising a nickel layer positioned beneath said silver and gold alloy.
83. A semiconductor product according to claim 78, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

84. A semiconductor product according to claim 79, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

85. A semiconductor product according to claim 78, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

86. A semiconductor product according to claim 79, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

87. A semiconductor product according to claim 83, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

88. A semiconductor product according to claim 84, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.
89. A semiconductor product according to claim 85, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

90. A semiconductor product according to claim 86, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

91. A Reed switch, comprising:
   a reed portion; and
   a silver and gold layer, wherein said silver and gold alloy layer forms an outside layer of said reed portion.

92. A semiconductor product according to claim 91, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

93. A semiconductor product according to claim 91, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

94. A semiconductor product according to claim 91, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

95. A semiconductor product according to claim 92, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.
96. A semiconductor product according to claim 92, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

97. A semiconductor product according to claim 91, further comprising a nickel layer positioned beneath said silver and gold alloy.

98. A semiconductor product according to claim 93, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

99. A semiconductor product according to claim 94, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

100. A semiconductor product according to claim 93, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

101. A semiconductor product according to claim 94, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

102. A semiconductor product according to claim 98, wherein a gold composition of
said silver and gold alloy layer ranges from 5 to 50 % by weight.

103. A semiconductor product according to claim 99, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

104. A semiconductor product according to claim 100, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

105. A semiconductor product according to claim 101, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

106. An electrical connector, comprising:

- a silver and gold alloy layer, wherein said silver and gold alloy layer forms an outside layer of said connector.

107. A semiconductor product according to claim 106, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

108. A semiconductor product according to claim 106, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

109. A semiconductor product according to claim 106, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.
110. A semiconductor product according to claim 107, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

111. A semiconductor product according to claim 107, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

112. A semiconductor product according to claim 106, further comprising a nickel layer positioned beneath said silver and gold alloy.

113. A semiconductor product according to claim 108, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

114. A semiconductor product according to claim 109, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

115. A semiconductor product according to claim 108, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

116. A semiconductor product according to claim 109, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.
layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

117. A semiconductor product according to claim 113, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

118. A semiconductor product according to claim 114, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

119. A semiconductor product according to claim 115, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

120. A semiconductor product according to claim 116, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

121. A semiconductor product according to claim 31, further comprising:

a semiconductor chip; and

a plurality of wires;

wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

122. A semiconductor product according to claim 32, further comprising:
a semiconductor chip; and

a plurality of wires;

wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

123. A semiconductor product according to claim 33, further comprising:

a semiconductor chip; and

a plurality of wires;

wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

124. A semiconductor product according to claim 34, further comprising:

a semiconductor chip; and

a plurality of wires;

wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

125. A semiconductor product according to claim 35, further comprising:

a semiconductor chip; and

a plurality of wires;
wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

126. A semiconductor product according to claim 36, further comprising:

   a semiconductor chip; and

   a plurality of wires;

   wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

127. A semiconductor product according to claim 37, further comprising:

   a semiconductor chip; and

   a plurality of wires;

   wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

128. A semiconductor product according to claim 38, further comprising:

   a semiconductor chip; and

   a plurality of wires;

   wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is
bonded onto to said layer.

129. A semiconductor product according to claim 39, further comprising:

    a semiconductor chip; and

5    a plurality of wires;

wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

130. A semiconductor product according to claim 40, further comprising:

    a semiconductor chip; and

10   a plurality of wires;

    wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

131. A semiconductor product according to claim 41, further comprising:

    a semiconductor chip; and

15   a plurality of wires;

20   wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.
132. A semiconductor product according to claim 42, further comprising:

    a semiconductor chip; and

    a plurality of wires;

    wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

133. A semiconductor product according to claim 43, further comprising:

    a semiconductor chip; and

    a plurality of wires;

    wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

134. A semiconductor product according to claim 44, further comprising:

    a semiconductor chip; and

    a plurality of wires;

    wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

135. A semiconductor product according to claim 45, further comprising:

    a semiconductor chip; and
a plurality of wires;
wherein a first end of each one of said plurality of wires is bonded onto said semiconductor chip and a second end of each one of said plurality of wires is bonded onto to said layer.

136. A semiconductor product according to claim 1, wherein said silver and gold alloy further comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

137. A semiconductor product according to claim 136, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

138. A semiconductor product according to claim 136, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

139. A semiconductor product according to claim 136, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

140. A semiconductor product according to claim 137, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

141. A semiconductor product according to claim 137, wherein a thickness of said
silver and gold alloy layer ranges from 5 to 20 microinches.

142. A semiconductor product according to claim 136, further comprising a nickel layer positioned beneath said silver and gold alloy.

143. A semiconductor product according to claim 138, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

144. A semiconductor product according to claim 139, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

145. A semiconductor product according to claim 138, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

146. A semiconductor product according to claim 139, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

147. A semiconductor product according to claim 143, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.
148. A semiconductor product according to claim 144, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

149. A semiconductor product according to claim 145, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

150. A semiconductor product according to claim 146, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

151. A semiconductor product according to claim 16, wherein said silver and gold alloy further comprises:
   1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

152. A semiconductor product according to claim 151, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

153. A semiconductor product according to claim 151, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

154. A semiconductor product according to claim 151, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.
155. A semiconductor product according to claim 152, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

156. A semiconductor product according to claim 152, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

157. A semiconductor product according to claim 151, further comprising a nickel layer positioned beneath said silver and gold alloy.

158. A semiconductor product according to claim 153, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

159. A semiconductor product according to claim 154, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

160. A semiconductor product according to claim 153, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

161. A semiconductor product according to claim 154, further comprising a nickel
layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

162. A semiconductor product according to claim 158, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

163. A semiconductor product according to claim 159, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

164. A semiconductor product according to claim 160, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

165. A semiconductor product according to claim 161, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

166. A semiconductor product according to claim 31, wherein said silver and gold alloy further comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

167. A semiconductor product according to claim 166, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.
168. A semiconductor product according to claim 166, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

169. A semiconductor product according to claim 166, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

170. A semiconductor product according to claim 167, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

171. A semiconductor product according to claim 167, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

172. A semiconductor product according to claim 166, further comprising a nickel layer positioned beneath said silver and gold alloy.

173. A semiconductor product according to claim 168, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

174. A semiconductor product according to claim 169, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.
175. A semiconductor product according to claim 168, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

176. A semiconductor product according to claim 169, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

177. A semiconductor product according to claim 173, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

178. A semiconductor product according to claim 174, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

179. A semiconductor product according to claim 175, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

180. A semiconductor product according to claim 176, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

181. A semiconductor product according to claim 46, wherein said silver and gold alloy further comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and
182. A semiconductor product according to claim 181, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

183. A semiconductor product according to claim 181, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

184. A semiconductor product according to claim 181, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

185. A semiconductor product according to claim 182, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

186. A semiconductor product according to claim 182, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

187. A semiconductor product according to claim 181, further comprising a nickel layer positioned beneath said silver and gold alloy.

188. A semiconductor product according to claim 183, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.
189. A semiconductor product according to claim 184, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

190. A semiconductor product according to claim 183, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

191. A semiconductor product according to claim 184, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

192. A semiconductor product according to claim 188, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

193. A semiconductor product according to claim 189, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

194. A semiconductor product according to claim 190, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

195. A semiconductor product according to claim 191, wherein a gold composition
of said silver and gold alloy layer ranges from 5 to 50 % by weight.

196. A semiconductor product according to claim 61, wherein said silver and gold alloy further comprises:
5
1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

197. A semiconductor product according to claim 196, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

198. A semiconductor product according to claim 196, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

199. A semiconductor product according to claim 196, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

200. A semiconductor product according to claim 197, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

201. A semiconductor product according to claim 197, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

202. A semiconductor product according to claim 196, further comprising a nickel
layer positioned beneath said silver and gold alloy.

203. A semiconductor product according to claim 198, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

204. A semiconductor product according to claim 199, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

205. A semiconductor product according to claim 198, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

206. A semiconductor product according to claim 199, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

207. A semiconductor product according to claim 203, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

208. A semiconductor product according to claim 204, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.
209. A semiconductor product according to claim 205, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

210. A semiconductor product according to claim 206, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

211. A printed circuit board according to claim 76, wherein said silver and gold alloy further comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

212. A semiconductor product according to claim 211, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

213. A semiconductor product according to claim 211, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

214. A semiconductor product according to claim 211, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

215. A semiconductor product according to claim 212, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.
216. A semiconductor product according to claim 212, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

217. A semiconductor product according to claim 211, further comprising a nickel layer positioned beneath said silver and gold alloy.

218. A semiconductor product according to claim 213, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

219. A semiconductor product according to claim 214, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

220. A semiconductor product according to claim 213, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

221. A semiconductor product according to claim 214, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.
222. A semiconductor product according to claim 218, wherein a gold composition
of said silver and gold alloy layer ranges from 5 to 50 % by weight.

223. A semiconductor product according to claim 219, wherein a gold composition
of said silver and gold alloy layer ranges from 5 to 50 % by weight.

224. A semiconductor product according to claim 220, wherein a gold composition
of said silver and gold alloy layer ranges from 5 to 50 % by weight.

225. A semiconductor product according to claim 221, wherein a gold composition
of said silver and gold alloy layer ranges from 5 to 50 % by weight.

226. A Reed switch according to claim 91, wherein said silver and gold alloy further
comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and
indium.

227. A semiconductor product according to claim 226, wherein a gold composition
of said silver and gold alloy layer ranges from 5 to 50 % by weight.

228. A semiconductor product according to claim 226, wherein a thickness of said
silver and gold alloy layer ranges from 3 to 160 microinches.
229. A semiconductor product according to claim 226, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

230. A semiconductor product according to claim 227, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

231. A semiconductor product according to claim 227, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

232. A semiconductor product according to claim 226, further comprising a nickel layer positioned beneath said silver and gold alloy.

233. A semiconductor product according to claim 228, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

234. A semiconductor product according to claim 229, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

235. A semiconductor product according to claim 228, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.
236. A semiconductor product according to claim 229, further comprising a nickel 
layer positioned beneath said silver and gold alloy, wherein a thickness of said 
nickel layer ranges from 20 to 100 microinches.

237. A semiconductor product according to claim 233, wherein a gold composition 
of said silver and gold alloy layer ranges from 5 to 50 % by weight.

238. A semiconductor product according to claim 234, wherein a gold composition 
of said silver and gold alloy layer ranges from 5 to 50 % by weight.

239. A semiconductor product according to claim 235, wherein a gold composition 
of said silver and gold alloy layer ranges from 5 to 50 % by weight.

240. A semiconductor product according to claim 236, wherein a gold composition 
of said silver and gold alloy layer ranges from 5 to 50 % by weight.

241. An electrical connector according to claim 106, comprising:

    a silver and gold alloy layer, wherein said silver and gold alloy layer forms 
an outside layer of said connector.

242. A semiconductor product according to claim 241, wherein a gold composition 
of said silver and gold alloy layer ranges from 5 to 50 % by weight.
243. A semiconductor product according to claim 241, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

244. A semiconductor product according to claim 241, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

245. A semiconductor product according to claim 242, wherein a thickness of said silver and gold alloy layer ranges from 3 to 160 microinches.

246. A semiconductor product according to claim 242, wherein a thickness of said silver and gold alloy layer ranges from 5 to 20 microinches.

247. A semiconductor product according to claim 241, further comprising a nickel layer positioned beneath said silver and gold alloy.

248. A semiconductor product according to claim 243, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.

249. A semiconductor product according to claim 244, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 10 to 300 microinches.
250. A semiconductor product according to claim 243, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

251. A semiconductor product according to claim 244, further comprising a nickel layer positioned beneath said silver and gold alloy, wherein a thickness of said nickel layer ranges from 20 to 100 microinches.

252. A semiconductor product according to claim 248, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

253. A semiconductor product according to claim 249, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

254. A semiconductor product according to claim 250, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

255. A semiconductor product according to claim 251, wherein a gold composition of said silver and gold alloy layer ranges from 5 to 50 % by weight.

256. A semiconductor product according to claim 121, wherein said silver and gold alloy further comprises:
1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

257. A semiconductor product according to claim 122, wherein said silver and gold alloy further comprises:
   1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

258. A semiconductor product according to claim 123, wherein said silver and gold alloy further comprises:
   1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

259. A semiconductor product according to claim 124, wherein said silver and gold alloy further comprises:
   1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

260. A semiconductor product according to claim 125, wherein said silver and gold alloy further comprises:
   1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.
261. A semiconductor product according to claim 126, wherein said silver and gold alloy further comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

262. A semiconductor product according to claim 127, wherein said silver and gold alloy further comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

263. A semiconductor product according to claim 128, wherein said silver and gold alloy further comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

264. A semiconductor product according to claim 129, wherein said silver and gold alloy further comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

265. A semiconductor product according to claim 130, wherein said silver and gold alloy further comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and
indium.

266. A semiconductor product according to claim 131, wherein said silver and gold alloy further comprises:

5 1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

267. A semiconductor product according to claim 132, wherein said silver and gold alloy further comprises:

10 1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

268. A semiconductor product according to claim 133, wherein said silver and gold alloy further comprises:

15 1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

269. A semiconductor product according to claim 134, wherein said silver and gold alloy further comprises:

20 1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.

270. A semiconductor product according to claim 135, wherein said silver and gold
alloy further comprises:

1% or less of one of selenium, antimony, bismuth, nickel, cobalt, and indium.
Fig. 3
Fig. 7a
Fig. 8c
Fig. 10a