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(54) Title: TRENCH DMOS DEVICE WITH IMPROVED TERMINATION STRUCTURE FOR HIGH VOLTAGE APPLICATIONS

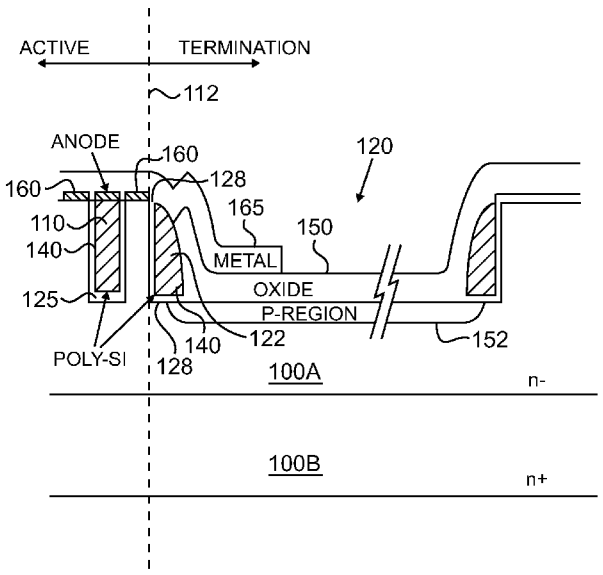


FIG. 2

(57) Abstract: A termination structure is provided for a power transistor. The termination structure includes a semiconductor substrate having an active region and a termination region. The substrate has a first type of conductivity. A termination trench is located in the termination region and extends from a boundary of the active region toward an edge of the semiconductor substrate. A doped region having a second type of conductivity is disposed in the substrate below the termination trench. A MaS gate is formed on a sidewall adjacent the boundary. The doped region extends from below a portion ofthe MaS gate spaced apart from the boundary toward the edge ofthe semiconductor substrate. A termination structure oxide layer is formed on the termination trench covering a portion of the MaS gate and extends toward the edge of the substrate.

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TRENCH DMOS DEVICE WITH IMPROVED TERMINATION STRUCTURE FOR HIGH VOLTAGE APPLICATIONS

Related Applications

[0001] This application claims priority from United States patent application no. 12/724,771, filed March 16, 2010, which is incorporated by reference herein in its entirety.

Field of the Invention

[0002] The present invention relates generally to a semiconductor device, and more particularly to a termination structure for a trench MOS device.

Background

[0003] Conventionally, a Schottky diode includes a heavily-doped semiconductor substrate, typically made of single-crystal silicon. A second layer covers the substrate, The second layer, called the drift region, is less heavily-doped with a material having carriers of the same conducting type as the substrate. A metal layer or or a metal silicide layer forms a Schottky contact with the lightly-doped drift region and forms the diode anode.

[0004] Two opposing constraints arise when forming a unipolar component such as a Schottky diode. In particular, the components should exhibit the lowest possible on-state resistance (Ron) while having a high breakdown voltage. Minimizing the on-state resistance imposes minimizing the thickness of the less doped layer and maximizing the doping of this layer. Conversely, to obtain a high reverse breakdown voltage, the doping of the less doped layer must be minimized and its thickness must be maximized, while avoiding the creation of areas in which the equipotential surfaces are strongly bent.

[0005] Various solutions have been provided to reconcile these opposite constraints, which has led to the development of trench MOS-capacitance Schottky diode structures, which are referred to as Trench MOS Barrier Schottky (TMBS) diodes. In an example of such structures, conductive areas, for example, heavily-doped N-type polysilicon areas, are formed in an upper portion of a thick drift region less heavily N-type doped than an underlying substrate. An insulating layer insulates the conductive areas from the thick layer. An anode

layer covers the entire structure, contacting the upper surface of the insulated conductive areas and forming a Schottky contact with the lightly-doped drift region.

[0006] When reverse biased, the insulated conductive areas cause a lateral depletion of into the drift region, which modifies the distribution of the equipotential surfaces in this layer. This enables increasing the drift region doping, and thus reducing the on-state resistance with no adverse effect on the reverse breakdown voltage.

[0007] FIG. 1 is a simplified, partial view of a conventional TMBS Schottky diode or rectifier. The diode is formed from a heavily-doped N-type silicon wafer 1 on which is formed a lightly-doped N-type epitaxial layer 2. Openings are formed in this epitaxial layer, which may be, for example, trench-shaped. Conductive regions 3 are formed in the openings, which are made, for example, of doped polysilicon. An insulating layer 4 is interposed between each conductive region and the walls of the corresponding opening (e.g., trench). The insulating layer 4 may be formed, for example, by thermal oxidation and the opening may be filled with polysilicon by conformal deposition, followed by a planarization step. After this, a metal, for example, nickel, capable of forming a silicide 5 above the single-crystal silicon regions and 6 above the polysilicon filling areas, is deposited. Once the silicide has been formed, the metal which has not reacted with the silicon is removed by selective etch. After this, an anode metal deposition 7 is formed on the upper surface side and a cathode metal deposition 8 is formed on the lower surface side.

[0008] A key issue for achieving a high voltage Schottky rectifier is the design of its termination region. As with any voltage design, the termination region is prone to higher electric fields due to the absence of self multi-cell protection and the curvature effect. As a result, the breakdown voltage is typically dramatically reduced from its ideal value. To avoid this reduction, the termination region should be designed to reduce the crowding of the electric field at the edge of the device (near the active region). Conventional approaches to reduce electric field crowding include termination structures with local oxidation of silicon (LOCOS) regions, field plates, guard rings, trenches and various combinations thereof. One example of a Schottky diode that includes such a termination region is shown in U.S. Patent No. 6,396,090.

[0009] Unfortunately, for high voltage applications these conventional designs for the termination region have had only limited success because the electric field distribution at the surface of the termination region is still far from ideal. At the same time, other problems arise because of degradations arising from hot carrier injection and the buildup of parasitic charges.

Summary of the Invention

[0010] In accordance with the present invention, a termination structure is provided for a power transistor. In one aspect of the invention the termination structure includes a semiconductor substrate having an active region and a termination region. The substrate has a first type of conductivity. A termination trench is located in the termination region and extends from a boundary of the active region toward an edge of the semiconductor substrate. A doped region having a second type of conductivity is disposed in the substrate below the termination trench. A MOS gate is formed on a sidewall adjacent the boundary. The doped region extends from below a portion of the MOS gate spaced apart from the boundary toward the edge of the semiconductor substrate. A termination structure oxide layer is formed on the termination trench covering a portion of the MOS gate and extends toward the edge of the substrate. A first conductive layer is formed on a backside surface of the semiconductor substrate and a second conductive layer is formed atop the active region, an exposed portion of the MOS gate, and extends to cover a portion of the termination structure oxide layer.

Brief Description Of The Drawings

[0011] FIG. 1 is a simplified, partial view of a conventional TMBS Schottky diode or rectifier.

[0012] FIG. 2 shows a cross-sectional view of the active and termination regions of a TMBS Schottky diode constructed in accordance with the present invention.

[0013] FIG. 3 shows the dependency of the leakage current on the reverse bias for the device of FIG. 2 both with and without the implantation region.

[0014] FIG. 4 shows the electric field at different positions along the A-A' line of the device of FIG. 2 both with and without the implantation region.

[0015] FIG. 5 shows the y-axis vector of the electric field for the device in FIG. 2 both with and without the implantation region.

[0016] FIGs. 6-11 illustrate one example of the process steps that may be employed to fabricate the device of FIG. 2

[0017] FIG. 12 shows a cross-sectional view of the active and termination regions of a TMBS Schottky diode constructed in accordance with another embodiment of the present invention.

[0018] FIG. 13 shows the dependency of the leakage current on the reverse bias for the devices of FIG. 2 and FIG. 12.

[0019] FIG. 14 shows the electric field at different positions along the devices of FIG. 2 and FIG. 12.

Detailed Description

[0020] As detailed below, a termination structure is provided which reduces the aforementioned problems. In particular, the device exhibits better immunity to hot carrier injection degradation by reducing the orthogonal electric field component at the silicon/dielectric interface, since it is this interface that enhances the degree to which charge is trapped in the dielectric. The problems caused by parasitic charges can be reduced by either (i) designing the termination structure so that the electric field can be "flexibly" distributed, which allows movement of the electric field in the presence of parasitic charges without increasing the peak of the electric field or (ii) shielding the parasitic charge with floating conductive plates.

[0021] FIG. 2 shows a cross-sectional view of the active and termination regions of a TMBS Schottky diode. The active region includes a semiconductor substrate 110B that is heavily doped with a dopant of a first conductivity type (e.g., n+ type). A first layer 100A is formed on the substrate 100B and is more lightly doped with a dopant of the first conductivity type (e.g., n- type). Trenches 110 (only one of which is shown) are formed in the first layer 100A. The trenches 110 are lined with an insulating layer 125 and filled with a conductive material 140 such as doped polysilicon. A metal layer 160 is formed over the exposed surfaces of the conductive material 140 and the first layer 100A. A Schottky contact is

formed at the interface between the metal layer 160 and the first layer 100A. An anode metal 165 is formed over the metal layer 160. A cathode electrode (not shown) is located on the backside of the semiconductor substrate 100B.

[0022] The termination region of the TMBS Schottky diode shown in FIG. 2 includes a termination trench 120 that extends from the boundary 112 with the active region to an edge of the semiconductor substrate 100B. A MOS gate 122 is formed on a sidewall of the termination region adjacent to the boundary 112 with the active region. The MOS gate 122 includes an insulating material 128 and a conductive material 122. The insulating material 128 lines the sidewall against which the MOS gate 122 is located and the portion of the first layer 100A adjacent to the sidewall. A conductive material 122 covers the insulating material 128. A termination oxide layer 150 is formed in the termination trench and extends from the MOS gate 122 toward the edge of the device. An implantation region 152 is formed in the first layer 100A and is doped with a dopant of a conductivity type (e.g., p-type) opposite to that of the first layer 100A. The implantation region 152 is located beneath a portion of the MOS gate 122 and the termination oxide layer 150. In some implementations the edge of the implantation region 152 may extend to the boundary 112 and surrounds the corner of the MOS gate 122.The metal layer 160 and the anode metal 165 located in the active region extend into the termination region and cover the MOS gate 122 and a portion of the termination oxide layer 150 to thereby define a field plate.

[0023] If the implantation region 152 were not employed in the termination structure, high electric fields would still arise at high voltages. This is because all the reverse bias is sustained within a limited depletion region between the anode and cathode electrodes and the electric field rises quickly at the edge of the active region since the growth of the depletion region is limited by the relatively high doping in the n-type drift layer. To relieve the degree to which the electric field is crowded, the applied reverse bias needs to be dropped across a much larger depletion region. At the same time, orthogonal electric fields are present across the semiconductor/oxide interface (i.e., the electric field components perpendicular to the semiconductor/oxide interface). This leads to HCI into the oxide and hence long term degradation of the breakdown voltage.

[0024] The implantation region 152 reduces this problem because it is fully depleted under a reverse bias and helps to push out the depletion region, effectively enlarging the width of the

depletion region and hence reducing the electric field peaks near the active region of the device. Compared to a termination structure that does not include the implantation region 152, the device shown in FIG. 2 has a breakdown voltage as high as 95% of the ideal breakdown voltage (i.e., the breakdown voltage of the active cell alone). This result is shown in FIG. 3, which shows the dependency of the leakage current on the reverse bias both with and without the implantation region 152.

[0025] In addition, the termination structure shown in FIG. 2 helps to lower the electric fields in the active region (specifically, the electric fields in the cells closer to the termination region). This is shown in FIG. 4, which shows the electric field at different positions along the device both with and without the implantation region 152. This reduction in electric field arises because the implantation region 152 serves to push the electric field further into the bulk, thereby reducing its presence at the trench surface.

[0026] The termination structure shown in FIG. 2 is also expected to have better reliability than conventional structures in terms of its immunity to HCI degradation. This is evident from FIG. 5, which shows the electric field along the y-axis (both with and without the implantation region 152), which provides the momentum for injecting the carriers into the oxide layer. To reduce the HCI, the electric field along the y-axis should be as small as possible. The termination structure significantly lowers this electric field in the active region and the MOS gate 122, which is most susceptible to HCI in a conventional structure.

[0027] One example of a method that may be employed to form the TMBS Schottky diode of FIG. 2 will be described with reference to FIGs. 6- 11. In this example the Schottky diode and its termination structure are formed simultaneously, though this need not always be the case.

[0028] FIG. 6 is a cross-sectional view of a semiconductor substrate 100 that includes a first layer 100A having a dopant of a first conductivity type (e.g., n- type) and a base substrate 100B which is more heavily doped with a dopant of the first conductivity type (e.g., n+ type). An oxide layer 101 is formed on the first substrate 100A by chemical vapor deposition (CVD), for example, to a thickness of about 2000-10,000 angstroms. Next, a photoresist (not shown) is coated on the oxide layer 101 to define a plurality of first trenches 110 in the active region and a second trench 120 in the termination region. The trenches 110 are spaced apart

from one another by mesas 115. In one example each of the first trenches 110 is about 0.2-2.0 microns in width The second trench 120 forms the boundary from the edge of the active region to an edge of the semiconductor substrate 100 (or a die) and defines the termination region.

[0029] In FIG. 7 a dielectric layer such as a TEOS layer 112 is deposited over the entire structure and etched back in FIG. 8 so that it is removed from the trench 120 except for a spacer 114 that is located against the sidewall of the trench 120 adjacent the active region of the device. A p-type dopant such as boron is then implanted into the first layer 110A to form the implantation region 152.

[0030] Referring to FIG. 9, after removal of the oxide layer 101 and TEOS spacer 114, a high temperature oxidation process is performed to form gate oxide layer 125. The gate oxide layer 125, which in some examples has a thickness between about 150 angstroms and 3000 angstroms, is formed on the sidewalls 110A, 120A and bottoms 110B, 120B of the first and second trenches 110, 120 and the surface of mesa 115. Instead of an oxidation process, the gate oxide layer 125 may be formed by high temperature deposition to form a HTO (high temperature oxide deposition) layer.

[0031] Next, a first conductive layer 140 is formed by CVD on the gate oxide 125 and fills the first trenches 110 and the second trench 120. The first conductive layer 140 has a thickness such that it extends over mesas 115. The first conductive layer 140 may be any suitable material such as a metal, doped-polysilicon or doped-amorphous silicon. The first conductive layer 140 may have a thickness of about 0.5 to 3.0 microns. In order to prevent voids from forming in the inner portion of the first trenches 110, the first conductive layer 140 may be polysilicon formed by an LPCVD (low pressure CVD) process, which has good step coverage. However, in some cases amorphous silicon may be better able to eliminate voids than polysilicon. To make the amorphous silicon conductive a recrystallization process may be employed.

[0032] Referring now to FIG. 10, an anisotropic etching is performed to remove the excess first conductive layer 140. After this etching process, a spacer-like MOS gate 122 is formed from a conductive material on the oxide layer 125 lining the sidewall 125A of the second

trench 120. In some examples the spacer-like MOS gate 122 has a width (along the cross-sectional view that is shown) that is about equal to the height of the second trench 120.

[0033] A dielectric layer 150 is next formed over the first layer 100A in the termination region using an etching process. The dielectric layer 150 may be, for example, a TEOS layer such as an LPTEOS or PETEOS layer or an O_3 -TEOS or HTO layer. In some examples the thickness of the dielectric layer 150 may be between about 0.2-1.0 micron. The dielectric layer 150 partially covers the MOS gate 122.

[0034] Next, in FIG. 11, a sputtering or other suitable process is performed to deposit a second conductive layer 160 so as to form Schottky contact regions 115A on mesas 115. The second conductive layer 160 may be formed from any material that can form a Schottky diode with the underlying first layer 100A. For example, second conductive layer 160 may be a metal silicide layer. After the formation of Schottky contacts, the conductive layer 160 may be removed.

[0035] The method continues to deposit and etch a conductor to form the diode anode electrode 165, which may co-extensive with conductive layer 160. Likewise a cathode electrode 170 is formed on the backside of substrate 100B.

[0036] FIG. 12 shows an alternative embodiment of the invention which is similar to the embodiment depicted in FIG. 2 except that in FIG. 12 one or more additional segmented metal regions 167 are located on the dielectric layer 150 in the termination trench 120. Segmented metal regions 167 are used to enhance the accommodation of the reverse bias and thus help to reduce the electric field near the active region. The segmented metal regions 167 may be formed along with the anode electrode 165 with an additional etching step. FIG. 13 shows the breakdown voltage performance of the embodiment depicted in FIG. 2 and in FIG. 12. Clearly, the embodiment of FIG. 12 has a higher breakdown voltage (97% of the ideal value). The superior breakdown voltage of the FIG. 12 embodiment is likely attributable to the slightly lower electric filed in the active cell and the end of anode, as indicated in the electrical field profile of FIG. 13.

Example

[0037] By way of illustration, various structural dimensions and parameters will be specified for one particular embodiment of the invention. In this embodiment the termination trench 120 has a width ranging from 10 – 50 microns and a depth that may be the same or different from the depth of the trenches 110 in the active region. Depending on the particular design and desired device characteristics (e.g., voltage capability, speed, leakage current) the depth of the termination trench 120 may range from 1 – 6 microns. The dielectric layer 150 located in the termination trench 120 may be silicon dioxide layer having a thickness between about 1500 – 15,000 angstroms, depending on the blocking voltage that is required and the composition of the material.

[0038] The field plate defined by the extension of conductive layers 160 and 165 into the termination region may have a length between about 4 and 45 microns in the termination trench 120. The implantation region 152 may be formed by ion implantation and driven into the layer 100A by a thermal process. The implantation dosage may range about $1x10^{11}$ atoms/cm^2 to $1x10^{13}$ atoms/cm^2. The dopant may be boron, BF_2, or another group-III element.

[0039] If one or more of the segmented metal regions 167 shown in FIG. 12 are employed, they may each have a width greater than about 0.4 microns with a spacing between them of between about 0.3 and 10 microns.

[0040] It should be noted that the termination structure described above may be used in connection with devices other than TMBS Schottky diodes, which has been presented by way of illustration only. For example, the termination structure can be applied to any power transistor such as a doubled diffused metal-oxide-semiconductor field effect transistor (DMOSFET), an insulated gate bipolar transistor (IGBT) and other trench MOS devices.

Claims

1. A termination structure for a power transistor, said termination structure comprising:

a semiconductor substrate having an active region and a termination region, the substrate having a first type of conductivity;

a termination trench located in the termination region and extending from a boundary of the active region toward an edge of the semiconductor substrate;

a doped region having a second type of conductivity disposed in the substrate below the termination trench;

a MOS gate formed on a sidewall adjacent the boundary, wherein the doped region extends from below a portion of the MOS gate toward the edge of the semiconductor substrate;

a termination structure oxide layer formed on the termination trench covering a portion of the MOS gate and extending toward the edge of the substrate;

a first conductive layer formed on a backside surface of the semiconductor substrate; and

a second conductive layer formed atop the active region, an exposed portion of the MOS gate, and extending to cover a portion of the termination structure oxide layer.

2. The termination structure of claim 1 further comprising a plurality of trench MOS devices spaced from each other and formed in the active region of the semiconductor substrate

3. The termination structure of claim 1, wherein said MOS gate comprises a conductive layer and a gate oxide layer formed between a bottom of the termination trench and the conductive layer.

4. The termination structure of claim 1, wherein said trench MOS device is a Schottky diode.

5. The termination structure of claim 4, wherein said Schottky diode is a TMBS Schottky diode that includes at least one trench in the active region of the substrate.

6. The termination structure of claim 1, wherein said power transistor is a device selected from the group consisting of Schottky diodes, DMOSs, and IGBTs.

7. The termination structure of claim 1, further comprising one or more segmented metal regions located on the termination structure oxide layer and spaced apart from the second conductive layer.

8. The termination structure of claim 1, wherein the doped region is an implantation region.

9. The termination structure of claim 1, wherein the implantation region is doped with an implantation dosage of between about $1x10^{11}$ atoms/cm^2 to $1x10^{13}$ atoms/cm^2.

10. A Schottky diode, comprising:

a semiconductor substrate having a plurality of trench MOS devices spaced from each other formed in an active region of the semiconductor substrate, the substrate having a first type of conductivity;

a termination trench located in a termination region and extending from a boundary of the active region toward an edge of the semiconductor substrate;

a doped region having a second type of conductivity disposed in the substrate below the termination trench;

a MOS gate formed on a sidewall adjacent the boundary, wherein the doped region extends from below a portion of the MOS gate toward the edge of the semiconductor substrate;

a termination structure oxide layer formed on the termination trench covering a portion of the MOS gate and extending toward the edge of the substrate;

a first conductive layer formed on a backside surface of the semiconductor substrate; and

a second conductive layer formed atop the active region to define one or more Schottky barriers with one or more portions of the substrate located between adjacent ones of the trench MOS devices; and

a field plate extending over an exposed portion of the MOS gate and a portion of the termination structure oxide layer.

11. The Schottky diode of claim 10 wherein said field plates includes an extension of the second conductive layer into the termination trench.

12. The Schottky diode of claim 10, wherein said semiconductor substrate comprises a first layer and a base substrate, and said first layer has a first type of conductive impurities lightly doped and said base substrate has said first type of conductive impurities heavily doped.

13. The Schottky diode of claim 12, wherein said trench MOS devices and said termination trench are formed in said first layer having a depth of between about 1-6 microns.

14. The Schottky diode of claim 13, wherein said termination trench has a width between about 10-50 microns.

15. The Schottky diode of claim 10, wherein said termination trench is formed from the boundary of the active region to an edge of the semiconductor substrate, so that said termination trench has one sidewall only.

16. The Schottky diode of claim 10 wherein said trench MOS devices and said MOS gate include a material selected from the group consisting of metal, polysilicon, and amorphous silicon.

17. The Schottky diode of claim 10, further comprising one or more segmented metal regions located on the termination structure oxide layer and spaced apart from the field plate.

18. The Schottky diode of claim 17, further comprising at least two segmented metal regions spaced apart from one another by between about 0.3 and 10 microns.

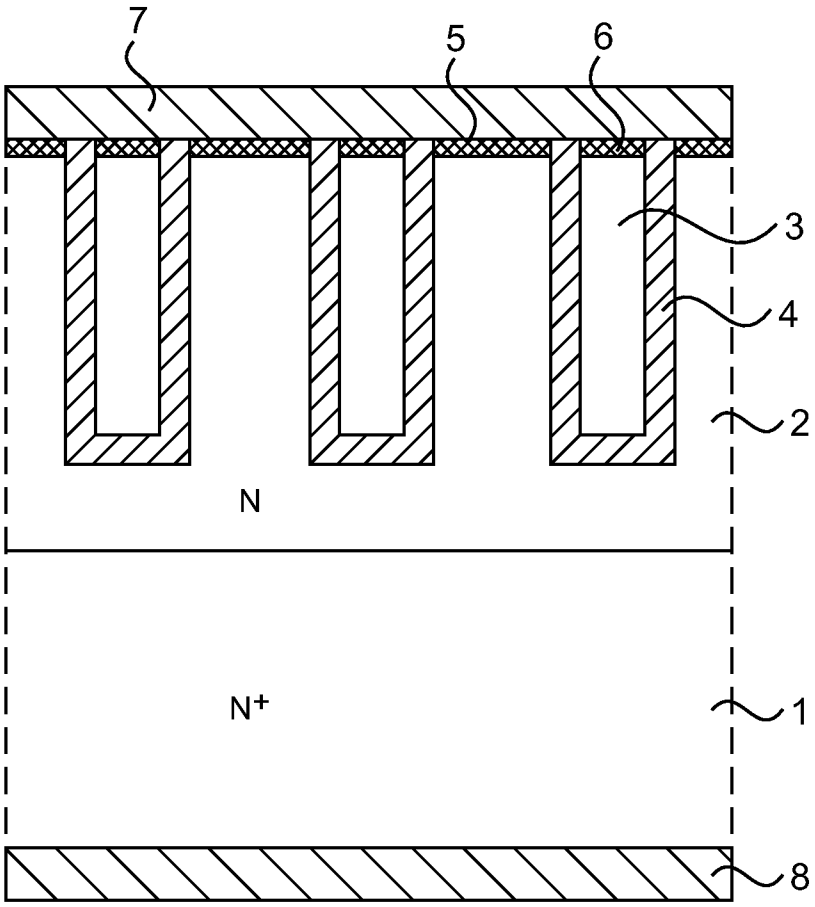


FIG. 1

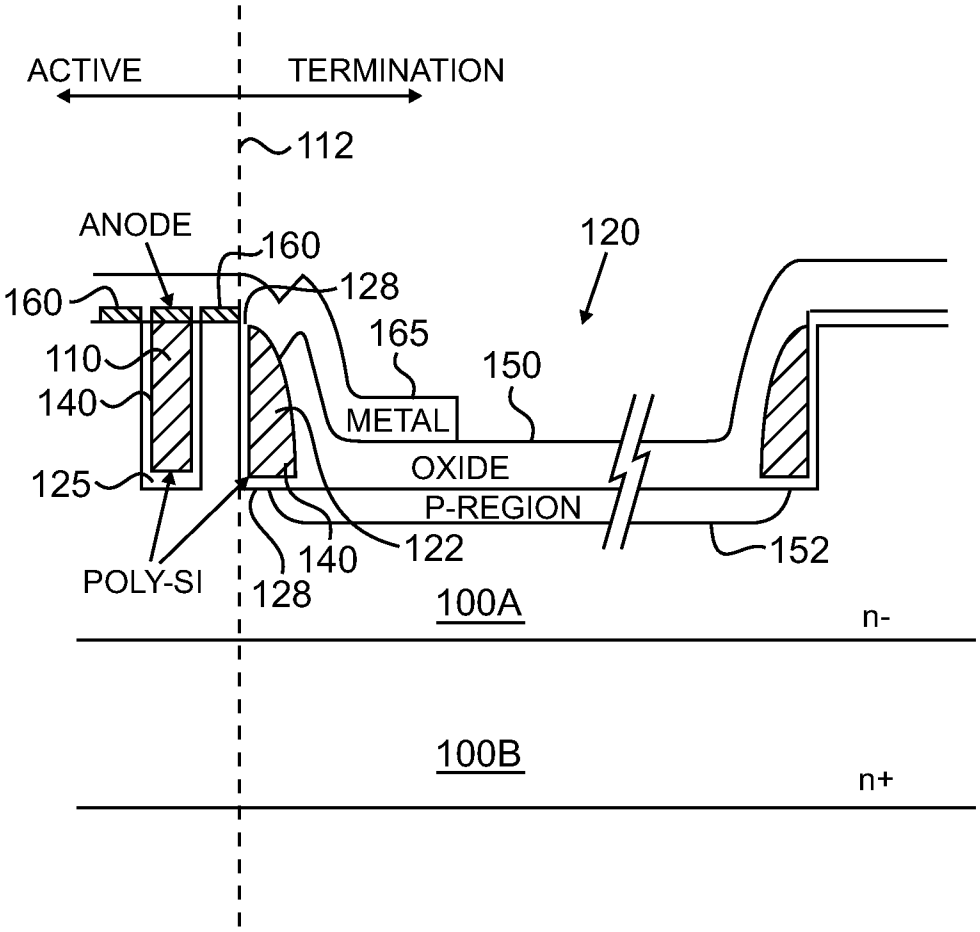
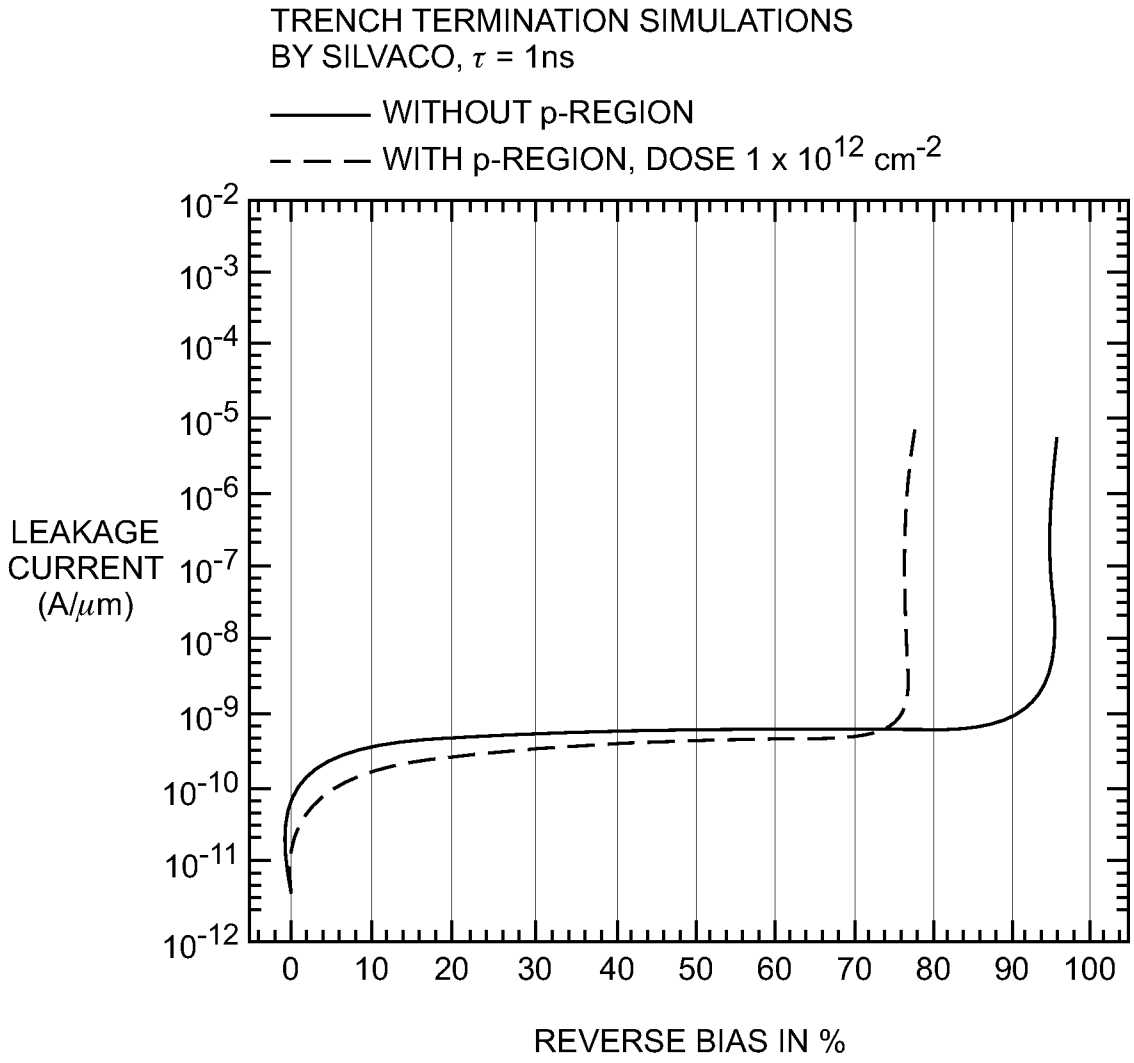
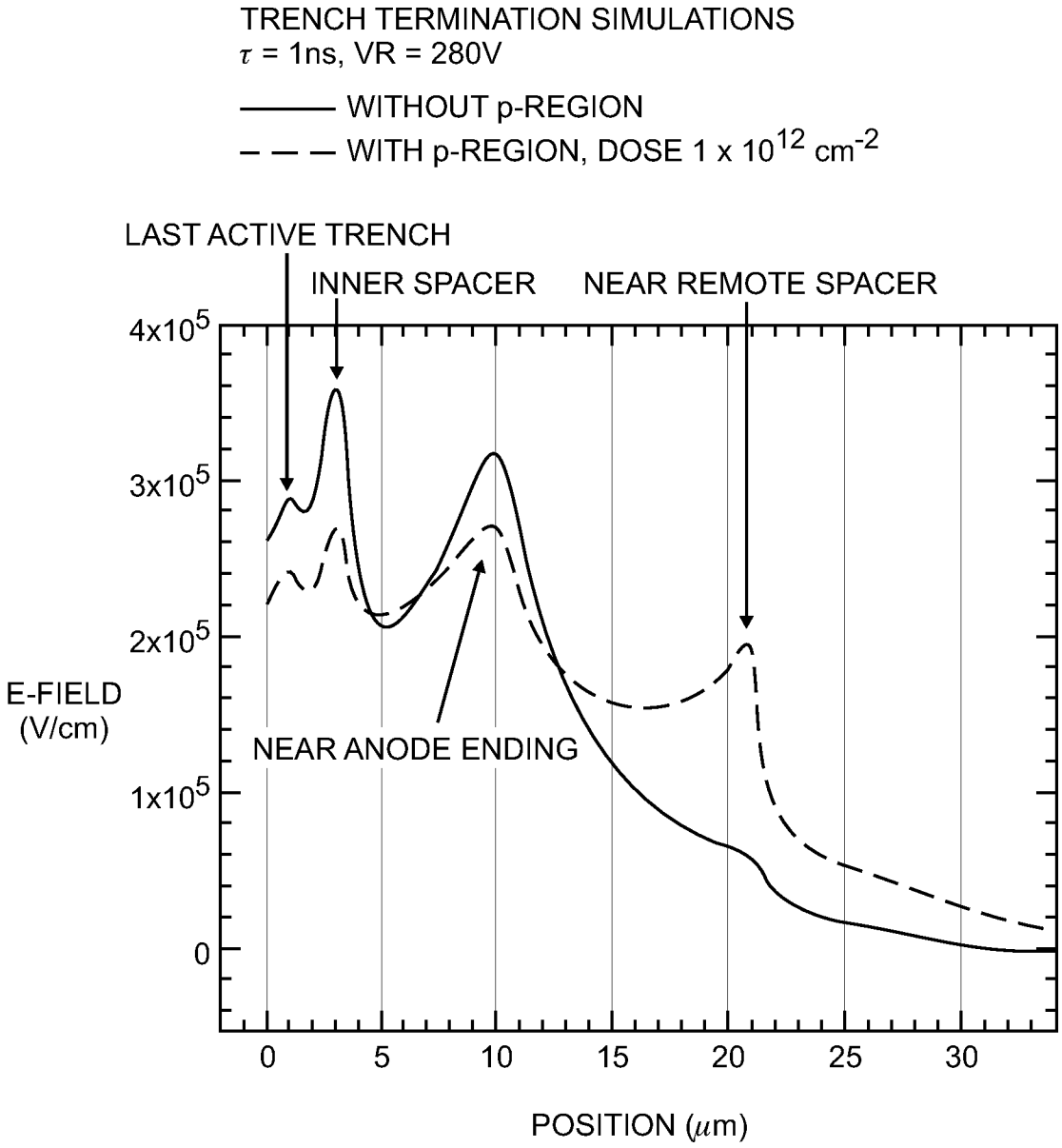

ACTIVE
TERMINATION
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ANODE
160
128
120
160
165
110
150
140
METAL
OXIDE
125
P-REGION
122
140
152
POLY-SI
128
100A
n-
100B
n+

FIG. 2



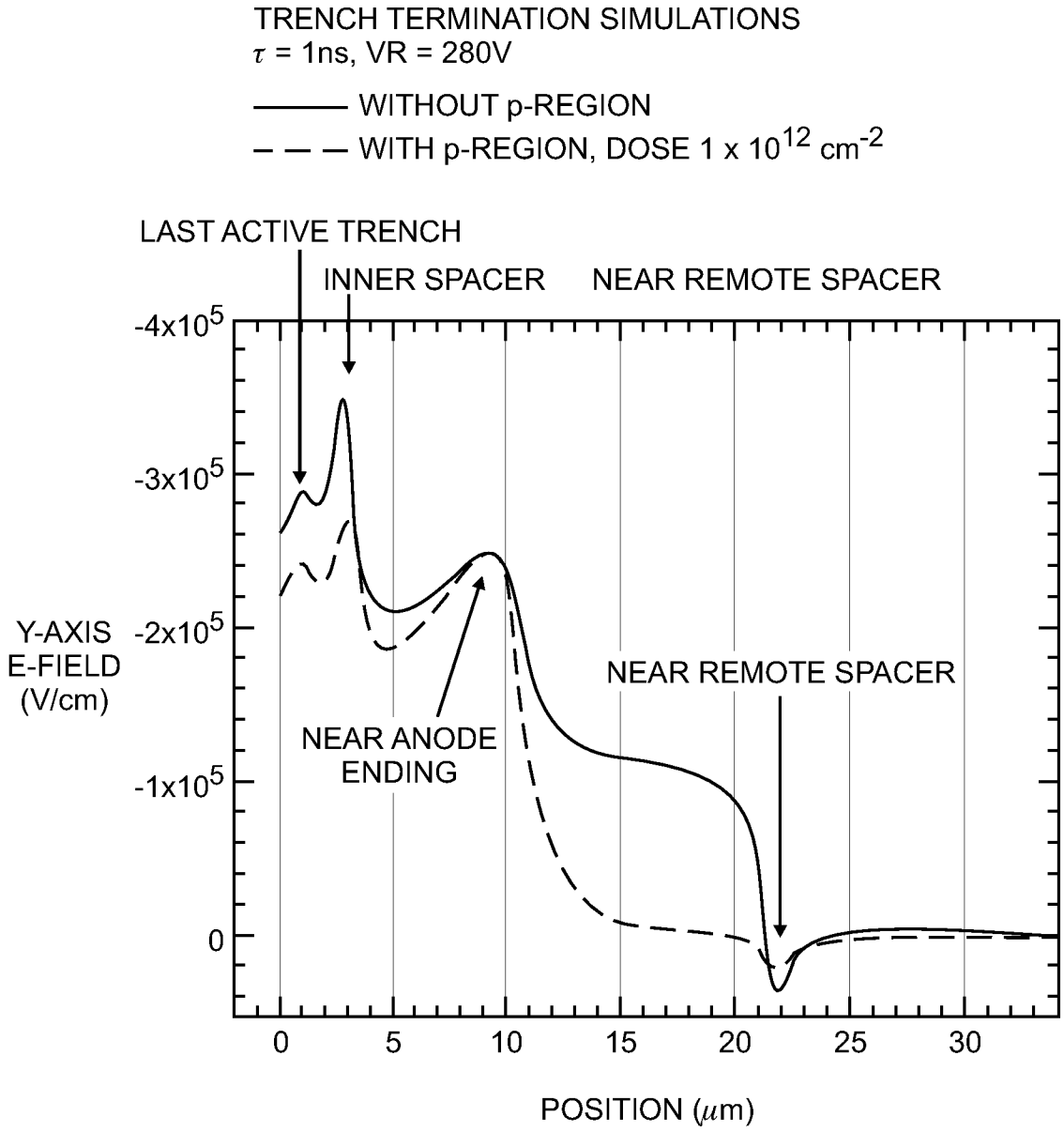
REVERSE CHARACTERISTICS

FIG. 3



ELECTRICAL FIELD PROFILES

FIG. 4



Y-AXIS E-FIELD PROFILE

FIG. 5

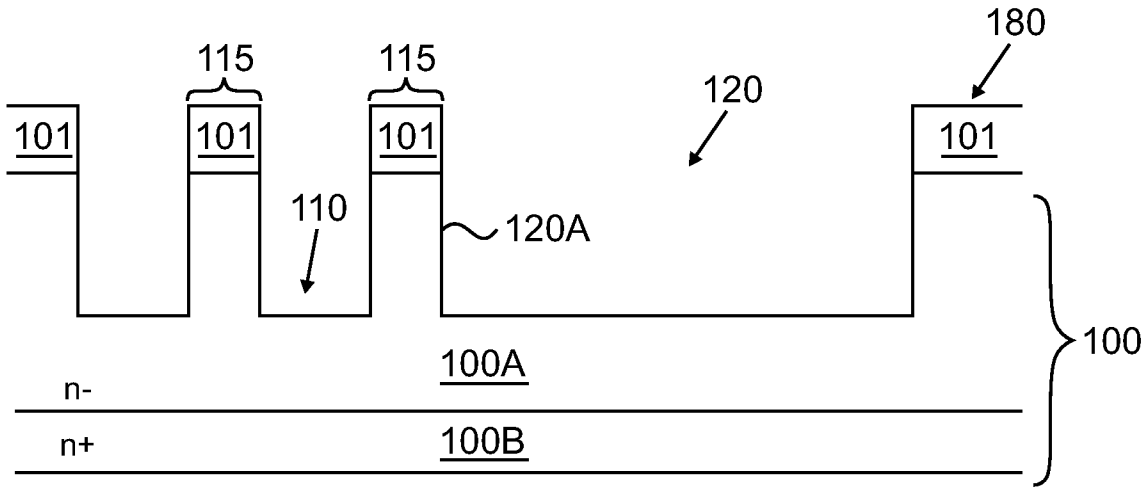

180
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120
101
101
101
101
110
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100A
n-
n+
100B

FIG. 6

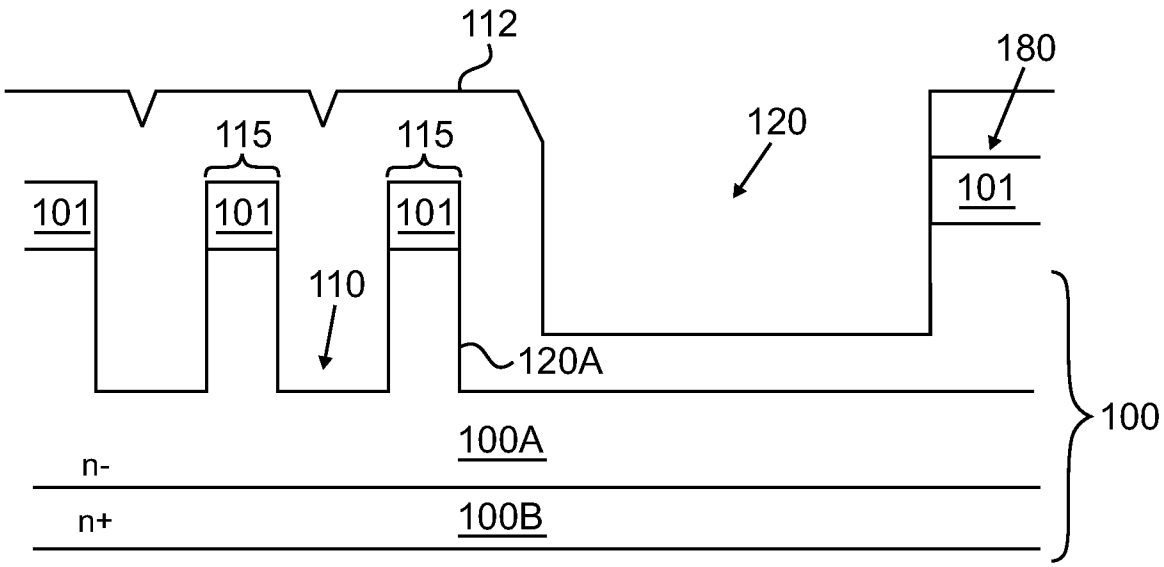

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100B

FIG. 7

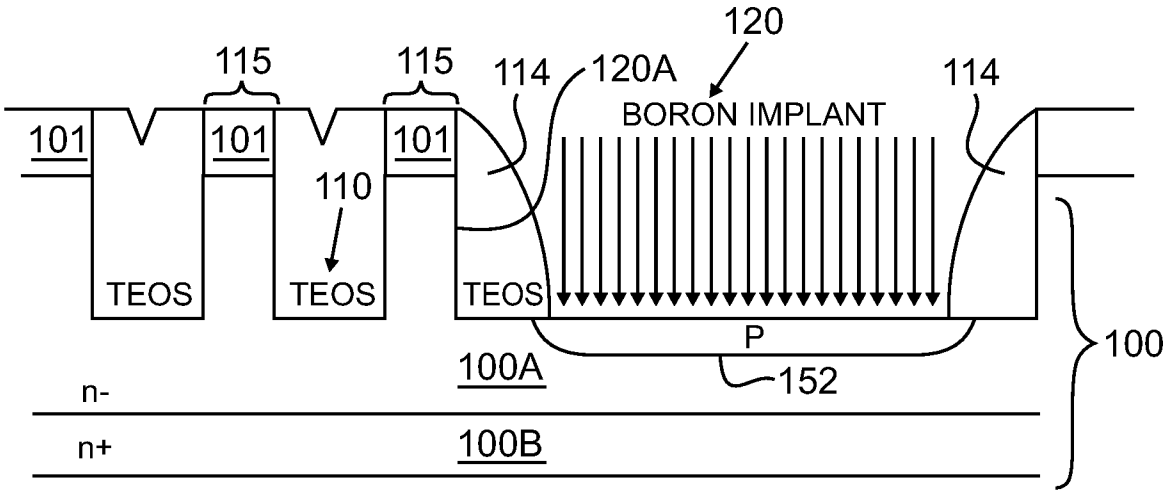

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114
BORON IMPLANT
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110
TEOS
TEOS
TEOS
P
100
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n+
100B

FIG. 8

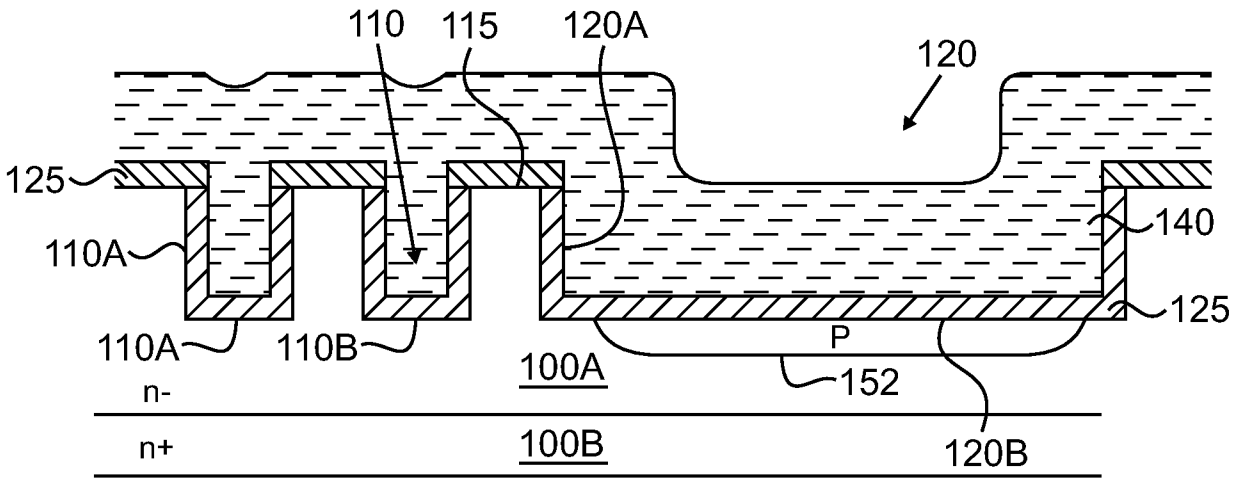

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100A
152
n-
n+
100B
120B

FIG. 9

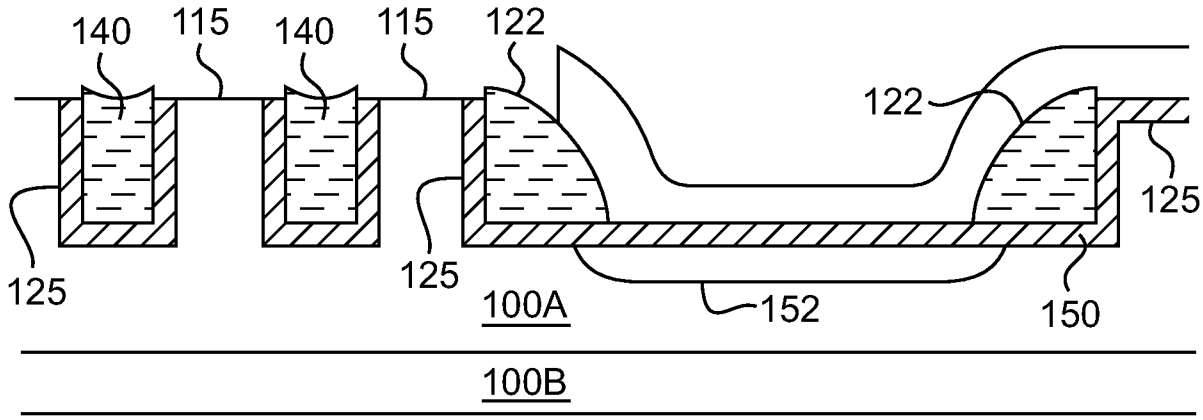

140
115
140
115
122
122
125
125
125
100A
152
150
100B

FIG. 10

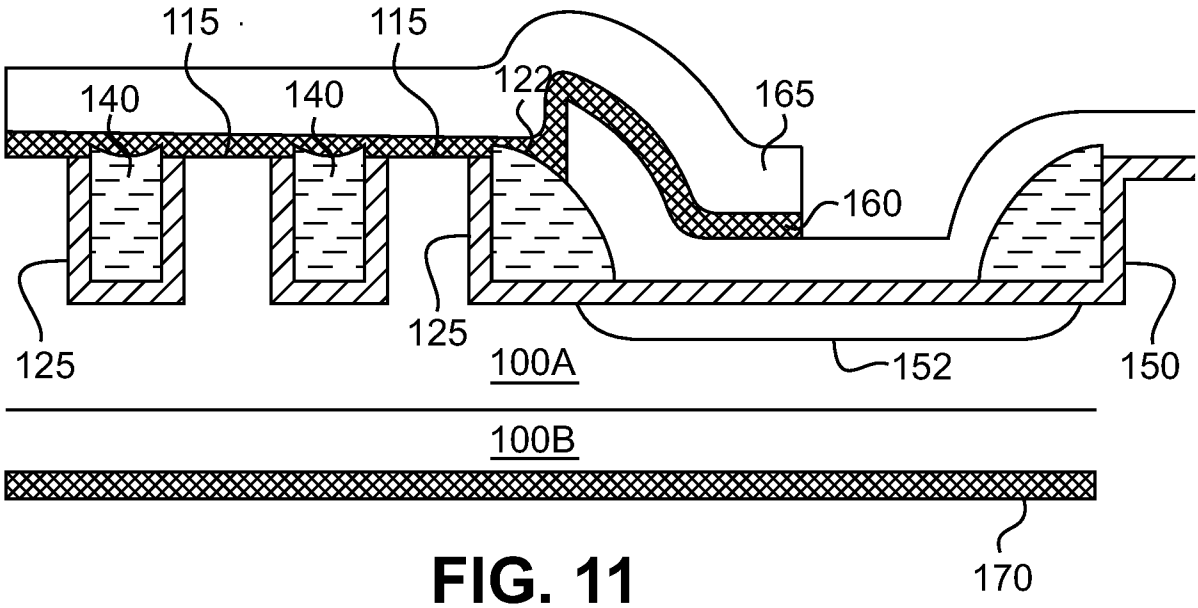

115
115
140
140
122
165
160
125
125
100A
152
150
100B
170

FIG. 11

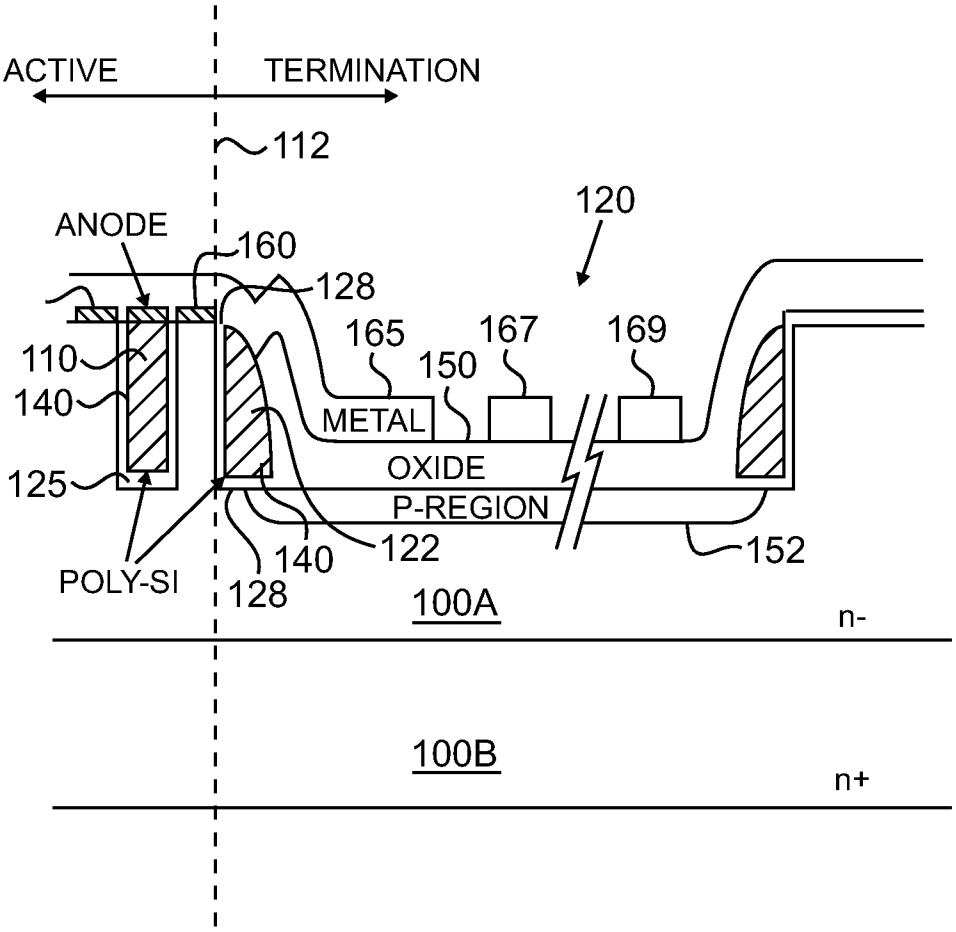
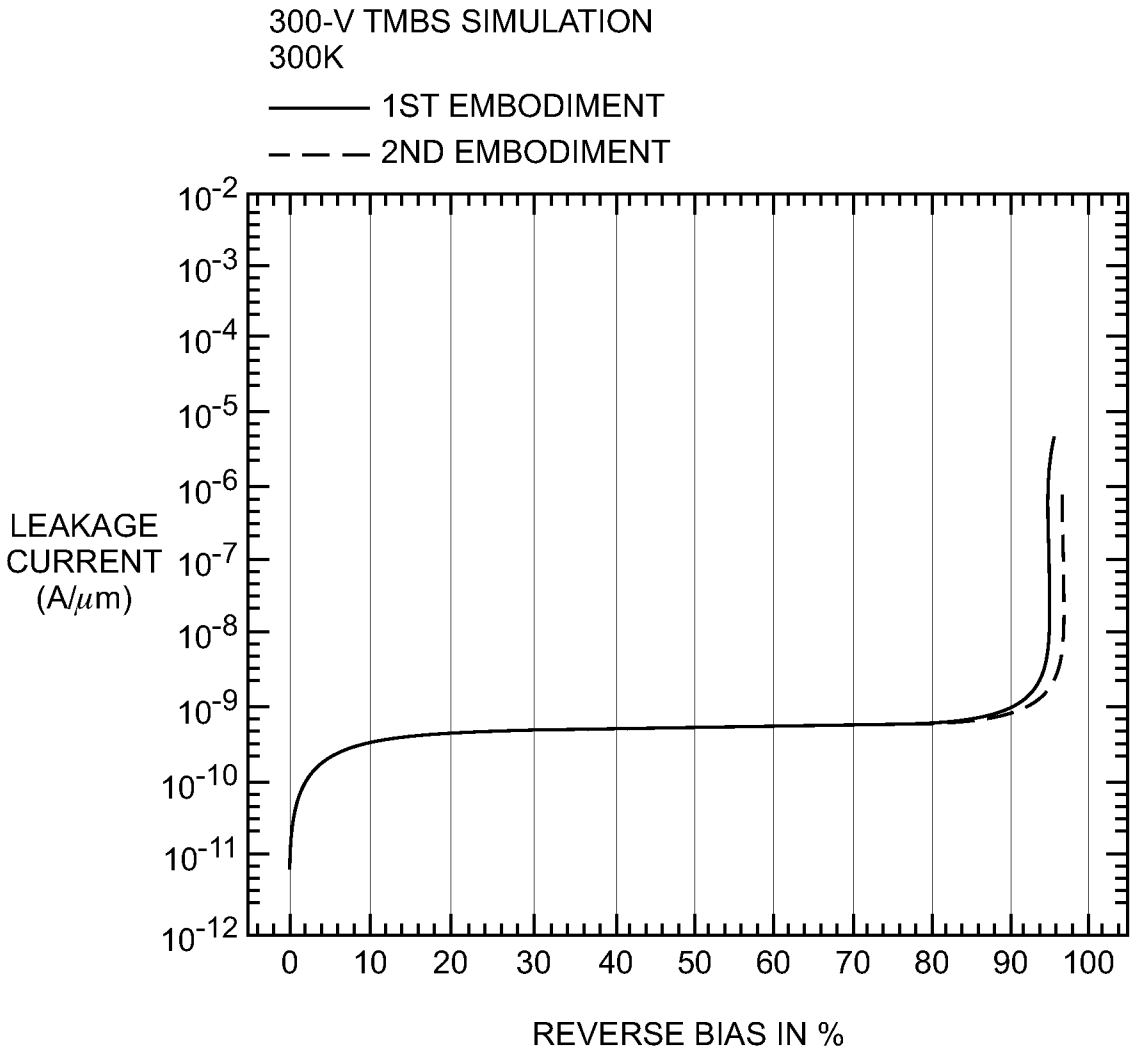
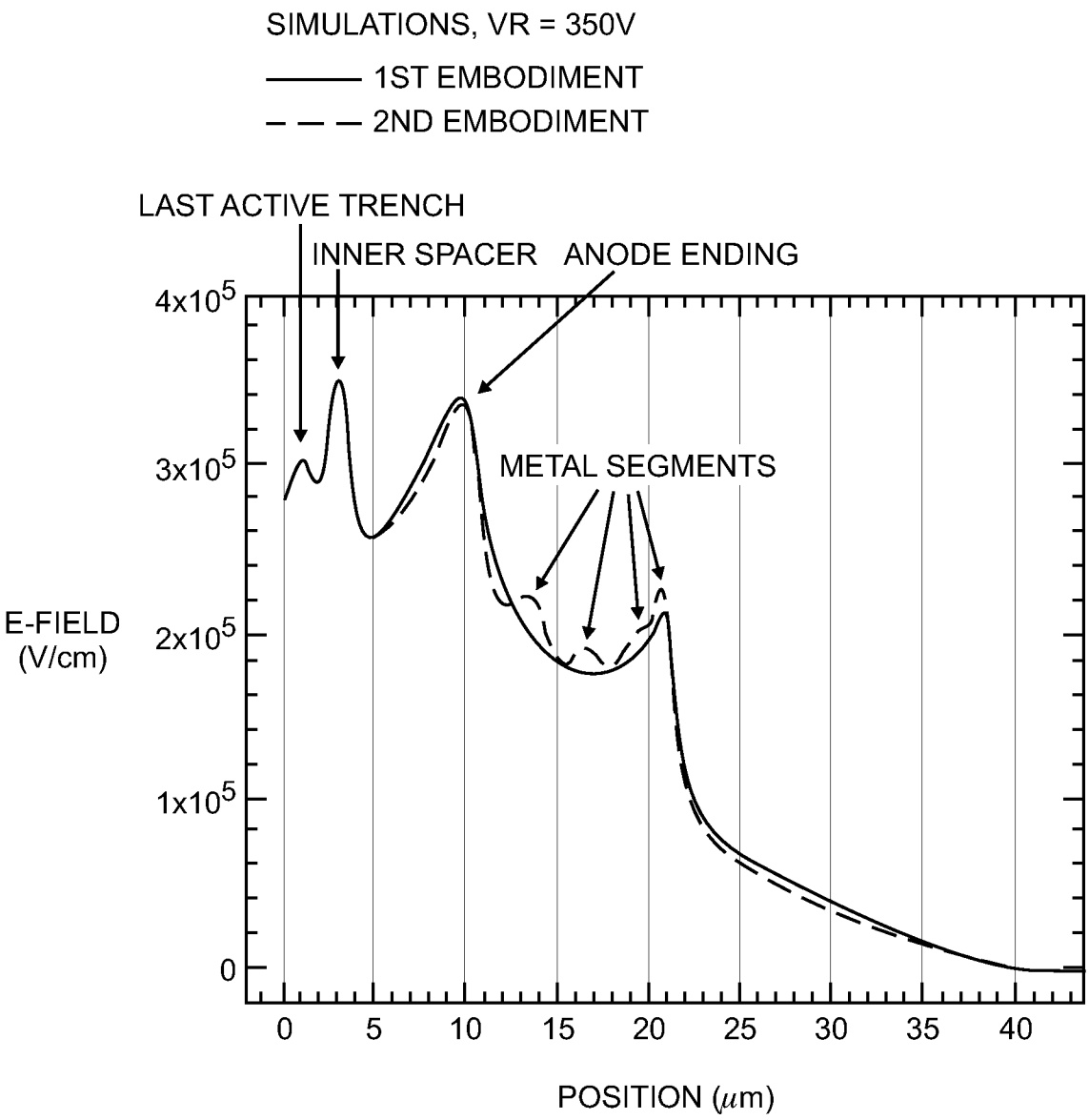

ACTIVE
TERMINATION
112
120
ANODE
160
128
165
167
169
110
150
140
METAL
OXIDE
125
P-REGION
140
122
152
POLY-SI
128
100A
n-
100B
n+

FIG. 12



REVERSE CHARACTERISTICS

FIG. 13



ELECTRICAL FIELD PROFILES

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/027464

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/66 (2011.01)
USPC - 257/280
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) -H01L 21/02, 27/07, 29/00, 29/40, 29/47, 29/66, 29/76, 29/93 (2011.01)
USPC - 257/280-288, 471-486

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent, Google Patent, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,396,090 B1 (HSU et al.) 28 May 2002 (28.05.2002) entire document	1-18
Y	US 7,253,477 B2 (LOECHELT et al.) 07 August 2007 (07.08.2007) entire document	1-18
Y	US 2008/0087896 A1 (CHIOLA) 17 April 2008 (17.04.2008) entire document	10-18
Y	US 2008/0029812 A1 (BHALLA) 07 February 2008 (07.02.2008) entire document	9
A	US 2005/0062124 A1 (CHIOLA) 24 March 2005 (24.03.2005) entire document	1-18

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 April 2011	27 APR 2011
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774