United States Patent [19]

Zurcher

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[54] **PITCH DETECTION PROCESSOR**

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Nov. 16, 1972 France 72.40703

[52] **U.S. Cl.** ..... **179/1 SA,** 179/1 SD

[51] **Int. Cl.** **G10l 1/00**

[58] **Field of Search** ..... 179/1 SD, 1 SA

[56] **References Cited**

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Assistant Examiner—Tommy P. Chin
Attorney, Agent, or Firm—Abraham A. Saffitz

[57] **ABSTRACT**

Processor for the detection of the pitch of a speech wave for use in connection with a vocoder system. It comprises means for detecting the major peaks of the speech wave, means for converting said major peaks into marker pulses defining therebetween pitch periods and a processor unit for treating the marker pulses. The program of treatment is the following: (i) omission of a marker pulse separated from the preceding marker pulse by an interval shorter than the preceding period by more than a tolerance amount with prohibition to omit two consecutive marker pulses; (ii) selection of the preceding period if the actual period is larger or shorter than the said preceding period by more than a tolerance amount with prohibition to select two times in succession the preceding period; (iii) division by two of the value of the pitch if it is larger than a lower limit, say 15ms or 8ms for respectively a male and a female voice.

3 Claims, 10 Drawing Figures

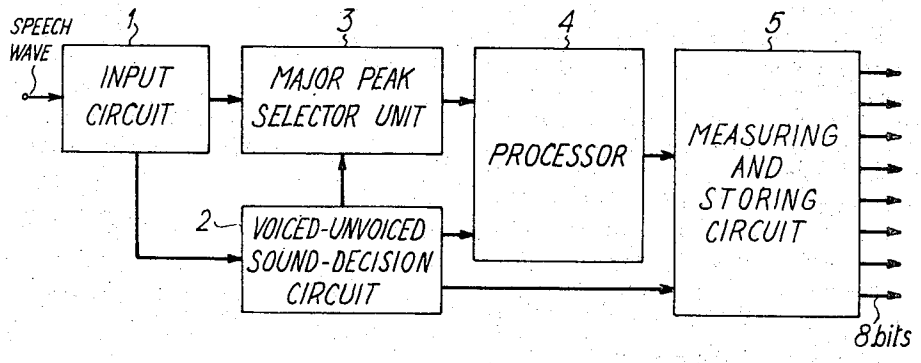


FIG.1

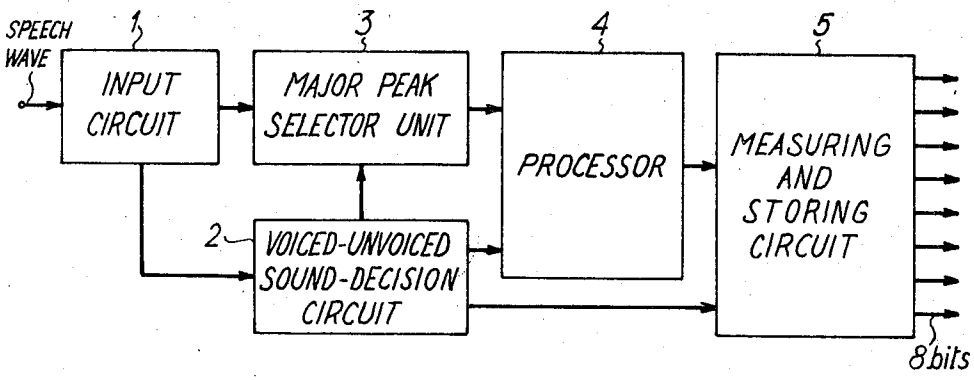

SPEECH WAVE
1
INPUT CIRCUIT
3
MAJOR PEAK SELECTOR UNIT
4
PROCESSOR
5
MEASURING AND STORING CIRCUIT
2
VOICED-UNVOICED SOUND-DECISION CIRCUIT
8 bits

FIG.3

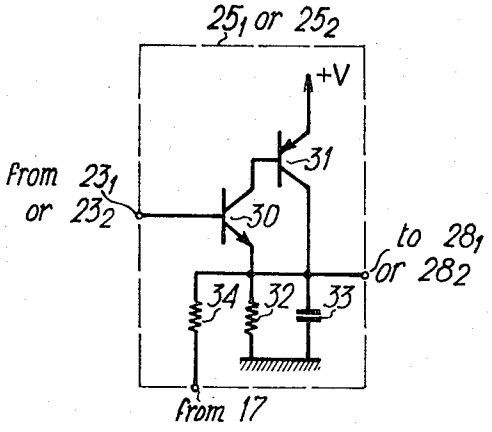

25₁ or 25₂
+V
31
From 23₁ or 23₂
30
to 28₁ or 28₂
34
32
33
from 17

FIG. 2

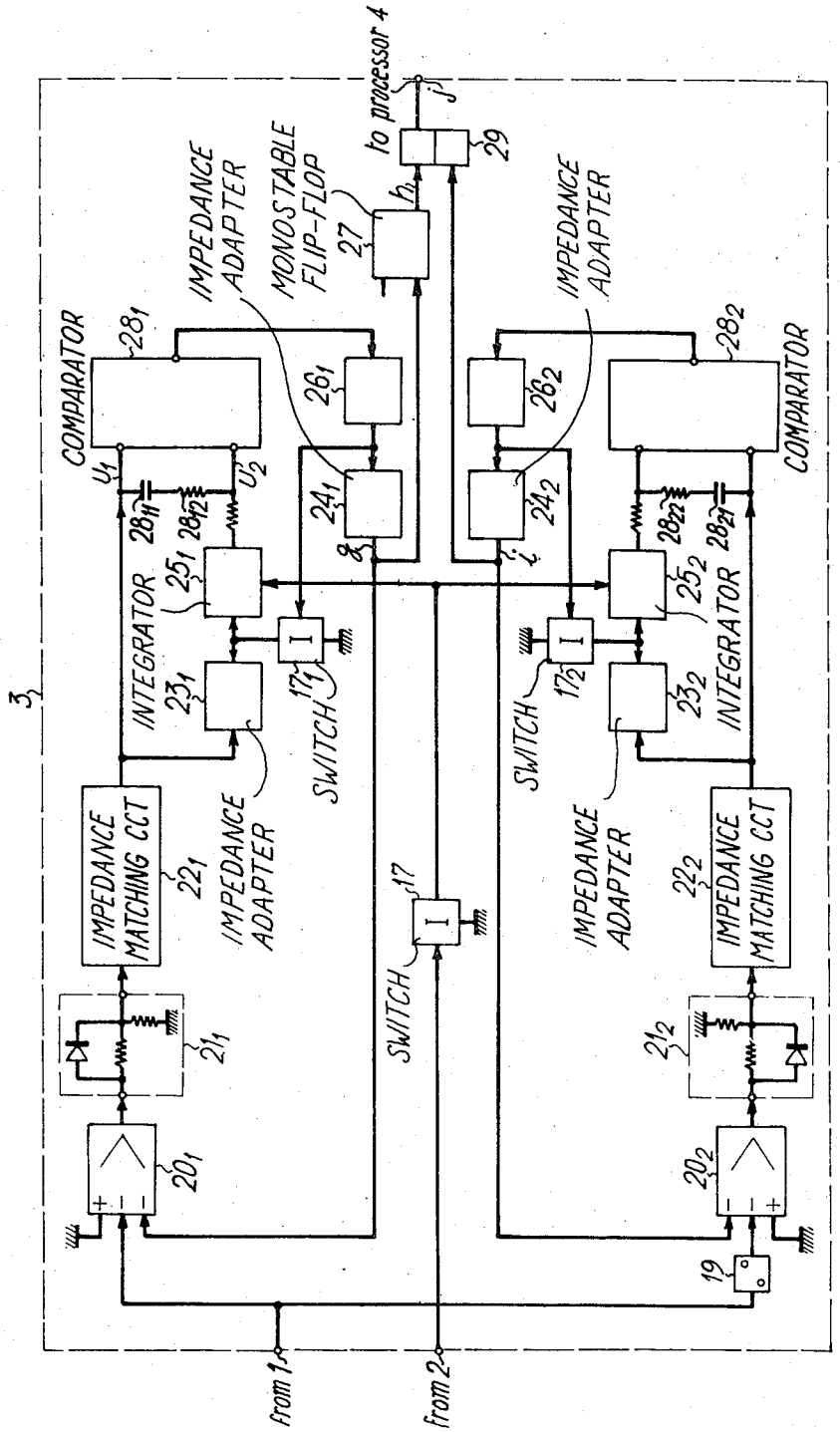

3
from 1
from 2
to processor 4
COMPARATOR
IMPEDANCE ADAPTER
MONOSTABLE FLIP-FLOP
INTEGRATOR
SWITCH
IMPEDANCE MATCHING CCT
IMPEDANCE ADAPTER
29
27
19

FIG.3a

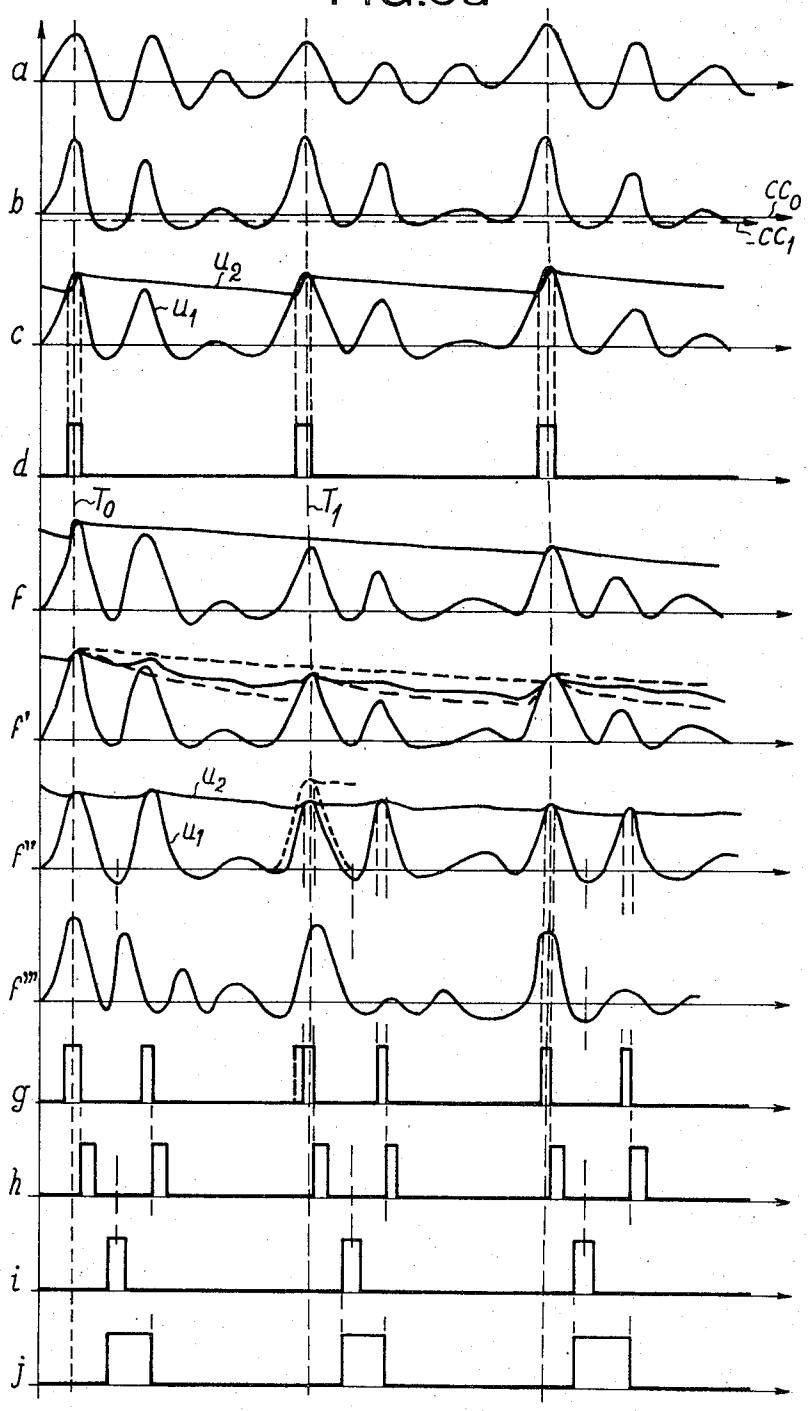


FIG. 4

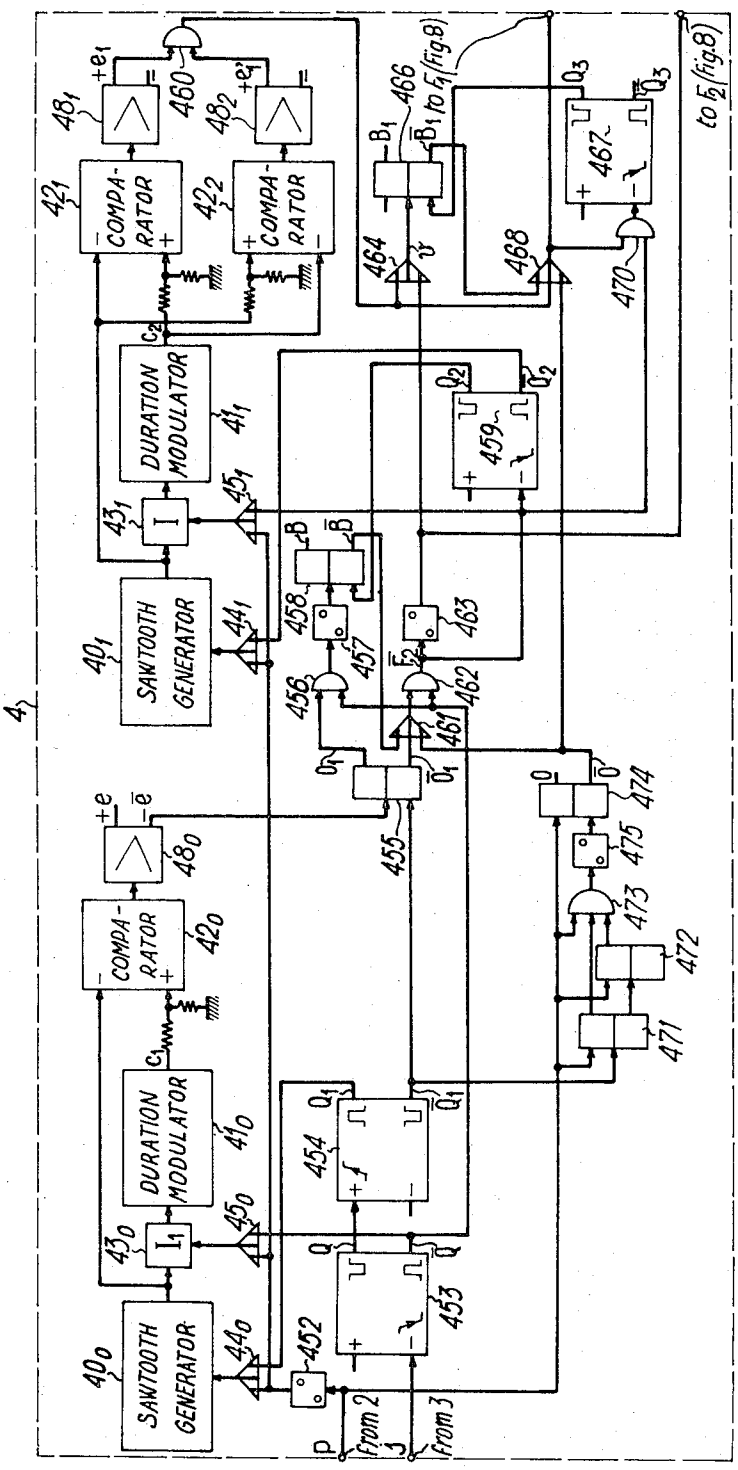

4
SAWTOOTH GENERATOR
DURATION MODULATOR
COMPARATOR
from 2
from 3
to 5 (fig.8)

FIG.5

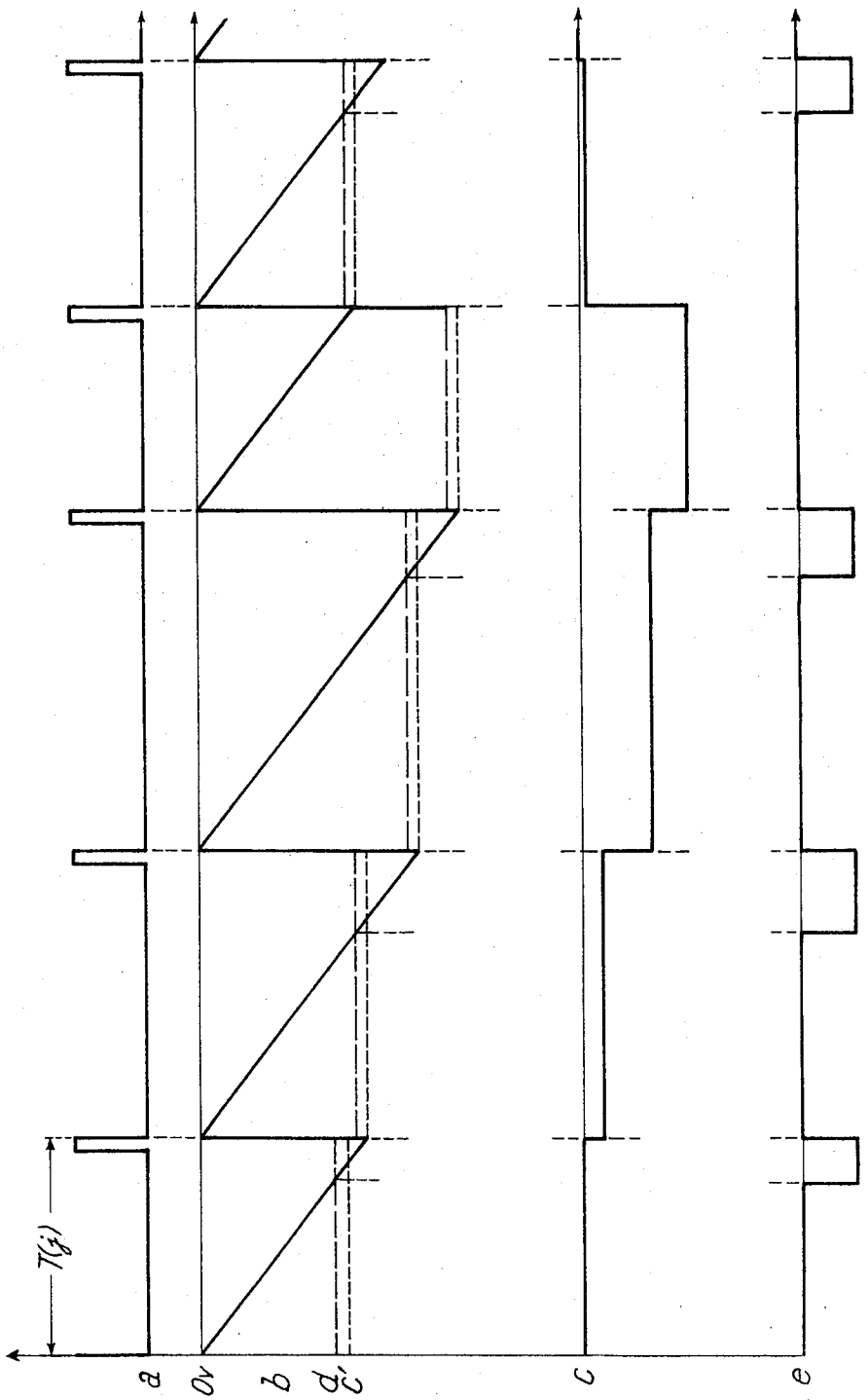


FIG.6

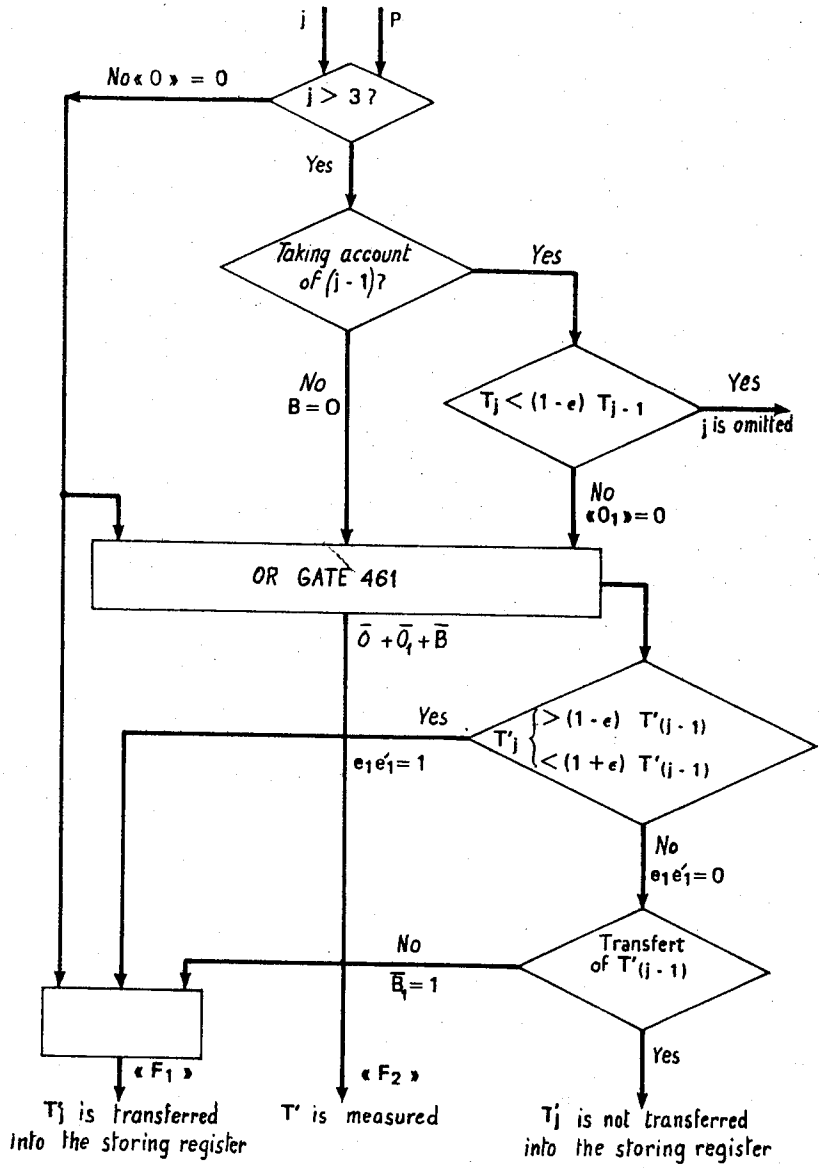

j
P
No « 0 » = 0
j > 3 ?
Yes
Taking account of (j - 1)?
Yes
No
B = 0
Tj < (1 - ε) Tj - 1
Yes
j is omitted
No
« O1 » = 0
OR GATE 461
Ō + Ō1 + B̄
Yes
T'j { > (1 - ε) T'(j - 1) / < (1 + ε) T'(j - 1)
e1e'1 = 1
No
e1e'1 = 0
No
Transfert of T'(j - 1)
B̄1 = 1
Yes
« F1 »
« F2 »
Tj is transferred into the storing register
T' is measured
Tj is not transferred into the storing register

FIG.7

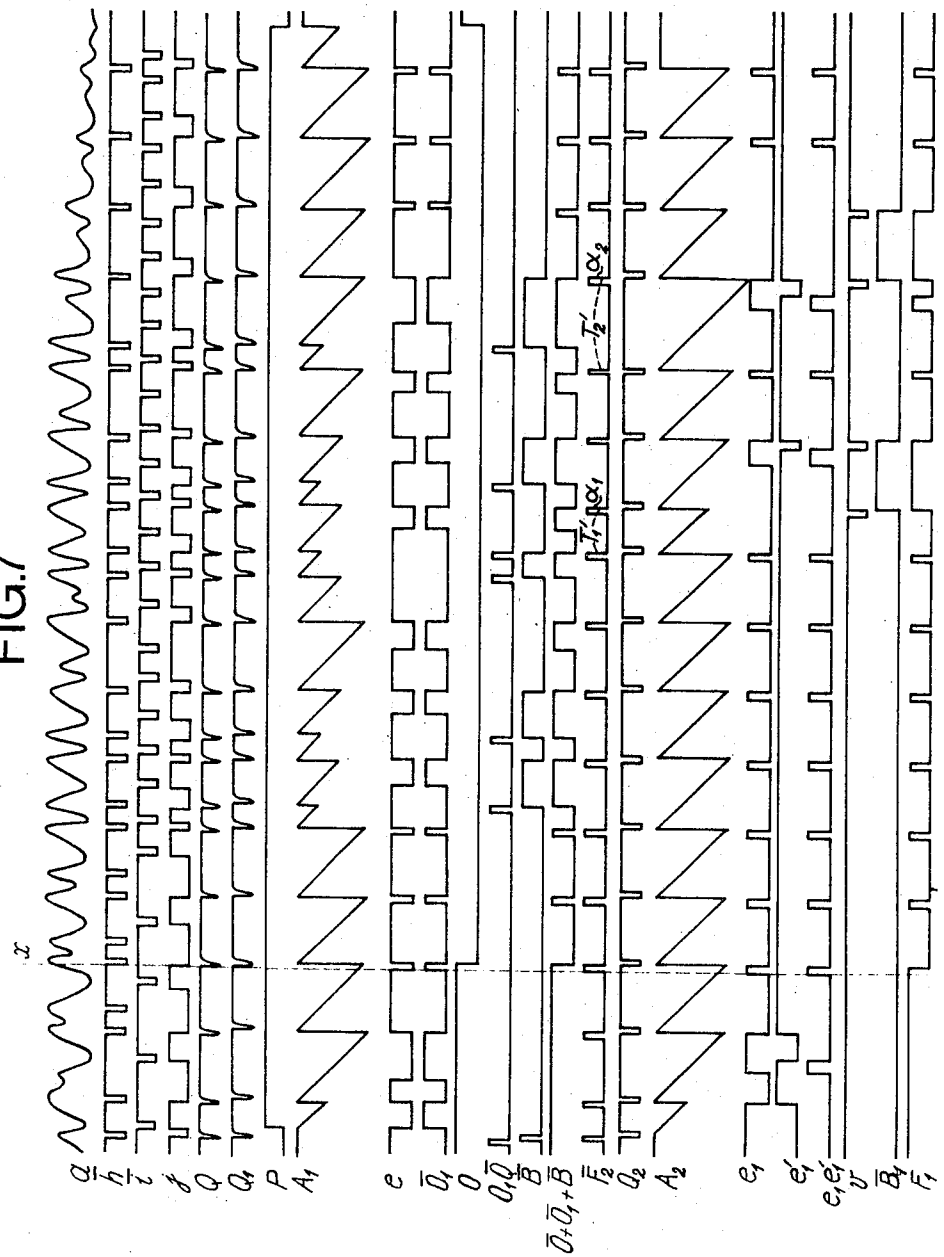

x
Q
h
i
f
Q
Q4
P
A1
e
Q1
O
O1Q
B
O+Q1+B
E2
Q2
A2
e1
e'1
e1e'1
V
B1
F1
T1-nα1
T'2-nα2

FIG. 8

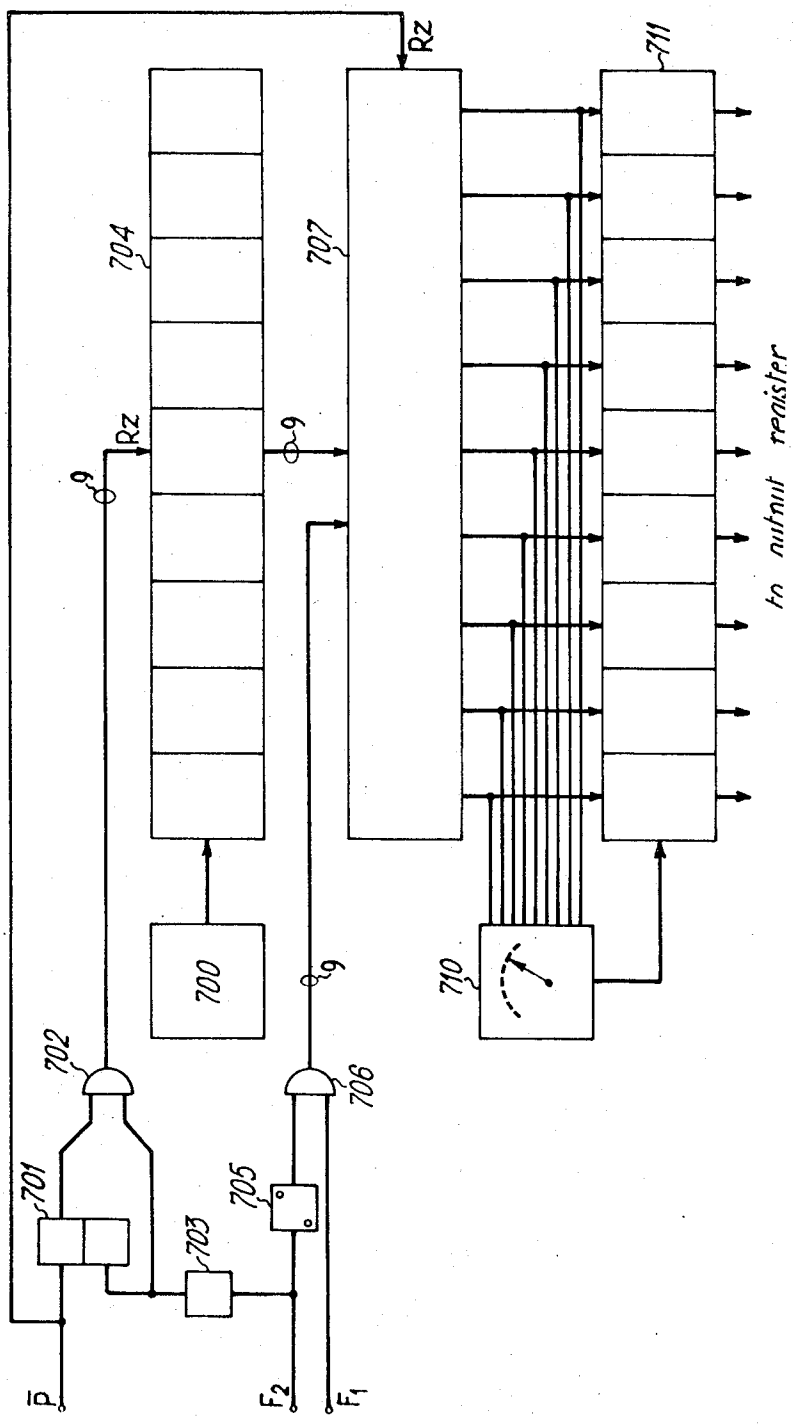
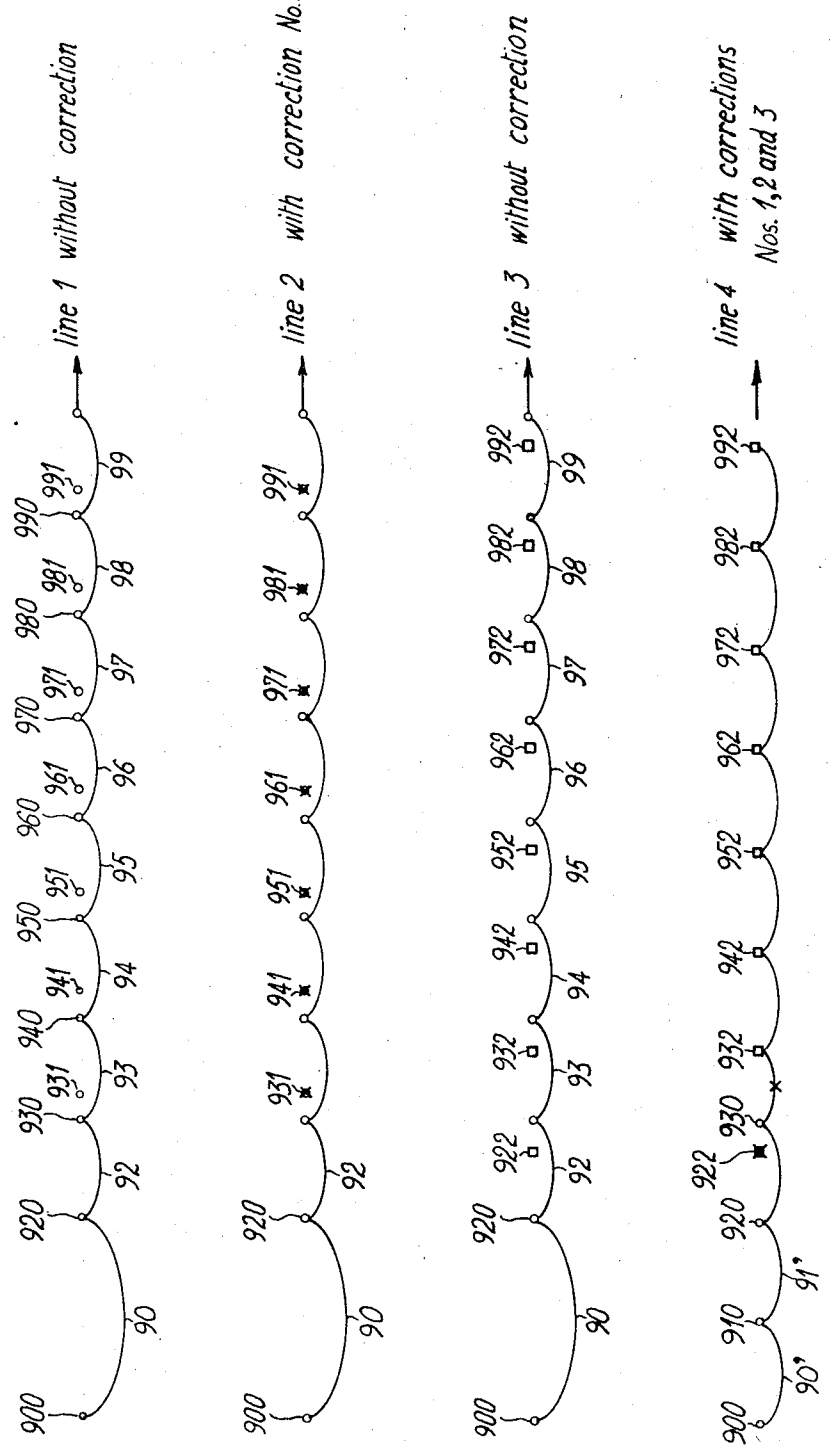

Rz
711
704
707
Rz
9
9
9
700
710
702
706
701
705
703
D
F2
F1
to output register

FIG.9


line 1 without correction
line 2 with correction No.1
line 3 without correction
line 4 with corrections Nos. 1,2 and 3

PITCH DETECTION PROCESSOR

This invention relates to the analysis of speech sound waves and, more particularly, to systems and means for instantaneous determination of the fondamental frequency or pitch of speech waves.

The pitch of speech waves is usually referred to as the repetition of wave patterns which are formed by certain combinations of frequency components having definite amplitude levels and frequency ratios, one with respect to another. In channel vocoder systems, the parameters which are extracted from the speech wave are the energies contained in adjacent frequency bands of the speech wave spectrum, a voiced-invoiced sound decision and pitch. The voiced-invoiced sound decision and the pitch are used to specify the harmonic content of the complex speech wave.

Numerous pitch detectors are described in the prior art. They generally detect the fondamental frequency of a complex speech wave by selecting the major peaks of said wave by means of an arrangement comprising RC elements to which is applied the rectified complex wave voltage. The purpose of such an arrangement is to charge the capacitor of the RC circuit to the level of a major peak and eliminate the minor peaks by way of a slow discharge through the resistor of the circuit. Thus the pitch detector converts the analog speech signal into a signal which retains the rising front edge of the major peaks, replaces the descending rear edge of these peaks by a decaying waveform and produces marker pulses each time the amplitude of the speech signal exceeds the decaying waveform signal.

The simple RC network arrangement which has been just referred to is insufficient, if used alone, to correctly select a major peak per pitch. It has been proposed in the prior art to non-linearly amplify the speech wave signal so that the differences in amplitude between major and minor peaks are partly exaggerated to a practical degree, then to equalize the amplitude of the major peaks by way of saturation feedback. It is also known to treat the marker pulses by comparing to each other the successive time intervals separating two adjacent marker pulses and to cancel those of the intervals which differ from the preceding one in any direction by more than a given percentage and replace them by the said preceding interval.

Thus the pitch detectors of the prior art processes the time intervals between adjacent marker pulses and they consider as a possible pitch each interval between two such marker pulses. Due to the fact that, during transmission it often occurs that the lower frequencies of the speech signal are firmly attenuated by the transmission medium, it results that the major peaks defining the fundamental frequency of the speech signal are practically not higher than the peaks due to the combination of harmonic components. In fact it is quite frequent that two or more major pulses of substantially equal amplitude coexist in the same period.

Is is an object of the present invention to improve the major peak selection process in the pitch detection processors.

Generally speaking, this improvement is obtained by processing both the marker pulses and the periods defined by the marker pulses.

The present invention uses the already known correction condition, namely:

— selection of the preceding period if the actual period is larger or shorter than the said preceding period by more than a tolerance amount, but it completes this correction condition to:

— (second condition), selection of the preceding period if the actual period is larger or shorter than the said preceding period by more than a tolerance amount with prohibition to select two times in succession the preceding period and adds the two following conditions:

— (first condition) omission of a marker pulse separated from the preceding marker pulse by an interval shorter than the preceding period by more than a tolerance amount with prohibition to omit two consecutive marker pulses;

— (third condition) division by two of the value of the pitch if it is larger than a lower limit, say 15 ms (65 Hz) for a male voice and 8 ms (125 Hz) for a female voice.

The correction process and the results deriving from the first, second and third conditions are explained in relation to FIG. **9.**

Line **1** of FIG. **9** shows nine idealized pitch periods **90** and **92–99,** whereof the seven latter ones comprise two marker pulses, **930, 931, 940, 941, 950, 951, 960, 961, 970, 971, 980, 981, 990, 991,** the first period **90** being equal to two times the others. In the prior art pitch detection systems, none of the periods **93–99** is retained since they are each formed of two periods largely differing therebetween and they would be replaced by the repetition of seven times the period **92.** If contrarily to FIG. **9,** periods **93–99** were not equal to period **92** or not equal therebetween, the pitch detection stands in error for seven periods.

In the pitch detector of the invention, according to the first condition, marker pulses **931, 941,... 991** are disregarded since they are very proximate to pulses **930, 940,... 990** respectively and periods **93–99** are detected without error (line **2** of FIG. **9**).

Let us assume now the marker pulse distribution of line **3** before correction. There are supplementary peaks **922, 932, 942,... 992** in periods **92** to **99.** Pulse **922** which is too proximate to pulse **920,** is cancelled. Pulse **930** is also too proximate to pulse **922** but it is not cancelled since cancellation of two successive marker pulses is prohibited. Pulse **932** is farther from pulse **930** than pulse **930** from pulse **922** and accordingly it is not cancelled. But pulses **940, 950,... 990** are cancelled. It results a period **930–932** which is shorter than the preceding one and which is omitted according to the second condition (line **4**).

According to the third condition period **90** is split into two halves **90′, 91′.**

The invention will be better understood with reference to the description which follows and to the attached drawings in which:

FIG. **1** shows a diagram in the form of blocks of the pitch detection processor according to the invention;

FIG. **2** shows a detailed diagram in the form of blocks of the major peak selector unit **3** of FIG. **1** according to the invention;

FIG. **3** shows one embodiment of one of the two integrators of FIG. **2**;

FIG. **3***a* shows a diagram of signals illustrating the operation of the apparatus of FIG. **2**;

FIG. 4 shows a detailed embodiment in the form of blocks of the processor unit 4 of FIG. 1 according to the invention;

FIG. 5 shows a second diagram of signals illustrating the operation of a duration modulator comprised in the processor unit of FIG. 4;

FIG. 6 shows the program of the pitch detection processor;

FIG. 7 shows a third diagram of signals illustrating the operation of the processor unit of FIG. 4;

FIG. 8 shows the mesuring and storing circuit of the pitch detection processor; and

FIG. 9 is a diagram of signals already explained in the introductory part of the specification.

In all these figures the same elements bear the same reference numbers.

FIG. 1 shows the general arrangement of the apparatus according to the invention in the form of blocks. This FIG. 1 shows the input circuit 1 which generates the vocal signals to be analysed in relation to the voiced-invoiced sound decision circuit 2 and the major peak selector unit 3. The two blocks 2 and 3 are connected to one another and with the processor unit 4, itself in communication with the measuring and storing circuit 5 controlled also by the decision circuit 2.

The circuit 2 which determines the presence or absence of voicing in the signal to be analysed and generates a corresponding decision signal P or $\overline{P}$ is of a known type. It applies the principle according to which the energy of the voiced sounds being especially concentrated in the band of frequencies lower than 700 Hz whilst that of the non-voiced sounds is beyond 1,500 Hz thus it suffices to compare the energy E_2 of the signal to be analysed taking in the band beyond 1,500 Hz with the energy E_1 of the signal taken below 700 Hz. The output signal of circuit 2 becomes equal to 1 when the energy detected E_1 is greater than E_2 but this condition must be confirmed. It is zero in the contrary case and this condition needs no confirmation.

To come to this result, it suffices to provide two fillering and detecting chains, one filtering the speech signal from the lowest audio-frequency to 700 Hz, thus generating the energy E_1 whilst the other filters the speech signal from the lowest audio-frequency to 1,500 Hz, thus generation the energy E_2. The output signals of the chains are compared in a differential amplifier which gives the signal P or $\overline{P}$.

These arrangements however would not be sufficient for ensuring the correct "voicing" detector operation. Also by precaution, a circuit detecting the presence of speech is added. This circuit comprises a chain similar to the two preceding ones but where the frequency pass-band is the ordinary vocal band without limitation. A comparator changes state when a threshold fixed experimentally is passed. Insofar as this threshold is not passed the apparatus considers that the signal submitted to its analysis is not speech and imposes therefore insofar as final result transmitted to the other part of the pitch detection processor a non-voiced signal $\overline{P}$.

FIG. 2 shows in the form of blocks, the diagram of the major peak selector unit 3. This circuit 3 receives at its inputs the signals *a* and P coming respectively from the circuits 1 and 2 of FIG. 1 and generates an output signal *j* which is transmitted to the circuit 4 of FIG. 1. The signals *a* and P are applied at homologous inputs of two chains of circuits the different elements of which are designated by the same reference numerals with a subscript 1 for the upper chain and a subscript 1 for the lower chain.

These two chains comprise amplifiers 20_1 and 20_2, the bottom chain being provided in addition with an analog inverter 19_1. The signal a coming from 1 therefore is subjected to the same treatment in these two chains except inversion, the top chain being allocated to the treatment of positive major peaks and that of the bottom to the treatment of negative major peaks. It suffices therefore to describe the top chain.

The amplifier 20_1 is followed by an expander 21_1 comprising a diode in parallel with a series resistor connected to a shunt resistance. This expander of known type (see U.S. Pat. No. 2,957,134 issued Oct. 18, 1960 to M.V. KALFAIAN) has function of favouring the passage of the positive peaks for which the diode presents in fact a low resistance whilst the remainder of the signal which passes this diode is weakened. This expander therefore renders the peaks finer so as to define better their position in time. The signal thus treated is admitted into an impedance matching CCT 22_1 which does not transmit its direct component and does generates a signal u_1. Impedance matching CCT 22_1 allows matching the output impedance of the expanser 21_1 to the input impedance of the comparator 28_1 as regards the signal u_1 and to the input impedance of a second impedance adapter 23_1. In adapter 23_1 there is superimposed to the signal a new direct component for restoring that which was suppressed by impedance matching CCT 22_1.

The output signal of 23_1 is then applied to an integrator of special type 25_1 which will be described hereinafter unless it is grounded through the switch 17_1. The signal u_2 generated by the integrator 25_1 is compared to the signal u_1 in the comparator 28_1. The signal resulting from the comparison is applied to adapter 26_1 which controls switch 17_1 and to an impedance adapter 24_1. The output signal of adapter 24_1 is applied to the input of amplifier 20_1 where it is added to the speech signal. In addition, this output signal is applied to monostable flipflop 27 which is triggered by the rear front of the comparison impulse (FIG. 3*a*, line *g*) and controls bistable flipflop 29 (FIG. 3*a*, line *h*). In addition, the signal P coming from the voiced-unvoiced sound decision circuit 2 controls the switch 17.

The diagram of one of the two integrators 25_1 and 25_2 is given in FIG. 3. It comprises two transistors mounted in the so-called "Complementary two-stage emitter follower", PNP 31 and NPN 30, the output terminal of which can be grounded either through a RC network 32, 33 or through this network in parallel with an additional resistor 34; this resistor is inserted by switch 17. The switch 17 behaves like a variable resistor passing progressively from a zero value to an infinite value within four to five periods when the signal P passes from state "0" to state "1". The integrator has therefore two time constants RC and $R\,R_1\,C/R + R_1$ (R, R_1 resistances of resistors 32, 34; C capacitance of capacitor 33). The operation of these integrators is the following : if a positive peak comes from 23_1 or 23_2 to the base of the transistor 30 the current supplied by the two transistors 30 and 31 causes the voltage at the terminals of the capacitor 33 to increase until the summit of the peak is reached. Then the amplitude of this peak decreases and the emitter-base circuit of the transistor 30 is polarized in opposite direction, since the voltage at the terminals of the capacitor 33 has not decreased as

rapidly as the voltage at the base of the transistor **30.** This explains that this complementary two stage emitter follower circuit although possessing a low output impedance can only supply a substantial current in a single direction like the so-called Darlington circuit.

Under these conditions the two transistors begin to block. The voltage u_2 then becomes greater than the voltage u_1, the comparator 28_1 changes state which has the effect of activating switch 17_1 and shortcircuiting the input of the integrator 25_1. The two transistors **30** and **31** then block completely and capacitor **33** discharges into the equivalent resistance $R\,R_1/R + R_1$.

It should be noted that the discharge of capacitor **33** is effected through an equivalent resistor which has two resistance limits namely the resistance of resistors **32** and **34** in parallel and the resistance of resistor **32** and progressively varies between these limits due to the passage of the transistor constituting the switch **17** from the conductor state to the blocked state.

FIG. 3*a* shows signal waveforms intended to explain how the circuits of FIG. **2** operate.

Line *a* shows the speech signal after low-pass filtering. In line *b* the direct component CC_1 of the speech signal is replaced by a larger direct component CC_0 which results in the cancellation of the minor peaks. In line *c*, the signal u_1 is replaced by a decaying signal u_2 in the intervals between the major peaks. Line *d* shows the marker pulses derived from the major peaks.

In line *f*, the decaying part of the signal has a too weak slope to intersect the major peak at T_1. Thus this major peak would not give rise to any marker pulse if special precautions were not taken. To mitigate it, a part of signal u_1 is subtracted from signal u_2 by means of capacitor 28_{11} and resistors 28_{12} and 28_{13}. Thus the decaying signal, instead of being a mere decreasing exponential signal, is a signal fluctuating about this exponential signal which, this time, intersects the major peak at T_1 (FIG. 3*a*, line *f'*).

The lines *f''* and *g* illustrate the usual operation of the apparatus and the corresponding marker pulses. The instant of occurrence of the forward front of the marker pulses is determined by the intersection of the curves representing u_1 and u_2 and this intersection is subject to displacements in time imparted by the variations of amplitude of the voltage u_1. This is shown by the peak in bloken line of line *f''* and the corresponding marker pulse in broken line of line *g*.

On the other hand the intersection relative to the rear front is marked by the origin of the decrease of u_2 which coincide with the peak of u_1. At the moment when u_2 becomes greater than u_1 the comparator 28_1 changes state happening which is produced at moments very close to the peaks of u_1 and explains the independence of the position of the second front in respect of the amplitude of u_1. An advantage of this is taken by triggering monostable flipflop **27** by the rear fronts of impulses *g*. The resulting pulses are pulses *h* of FIG. 3*a*.

In other respects to confirm the change of stage of comparator 28_1 its output impulses after passage through the adapter 24_1 are superimposed on the peaks by addition that has already been stated. There is therefore set a feedback effect by the chain of circuits 26_1 and 24_1 which is illustrated by the signal *f'''*. This signal shows that a peak having caused a change of state is likely more amplified than that which altough of little different amplitude has not caused such a change of state. This feedback facilitates therefore the taking into account of a single peak on two peaks which follow very closely and which are almost equal.

At the beginning of a voiced sound, a compressor comprised in the input circuit **1** is put into operation. Thus the voiced signal decreases during a time interval of, say, four to five periods of the basic frequency of the voice. During this decreasing period, the selection of the major peaks cannot be achieved by the means which have just been described because the decrease of the signal u_2 is not sufficiently rapid. For increasing the decaying constant of signal u_2, resistor **34**, which minimizes the constant to $R\,R_1\,C/(R + R_1)$, is inserted in the RC network of FIG. **3** by means of switch **17.** The progressive passage of the decaying factor from its minimum to its maximum value which latter value corresponds to the stable phase of the compressor, is effected in four or five pitch periods.

The operation of the chain of the bottom of FIG. **2** is similar to that of the chain at the top by substituting for the positive peaks the negative peaks of the signal to give rise to impulses *i* similar to the impulses *g* which have just been discussed and which are directed towards the bistable flipflop **29** whilst that of the chain at the top are applied to this bistable flipflop through the monostable flipflop **27.** The reason of this difference is that the pulses *g* and the pulses *h* derived therefrom which change the flip-flop **29** to state zero define the beginning of the pitch periods whilst the pulses *i* which change the flipflop **29** to state one are only reset pulses.

The signal *j* generated by flipflop **29** and the signal P generated by decision circuit **2** controls the processor unit **4** of FIG. **1** the detailed diagram of which is given in FIG. **4.** The output signals of the processor unit **4** are the signals F_1 and F_2.

The signal P is utilised directly to reset a counter formed by the flipflops **471, 472** and **474** and the complementary signal $\overline{P}$ obtained in the inverter **452** is utilised to feed the OR-gates 44_0, 45_0, 44_1 and 45_1. These gates serve similar members : saw-tooth voltage generators 40_0 and 40_1 and switches 43_0 and 43_1, said switches being identical with switch **17** of FIG. **2** and controlling respectively pulse duration modulators 41_0 and 41_1. The saw-tooth voltage generators are started and stopped by the fronts of pulses P and by control pulses Q or Q_1 derived from the negative fronts of pulses *j*. The saw-tooth voltage **502** decreases from zero to a level **503** reached at the next control pulse. During the preceding saw-tooth signal **500,** the duration modulator has stored therein the level **501** which was the maximal amplitude reached by the saw-tooth voltage **500.** The saw-tooth voltage **504** and an attenuated level **503'** derived from level **503** through an attenuator connected between duration modulators 41_0 and comparator 42_0 are applied to the said comparator. Comparator 42_0 produces pulses *e* whose front edges coincide with the equality of the actuel saw-tooth voltage and the attenuated maximal level of the preceding saw-tooth voltage and whose rear edges coincide with the control pulses.

The output signals of the comparators 42_0, and 42_1 are put in form and amplified in amplifiers 48_0, 48_1 and 48_2 which have two outputs + and − giving complementary signals. The logical signals *e* coming from the chain 40_0 to 48_0 control the flipflop **455** and those e_1 and e_1' coming from the chains 40_1 to 48_1 and 48_2 control the

AND-gates **460** which itself controls the OR-gates **464** and **468.**

According to FIG. **5,** comparator 42_0 and comparator 42_1 do not produce output marker pulses when the actual pitch period is shorter than the preceding period by a given amount and comparator 42_2, due to the fact that its input leads are crossed, do not produce output marker pulses when the actual pitch period is longer than the preceding period by a given amount. The amount is defined by the attenuator connected to the input of the comparator across the lead coming from the duration modulator.

Referring now to the lower part of FIG. **4,** signal *j* coming from the selector unit **3** is applied to the input of the monostable flipflop **453** which utilises the descending fronts of this signal and generates pulses Q and $\overline{Q}$ (FIG. 7) having a duration of 10 ms. The signal Q drives in its turn a monostable flipflop **454** which utilises the ascending fronts of the driving pulses and generates pulses of duration equal to **15** ms and designated by Q_1 and $\overline{Q_1}$ (FIG. 7). The signal $\overline{Q}$ controls AND-gates **456** and **462** and together with signal $\overline{P}$ OR-gate 45_0. This signal $\overline{P}$ is also applied to the input of the OR-gate 44_0 together with signal Q_1 and signal $\overline{Q_1}$ causes the flipflops **471** and **472** to progress. $\overline{Q_1}$ also resets the flipflop **445** which counts pulses $\overline{e}$.

The flipflops **471** and **472** control the AND-gate **473** which when these flipflops are both in state one and when P is also in state "1" is open and sets flipflop **474** in state "0." When the signal P is in the state "0," it resets the flipflops **471, 472** and **474.**

The flipflop **455** produces from pulses $\overline{e}$ the pulses $\mathbf{0}_1$ and their complements $\overline{\mathbf{0}_1}$. $\mathbf{0}_1$ together with $\overline{Q}$ is applied to the input of AND-gate **450** and causes, by means of the inverter **457,** the flip-flop **458** to change over which generates signals B, $\overline{B}$ (FIG. 7). $\overline{\mathbf{0}_1}$ together with $\overline{B}$ and $\overline{\mathbf{0}}$ is applied to the input of the OR-gate **461** and the signal $\overline{\mathbf{0}_1} + \overline{B} + \overline{\mathbf{0}}$ thus obtained is applied together with $\overline{Q}$ to the input of AND-gate **462** to give the signal $\overline{F_2} = \overline{Q}$ $(\overline{\mathbf{0}_1} + \overline{B} + \overline{\mathbf{0}})$ utilised at several points in particular in the OR-gate 45_1 where it is applied together with the signal $\overline{P}$ for controlling switch 43_1. Signal $\overline{F_2}$ is also applied to monostable flipflop **459** which generates the signal Q_2 lag-shifted with respect to $\overline{F_2}$. Q_2 resets flipflop **458** whilst $\overline{Q_2}$ feeds OR-gate 44_1 controlling saw-tooth generator 40_1.

In addition this same signal $\overline{F_2}$ is inverted in **463** and becomes F_2 which is applied to the measuring and storing circuit **5.** The signal F_2 is also applied to OR-gate **464** together with the product $(e_1 \times e_1')$ to give the signal *v* which controls the flipflop **466** which supplied the signals B_1 and $\overline{B_1}$.

Different signals above referred to, namely $\overline{\mathbf{0}}$ coming from flipflop **474,** $(e_1 \times e_1')$ coming from AND-gate **460** and $\overline{B_1}$ coming from flipflop **466** are applied to OR-gate **468** generating the signal $F_1 = B + (e_1 \times e_1') + \overline{\mathbf{0}}$ which is applied to the input of AND-gate **470** together with signal $\overline{F_2}$ for forming the signal F_1 which controls monostable flipflop **467.** The signal Q_3 obtained at the output of **467** resets flipflop **466.**

The circuit of FIG. **4** operates according to the algorithm of FIG. **6.**

The *j* pulses are counted, the first being that which appears after the signal P has taken the value 1 and has reset the counter formed by flipflops **471, 472, 474.** If three *j* pulses have been counted, **471** and **472** are both in state one and flipflop **474** changes over to state one, thus generating signal 0 which lasts during all the time where P = 1. Thus is achieved the first phase of the program : $j > 3$? As long as $j \leq 3$, $\overline{\mathbf{0}}$ activates OR-gate **461** and pulses $\overline{F_2}$ are transmitted to the measuring and storing circuit **5.** OR-gate **468** being also activated, transfer pulses F_1 are also transmitted to circuit **5.**

Pulses *j* control the circuit chain producing pulses $\overline{e}$ for detecting whether a period T_j is shorter than the preceding T_{j-1} or not:

$$T_j < (1 - \epsilon)T_{j-1}$$

where ϵ is the attenuation factor.

If the answer is negative, the signal $\overline{e}$ changes over flipflop **455** to $\mathbf{0}_1$ which activates OR-gate **461** and AND-gate **462.** The signal F_2 is then applied to measuring and storing circuit **5.**

If the answer is positive, pulse F_2 is generated or not according to the value of signal B which answer the question: Was pulse $(j - 1)$ taken into account or not?

If the impulse $(j - 1)$ has not been taken into account, $\overline{B} = 1$, the OR-gate **461** is active and F_2 is generated and causes the measurement of T_j' by the circuit **5.**

On the other hand it must be verified that the period T_j' determined by the interval between two impulses of F_2 is comprised between the limits given by the previous situation namely the period $T'_{(j-1)}$ with a tolerance fixed by a parameter ϵ as previously which poses the question: :

$$(1 - \epsilon)\ T'_{(j-1)} < T'_j \leq (1 + \epsilon)\ T'_{(j-1)}\ ?$$

to which the chains $40_1, 41_1, 42_1, 42_2, 48_1$ and 48_2 (FIG. 4) reply by way of the AND-gate **460** giving the function $(e_1 \times e'_1)$ the value 0 or 1. If $(e_1 \times e'_1) = 1$, the OR-gate **468** is active and the transfer of the period T'_j is authorised by F_1.

If $(e_1 \times e'_1) = 0$, the transfer of the period T'_j may take place or not according to the value of B_1; if the preceding transfer has not taken place the signal B_1 representing the reply to the question of the transfer of $T'_{(j-1)}$ is equal to 0 ($\overline{B_1} = 1$) and the signal F_1 is generated by giving the autorisation of transfer of the contents of the counter of the block **5** to the register of the same block.

FIG. **7** shows a complete operation of a system from the signal *a* similar to the signal *a* of FIG. **3***a*. The signals *h* and *i* are generated as has been stated and are shown here by their complements $\overline{h}$ and $\overline{i}$ from where the output signal *j* of the flipflop **29** (FIG. **3**) results. These pulses *j* give rise to pulses Q in **459** and pulses Q_1 in **454** (FIG. **4**).

The signal P obtained in the decision circuit **2** triggers the saw-tooth voltage generator 40_0 (FIG. **4**) and the duration modulator 41_0. The comparator 42_0 gives rise to the signal *e* at the output of amplifier 48_0. The negative front of this *e* signal causes the flipflop **455** to change over and this flipflop is reset by the $\overline{Q}$ signal which gives the signal $\overline{\mathbf{0}_1}$.

The first Q_1 pulses located at the left hand side of the vertical line *xx'* correspond to the start of a voiced sound and it requires at least three Q_1 pulses for the counters **471, 472** causing the change of the state of **474** generate the signal **0.** Flipflop **474** is reset when the signal P comes to zero. In the AND-gate **456** the product $(\mathbf{0}_1 \times \overline{Q})$ is obtained and causes the state of **458** to change. Thus the ascending fronts of the signal $\overline{B}$ are

obtained whilst the OR-gate **461** generates the $(\overline{0} + \overline{0}_1 + \overline{B})$ signal. This signal is applied together with signal $\overline{Q}$ to AND-gate **462** which generates signal $\overline{F_2}$ the negative fronts of which give rise to the signal Q_2 by the action of monostable flipflop **459.** These pulses delayed with regard to $\overline{Q}$ reset flipflop **458.** The vertical *xx'* determines a transitory time in the course of which the apparatus detects the nature of the signal "a," voiced or unvoiced, and defines the period.

The continuation of the diagram of FIG. **7** concerns the second stage of the processor unit of FIG. **4** in which are located the sawtooth voltage generator 40_1, the duration modulator 41_1 and the comparators 42_1 and 42_2. These comparators produce the pulses e_1 and e'_1 which together with the signal F_2 are applied to OR-gate **464** to form the signal *v*. The flipflop **466** changes state on the ascending fronts of *v* and generates the signal $\overline{B_1}$ which together with $(e_1 \times e'_1)$ and $\overline{0}$ is applied to OR-gate **468** for generating the train of pulses F_1 authorizing or not the transfer of T'_j in the register of the measuring and storing circuit **5.**

To reset flipflop **466** a signal Q_3 is produced by the monostable flipflop **467** activated by the rear edges of the signal $(F_1 \times \overline{F_2})$ generated by the AND-gate **470.**

Referring now to FIG. **8,** there is shown the measuring and storing circuit **5** whose input signals are the signals $\overline{P}$, F_1 and F_2. The signal $\overline{P}$ when it is in the state "1" resets flipflop **701** and this flipflop is set to one by the signal F_2 delayed by the delay circuit **703;** the signal $(\overline{P} \times F_2)$ generated by AND-gate **702** serves as a reset signal for the counter **704** which comprises here seven flipflops and which counts the clock pulses generated by pulse generator **700.**

The signal $(F_1 \times \overline{F_2})$ is effected by means of inverter **705** and AND-gate **706.** This signal is utilised as a transfer signal for transferring the contents of counter **704** into register **707.** The contents of this register is received in decoder **710** and when it is greater than a predetermined number, a displacement order of one binary weight is sent to the output register **711** and this register stores a corrected combination equal to the combination registered in **707** divided by **2.**

When the signal P of FIG. **7** passes to the state "1" the flip-flop **701** is held at zero until the first pulse F_2 which is delayed in delay circuit **703** by a delay during which the transfer of the preceding information recorded in the register **707** takes place if a transfer pulse F_1 has appeared before the signal P takes up again the state zero, this latter state resetting the register **707.**

It results from the arrangement of FIG. **8** that the time between two successive pulses F_2 is always counted between two resets of counter **704,** but the count is transferred into register **707** only when a pulse F_1 coincides with a pulse F_2.

It is to be noted that decoder **710** performs the third correction listed in the introductory part by shifting by a binary weight towards the right the binary number being transferred, thus dividing it by two.

What I claim is:

1. A processor for the detection of the pitch of a speech wave for use in connection with a vocoder system comprising means for detecting the major peaks of said speech wave, means for converting said major peaks into a train of marker pulses, each pair of consecutive marker pulses of said train defining a pitch period, means for cancelling in said train each marker pulse separated from the preceding marker pulse by an interval shorter than the preceding pitch period by more than a tolerance amount, means for prohibiting the cancellation of more than a first given number of consecutive marker pulses, means for storing the value of each pitch period defined by two consecutive non-cancelled marker pulses and not differing from the preceding pitch period by more than a tolerance amount, means for substituting the preceding pitch period for each pitch period differing from said preceding pitch period by more than a tolerance amount and means for prohibiting the substitution for more than a second given number of consecutive pitch periods, of the respective preceding pitch periods.

2. A processor for the detection of the pitch of a speech wave as set forth in claim **1,** in which said first and second numbers are both equal to 2.

3. A processor for the detection of the pitch of a speech wave for use in connection with a vocoder system comprising means for detecting the major peaks of said speech wave, means for converting said major peaks into a train of marker pulses, each pair of consecutive marker pulses of said train defining a pitch period, means for cancelling in said train each marker pulse separated from the preceding marker pulse by an interval shorter than the preceding pitch period by more than a tolerance amount, means for prohibiting the cancellation of more than a first given number of consecutive marker pulses, means for storing the value of each pitch period defined by two consecutive non-cancelled marker pulses and not differing from the preceding pitch period by more than a tolerance amount, means for substituting the preceding pitch period for each pitch period differing from said preceding pitch period by more than a tolerance amount, means for prohibiting the substitution for more than a second given number of consecutive pitch periods, of the respective preceding pitch periods and means for dividing by two the value of those of the recorded pitch periods that are larger than a predetermined value.

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