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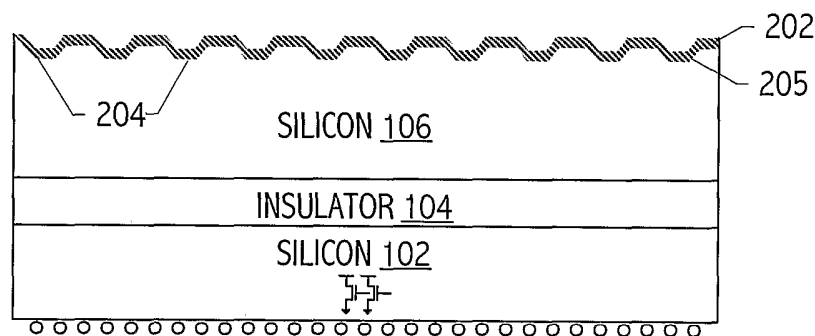
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(54) Title: INTEGRATED CIRCUIT WITH INCREASED HEAT TRANSFER



(57) Abstract: A technique for improving the thermal power dissipation of an integrated circuit (100) includes reducing the thermal resistivity of the integrated circuit (100) by increasing heat transfer in vertical and/or lateral directions. These results are achieved by increasing the surface area of the backside (105) and/or the surface area of the lateral sides of the integrated circuit die. In some embodiments of the invention, an integrated circuit (100) includes circuit elements formed closer to a first surface (101) of a semiconductor substrate (106) than to a second surface (105) of the semiconductor substrate (106). The semiconductor substrate (106) has a varying profile (204) that substantially increases the surface area of a thermal interface (205) formed on the second surface (105) as compared to the second surface (105) being substantially planar. A maximum depth of the profile is less than the thickness of the semiconductor substrate.

INTEGRATED CIRCUIT WITH INCREASED HEAT TRANSFER

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BACKGROUND**Technical Field**

[1001] The present invention relates to integrated circuits, and more particularly to thermal power dissipation of integrated circuits.

Background Art

[1002] High temperatures of integrated circuits may decrease reliability and efficiency of the integrated circuit. As the density of transistors on an integrated circuit increases and transistor sizes decrease, thermal power generated by the circuit increases, thus increasing the need for removing heat from a packaged integrated circuit. For example, an increase in transistor density may result in an increase in power density by a factor of two or three.

[1003] The thermal resistance of a packaged part typically includes thermal resistance contributions from a lid, a thermal interface material (TIM) between the lid and a backside of an integrated circuit, and the integrated circuit itself. To reduce the overall thermal resistance of the packaged part, one or all of these contributions may be reduced. To improve a thermal resistance of the lid or the TIM, new materials may be used. However, silver or gold alloys which have a low thermal resistance, may be cost prohibitive for the lid of typical integrated circuits. The thickness of the lid may be reduced to reduce the lid's thermal resistance, but elimination of the lid leaves the integrated circuit vulnerable to cracking. Reducing the thermal resistance of the TIM also may be impracticable because although a thermal interface provided by typical TIMs is inferior to thermal interfaces provided by other materials (e.g., some metals or diamond), TIMs are softer than other materials and reduce cracking of the integrated circuit die.

[1004] Accordingly, improved techniques for removing heat from a packaged integrated circuit are desired.

DISCLOSURE OF THE INVENTION

[1005] A technique for improving the thermal power dissipation of an integrated circuit includes reducing the thermal resistivity of the integrated circuit by increasing heat transfer in vertical and/or lateral directions. These results are achieved by increasing the surface area of the backside and/or the surface area of the lateral sides of the integrated circuit die. In some embodiments of the invention, an integrated circuit includes circuit elements formed closer to a first surface of a semiconductor substrate than to a second surface of the semiconductor substrate. The semiconductor substrate has a varying profile that substantially increases the surface area of a thermal interface formed on the second surface as compared to the second surface being substantially planar. A maximum depth of the profile is less than the thickness of the semiconductor substrate.

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[1006] In some embodiments of the present invention, a method includes reducing a thermal resistivity of an integrated circuit die by increasing a surface area of a first surface of a semiconductor substrate. Circuit elements are formed closer to a second surface of the semiconductor substrate than to the first surface. A maximum depth of a profile of the first surface is less than a thickness of the semiconductor substrate.

MODE(S) FOR CARRYING OUT THE INVENTION

[1007] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[1008] **FIG. 1** illustrates a cross-sectional view of an exemplary packaged integrated circuit.

[1009] **FIG. 2A** illustrates a cross-sectional view of an exemplary integrated circuit including a semiconductor substrate having a backside with a varying profile consistent with some embodiments of the present invention.

[1010] **FIG. 2B** illustrates a top-down view of an exemplary integrated circuit including a semiconductor substrate having a backside with a varying profile consistent with some embodiments of the present invention.

[1011] **FIG. 3** illustrates a cross-sectional view of an exemplary integrated circuit including a semiconductor substrate having a backside with a varying profile and a thermally conductive layer with a planar profile consistent with some embodiments of the present invention.

[1012] **FIG. 4A** illustrates a cross-sectional view of an exemplary integrated circuit having lateral sides with a varying profile consistent with some embodiments of the present invention.

[1013] **FIG. 4B** illustrates a top-down view of an exemplary integrated circuit having lateral sides with a varying profile consistent with some embodiments of the present invention.

[1014] **FIG. 5A** illustrates a cross-sectional view of an exemplary integrated circuit including a semiconductor substrate having a backside with a non-uniformly varying profile consistent with some embodiments of the present invention.

[1015] **FIG. 5B** illustrates a top-down view of an exemplary integrated circuit including a semiconductor substrate having a backside with a non-uniformly varying profile consistent with some embodiments of the present invention.

[1016] The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[1017] Referring to FIG. 1, an exemplary integrated circuit and cooling technique includes a silicon substrate 106, insulator layer 104, and silicon layer 102. Silicon layer 102 includes substantially all of the circuit devices in packaged integrated circuit 100. The interface, e.g., interface 101, between silicon layer 102 and conductive bumps 103 is the front side of the integrated circuit. Interface 105, i.e., the interface between silicon substrate 106 and thermal interface material (TIM) 108, is the backside of the integrated circuit and is substantially planar.

[1018] Thermal interface material 108 is included between metal lid 110 and silicon substrate 106 to eliminate air gaps produced by surface irregularities of metal lid 110 and silicon substrate 106 and to increase joint conductivity to improve heat transfer between metal lid 110 and silicon substrate 106. Thermal interface material 108 may be a thermal grease, thermally conductive compound (e.g., an aluminum compound), thermally conductive elastomer, thermally conductive adhesive tape, or other suitable material.

[1019] Heat sink 112 (e.g., a fan or other power dissipating structure) is attached to metal lid 110 to increase the heat transfer between metal lid 110 and the ambient environment (e.g., surrounding air). An additional thermal interface material layer may be included between metal lid 110 and heat sink 112 to eliminate air gaps between metal lid 110 and heat sink 112 and to increase joint conductivity to improve heat transfer from metal lid 110 to heat sink 112.

[1020] An exemplary TIM transfers less heat from the silicon interface than other low-thermal resistance materials (e.g., metals). A technique for increasing the heat transfer of the cooling scheme illustrated in FIG. 1 includes inserting a layer of material having a high thermal conductivity (i.e., greater than approximately 10W/mK) between silicon substrate 106 and TIM 108. However, the rate of heat transfer by this cooling technique may be limited by the surface area of the substantially planar interface 105. Interface 105 is fixed to the size of the integrated circuit backside, limiting the rate of power dissipation. Typically, approximately 90% of heat transferred from the integrated circuit is transferred in a positive z-direction (i.e., vertically, in a direction orthogonal to interface 105) and approximately 10% of heat transferred from the integrated circuit is transferred in a negative z-direction. A negligible amount of heat (typically no more than approximately 1 to 2%) is transferred in a lateral direction (i.e., a direction parallel to interface 105) from the lateral sides of the integrated circuit.

[1021] Techniques for improving the heat transfer of the aforementioned cooling techniques are illustrated in FIGS. 2A-5B. Referring to FIGS. 2A and 2B, an integrated circuit formed by silicon substrate 106, insulator layer 104, and silicon layer 102 has at least a portion of its backside (i.e., interface 205) that has a varying profile (i.e., a substantially non-planar profile). Although it is customary to fabricate integrated circuit devices circuit-side up, backside processing may be performed after completion of the front side processing. Interface 205 may be formed by any suitable manufacturing technique (e.g., patterning and etching the backside of silicon substrate 106) to form trenches (e.g., trenches 204), vias, holes, grooves, or other suitable non-planar structures in silicon substrate 106. In one embodiment of the invention, roughing-up

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the backside of silicon substrate 106 forms scratches in the backside of silicon substrate 106. The varying profile increases the surface area of at least a portion of the interface between silicon substrate 106 and thermally conductive layer 205, thus increasing the vertical heat transfer from the backside of silicon substrate 106 to an adjacent material.

[1022] Thermally conductive layer 202 may be formed on the substantially nonplanar backside of silicon substrate 106. Thermally conductive layer 202 may be a metal, diamond, or other suitable thermally conductive material. In some embodiments of the invention, thermally conductive layer 202 may be a TIM (e.g., a TIM having a high thermal conductivity), and a separate thermally conductive layer may be excluded. The thickness of thermally conductive layer 202 may vary with the depth of the trenches and the material used. For example, although a thinner thermally conductive layer may be preferable to a thicker thermally conductive layer, the thermally conductive layer is typically thick enough to provide substantially complete coverage of the trench or other non-planar structure. In addition, if the thermally conductive layer is too thin, it may be brittle, increasing the likelihood of fracturing the thermally conductive layer, which may impede lateral heat transfer across the layer. Although other materials (e.g., silver, gold, diamond, etc.) are better thermal conductors than copper, copper may be used because it is softer and less expensive than other thermal conductors. Although diamond is a better thermal conductor than other materials (e.g., materials including copper, silver, or gold), in general, to form a diamond layer on the integrated circuit, the integrated circuit is typically exposed to hot conditions and high pressure, which may be undesirable in some applications. In addition, forming thicknesses of a diamond layer greater than approximately 1000 μ m may be too time consuming for some applications.

[1023] The depth of the profile of the backside of silicon substrate 106 may depend on the material chosen to be the thermal conductor. For example, when using diamond as the thermal conductor, since diamond is also an electrical insulator, the profile depth may extend through the silicon substrate to insulator layer 104. However, the profile depth may extend through less than the entire silicon substrate to reduce the likelihood of electrical coupling to circuitry in silicon layer 102, e.g., when an electrically conductive material is chosen as the thermal conductor.

[1024] In one embodiment of the present invention, the integrated circuit of FIG. 2A is packaged in a lidless package, transferring heat from the backside of silicon substrate 102 to the ambient environment via a substantially non-planar interface between thermally conductive layer 202 and the ambient environment. However, in some embodiments of the invention, e.g., an integrated circuit package including a lid, a thermally conductive layer (e.g., thermally conductive layer 302 of FIG. 3) having one substantially planar interface between the thermally conductive layer and an adjacent material (e.g., a TIM layer or a metal lid) may be used. In some embodiments of the invention, thermally conductive layer 302 may be a TIM (e.g., a TIM having a high thermal conductivity), and a separate thermally conductive layer may be excluded.

[1025] One technique for improving the vertical heat transfer includes thinning the integrated circuit die, which may make thermal dissipation in the lateral direction more critical. In one embodiment of the invention, the lateral heat transfer of an integrated circuit may be increased by increasing the surface area of the lateral

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sides of the integrated circuit as illustrated in FIGS. 4A and 4B. Conventional techniques to form a varying profile may be used to vary the profile of a portion of a lateral side of an integrated circuit, prior to the integrated circuits being separated from a wafer into individual die. Conventional techniques for forming a varying profile on the front side or backside of an integrated circuit may be adapted to form a varying profile on a lateral side of the integrated circuit (e.g., using specialized chambers) after the integrated circuit die has been separated from the wafer. A laser or other suitable technique may also be used to vary the profile of the lateral sides of the integrated circuit die.

[1026] After forming a varying profile on the lateral sides, a layer of a thermally conductive material (e.g., thermally conductive layer 402) may be formed on the lateral sides. As described above for thermally conductive layer 202, thermally conductive layer 402 may include copper, silver, gold, diamond, a TIM, or other suitable thermally conductive materials. The depth of thermally conductive layer 402 may be chosen according to the material chosen for the layer, as described above, and according to the location of devices in silicon layer 102.

[1027] In some embodiments of the invention, the profile of the silicon substrate backside or lateral sides may be tailored according to a heat profile of the integrated circuit design. For example, some portions of the integrated circuit (i.e., hot spots, e.g., those portions exercised at a high rate) may generate more heat than others. Hot spots may slow down transistors proximate to the hot spots and contribute to race conditions in the integrated circuit. Regions of a lateral side or backside having greater profile variations than other locations of the integrated circuit (e.g., trenches 502) may be included to improve thermal power dissipation of these hot spots, as illustrated in FIGS. 5A and 5B. Thus, this technique may reduce the occurrence of hot spots and race conditions produced by those hot spots. The varying profile may also be configured in patterns that strengthen the integrated circuit die as compared to other profiles (e.g., cross-hatching or serpentine patterns).

[1028] The description of the invention set forth herein is illustrative, and is not intended to limit the scope of the invention as set forth in the following claims. For example, while the invention has been described in an embodiment implemented in silicon-on-insulator and silicon semiconductor technology, one of skill in the art will appreciate that the teachings herein can be utilized with other integrated circuit manufacturing technologies, e.g., bulk silicon technology, gallium arsenide technology, etc. Variations and modifications of the embodiments disclosed herein, may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims.

WHAT IS CLAIMED IS:

1. An integrated circuit die comprising:
circuit elements formed closer to a first surface (101) of a semiconductor substrate (106) than to a second surface (105) of the semiconductor substrate (106);
the semiconductor substrate having a varying profile (204), the varying profile (204) substantially increasing the surface area of a thermal interface (205) formed on the second surface (105) as compared to the second surface (105) being substantially planar; and
wherein a maximum depth of the profile is less than the thickness of the semiconductor substrate (106).
2. The integrated circuit die, as recited in claim 1, further comprising:
a thermally conductive layer thermally coupled to the semiconductor substrate, the thermally conductive layer being electrically isolated from the circuit elements.
3. The integrated circuit die, as recited in claim 2, wherein the thermally conductive layer comprises an interface to ambient having a varying profile, the varying profile substantially increasing the surface area of the interface to ambient as compared to the interface to ambient being substantially planar.
4. The integrated circuit die, as recited in claim 2 or 3, wherein the thermally conductive layer has a substantially planar interface to a thermal interface material (TIM).
5. The integrated circuit die, as recited in claim 1, 2, 3, or 4, wherein increases in density of profile variations are based at least in part on portions of the integrated circuit generating greater thermal power than other portions of the integrated circuit.
6. The integrated circuit die, as recited in claim 2, 3, 4, or 5 wherein the thermally conductive layer is a thermal interface material (TIM).
7. The integrated circuit die, as recited in claim 2, 3, 4, or 5 further comprising:
a thermal interface material (TIM) layer adjacent to the thermally conductive layer.
8. A method comprising:
reducing a thermal resistivity of an integrated circuit die (100) by increasing a surface area of a first surface (105) of a semiconductor substrate, circuit elements being formed closer to a second surface (101) of the semiconductor substrate than to the first surface (105), a maximum depth of a profile of the first surface (105) being less than a thickness of the semiconductor substrate (106).

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9. The method, as recited in claim 8, further comprising:
reducing the thermal resistivity of the die by thermal dissipation via a thermally conductive layer
formed on the first surface.
10. The method, as recited in claim 9, further comprising:
further reducing the thermal resistivity of the die by increasing the surface area of the thermally
conductive layer.

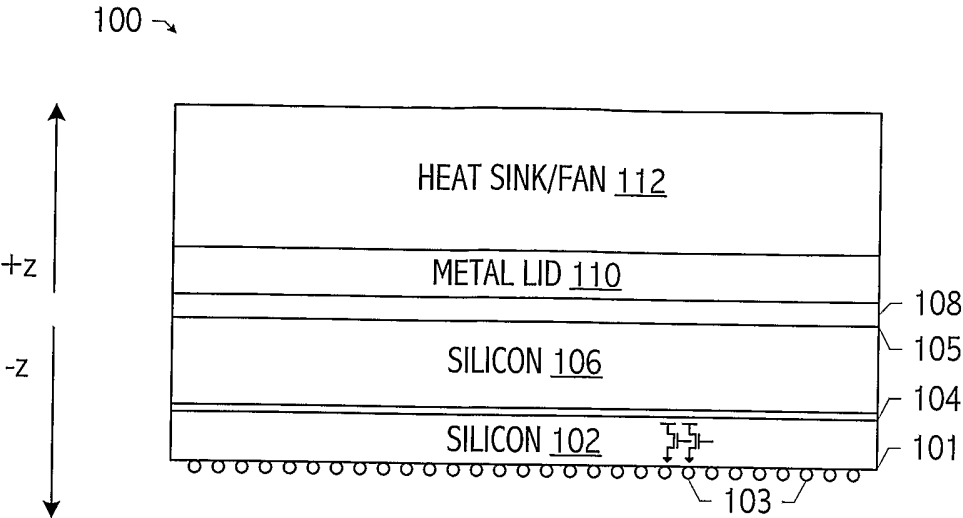


FIG. 1

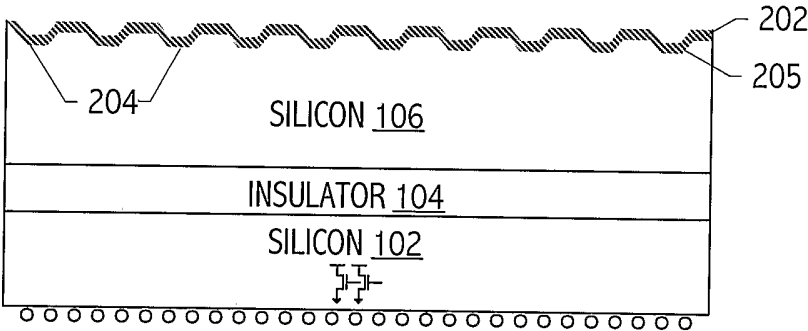


FIG. 2A

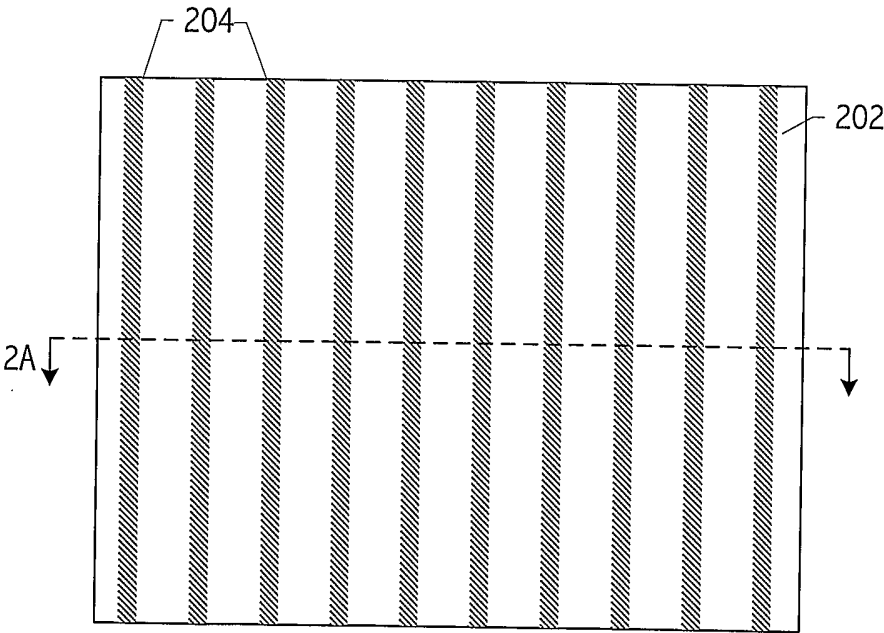


FIG. 2B

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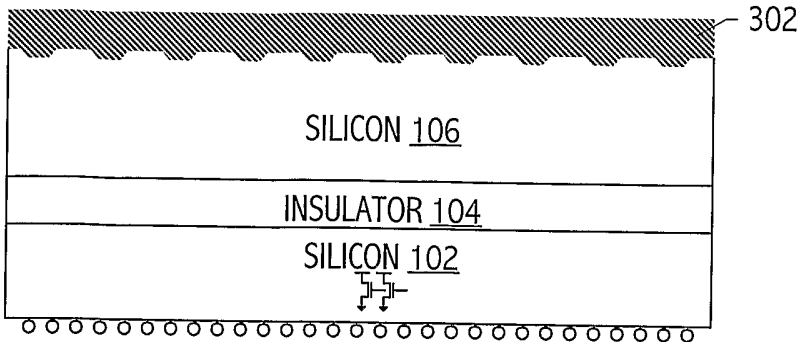


FIG. 3

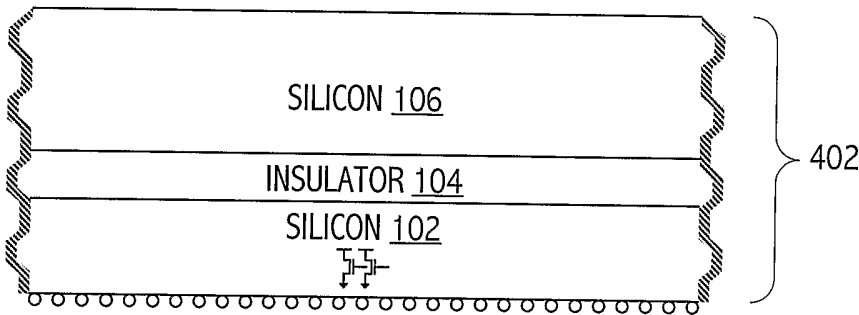


FIG. 4A

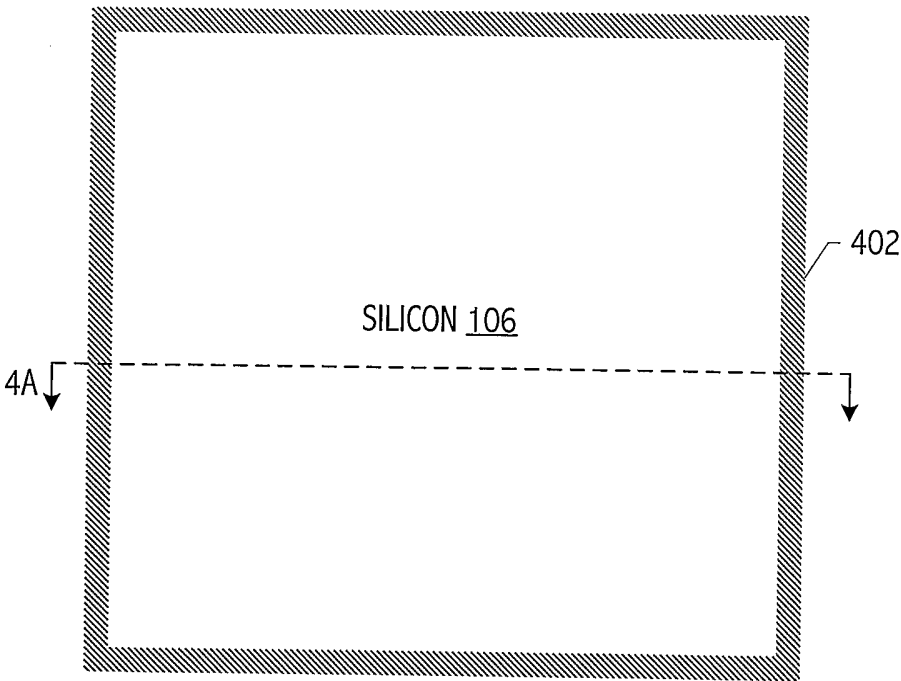


FIG. 4B

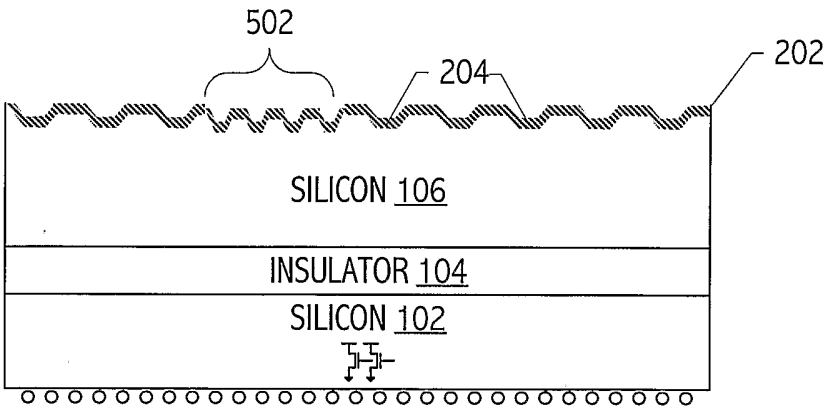


FIG. 5A

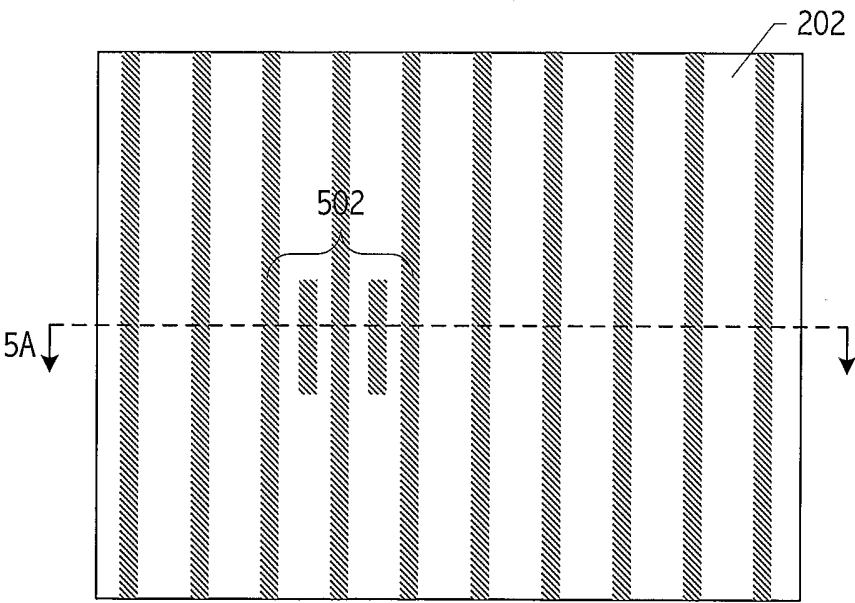


FIG. 5B

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US2005/015048

A. CLASSIFICATION OF SUBJECT MATTER

H01L23/367 H01L29/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 5 223 747 A (TSCHULENA ET AL) 29 June 1993 (1993-06-29) abstract; figure 3a column 6, line 54 - column 8, line 33	1-10
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Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

11 January 2006

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26/01/2006

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INTERNATIONAL SEARCH REPORT

International Application No

TCT/US2005/015048

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