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Packaged semiconductor product and method for manufacture thereof

5 FIELD OF THE INVENTION

The invention relates to a packaged semiconductor product including a semiconductor device having a substrate comprising a first material, and a packaging structure comprising a second material and having an inner surface, the

10 semiconductor device having a first main surface, a second main surface opposite to the first main surface and side surfaces that extend from the second main surface to the first main surface, the first main surface comprising contact pads of the semiconductor device, wherein the packaging structure supports the semiconductor device.

15 The invention also relates to an electric product including a packaged semiconductor product according to the invention.

The invention further relates to a method of manufacturing a packaged semiconductor product that includes a semiconductor device having a substrate comprising a first material, and includes a packaging structure for the semiconductor
20 device comprising a second material.

Packaged semiconductor products, as described above, are available in many different types, such as for example a ball grid array type and a flip-chip type. A packaged semiconductor product can be susceptible to mechanical damage, in particular at an interface between the semiconductor device and the packaging
25 structure. The mechanical damage can result from, possibly repeated, thermo-mechanically induced stress at or adjacent to the interface. The thermo-mechanically induced stress in itself can lead to damage, but existing thermo-mechanically induced stress can also promote damage as a result of mechanical loading, such as accidental dropping of the packaged semiconductor product during use of an electric product that
30 includes the packaged semiconductor product. The susceptibility to damage decreases reliability of the packaged semiconductor product, which can lead to a lower yield in production, increased productions costs and even to unreliable products.

It is an object of the invention to provide a semiconductor device with improved reliability.

Accordingly, the invention provides a packaged semiconductor product including a semiconductor device having a substrate comprising a first material, and a
5 packaging structure comprising a second material and having an inner surface, the semiconductor device having a first main surface, a second main surface opposite to the first main surface and side surfaces that extend from the second main surface to the first main surface, the first main surface comprising contact pads of the semiconductor device, wherein the packaging structure supports the semiconductor
10 device via the second main surface and/or the side surfaces, wherein the packaged semiconductor product includes a thermo-mechanical-stress distribution layer that comprises a third material, and wherein the thermo-mechanical-stress distribution layer provides a mechanical connection between the inner surface of the packaging structure and at least a substantial part of the second main surface and/or at least a
15 substantial part of the side surfaces of the semiconductor device, and enables the inner surface of the packaging structure to substantially displace relative to the semiconductor device. Such a thermo-mechanical-stress distribution layer significantly influences a stress distribution. By enabling the inner surface of the packaging structure to substantially displace relative to the semiconductor device, the
20 thermo-mechanical-stress distribution layer reduces build-up of excessive thermo-mechanical stress in a region of the packaged semiconductor product at or adjacent to the semiconductor device and the packaging material. This makes the packaged semiconductor product more robust with respect to damage, such as fracturing, along a surface of the semiconductor device or along the inner surface of the packaging
25 structure. Such damage may result from, possibly repeated, thermo-mechanical stress as a result of temperature variations of the packaged semiconductor product.

The thermo-mechanical-stress distribution layer enables the inner surface of the packaging structure to substantially displace relative to the semiconductor device. A displacement caused by a significant temperature variation
30 of the packaged semiconductor product is considered a substantial displacement. Such a significant temperature variation can be uniform over the packaged semiconductor product, and can be at least 50 kelvin, 100 kelvin and/or 150 kelvin. A displacement causing a maximum longitudinal strain in the thermo-mechanical-stress distribution layer of at least 0.2%, 0.5%, 1%, 2%, 5%, 10%, 25%, or 50%, as a result of the

significant temperature variation or by another cause, is also considered a substantial displacement. It may be clear that in general the first, second, and third material are distinct from each other.

Preferably, the thermo-mechanical stress distribution layer enables the
5 inner surface of the packaging structure to substantially displace relative to the semiconductor device without being mechanically disconnected from the semiconductor device. The packaging structure is mechanically disconnected from the semiconductor device for example when damage, such as a fracture, is present between the packaging structure and the semiconductor device, for example at an
10 interface of the inner surface of the packaging structure and the semiconductor device, at an interface of the thermo-mechanical-stress distribution layer and one of the packaging structure and the semiconductor device, or inside or adjacent to the thermo-mechanical-stress distribution layer.

The thermo-mechanical-stress distribution layer provides a mechanical
15 connection between the inner surface of the packaging structure and at least a substantial part of the second main surface and/or at least a substantial part of the side surfaces of the semiconductor device. This means that the thermo-mechanical-stress distribution layer provides a mechanical connection between the inner surface of the packaging structure and at least 20% of the second main surface and/or at least 20%
20 of the side surfaces of the semiconductor device. The thermo-mechanical-stress distribution layer providing a mechanical connection between the inner surface of the packaging structure and at least 80% of the second main surface and/or at least 80% of the side surfaces of the semiconductor device, further increases the robustness of the packaged semiconductor product.

25 In an embodiment, the packaged semiconductor product includes a redistribution layer being provided with inner contact elements and outer contact elements, wherein the redistribution layer covers the first main surface with the inner contact elements in electrical connection with the contact pads of the semiconductor device. The redistribution layer reroutes the contact pads of the semiconductor device.
30 As a result, a space available for mounting connections of the semiconductor device, such as solder bumps of a flip-chip semiconductor device, with for example a printed circuit board is increased. The redistribution layer may be necessary as a result of the ongoing miniaturisation of integrated circuits of semiconductor devices, which leads to an increasingly smaller silicon surface necessary for the integrated circuit. The

silicon surface can become so small that a space necessary for mounting the connections of the chip, is lacking. The redistribution layer may allow for larger bending out of the plane of the first and second main surface than the substrate does. However, thermo-mechanical damage can occur at or adjacent to the redistribution layer. In case the redistribution layer reroutes the contact pads to a relatively large area, an increased amount of package material is needed. This can increase thermo-mechanically-induced stress at or adjacent to the interface of the package and the semiconductor device, and/or at or adjacent to the redistribution layer. The thermo-mechanical-stress distribution layer is especially valuable in this embodiment because it reduces this thermo-mechanically-induced stress.

In an embodiment, the thermo-mechanical-stress distribution layer is arranged in between the packaging structure and the substantial part of the second main surface and/or the substantial part of the side surfaces of the semiconductor device. In this way, the thermo-mechanical-stress distribution layer provides a mechanical connection between the inner surface of the packaging structure and at least a substantial part of the second main surface and/or at least a substantial part of the side surfaces of the semiconductor device, and enables the inner surface of the packaging structure to substantially displace relative to the semiconductor device. Preferably, the thermo-mechanical-stress distribution layer at least partly covers the edges of the second main surface and the side surfaces of the semiconductor device, as these can be rather susceptible to damage. Preferably, the thermo-mechanical-stress distribution layer extends along the side surfaces up to the redistribution layer, thus reducing stress in a part of the packaged semiconductor product adjacent to the packaging structure, the redistribution layer, and the semiconductor device, which part can be especially susceptible to failure.

In an embodiment, the contact pads of the semiconductor device are distributed over a first area and the outer contact elements are distributed over a second area that is larger than the first area, wherein the redistribution layer also covers the packaging structure and the packaging structure also supports the redistribution layer. The presence of a thermo-mechanical-stress distribution layer is especially valuable in such a packaged semiconductor product, because of the relatively large size of the packaging structure with respect to the semiconductor device. The redistribution layer can increase the IO-count, that is the number of terminals for input and output, of the semiconductor device.

In an embodiment, a linear coefficient of thermal expansion of the third material is larger than a linear coefficient of thermal expansion of the first material and is smaller than a linear coefficient of thermal expansion of the second material. As a result, a tendency for developing thermally induced deformations gradually changes from the semiconductor device via the thermo-mechanical-stress distribution layer to the packaging structure. In this embodiment of the packaged semiconductor product, the thermo-mechanical-stress distribution layer effectively reduces the thermo-mechanical stress. However, an effective reduction of the thermo-mechanical stress can also be achieved in other embodiments.

In an alternative embodiment, a Young's modulus of the third material is smaller than both a Young's modulus of the first material and a Young's modulus of the second material. As a result, the thermo-mechanical-stress distribution layer can have relatively large deformations without developing excessive stress so that it effectively reduces the thermo-mechanical stress in the packaged semiconductor product. In addition, the alternative embodiment offers the unexpected advantage of an additional improvement in shock absorption of the packaged semiconductor product, in particular when the thermo-mechanical-stress distribution layer includes an anelastic material that dissipates the energy of the shock effectively. In this alternative embodiment, there is no need for restrictions on the linear coefficient of thermal expansion of the third material. Nevertheless, if the linear coefficient of thermal expansion of the third material is larger than the linear coefficient of thermal expansion of the first material and is smaller than the linear coefficient of thermal expansion of the second material, the thermo-mechanical stress in the packaged semiconductor product is even further reduced.

In an embodiment, the Young's modulus of the third material is at least two times and preferably at least five times smaller than the Young's modulus of the second material. A clear improvement in robustness against thermo-mechanical stress is obtained when the Young's modulus of the third material is at least two times smaller than the Young's modulus of the second material. For applications that require a relatively high robustness against shocks, as can for example be found in automotive applications, it is advantageous that the Young's modulus of the third material is at least five times smaller than the Young's modulus of the second material. In particular, the Young's modulus of the thermo-mechanical-stress distribution layer is smaller than 4 gigapascal and preferably is smaller than 1

gigapascal. In this way a significant effect of the thermo-mechanical-stress distribution layer can be achieved for commonly used versions of the first and second materials, being respectively silicon and epoxy.

5 In particular, the ratio of a Young's modulus and a linear coefficient of thermal expansion of the third material is smaller than the ratio of a Young's modulus and a linear coefficient of thermal expansion of the first material and is larger than the ratio of a Young's modulus and a linear coefficient of thermal expansion of the second material.

10 More in particular, the ratio of a Young's modulus and a linear coefficient of thermal expansion of the third material is within a range from 20 gigapascal megakelvin to 40 gigapascal megakelvin.

In an embodiment, a thickness of the thermo-mechanical-stress distribution layer is at least 15 micrometer. Such a lower limit of 15 micrometer promotes a significant effect of the thermo-mechanical-stress distribution layer on
15 reliability of the packaged semiconductor product. In particular, the thickness of the thermo-mechanical-stress distribution layer along at least two of the side surfaces that are transverse to each other, is at least 50 micrometer, for example 100 micrometer. This has the advantage that a pick- and place machine can accurately place the semiconductor device by using a method according to the invention. It also further
20 promotes a significant effect of the thermo-mechanical-stress distribution layer on reliability of the packaged semiconductor product.

In an embodiment, the thickness of the thermo-mechanical-stress distribution layer is smaller than 0.5 millimeter, and preferably smaller than 0.25 millimeter. Limiting the thickness of the thermo-mechanical-stress distribution layer
25 also limits a total size of the packaged semiconductor product.

In an embodiment, the thermo-mechanical-stress distribution layer further comprises a fourth material being distinct from the first, second, and third material, wherein the fourth material is present along the second main surface and the third material is present along the side surfaces.

30 In an embodiment, the second material is a moulding compound such as an epoxy material. Alternatively, the second material is a glass material or a ceramic material. In an embodiment, the third and/or fourth material are formed out of at least one of a semiconductor device coating material, a wafercoat material, a die-attach material, an underfill material, and a glue. Alternatively or additionally, the

third and/or fourth material comprise polyimide. Polyimide has the additional advantage of having a good adhesion with both silicon and epoxy material.

In an embodiment, the semiconductor device consists for at least 90% by weight of the first material, the packaging structure consists for at least 90% by weight of the second material, and/or the thermo-mechanical-stress distribution layer consists for at least 90% by weight of the third material. In particular, the thermo-mechanical-stress distribution layer consists of the third material only.

In an embodiment, the redistribution layer includes a patterned isolating sublayer and metal layer portions that fill openings in the patterned isolating sublayer. Preferably, the patterned isolating sublayer includes a polyimide or epoxy material, and/or the patterned conducting layer includes a metal.

In an embodiment, the redistribution layer comprises a flexible material, which can for example be formed out of a glue. Preferably, the flexible material can withstand a strain up to 60%, more preferably up to 80% and possibly up to 100%. This reduces a probability of damage adjacent to the part of the packaged semiconductor product adjacent to the packaging structure, the redistribution layer, and the semiconductor device. In addition, the flexible material is advantageous for relatively large packaging structures.

The invention also provides an electric product including a packaged semiconductor product according to the invention. Such an electric product can for example be a mobile electric product, such as a mobile phone, a lap top computer, or a car. The packaged semiconductor product according to the invention offers a special advantage for use in mobile electric products, as these have a relatively high risk for experiencing mechanical shocks.

It is another object of the invention to provide an improved method of manufacturing a packaged semiconductor product.

Accordingly, the invention further provides a method of manufacturing a packaged semiconductor product that includes a semiconductor device having a substrate comprising a first material, and includes a packaging structure for the semiconductor device comprising a second material, the method comprising the steps of: a) providing the packaging structure with a cavity that is arranged to receive the semiconductor device; b) applying a precursor of a third material inside the cavity; c) placing the semiconductor device into the cavity against the precursor of the third material, wherein the precursor of the third material is arranged in between the

packaging structure and the semiconductor device; and d) curing the precursor of the third material in order to obtain a thermo-mechanical-stress distribution layer. By manufacturing the packaged semiconductor product in this way, a better robustness of the packaged semiconductor product can be achieved with respect to damage, such as fracturing, along a surface of the semiconductor device or along a surface of the packaging structure. The semiconductor devices are preferably known-good-dies, which are tested and approved before packaging.

In an embodiment, the method includes the step of: e) applying a redistribution layer, having inner contact elements and outer contact elements, with its inner contact elements against contact pads of the semiconductor device in electrical connection with the contact pads of the semiconductor device.

In an embodiment, the thermo-mechanical-stress distribution layer provides a mechanical connection between the cavity and the semiconductor device, and enables the cavity to substantially displace relative to the semiconductor device. Preferably, an inner surface of the packaging structure is formed by a boundary of the cavity.

In an embodiment, the contact pads of the semiconductor device are distributed over a first area and the outer contact elements are distributed over a second area that is larger than the first area, and step e) includes applying the redistribution layer on the packaging structure. Applying a thermo-mechanical-stress distribution layer is especially valuable in such a packaged semiconductor product, because of the relatively large size of the packaging structure with respect to the semiconductor device. The redistribution layer can increase the IO-count of the semiconductor device, for example up to an IO-count in a range from 50 to 2000.

In an embodiment, the method further includes carrying out steps a)-d) and optionally step e) for manufacturing a multitude of packaged semiconductor products, wherein the packaging structures for said packaged semiconductor products are formed by a common packaging wafer that is provided with a multitude of the cavities, including the step of: f) separating the multitude of packaged semiconductor products obtained after step e). This provides an efficient way of manufacturing the multitude of packaged semiconductor products. In addition, warpage of the common packaging wafer can be reduced with respect to a wafer that is manufactured in a known way by moulding packaging material around the semiconductor devices, held in place by a carrier.

In an embodiment, step a) includes embossing the cavity in the packaging structure or moulding the packaging structure around a mould in order to form the cavity.

5 In an embodiment, step b) includes applying the precursor of the third material of the thermo-mechanical-stress distribution layer by using one or more of spray coating, ink jet printing, screen printing, spin coating, and a die-attach process. These processes enable accurate application of the precursor of the third material. The die-attach process may include placing a quantity of the precursor of the third material in the cavity by using a dispensing machine.

10 In an embodiment, step c) may include aligning the semiconductor device to the cavity, preferably by using a pick-and-place machine.

In an embodiment, the packaging structure is made out of a moulding material, and in particular consists of one and the same moulding material.

15 In an embodiment, the semiconductor device includes one of a micro electro mechanical system, such as a pressure sensor or an accelerometer, an integrated circuit, a light emitting diode, and a passive component, such as a diode or a condensator.

BRIEF DESCRIPTION OF THE DRAWINGS

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The invention will now be described, in a non-limiting way, with reference to the accompanying drawings, in which:

Fig. 1 shows a packaged semiconductor product that includes a semiconductor device in a first embodiment according to the invention;

25 Fig. 2 shows a transparent plan view through a redistribution layer of the packaged semiconductor product in a second embodiment according to the invention;

Fig. 3 shows a third embodiment of a packaged semiconductor product according to the invention;

30 Fig. 4 shows a fourth embodiment of a packaged semiconductor product according to the invention;

Fig. 5A shows a way of providing a packaging structure with a cavity;

Fig. 5B shows an embossing stamp pressed in a packaging structure;

Fig. 5C shows application of a heat sink;

Fig. 5D shows a mould and moulded material of a packaging structure;

Fig. 5E shows a packaging structure provided with cavities.

Fig. 6 shows application of a precursor of a third material of a thermo-mechanical-stress distribution layer inside a cavity;

5 Fig. 7 shows placement of a semiconductor device into a cavity;

Fig. 8 shows a common packaging wafer, provided with cavities filled with semiconductor devices;

Fig. 9A shows a packaging structure, a semiconductor device with contact pads of the semiconductor device, and a thermo-mechanical-stress distribution
10 layer;

Fig. 9B shows a semiconductor device and a packaging structure after depositing part of a first metal layer portion;

Fig. 9C shows a redistribution layer after application of second and third patterned isolating sublayers;

15 Fig. 9D schematically shows a packaged semiconductor product after mounting solder bumps; and

Fig. 10 shows a fifth embodiment of a packaged semiconductor product.

20 Figs. 11A-C show packaged semiconductor products in respectively a sixth, seventh, and eighth embodiment according to the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

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Unless stated otherwise, like components will have the same reference number throughout the drawings.

Fig. 1 shows a packaged semiconductor product 2 that includes a semiconductor device 4 in a first embodiment according to the invention. The
30 semiconductor device 4 has a substrate 5 comprising a first material, in this example silicon. The packaged semiconductor product 2 further includes a packaging structure 6 having an inner surface 7 and comprising a second material, in this example being a moulding compound, for example an epoxy material. The packaging structure 6 can protect the semiconductor device 4 against unwanted types of electrical and

mechanical damage, and against moisture. The semiconductor device 4 has a first main surface 8, a second main surface 10 opposite to the first main surface 8, and side surfaces 12 that extend from the second main surface 10 to the first main surface 8. In this example, these form surfaces of a substantially rectangular box. The first main surface 8 comprises contact pads 16 of the semiconductor device, one of which is shown in Fig. 1. The semiconductor device 4 can include a passivation layer 15 that forms a substantial part of the first main surface 8, but leaves the contact pads 16 at least partially uncovered. The contact pads 16 of the semiconductor device are for example formed by an integrated circuit structure (not shown). The passivation layer 15 may be made out of silicon nitride (Si_3N_4), and may have a thickness in a range from 0.5 micrometer to 1 micrometer. The passivation layer 15 may substantially cover the semiconductor device 4 along the first main surface, and the integrated circuit structure outside the contact pads 16.

The packaged semiconductor product 2 in the first embodiment may further include a redistribution layer 18 that includes a stack of a first patterned isolating sublayer 18A, a second patterned isolating sublayer 18B, and a third patterned isolating sublayer 18C. Alternatively, the redistribution layer 18 can include a stack of another number, for example two, four, five, or more than five, of patterned isolating sublayers. Alternatively, the redistribution layer 18 can include only one patterned isolating sublayer. The first, second, and third patterned isolating sublayer 18A, 18B, 18C are for example made out of polyimide. The redistribution layer 18 is provided with inner contact elements 22 and outer contact elements 26 that are electrically connected with the inner contact elements 22. This electrical connection is established via metal layer portions 28 that are included by the redistribution layer 18. The metal layer portions fill openings in the patterned isolating sublayers 18A, 18B, and 18C.

The redistribution layer 18 may cover the first main surface 8 with the inner contact elements 22 in electrical connection with the contact pads 16 of the semiconductor device. The solder bumps 30 can be mounted on the redistribution layer 18 in electrical contact with the outer contact elements 26. Under-bump metallisation layer portions 32 can be present between the solder bumps 30 and the outer contact elements 26.

The packaged semiconductor product 2 further includes a thermo-mechanical-stress distribution layer 34 that comprises a third material. The thermo-

mechanical-stress distribution layer 34 is arranged in between the packaging structure 6 on the one hand, and the second main surface 10 and the side surfaces 12 of the semiconductor device on the other hand. The thermo-mechanical-stress distribution layer 34 is mechanically connected to the packaging structure 6 and to the semiconductor device 4 and thus provides a mechanical connection between the inner surface 7 of the packaging structure, and the second main surface and the side surfaces of the semiconductor device 4. In this example, the thermo-mechanical-stress distribution layer abuts directly against the semiconductor device 4. In general, it will be appreciated that the thermo-mechanical-stress distribution layer may also abut against a thin layer that is included by the semiconductor device 4, at the second surface 10 and/or the side surfaces 12 of the semiconductor device 4. Such a thin layer may be an adhesion layer with a thickness smaller than 1 micrometer. The third material in the first embodiment can be a polyimide material. Using polyimide has the advantage of an improved adhesion with the packaging structure 6 that may be made out of epoxy, and with the substrate 5 that may be made out of silicon. In this way, the thermo-mechanical-stress distribution layer 34 is strongly mechanically connected to the packaging structure 6 and to the semiconductor device 4. The third material may also be formed by a semiconductor device coating material, a wafercoat material, a die-attach material, or an underfill material. Such materials may include epoxy-like substances, may be soft (low Young's modulus), and/or may have a good adhesion with the silicon substrate 5 and the second material of the packaging structure 6.

The packaging structure 6 supports the semiconductor device 4 via the second main surface 10 and the side surfaces 12. Support of the semiconductor device 4 is established by the mechanical connection between the thermo-mechanical-stress distribution layer 34 and the packaging structure 6 on the one hand, and by the mechanical connection between the thermo-mechanical stress distribution layer 34 and the semiconductor device 4 on the other hand. In the first embodiment, the redistribution layer 18 can cover the packaging structure 6. As a result, the packaging structure 6 supports the redistribution layer 18 via a mechanical connection formed by an interface 36 between the packaging structure 6 and the redistribution layer 18.

In the first embodiment, an area of mechanical contact in which the thermo-mechanical-stress distribution layer 34 is mechanically connected to the semiconductor device 4 extends over the second main surface 10 and the side surfaces 12 of the semiconductor device 4 so as to prevent direct contact between the

semiconductor device 4 and the packaging structure 6. As a result, the thermo-mechanical-stress distribution layer extends along the side surfaces 12 up to the redistribution layer 18, thus reducing stress in a part 38 of the packaged semiconductor product 2 adjacent to the packaging structure 6, the redistribution layer 18, and the semiconductor device 4, which part can be especially susceptible to failure.

Fig. 2 shows a transparent plan view through the redistribution layer 18 of the packaged semiconductor product 2 in a second embodiment according to the invention. Fig. 2 shows the first main surface 8 of the semiconductor device 4. Fig. 2 also shows the contact pads 16 of the semiconductor device 4, which are distributed over a first area 40 whose circumference narrowly encloses the contact pads 16. In the second embodiment, the outer contact elements 26 are distributed over a second area 41 whose circumference narrowly encloses the outer contact elements 26. The second area 41 is larger than the first area 40, which offers an increased space for mounting the solder bumps 30 (Fig. 1) for establishing electrical connections to for example a printed circuit board to which the packaged semiconductor product 2 can be mounted.

In general, the first, second, and third material may be distinct from each other. In addition, a linear coefficient of thermal expansion of the third material can be larger than a linear coefficient of thermal expansion of the first material and can be smaller than a linear coefficient of thermal expansion of the second material. In this way, the build-up of thermal stress as a result of temperature changes of the packaged semiconductor product 2 or as a result of a temperature gradient within the packaged semiconductor product 2, can be diminished. Such thermal stress in particular builds up in a region adjacent to both the semiconductor device 4 and the packaging structure 6. A linear coefficient of thermal expansion may be measured by isolating a part of the first, second, or third material, and measuring elongation of that part as a function of temperature. Alternatively or additionally, the linear coefficient of thermal expansion may be determined by analysing the constituents of the first, second, or third material, and using known values for these constituents.

A Young's modulus of the third material can be smaller than both a Young's modulus of the first material and a Young's modulus of the second material. As a result, the thermo-mechanical-stress distribution layer can have relatively large deformations without developing excessive stress so that it effectively reduces the thermo-mechanical stress in the packaged semiconductor product. A value of the

Young's modulus can be determined for example by carrying out a micro-indentation test or a nano-indentation test on the first, second, or third material. Such testing can be preceded by splitting the packaged semiconductor product 2 to expose the first, second, and/or third material, according to known sample preparation techniques. The

5 Young's modulus can for example be determined during loading or during unloading, near a certain stress level or deformation level. Determining the Young's modulus can be performed in a similar way when comparing the first, second, and/or third material. Such indentation tests are known to the person skilled in the art and a further description is deemed superfluous.

10 The Young's modulus of the third material can be at least two times smaller than the Young's modulus of the second material. This will significantly diminish stress build-up inside and adjacent to the thermo-mechanical-stress distribution layer 34, and offer a clear improvement in robustness against thermo-mechanical stress. For example, the Young's modulus of the first material can be

15 around 150 gigapascal, the Young's modulus of the second material can be around ten gigapascal, and the Young's modulus of the third material can be smaller than four gigapascal, for example around three gigapascal. Alternatively, the Young's modulus of the third material can be at least five times smaller than the Young's modulus of the second material, for example 1 gigapascal. In this way an even more significant

20 effect of the thermo-mechanical-stress distribution layer can be achieved in diminishing stress build-up, relevant for example for applications that require a relatively high robustness against shocks, as can for example be found in automotive applications.

In the first embodiment and the second embodiment, a thickness of the

25 thermo-mechanical-stress distribution layer 34 along the second main surface 10 of the semiconductor device and along the side surfaces 12 of the semiconductor device, for example along at least one of the side surfaces 12 of the semiconductor device, can be at least 15 micrometer. In this way the thermo-mechanical-stress distribution layer 34 significantly reduces the stress in the packaged semiconductor product 2.

30 Additionally, the thickness of the thermo-mechanical-stress distribution layer 34 along the side surfaces 12 of the semiconductor device, for example along at least two of the side surfaces 12 of the semiconductor device that are transverse to each other, can be larger than 50 micrometer, for example 100 micrometer. In this way,

placement of the semiconductor device 4 by a pick-and place machine in a method according to the invention is facilitated.

It is not necessary to combine restrictions on the linear coefficient of thermal expansion, restrictions on the Young's modulus of the third material, and
5 restrictions on the layer thickness of the thermo-mechanical-stress distribution layer, since each of these measures contributes to the robustness of the packaged semiconductor product 2 against thermo-mechanical stress. Nevertheless, such a combination would further reduce the thermo-mechanical stress in the packaged semiconductor product 2 and could be useful in packaged semiconductor products 2
10 that are used in harsh environments where the packaged semiconductor products 2 experience relatively severe mechanical and thermal loading.

In general, the thickness of the thermo-mechanical-stress distribution layer 34 along the second main surface 10 and the side surfaces 12 of the semiconductor device is preferably smaller than 0.25 millimeter. This further
15 diminishes a size of the packaged semiconductor product 2, so that it takes less space in an electric product that includes the packaged semiconductor product 2. Such an electric product is for example a mobile phone or a lap top computer. Increasing the thickness of the thermo-mechanical-stress distribution layer 34 significantly beyond 0.5 millimeter, for example beyond 1 millimeter, does not significantly improve the
20 robustness of the packaged semiconductor product 2 against thermally induced stress anymore, while it results in an increased size of the packaged semiconductor product 2.

In the first embodiment and the second embodiment, a thickness of the thermo-mechanical-stress distribution layer along the second main surface can be
25 substantially smaller than a thickness of the thermo-mechanical-stress distribution layer along the side surfaces. In general, the thickness of the thermo-mechanical-stress distribution layer 34 along the second main surface 10 is for example less than 85% of the thickness of the thermo-mechanical-stress distribution layer 34 along the side surfaces. The thickness of the thermo-mechanical-stress distribution layer 34
30 along the second main surface 10 can for example also be less than 50% or even less than 25% percent of the thickness of the thermo-mechanical-stress distribution layer 34 along one or more of the side surfaces 12. Such limitations of the thickness of the thermo-mechanical-stress distribution layer 34 along the second main surface 10 all

lead to a more compact packaged semiconductor product 2, while still diminishing thermo-mechanical peak stresses.

Fig. 3 shows a third embodiment of the packaged semiconductor product 2 according to the invention. Fig. 3 shows the semiconductor device 4, the packaging structure 6, the redistribution layer 18, the solder bump 30, and the thermo-mechanical-stress distribution layer 34. The thermo-mechanical-stress distribution layer 34 in the third embodiment further comprises a fourth material being distinct from the first, second, and third material, wherein the fourth material is present along the second main surface 10 and the third material is present along the side surfaces 12.

In the third embodiment, the fourth material may comprise a carbon-based resin, and possibly also an epoxy material or a polymer, which materials can be applied as substances of a glue, and the third material may comprises polyimide. Alternatively or additionally, the third material can be formed out of a semiconductor device coating material, a wafercoat material, a die-attach material, an underfill material, or a glue.

The packaged semiconductor product 2 in the third embodiment of Fig. 3 can be provided with a heat sink 42. The heat sink 42 can be made out of metal and comprises for example aluminium and/or silver, and is part of the packaging structure 6. In general, the packaged semiconductor product 2 with the heat sink 42 is especially suited for power applications.

Fig. 4 shows a fourth embodiment of the packaged semiconductor product 2 according to the invention. Fig. 4 shows the semiconductor device 4, the packaging structure 6, the solder bump 30, and the thermo-mechanical-stress distribution layer 34. The inner contact elements 16 of the redistribution layer 18 in the fourth embodiment are formed by a protecting layer 44, which is for example substantially made out of aluminium. Such a protecting layer offers a good shock protection. On the protecting layer the under-bump metallisation layer portion 32 is deposited, for example an electrolessly deposited nickel layer 32. The nickel layer 32 is electrically connected with the solder bump 30 via the metal layer portions 28. The redistribution layer 18 may comprises a flexible material, for example formed out of a glue.

The packaged semiconductor product 2 in the second embodiment, the third embodiment, and the fourth embodiment can have elements of the packaged semiconductor product 2 in the first embodiment.

The packaged semiconductor product 2 can be manufactured by using a method according to the invention, which comprises the step of providing the packaging structure 6 with a cavity that is arranged to receive the semiconductor device 4. This step is illustrated in Figs. 5A through 5E.

5 Fig. 5A shows a way of providing the packaging structure 6 with the cavity that includes embossing the cavity into the packaging structure, illustrated for two cavities. During embossing, an embossing stamp 50 can be forced in the direction of arrows 52 towards the packaging structure 6 and subsequently can be pressed into the packaging structure 6. Material of the packaging structure 6 in this stage is soft
10 and has viscous properties, so that the packaging structure 6 will deform plastically and flow around the stamp 50.

Fig. 5B shows the embossing stamp 50 pressed in the packaging structure 6. The embossing stamp 50 can be forced to substantially push away all of the material of the packaging structure 6 below the projections 54 of the embossing
15 stamp 50. Before or after removal of the embossing stamp 50 from the packaging structure 6, the material of the packaging structure can be cured, for example by heating the packaging structure in an oven.

Fig. 5C shows application of the heat sink 42, after curing of the packaging structure 6 and removal of the stamp 50. The heat sink 42 can be glued
20 against the packaging structure 6 in order to form the cavities 56. Instead of substantially removing all of the material of the packaging structure 6 below the projections 54 of the embossing stamp 50 during embossing as indicated in Figs. 5A and 5B, the projections 54 may also be pressed into the packaging structure 6 to a maximum depth that is less than 90% of a thickness D of the packaging structure 6. In
25 this case applying the heat sink 42 for forming the cavities 56 may be omitted.

An alternative way of providing the packaging structure 6 with the cavity 56 includes moulding the packaging structure around a mould in order to form the cavity 56. Fig. 5D shows the mould 57 and the moulded material of the packaging structure 6. The mould 57 can be provided with a thin release layer, in order to
30 facilitate removal of the stamp after moulding and curing. Curing of the material of the packaging structure 6 and removal of the mould yields the packaging structure 6 provided with the cavities 56, as shown in Fig. 5E.

The method can further include applying the thermo-mechanical-stress distribution layer inside the cavity. This can include applying of a precursor 59 of the

third material of the thermo-mechanical-stress distribution layer 34 inside the cavity 56, as shown in Fig. 6. This can be achieved by for example spray coating the precursor 59 into the cavities 56. A mask 58 is used in order to shield parts of the packaging structure 6 in order to leave the packaging structure 6 substantially free of the precursor 59 outside the cavities 56. Alternatively or additionally, screen printing or spin coating may be used for applying the precursor of the third material. Alternatively or additionally, a dispensing technique, such as ink jet printing, may be used for applying the precursor 59 in the cavities 56. In this case, the mask 58 may be omitted.

The method further includes placing the semiconductor device 4 into the cavity 56, which is shown in Fig. 7. The semiconductor device can be placed into the cavity 56 by using a pick-and place machine 60. The precursor 59 of the third material can be still viscous when the semiconductor device 4 is placed inside the cavity 56. This has the advantage that a good connection can be achieved between the semiconductor device 4 and the mechanical-stress-distribution layer 34. Vacuum may be used to remove possible air inclusions in the viscous precursor 59. Afterwards, the precursor 59 can be cured, for example by drying and/or heating, for example in an oven or on a hot plate. After curing, the thermo-mechanical-stress distribution layer 34 is obtained, which is arranged in between the packaging structure 6 and the semiconductor device 4.

The method can be carried out for manufacturing a multitude of packaged semiconductor products. In this case, the packaging structures 6 for said packaged semiconductor products can be formed by a common packaging wafer that is provided with a multitude of the cavities 56. Fig. 8 shows the common packaging wafer 62, provided with the multitude of cavities 56 filled with the semiconductor devices 4. The method can include separating the multitude of packaged semiconductor products 2 by sawing the common packaging wafer along lines 64 and 66 that are transverse to each other.

The method can include applying the redistribution layer 18. Figs. 9A through 9D illustrate a way for applying the redistribution layer 18. Fig. 9A shows the packaging structure 6, the semiconductor device 4 with the contact pads 16 of the semiconductor device, and the thermo-mechanical-stress distribution layer 34. Fig. 9A also shows the first patterned isolating sublayer 18A, which can be applied by spin

coating followed by curing and etching in order to achieve that the contact pads 16 of the semiconductor device are free of the first patterned isolating sublayer 18A.

Fig. 9B shows the semiconductor device 4 and the packaging structure 6 after depositing part of the first metal layer portions 28, which can be made of copper and can be applied by sputtering followed by photolithographic patterning using a resist layer and etching. Part of the first metal layer portion 28 is applied against the contact pads 16 of the semiconductor device 4.

Fig. 9C shows the redistribution layer 18 after application of the second and third patterned isolating sublayers 18B and 18C, which are applied analogous to applying the first patterned isolating sublayer. In addition, under-bump metallisation layer portions 32 may be deposited on the third patterned isolating sublayer 18C. This can for example be done using electroless nickel deposition.

Fig. 9D schematically shows the packaged semiconductor product 2 after mounting the solder bumps 30. The solder bumps 30 may be mounted on the under-bump metallisation layer portions 32 in electrical contact with the outer contact elements 26. Mounting of the solder bumps 30 can be performed for example by a screen printing process or by a dispensing process of solder paste. Alternatively, the solder bumps can be mounted as solder balls. In that case, a sticky solder flux is applied to the under-bump metallisation portions 6 first, by forcing the sticky solder flux through a mask using a squeegee. Second, the solder balls are forced through a similar mask by means of a similar squeegee and stick to the sticky solder flux. After mounting, the solder bumps 30 or the solder balls can be reflowed in order to improve their mechanical connection to the under-bump metallisation layer portions 32.

Part of the metal layer portions 28 form the inner contact elements 22 of the redistribution layer 18. The redistribution layer 18 may be applied with its inner contact elements 22 against the contact pads 16 of the semiconductor device so that the inner contact elements 22 are electrically connected to the contact pads 16 of the semiconductor device.

A basic embodiment of a method according to the invention comprises the step of providing the packaging structure with the cavity that is arranged to receive the semiconductor device. The basic embodiment of the method also includes applying the precursor of the third material inside the cavity and placing the semiconductor device into the cavity against the precursor of the third material. The precursor of the third material is arranged in between the packaging structure and the

semiconductor device. The basic embodiment of the method also includes curing the precursor of the third material in order to obtain the thermo-mechanical-stress distribution layer arranged in between the packaging structure and the semiconductor device.

5 Fig. 10 shows a fifth, rather basic, embodiment of the packaged semiconductor product 2, which can be manufactured by the basic embodiment of the method according to the invention. Fig. 10 shows the semiconductor device 4, the packaging structure 6, the solder bumps 30, and the thermo-mechanical-stress distribution layer 34. The semiconductor device 4 may include one of a micro electro
10 mechanical system, an integrated circuit, a light emitting diode, and a passive component. The packaged semiconductor product 2 has an improved shock protection, as a result of the presence of the thermo-mechanical-stress distribution layer. In general, the third material can have anelastic properties so that it can absorb energy relatively strongly. The packaged semiconductor product 2 in the fifth
15 embodiment may have elements of the packaged semiconductor product 2 in the first embodiment, the second embodiment, the third embodiment, and/or the fourth embodiment.

 The basic embodiment of the method can be used for manufacturing of packaged semiconductor products 2 in the first embodiment, the second embodiment,
20 the third embodiment, the fourth embodiment, and the fifth embodiment, but also for other packaged semiconductor products.

 Figs. 11A-C show packaged semiconductor products 2 in respectively a sixth, seventh, and eighth embodiment according to the invention. In these embodiments, the packaging structure 6 is formed by a flexible sheet, for example a
25 paper sheet or a plastic sheet, for example the plastic sheet of a smart card. In order to increase flexibility of the semiconductor devices 4 in these embodiments, the semiconductor devices 4 may be substantially thinned, for example by etching away most of the substrate 5 of the semiconductor device 4 in a late or even final step in manufacture of the semiconductor device 4. As a result of the etching, a thickness of
30 the substrate 4 may be at most 20 micrometer or at most 10 micrometer. Alternatively or additionally, more than 80% of the second main surface may be free of the substrate 5 as a result of the etching. Such thin semiconductor devices 4 are susceptible to thermo-mechanically induced deformations out of a plane of the first and second main surface, such as warping. Simply blocking these deformation can

give rise to fracture or delamination inside or adjacent to the semiconductor device 4. In order to prevent such damage, the thermo-mechanical-stress distribution layer 34 is applied. The thermo-mechanical-stress distribution layer allows a certain amount of thermo-mechanically induced deformation of the semiconductor device 4 out of a plane of a the first and second main surface, without developing excessive stress which causes the damage. In addition, it decreases a required degree of flexibility of the semiconductor device 4 because it can absorb a difference in flexure between the flexible sheet 6 and the semiconductor device 4.

The thermo-mechanical-stress distribution layer 34 can take various configurations. In the sixth embodiment (see Fig. 11A), the thermo-mechanical-stress distribution layer 34 extends along a substantial part of the first main surface. This offers increased protection to the semiconductor device 4. In the seventh embodiment (see Fig. 11B), the thermo-mechanical-stress distribution layer extends along a substantial part of the second main surface 10 and the side surfaces 12, while the first main surface 8 is substantially free of the thermo-mechanical-stress distribution layer. Alternatively, the thermo-mechanical-stress distribution layer may extend along a substantial part of the first main surface and the side surfaces 12, while the second main surface 10 is substantially free of the thermo-mechanical-stress distribution layer 34. In the latter variant, the thermo-mechanical-stress distribution layer 34 may offer mechanical protection to the integrated circuit structure. In the eighth embodiment (see Fig. 11C), the thermo-mechanical-stress distribution layer extends along the side surfaces 12 of the semiconductor device 4, while the first and second main surface are substantially free of the thermo-mechanical-stress distribution layer 34. This lowers a minimum thickness of the flexible sheet 6 for forming the packaged semiconductor product 2. The thermo-mechanical-stress distribution layer 34 enables the inner surface 7 of the flexible sheet 6 to substantially displace relative to the semiconductor device 4.

The invention is not limited to any embodiment herein described and, within the purview of the skilled person, modifications are possible which may be considered within the scope of the appended claims. Equally all kinematic inversions are considered inherently disclosed and to be within the scope of the present invention. The use of expressions like: "preferably", "in particular", "more in particular", "basic", etc. is not intended to limit the invention. The indefinite article "a" or "an" does not exclude a plurality. Features which are not specifically or

explicitly described or claimed may be additionally included in the structure according to the present invention without deviating from its scope.

CLAIMS:

1. Packaged semiconductor product including a semiconductor device having a substrate comprising a first material, and a packaging structure comprising a second material and having an inner surface, the semiconductor device having a first main surface, a second main surface opposite to the first main surface and side
5 surfaces that extend from the second main surface to the first main surface, the first main surface comprising contact pads of the semiconductor device, wherein the packaging structure supports the semiconductor device via the second main surface and/or the side surfaces, wherein the packaged semiconductor product includes a thermo-mechanical-stress distribution layer that comprises a third material, and
10 wherein the thermo-mechanical-stress distribution layer provides a mechanical connection between the inner surface of the packaging structure and at least a substantial part of the second main surface and/or at least a substantial part of the side surfaces of the semiconductor device, and enables the inner surface of the packaging structure to substantially displace relative to the semiconductor device.
15
2. Packaged semiconductor product according to claim 1, including a redistribution layer being provided with inner contact elements and outer contact elements, wherein the redistribution layer covers the first main surface with the inner contact elements in electrical connection with the contact pads of the semiconductor
20 device.
3. Packaged semiconductor product according to claim 1 or 2, wherein the thermo-mechanical-stress distribution layer is arranged in between the packaging structure and the substantial part of the second main surface and/or the substantial part
25 of the side surfaces of the semiconductor device.
4. Packaged semiconductor product according to one of claims 1-3, wherein a linear coefficient of thermal expansion of the third material is larger than a

linear coefficient of thermal expansion of the first material and is smaller than a linear coefficient of thermal expansion of the second material.

5. Packaged semiconductor product according to one of claims 1-4,
5 wherein the linear coefficient of thermal expansion of the third material is within a range from $4 \cdot 10^{-6}$ to $8 \cdot 10^{-6}$ per kelvin.

6. Packaged semiconductor product according to one of claims 1-5,
10 wherein a Young's modulus of the third material is smaller than both a Young's modulus of the first material and a Young's modulus of the second material.

7. Packaged semiconductor product according to claim 6, wherein the Young's modulus of the third material is at least two times and preferably at least five times smaller than the Young's modulus of the second material.

15

8. Packaged semiconductor product according to one of claims 1-7, wherein a thickness of the thermo-mechanical-stress distribution layer is at least 15 micrometer and possibly at least 50 micrometer.

20 9. Packaged semiconductor product according to one of claims 1-8, wherein a thickness of the thermo-mechanical-stress distribution layer is smaller than 0.5 millimeter, and preferably smaller than 0.25 millimeter.

10. Packaged semiconductor product according to one of claims 1-9,
25 wherein a thickness of the thermo-mechanical-stress distribution layer along the second main surface is substantially smaller than a thickness of the thermo-mechanical-stress distribution layer along the side surfaces.

11. Packaged semiconductor product according to one of claims 1-10,
30 wherein an area of mechanical contact in which the thermo-mechanical-stress distribution layer is mechanically connected to the semiconductor device extends over the second main surface and the side surfaces of the semiconductor device so as to prevent direct contact between the semiconductor device and the packaging structure.

12. Packaged semiconductor product according to one of claims 1-11,
wherein the thermo-mechanical-stress distribution layer further comprises a fourth
material being distinct from the first, second, and third material, wherein the fourth
5 material is present along the second main surface and the third material is present
along the side surfaces.

13. Packaged semiconductor product according to one of claims 1-12,
wherein the third material comprises polyimide.

10

14. Packaged semiconductor product according to one of claims 1-13,
wherein the contact pads of the semiconductor device are distributed over a first area
and the outer contact elements are distributed over a second area that is larger than the
first area, and wherein the redistribution layer also covers the packaging structure and
15 the packaging structure also supports the redistribution layer.

15. Electric product including a packaged semiconductor product
according to one of claims 1-14.

20 16. Method of manufacturing a packaged semiconductor product that
includes a semiconductor device having a substrate comprising a first material, and
includes a packaging structure for the semiconductor device comprising a second
material, the method comprising the steps of:

- a) providing the packaging structure with a cavity that is arranged to
25 receive the semiconductor device;
- b) applying a precursor of a third material inside the cavity;
- c) placing the semiconductor device into the cavity against the precursor
of the third material, wherein the precursor of the third material is arranged in
between the packaging structure and the semiconductor device; and
- 30 d) curing the precursor of the third material in order to obtain a thermo-
mechanical-stress distribution layer.

17. Method according to claim 16, including the step of:

e) applying a redistribution layer, having inner contact elements and outer

contact elements, with its inner contact elements against contact pads of the semiconductor device in electrical connection with the contact pads of the semiconductor device.

5 18. Method according to claim 17, wherein the contact pads of the semiconductor device are distributed over a first area and the outer contact elements are distributed over a second area that is larger than the first area, and wherein step e) includes applying the redistribution layer on the packaging structure.

10 19. Method according to one of claims 16-18, including carrying out steps a)-d) and optionally step e) for manufacturing a multitude of packaged semiconductor products, wherein the packaging structures for said packaged semiconductor products are formed by a common packaging wafer that is provided with a multitude of the cavities, including the step of:

15 f) separating the multitude of packaged semiconductor products obtained after step e).

20 20. Method according to one of claims 16-19, wherein step a) includes embossing the cavity in the packaging structure and/or moulding the packaging structure around a mould in order to form the cavity.

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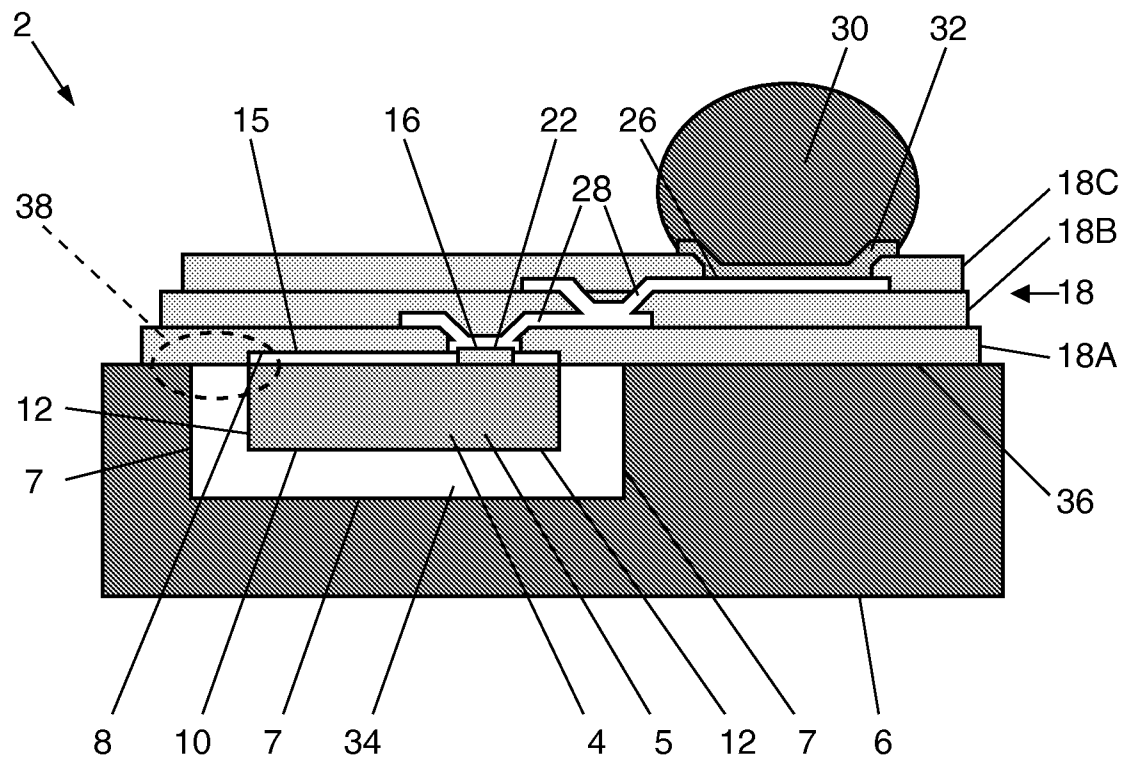


FIG. 1

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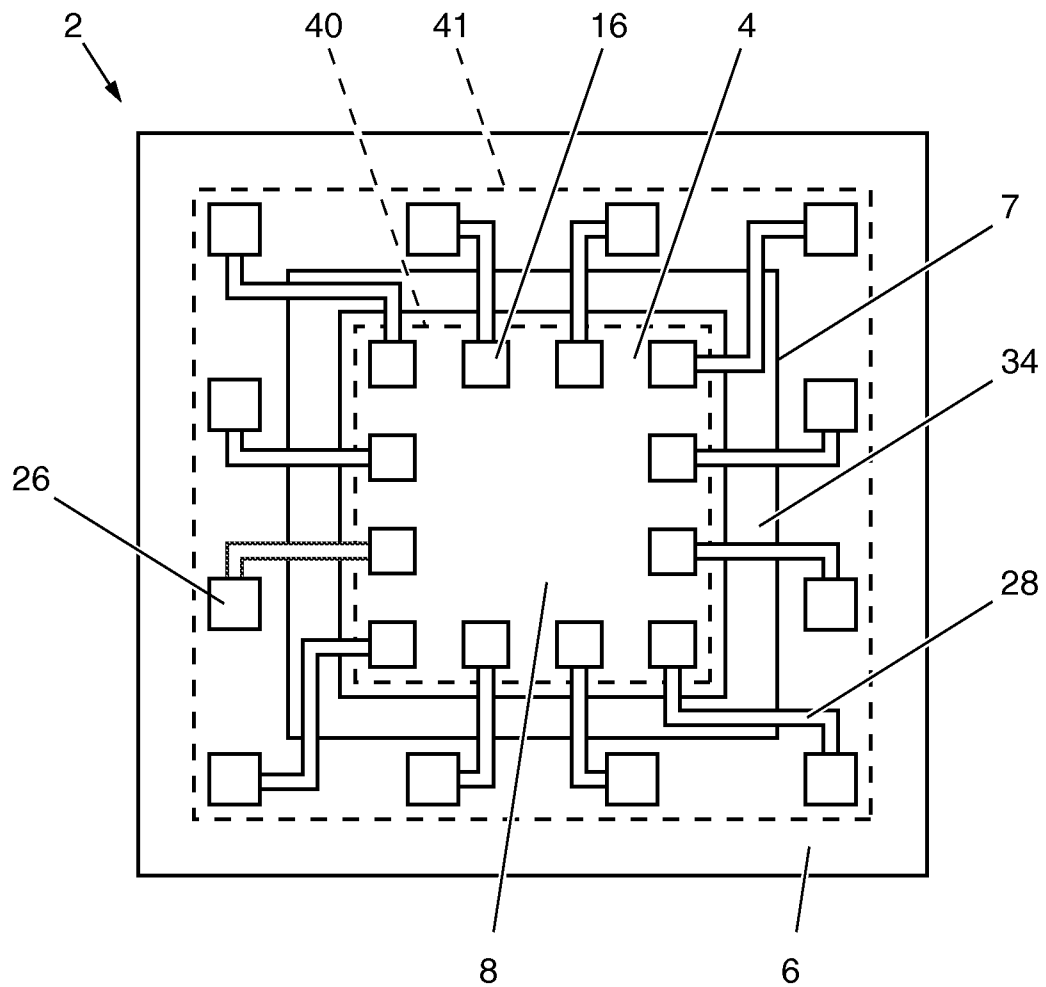


FIG. 2

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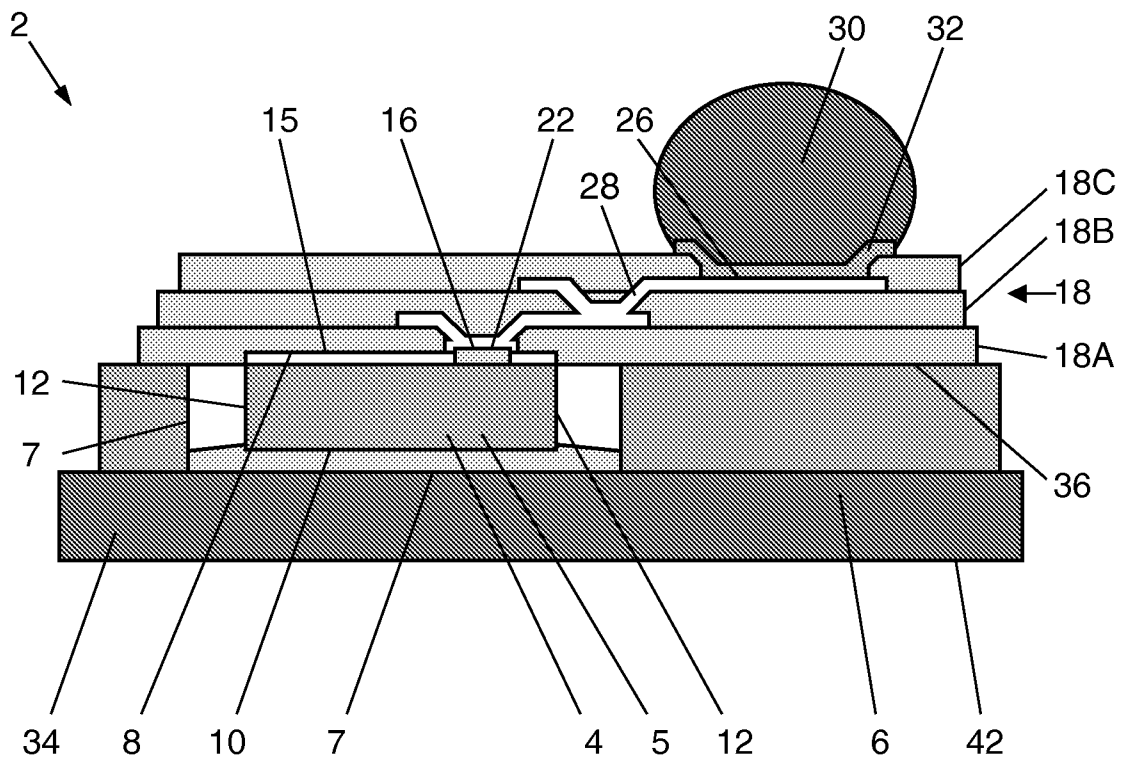


FIG. 3

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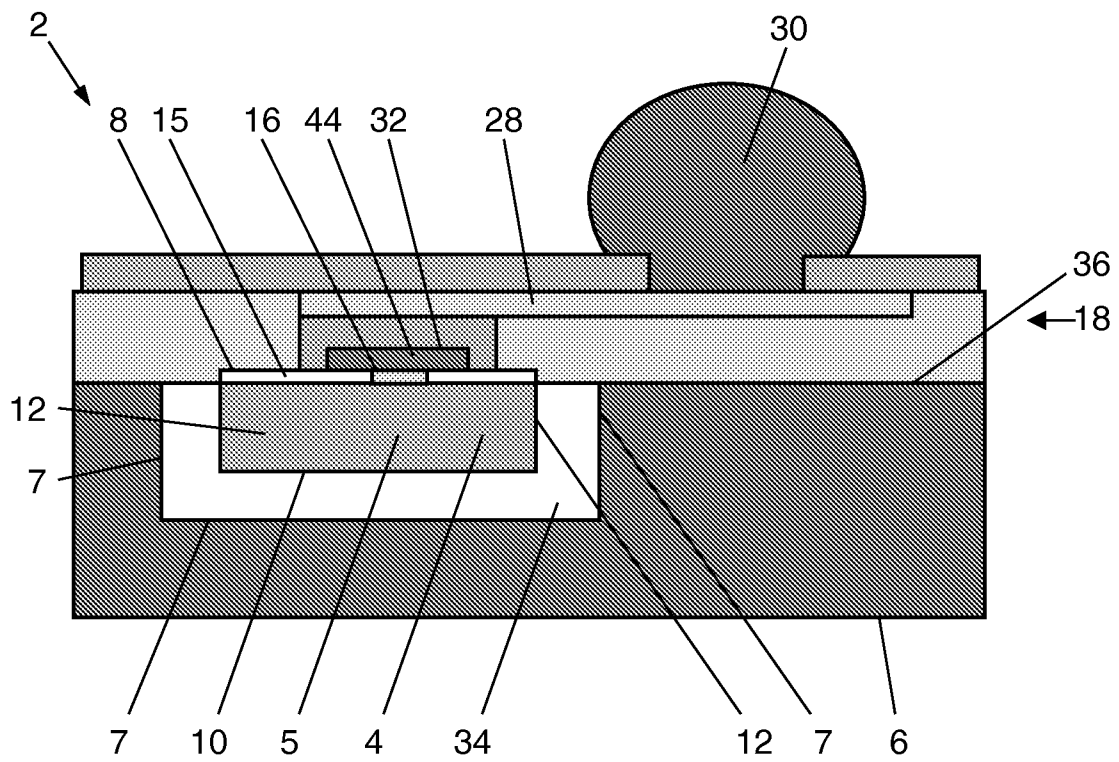


FIG. 4

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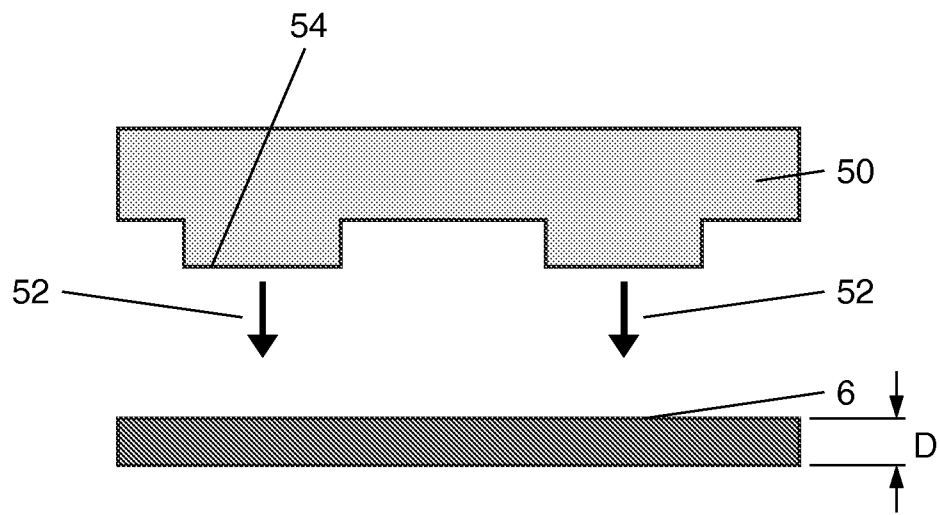


FIG. 5A

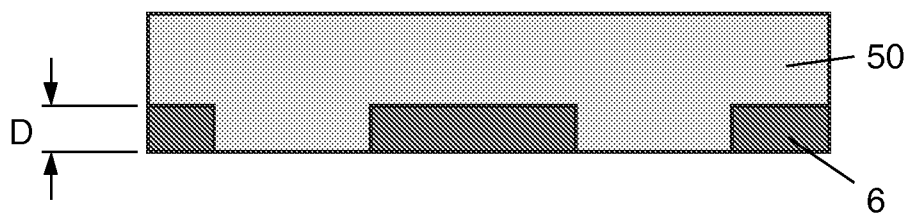


FIG. 5B

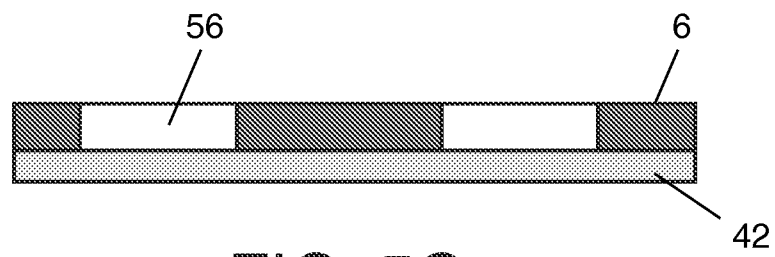
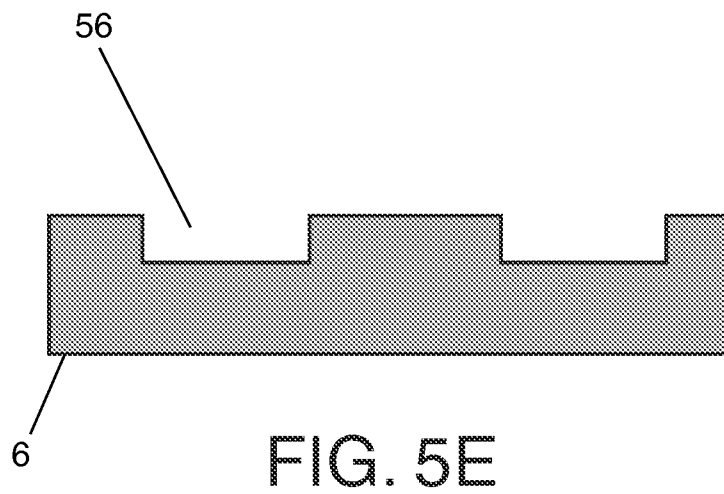
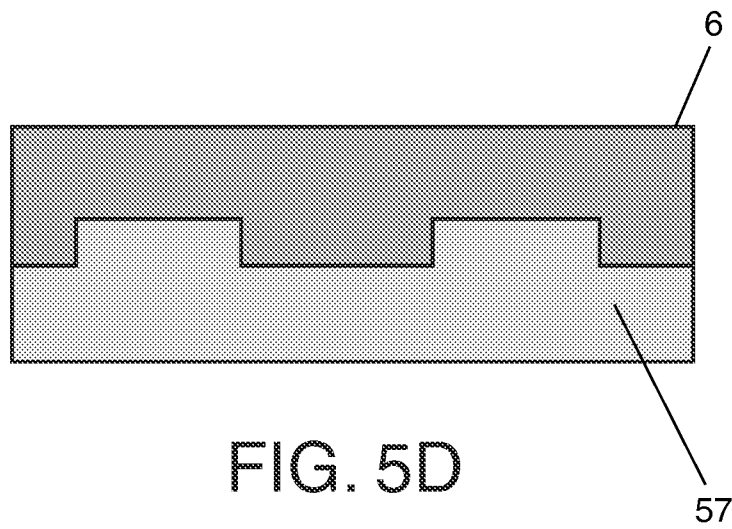


FIG. 5C

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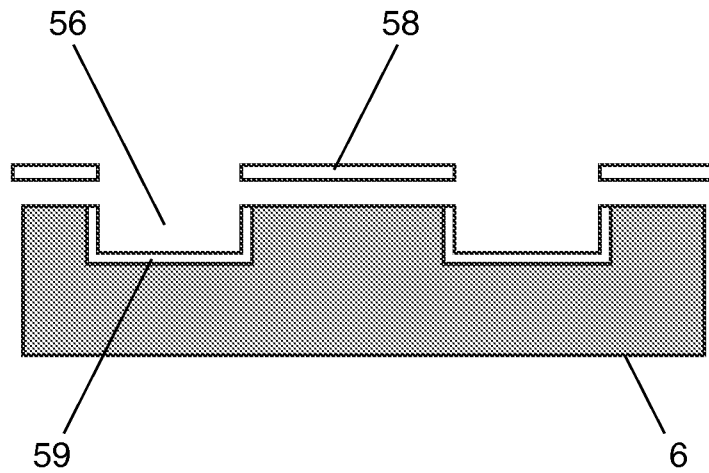


FIG. 6

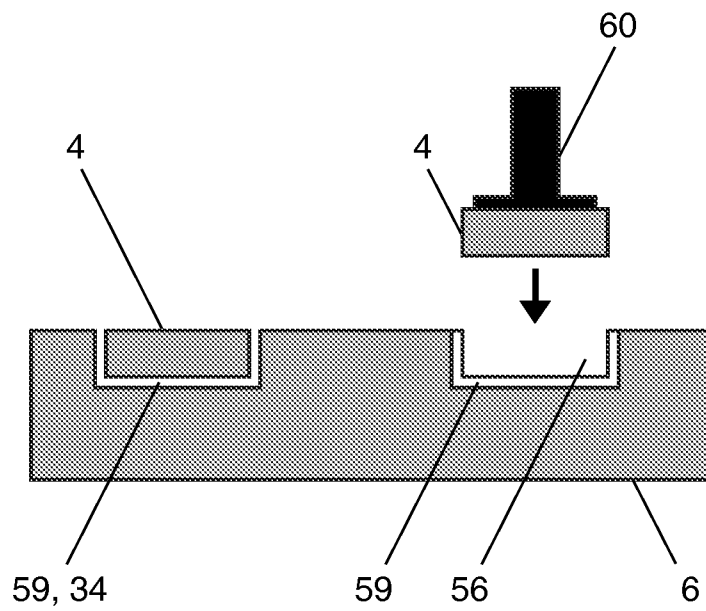


FIG. 7

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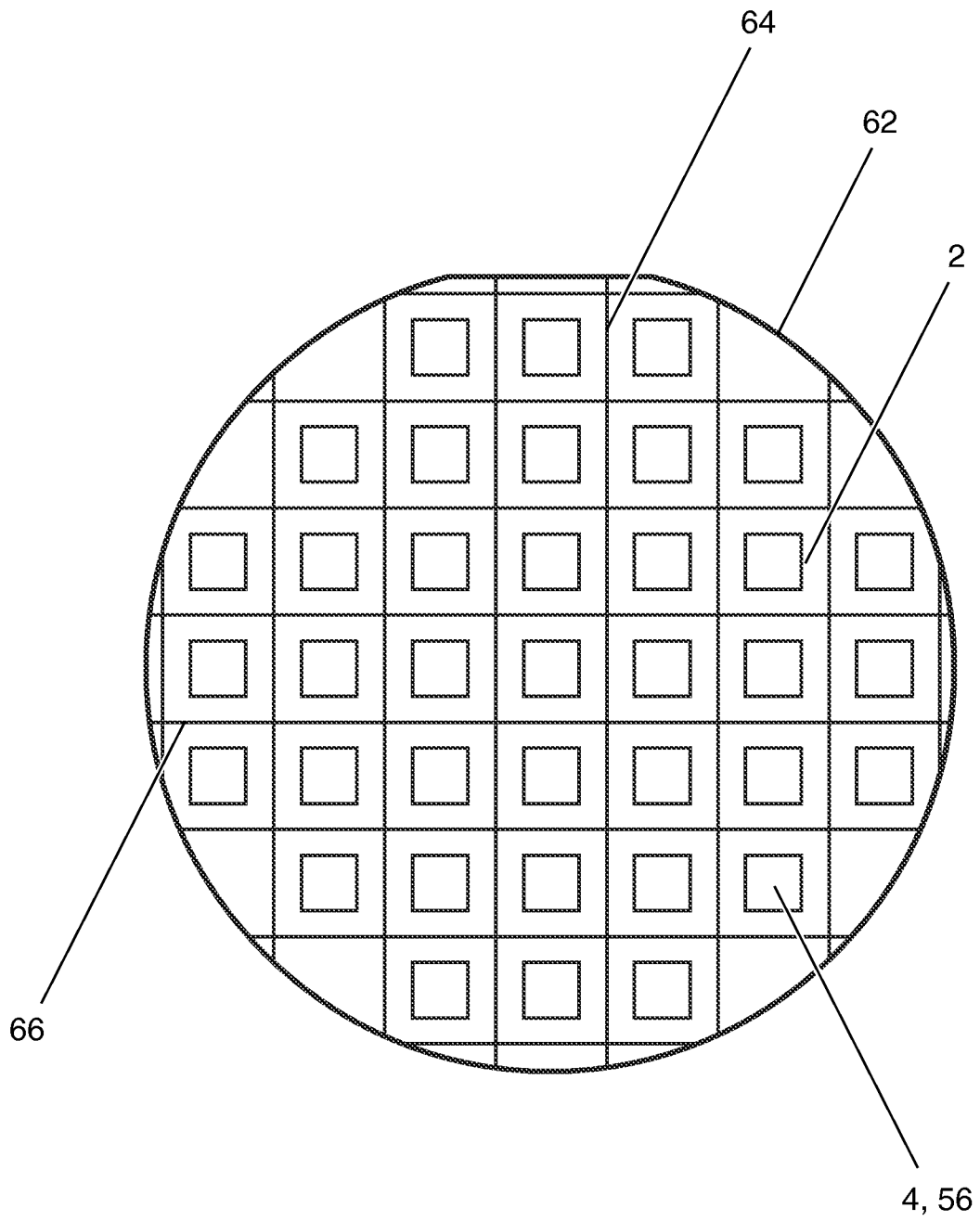


FIG. 8

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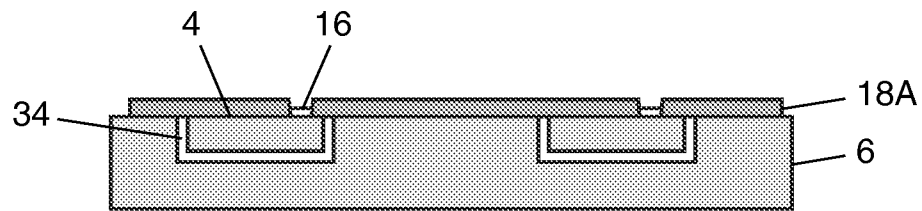


FIG. 9A

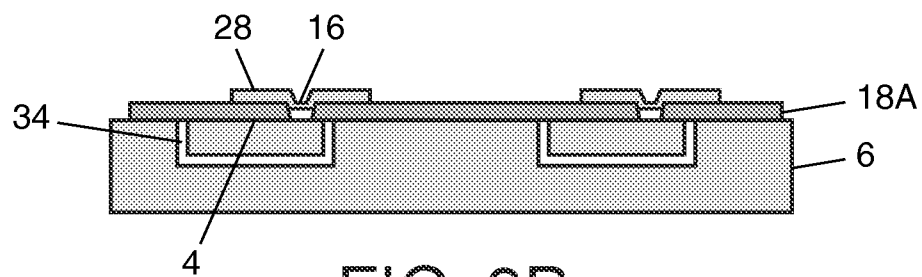


FIG. 9B

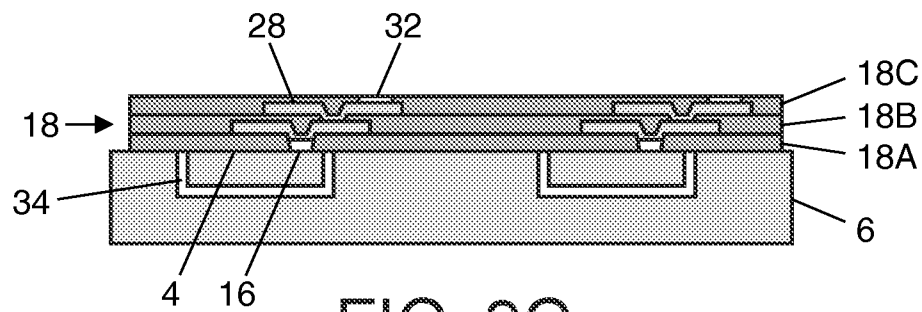


FIG. 9C

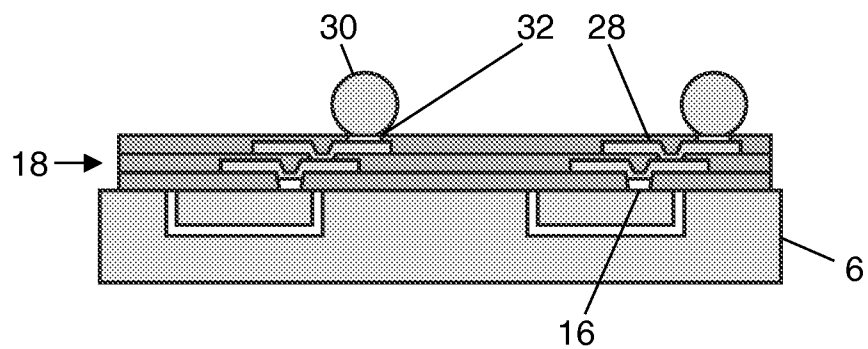


FIG. 9D

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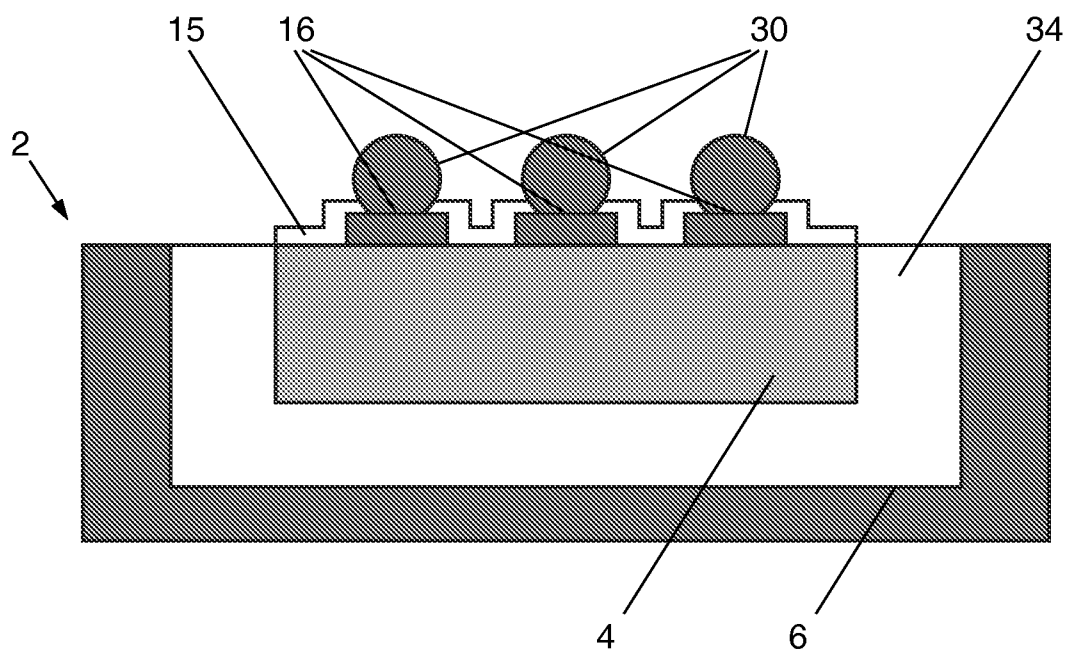


FIG. 10

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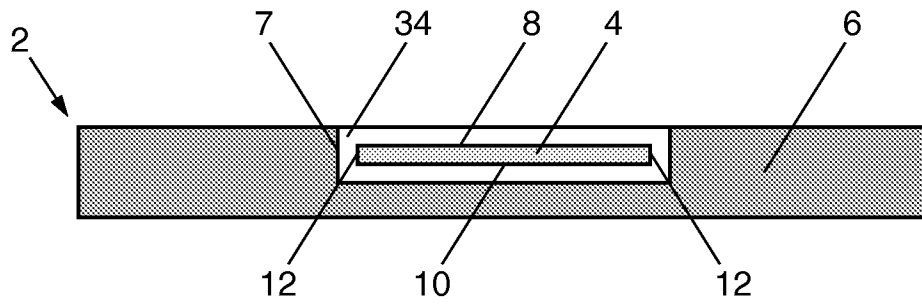


FIG. 11A

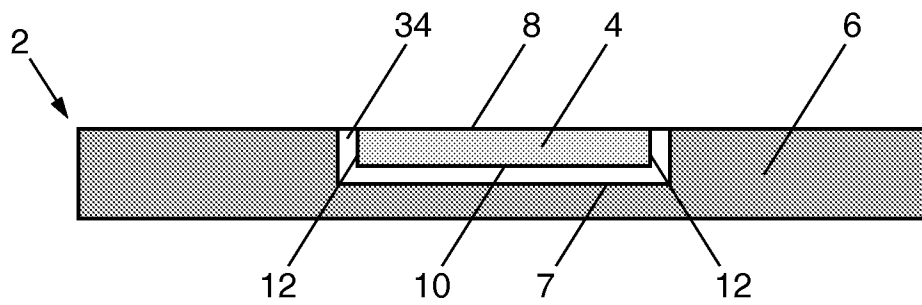


FIG. 11B

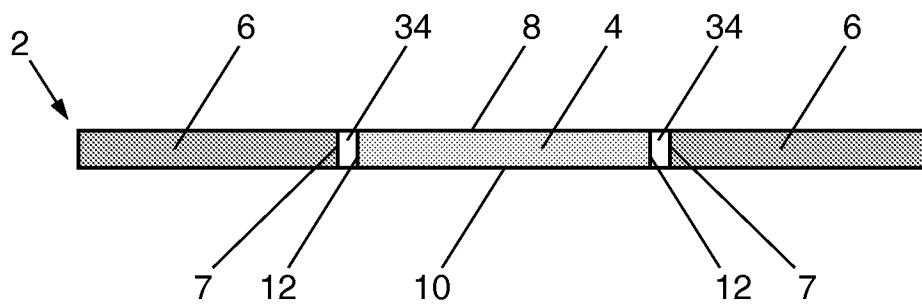


FIG. 11C

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2010/051064

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L23/00 H01L23/525 H01L23/538 H01L21/60
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/152318 A1 (CHIANG CHIA-WEN [TW] ET AL) 5 July 2007 (2007-07-05) figures 2, 3E, 4E	1-20
X	US 2008/142946 A1 (YANG WEN-KUN [TW] ET AL) 19 June 2008 (2008-06-19) figure 6	1-20
X	US 2008/132006 A1 (JIANG TONGBI [US] ET AL) 5 June 2008 (2008-06-05) figure 6	1-20
A	US 2008/237836 A1 (CHIA KAN-JUNG [TW] ET AL) 2 October 2008 (2008-10-02) figure 2D	1-20
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☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

16 June 2010

Date of mailing of the international search report

01/07/2010

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Authorized officer

Kuchenbecker, J

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2010/051064

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/237879 A1 (YANG WEN-KUN [TW]) 2 October 2008 (2008-10-02) figure 5 -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2010/051064

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