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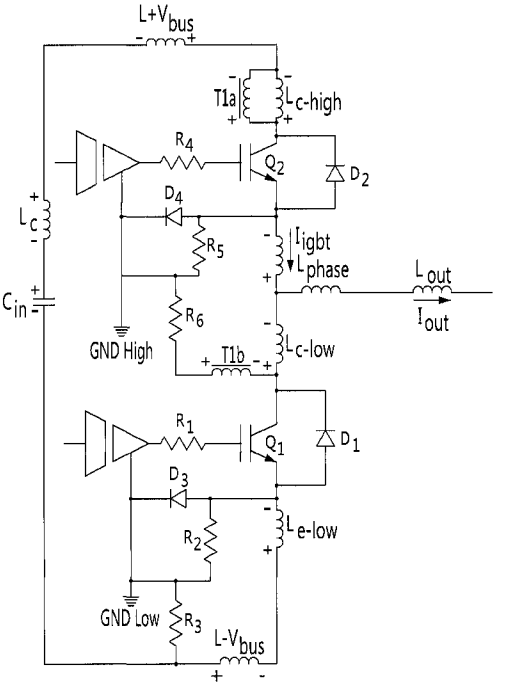


(57) Abrégé/Abstract:
A turn-off overvoltage limiting for IGBT is described herein. The injection of a sample of the overvoltage across the IGBT in the gate drive to slow down the slope of the gate voltage decrease only during the overvoltage above a predetermined value is described herein. Techniques to increase the parasitic inductance to allow the control to limit an overvoltage at turn off of the second IGBT are also described herein.

ABSTRACT

A turn-off overvoltage limiting for IGBT is described herein. The injection of a sample of the overvoltage across the IGBT in the gate drive to slow down the slope of the gate voltage decrease only during the overvoltage above a predetermined value is described herein. Techniques to increase the parasitic inductance to allow the control to limit an overvoltage at turn off of the second IGBT are also described herein.

TITLE

Turn-off overvoltage limiting for IGBT

FIELD

[0001] The present disclosure generally relates to insulated gate bipolar transistors (IGBT). More specifically, the present disclosure is concerned with a configuration and a method to limit the turn-off overvoltage on the IGBTs to thereby improve their overall efficiency.

BACKGROUND

[0002] With the limited space allowed for the power inverter circuits in electric and/or electric hybrid automotive applications and the high cost of the semiconductors, the demand for integration of power electronics increases.

[0003] A known way of reducing the space occupied by the semiconductors in vehicles inverters is to increase their efficiency to allow the size of the cooling surface to be reduced.

[0004] The losses in IGBT modules present in conventional inverter designs are mainly caused by two sources; conduction losses and switching losses. One way to improve IGBT module switching losses is generally by accelerating the IGBT turn-on and turn-off. However, with faster IGBT turn-off, the overvoltage due to the stray inductance of the high-frequency loop increases so much that slow down of the turn-off is often required to protect the device, thereby seriously impacting the efficiency of the inverter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] In the appended drawings:

[0006] Figure 1 is a circuit diagram of a typical gate drive IGBT configuration with the high frequency loop, illustrating the stray inductances and the logical connection where the gate drivers take their reference;

[0007] Figure 2 is a diagram showing the current and voltage waveforms pointing out the overvoltage during short-circuit condition;

[0008] Figure 3 is a circuit diagram of a gate drive IGBT reducing the overvoltage using a resistive divider connected across the emitter stray inductance, according to an illustrative embodiment;

[0009] Figure 4 is a diagram showing the turn-off waveforms of an IGBT using the resistive divider in short circuit condition with a bus voltage of 500V;

[0010] Figure 5 is a diagram showing the turn-off waveforms of an IGBT using the resistive divider adjusted for a maximum bus voltage of 300V in short circuit condition;

[0011] Figure 6 is a circuit diagram of a drive IGBT reducing the overvoltage by using a transformer for the top IGBT according to another illustrative embodiment;

[0012] Figure 7 is a circuit diagram of a drive IGBT reducing the overvoltage by using a transformer and a resistive divider according to another illustrative embodiment;

[0013] Figure 8 is a schematic layout for an IGBT module where the emitted inductance of the top IGBT may be adjusted; and

[0014] Figure 9 is another schematic layout for an IGBT module similar to the one of Figure 8.

DETAILED DESCRIPTION

[0015] According to an illustrative aspect, there is provided a DC to AC power converter including first and second IGBTs each provided with a gate, a collector and an emitter, the gate of the each IGBT is connected to a gate driver including a reference; the gate driver reference of the first IGBT being connected to a ground bus of the power converter while the gate driver reference or the second IGBT being connected to the collector of the first IGBT; the parasitic inductance of the emitter of the second IGBT being increased to allow the control to limit an overvoltage at turn off of the second IGBT.

[0016] In accordance to another illustrative aspect, there is provided a DC to AC power converter including a first IGBT provided with a collector, an emitter, a gate and a gate driver including a reference and a second IGBT provided with a collector, an emitter, a gate and a gate driver including a reference, the power converter including:

first and second resistors connected in series and connected across a parasitic inductance of an emitter of the first IGBT; the gate driver

reference of the first IGBT being connected to the connection point between the first and second resistor;

a transformer having a primary connected across the parasitic inductance of a collector of the second IGBT and a secondary connected to the parasitic inductance of an emitter of the second IGBT, the reference of the gate driver of the second IGBT being connected to the secondary of the transformer.

[0017] According to yet another illustrative aspect, there is provided a DC to AC power converter including a first IGBT provided with a collector, an emitter, a gate and a gate driver including a reference and a second IGBT provided with a collector, an emitter, a gate and a gate driver including a reference, the power converter including:

first and second resistors connected in series and connected across a parasitic inductance of the emitter of the first IGBT; the gate driver reference of the first IGBT being connected to the connection point between the first and second resistor;

a transformer having a primary connected across the parasitic inductance of the collector of the second IGBT and a secondary connected in series with the parasitic inductance of the emitter of the second IGBT, the gate driver reference of the second IGBT being connected to the secondary of the transistor.

[0018] The use of the word "a" or "an" when used in conjunction with the term "comprising" in the claims and/or the specification may mean "one", but it is also consistent with the meaning of "one or more", "at least one", and "one or more than one". Similarly, the word "another" may mean at least a second or more.

[0019] As used in this specification and claim(s), the words "comprising" (and any form of comprising, such as "comprise" and "comprises"), "having" (and any form of having, such as "have" and "has"), "including" (and any form of including, such as "include" and "includes") or "containing" (and any form of containing, such as "contain" and "contains"), are inclusive or open-ended and do not exclude additional, unrecited elements or process steps.

[0020] In the present specification and in the appended claims, various terminology which is directional, geometrical and/or spatial in nature such as "longitudinal", "horizontal", "front", rear", "upwardly", "downwardly", etc. is used. It is to be understood that such terminology is used for ease of description and in a relative sense only and is not to be taken in any way as a limitation upon the scope of the present disclosure.

[0021] Other objects, advantages and features will become more apparent upon reading of the following non-restrictive description of illustrative embodiments thereof, given by way of example only with reference to the accompanying drawings.

[0022] The dI/dt at turn-off of the IGBT generates a voltage across the stray inductance of the high frequency loop that is applied across the IGBT above the bus voltage. Proposed herein is a solution based on the injection of a sample of the overvoltage across the IGBT in the gate drive to slow down the slope of the gate voltage to decrease the overvoltage only during the overvoltage period above a predetermined value.

[0023] Figure 1, which is labeled prior art, discloses a third of a three-phase power converter 10 used, for example, in the powering of a three-phase electric motor (not shown) from a battery (also not shown).

[0024] Since this kind of converter is believed well known it will not be described in details herein. It is however to be noted that the inductances, inherently provided in the wires, connections, decoupling capacitor and circuit board traces, have been represented in Figure 1.

[0025] As can be seen from Figure 1, the reference of each gate driver is connected to the emitter, typically known as the logical pin, of a corresponding IGBT. For concision purpose, we will describe the bottom portion including the IGBT Q_1.

[0026] When the IGBT Q_1 is turned off, the current transit from Q1 to D2, the period of the overvoltage; the IGBT must be able to support the overvoltage created by the dI/dt across the various parasitic inductances (L_c, L_{+bus}, $L_{c\text{-}high}$, $L_{e\text{-}high}$, $L_{c\text{-}low}$ and $L_{e\text{-}low}$) that are present in the circuit. Indeed, since the inductances resist change of current therein, additive voltages develop in the circuit as can be seen by the polarity of the parasitic inductances illustrated in Figure 1. These voltages added to the source voltage often result in a voltage that is often greater than the usual maximal voltage that may safely be present between the collector and the emitter (V_{ce}) of the IGBT.

[0027] Figure 2 illustrates V_{ce}, V_{ge} and the current I at turn-off. One will notice that there is a major overvoltage of V_{ce} above the bus voltage at the time of turn-off.

[0028] Generally stated, by changing the reference of the gate driver from the logical pin of Figure 1 to the ground bus (for the bottom IGBT Q_1) and to the collector of the bottom IGBT (for the top IGBT Q_2), it is possible to decrease this overvoltage of V_{ce} during turn-off.

[0029] In other words, a technique for connecting reference of the gate driver to the power tab of the IGBT instead of to the logical pin has been developed. The voltage across the emitter inductance is injected in the gate driver to create a negative voltage at the emitter of the IGBT to slow down the negative slope of V_{ge}, as will be discussed hereinbelow. The result is a direct action on the gate voltage without any delay and dI/dt limitations.

[0030] Because there is no optimal emitter inductance between the logical and power connections of the emitter in a commercial IGBT module, a technique has been developed to optimize the sample of the overvoltage injected in the gate drive circuit using a resistive divider.

[0031] Figure 3 shows the optimization of the overvoltage with a resistive divider technique and Figure 4 the associated wave shape for a bus voltage as high as 500 Vdc.

[0032] Again, discussing the bottom portion of the three-phase power converter 12 of Figure 3, the IGBT Q_1 includes a collector 14 having a parasitic inductance $L_{c\text{-}low}$, an emitter 16 having a parasitic inductance $L_{e\text{-}low}$ and a gate 18 connected to the gate driver 20 via a resistor R_1. The reference 22 of the gate driver 20 is connected to a resistive divider circuit including two resistors R_2 and R_3 and a diode D_3 that allows the turn-on not to be impacted.

[0033] The values of the resistors R_2 and R_3 are selected according to the level of overvoltage allowed across Q_1. Figure 4 show the result of a resistive divider optimized for an operation at a bus voltage of 500 Vdc and Figure 5 at a bus voltage of 300 Vdc. The ratio of R_2 over R_3 increases to reduce the overvoltage. The value of the two resistor in parallel is set, in series with R_1, as the gate driver resistor. This value of the gate resistor is adjusted according to the proper commutation behavior.

[0034] By setting the resistor values correctly, it is possible to reduce the effect of the emitter inductance to get the maximum overvoltage allowed to therefore improve the efficiency.

[0035] In other words, the normal practice consisting in using a resistor in the ground connection of the gate drive to limit the current in the diodes that protect the gate drive of the lower IGBT from a negative voltage when the upper IGBT turns off has been modified by splitting the resistor in two and adapt the ratio between them to limit the effect of the emitter inductance on the dI/dt. The total resistor remains the same but the voltage divider gives the desired weight of the emitter inductance to limit the overvoltage at the desired level.

[0036] The overvoltage should obviously be optimized as much as possible to reach the maximum IGBT rating; this is done by reducing the resistor connected to the logical emitters R_3 compared to the resistor connected to the power tab R_2. The voltage across the emitter inductance will be split in two and only the voltage across the logical resistor will be applied in the gate drive circuit to limit the gate voltage drop.

[0037] It is to be noted that while the resistors R_2 and R_3 are shown connected across both parasitic inductances $L_{e\text{-}low}$ and $L_{\text{-}Vbus}$, they could be connected solely across parasitic inductance $L_{e\text{-}low}$ should this parasitic inductance be sufficient.

[0038] Figure 4 shows the current I and the voltages V_{ge} and V_{ce} during turn-off for the circuit of Figure 3. One skilled in the art will note that the overvoltage of V_{ce} during turn-off is greatly reduced (see plateau 24). This plateau 24 occurs while the rate of drop of the voltage V_{ge} is reduced by the insertion of the voltage from the parasitic inductance.

[0039] The duration of the plateau will impact greatly the losses during turn-off: the longer the plateau, the higher the losses. Because of the desire to limit at the same time the overvoltage and its length, a square wave shape of the overvoltage plateau is suitable. The intrinsic behavior (natural feedback) of the overvoltage gives this shape.

[0040] Figures 4 and 5 show the square shape of the overvoltage when using the resistive divider at different bus voltages.

[0041] This technique works very well for the bottom IGBT because the emitter inductance is large enough but, for the top IGBT, the emitter inductance is often too small to suitably clamp the voltage without increasing the gate resistor to protect the device. In fact, in practice, the emitter inductance of the top IGBT is very often too low to be used to limit the overvoltage across the top IGBT at the desired level.

[0042] Indeed, because of the constraints on packaging of IGBT modules, the upper and lower semiconductors are packaged within close proximity of each other so the inductance of the upper IGBT, $L_{e\text{-}high}$, is quite small, in the order of a few nH. On the other hand, because the only point of connection other than the logical emitter of the lower IGBT is the power tab of -Vbus, the inductance of the lower IGBT, $L_{e\text{-}low}$, is 5 times the upper emitter inductance $L_{e\text{-}high}$. The connection of the –Vbus tab is highly inductive because of its length and curves.

[0043] In other words, all IGBT modules have two power connections, part of the high-frequency loop, that are the most inductive: +Vbus and –Vbus. Because –Vbus is in the path of the emitter of the bottom IGBT, it can be used to inject a sample of the overvoltage across the IGBT in the gate driver of the bottom IGBT. Unfortunately, since the +Vbus connection is

connected to the collector of the top IGBT, this inductance cannot be used directly as a feedback in the gate driver.

[0044] To use Le-high as a feedback in the gate driver, it is therefore required to somehow increase its inductance without unduly increase the overall inductance of the high frequency loop. Two possible techniques to increase the $L_{e\text{-}high}$ inductance will be described hereinbelow.

[0045] In order to optimize the top IGBT turn-off, a first technique using the collector parasitic inductance to inject a sample of the overvoltage across the top IGBT using a transformer to isolate the collector from the emitter has been designed.

[0046] Figure 6 shows the connections of the transformer. More specifically, the primary of the transformer T1a is connected across the $L_{c\text{-}high}$ parasitic inductance while the secondary of the transformer T1b is connected in series with the resistor R_5.

[0047] Therefore, a negative voltage appears across the transformer when the current decrease in the top IGBT that applies a negative voltage at the emitter to slow down the slope of the gate voltage. In that case, the optimization of the overvoltage is also performed by the turn ratio of the transformer.

[0048] It will be understood that the principle of operation of the circuit of Figure 6 is very similar to the principle of operation of the circuit of Figure 3, however, since the parasitic inductance of the emitter of the top IGBT Q_2 ($L_{e\text{-}high}$) is not enough to properly slow down the negative slope of V_{ce} at

turn-off, a sample of the parasitic inductance of the collector of the top IGBT Q_2 ($L_{c\text{-}high}$) is placed in series with $L_{e\text{-}high}$ through a transformer.

[0049] Figure 7 of the appended drawings is a circuit diagram of an IGBT drive reducing the overvoltage by using a combination of a transformer and a resistive divider according to another illustrative embodiment. Figure 7 illustrates a circuit similar to that of Figure 6. The main difference between these circuits is concerned with a resistive divider including resistors R_5 and R_6 enabling the fine tune of the shape of the negative slope of the V_{ge}.

[0050] A second technique to increase the emitter inductance of the top IGBT Q2 will now be described with reference to Figures 8 and 9, which both illustrates variations of a layout of an IGBT module. These IGBT module layouts are used to make the circuit illustrated in Figure 3 where, as will be explained hereinbelow, the parasitic inductance $L_{e\text{-}high}$ has been adjusted adequately.

[0051] One skilled in the art will understand that increasing the parasitic inductance of the upper IGBT may have an impact on the inductance of the total high frequency loop but its impacts on the control of the overvoltage is much more significant.

[0052] As can be seen from Figure 8, the IGBTs 102 forming the IGBT Q2 have a collector mounted to a trace 104, the trace 104 therefore being referred to as C-High and their emitters are connected to emitter pads 106 via wire bonds 110. Similarly, the IGBT 112 forming the IGBT Q1 have a collector mounted to a trace 114 therefore being referred to as C-Low and their emitters are connected to a trace 118 via wire bonds 120, the trace 118 therefore being referred to as E-Low.

[0053] The trace 114 also has collector pads 116 that are connected thereto.

[0054] The +Vbus tab is connected to trace 104 while the –Vbus tab is connected to trace 118. The phase tab 126 is connected to trace 114.

[0055] It is to be noted that the gates of the IGBTs 102 and 112 are not illustrated in Figure 8 for clarity purpose and since this figures is schematic.

[0056] The pads 106 and 116 are interconnected by a U-shaped connector128 having six (6) legs 130 so configured, sized and positioned as to connect to the pads 106 and 116.One skilled in the art will understand that the U-shaped connector 128 defined the parasitic inductance $L_{e\text{-}high}$ since it interconnects the emitter of Q2 and the collector of Q1. Since the U-shape connector 128 is relatively large and includes right angles, the $L_{e\text{-}high}$ inductance is relatively high and can be used to limit the overvoltage in the IGBT Q2 as discussed hereinabove. It will also be understood that the size and shape of the connector 128 may be determined according to the desired parasitic inductance required.

[0057] Turning now briefly to Figure 9, a similar layout for an IGBT module will be described.

[0058] Generally stated, the main difference between the layout of Figure 8 and the layout of Figure 9 is the position of the tabs 106 which are positioned farther away from the pads 110 to thereby allow a larger connector 132 and therefore a larger parasitic inductance $L_{e\text{-}high}$ to be used.

[0059] It is to be understood that the turn-off overvoltage limiting for IGBT is not limited in its application to the details of construction and parts illustrated in the accompanying drawings and described hereinabove. The turn-off overvoltage limiting for IGBT is capable of other embodiments and of being practiced in various ways. It is also to be understood that the phraseology or terminology used herein is for the purpose of description and not limitation. Hence, although the above description has been done by way of illustrative embodiments thereof, it can be modified, without departing from the spirit, scope and nature of the subject invention.

What is claimed is:

1. A DC to AC power converter including first and second IGBTs each provided with a gate, a collector and an emitter and a transformer having a primary connected across a parasitic inductance of the collector of the second IGBT and a secondary, the gate of the each IGBT is connected to a gate driver including a reference; the gate driver reference of the first IGBT being connected to a ground bus of the power converter while the gate driver reference of the second IGBT being connected to the collector of the first IGBT via the secondary of the transformer; the parasitic inductance of the emitter of the second IGBT being increased by the secondary of the transformer to limit an overvoltage at turn off of the second IGBT.

2. The DC to AC power converter as recited in claim 1, wherein, for each IGBT, the gate driver includes first and second resistors connected in series and connected across a parasitic inductance of the emitter of the corresponding IGBT; the gate driver reference being connected to the connection point between the first and second resistors.

3. The DC to AC power converter as recited in claim 1, wherein the secondary of the transformer is connected in series with the parasitic inductance of the emitter of the second IGBT and the first and second resistors.

4. The DC to AC power converter as recited in claim 1, wherein the parasitic inductance of the emitter of the second IGBT is increased by providing a connector between the emitter of the second IGBT and the collector of the first IGBT, the connector being configured as to provide an increased equivalent parasitic inductance.

5. The DC to AC power converter as recited in claim 4, wherein the emitter of the second IGBT is connected to emitter pad and wherein the collector of the first IGBT is connected to collector pad; the connector being provided between the emitter pad and the collector pad.

6. The DC to AC power converter as recited in claim 5, wherein the emitter pad includes multiple emitter pads and wherein the collector pad includes multiple collector pads.

7. The DC to AC power converter as recited in claim 5, wherein the connector has a U-shaped cross section.

8. The DC to AC power converter as recited in claim 7, wherein the connector includes legs configured to be interconnected with the pads.

9. A DC to AC power converter including a first IGBT provided with a collector, an emitter, a gate and a gate driver including a reference and a second IGBT provided with a collector, an emitter, a gate and a gate driver including a reference, the power converter including:

first and second resistors connected in series and connected across a parasitic inductance of an emitter of the first IGBT; the gate driver reference of the first IGBT being connected to the connection point between the first and second resistor;

a transformer having a primary connected across the parasitic inductance of a collector of the second IGBT and a secondary connected to the parasitic inductance of an emitter of the second IGBT, the reference of the gate driver of the second IGBT being connected to the secondary of the transformer.

10. The DC to AC power converter as recited in claim 9, wherein of the gate driver reference is connected to the secondary of the transformer via a third resistance.

11. A DC to AC power converter including a first IGBT provided with a collector, an emitter, a gate and a gate driver including a reference and a second IGBT provided with a collector, an emitter, a gate and a gate driver including a reference, the power converter including:

first and second resistors connected in series and connected across a parasitic inductance of the emitter of the first IGBT; the gate driver reference of the first IGBT being connected to the connection point between the first and second resistor;

a transformer having a primary connected across the parasitic inductance of the collector of the second IGBT and a secondary connected in series with the parasitic inductance of the emitter of the second IGBT, the gate driver reference of the second IGBT being connected to the secondary of the transformer.

12. The DC to AC power converter as recited in claim 11, wherein the secondary of the transformer is connected in series with both the parasitic inductance of the emitter of the second IGBT and a third and fourth resistors, the gate driver reference of the second IGBT being connected to the connection point between the third and fourth resistors.

13. A DC to AC power converter as recited in claim 12, wherein the secondary of the transformer is connected in series with the parasitic inductance of the emitter of the second IGBT, the parasitic inductance of the collector of the first IGBT and the third and fourth resistors.

14. A DC to AC power converter including a high frequency loop provided with:

bottom and top IGBTs each provided with a gate, a collector and an emitter, the gate of the each IGBT is connected to a gate driver including a reference; the gate driver reference of the bottom IGBT being connected to a ground bus of the power converter while the gate driver reference of the top IGBT being connected to the collector of the bottom IGBT;

a parasitic inductance defined by the interconnection of various elements of the high frequency loop; a parasitic inductance of the emitter of the top IGBT and of the collector of the bottom IGBT being part of the parasitic inductance of the high frequency loop;

wherein a portion of a voltage induced in the parasitic inductance of the high frequency loop is added to a voltage induced in a parasitic inductance of the emitter of

the top IGBT and of the collector of the bottom IGBT by a transformer to slow down a slope of a gate-emitter voltage (Vge) of the top IGBT, the transformer having a primary connected across a parasitic inductance of the high frequency loop and a secondary connected to the gate driver of the top IGBT in series with the parasitic inductance of the emitter of the top IGBT.

15. The DC to AC power converter as recited in claim 14, wherein, for each IGBT, the gate driver includes first and second resistors connected in series and connected across a parasitic inductance of the emitter of the corresponding IGBT; the gate driver reference being connected to the connection point between the first and second resistors.

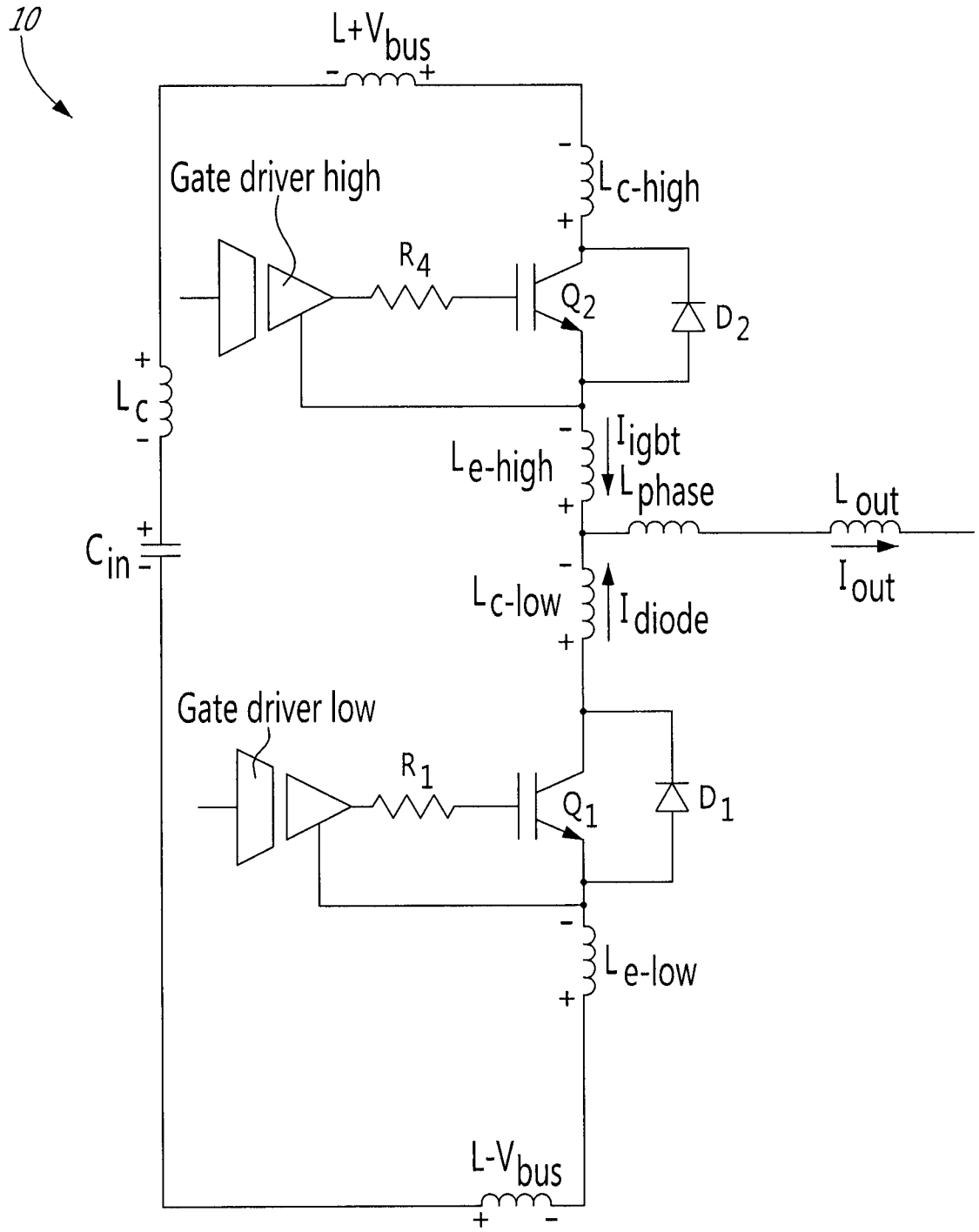


Fig. 1 (PRIOR ART)

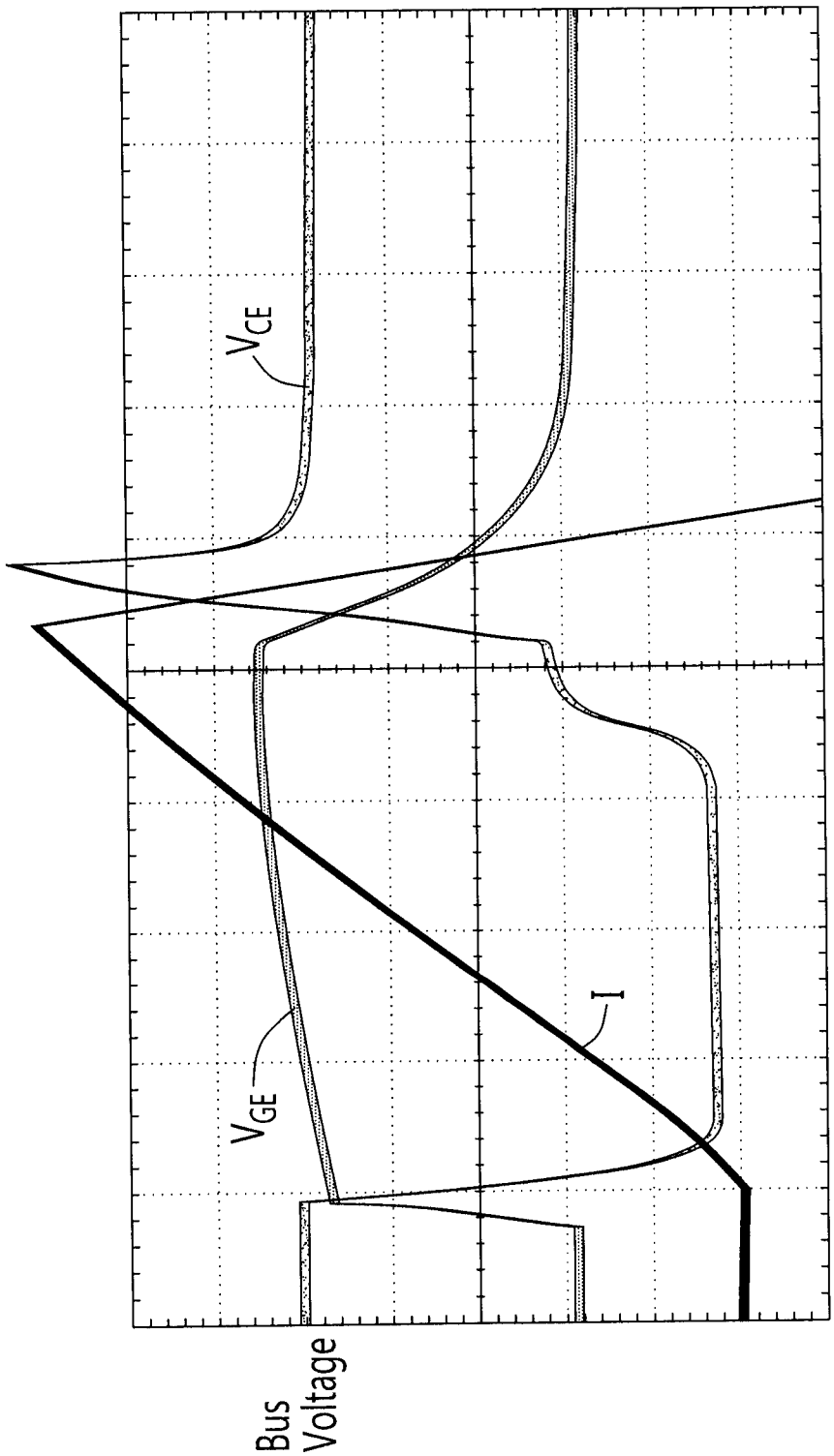
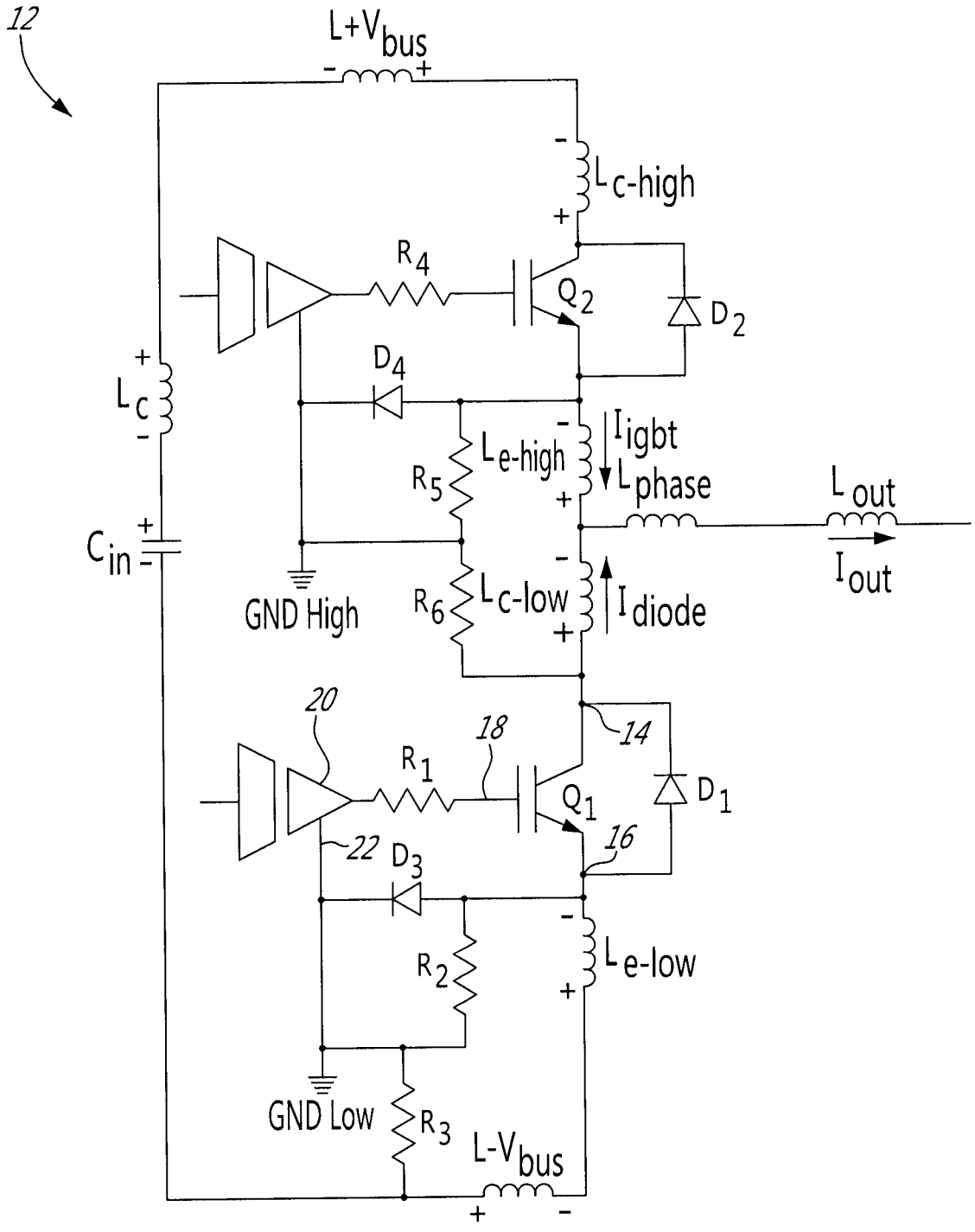


Fig. 2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Lc-high
R4
Q2
D2
D4
Lc
Cin
Le-high
R5
Iigbt
Lphase
Lout
Iout
GND High
R6
Lc-low
Idiode
20
18
14
R1
Q1
D1
22
D3
16
R2
Le-low
GND Low
R3
L-Vbus

Fig 3

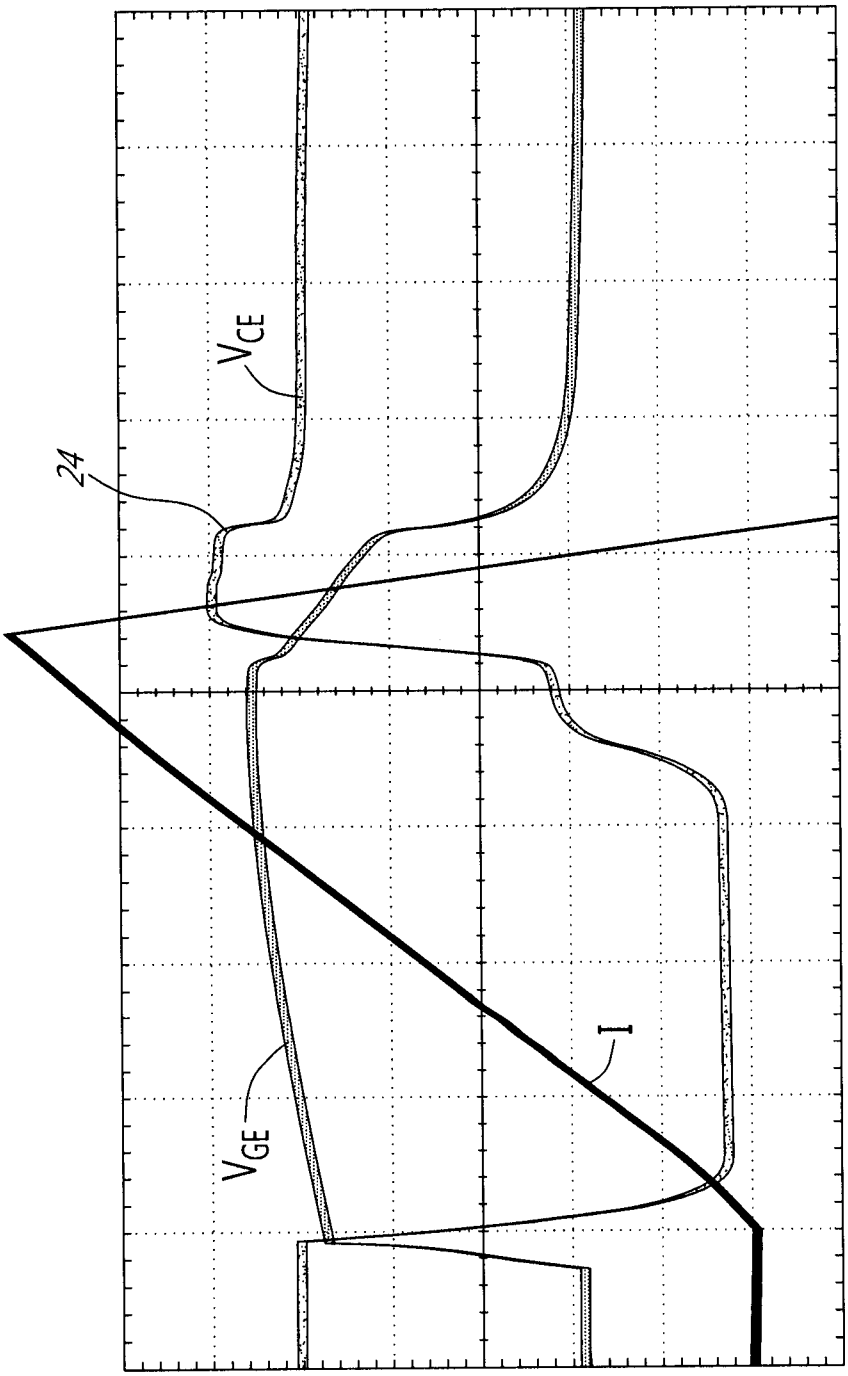


Fig. 4

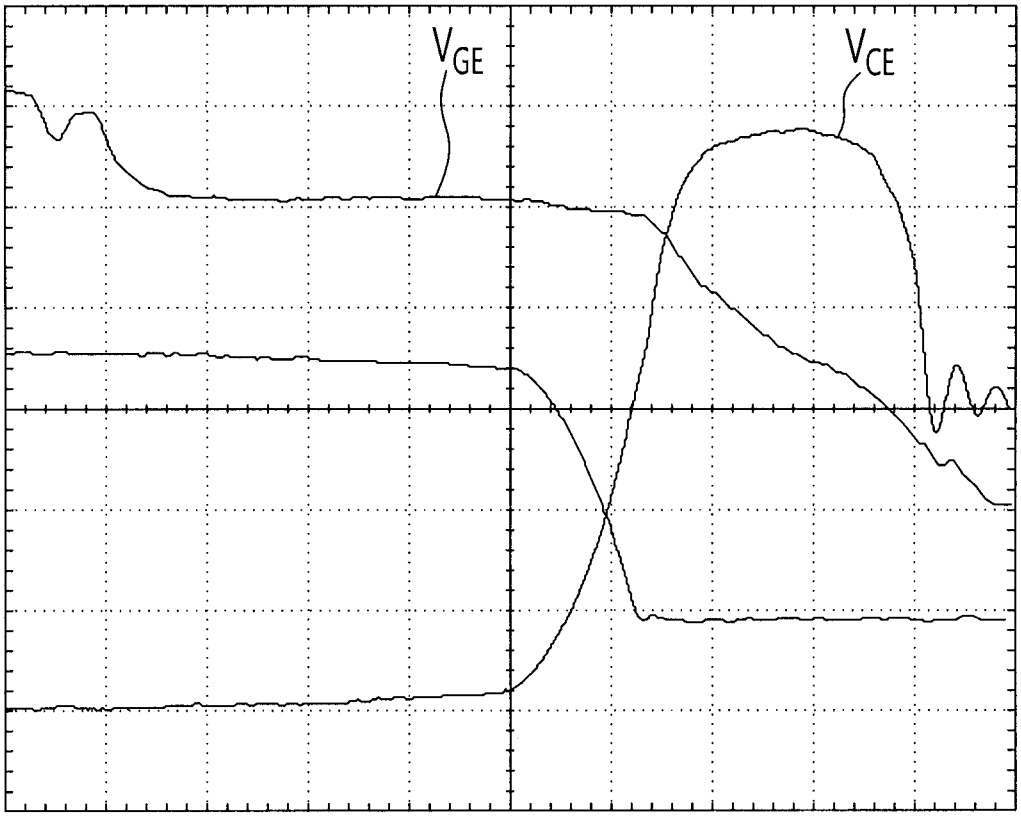
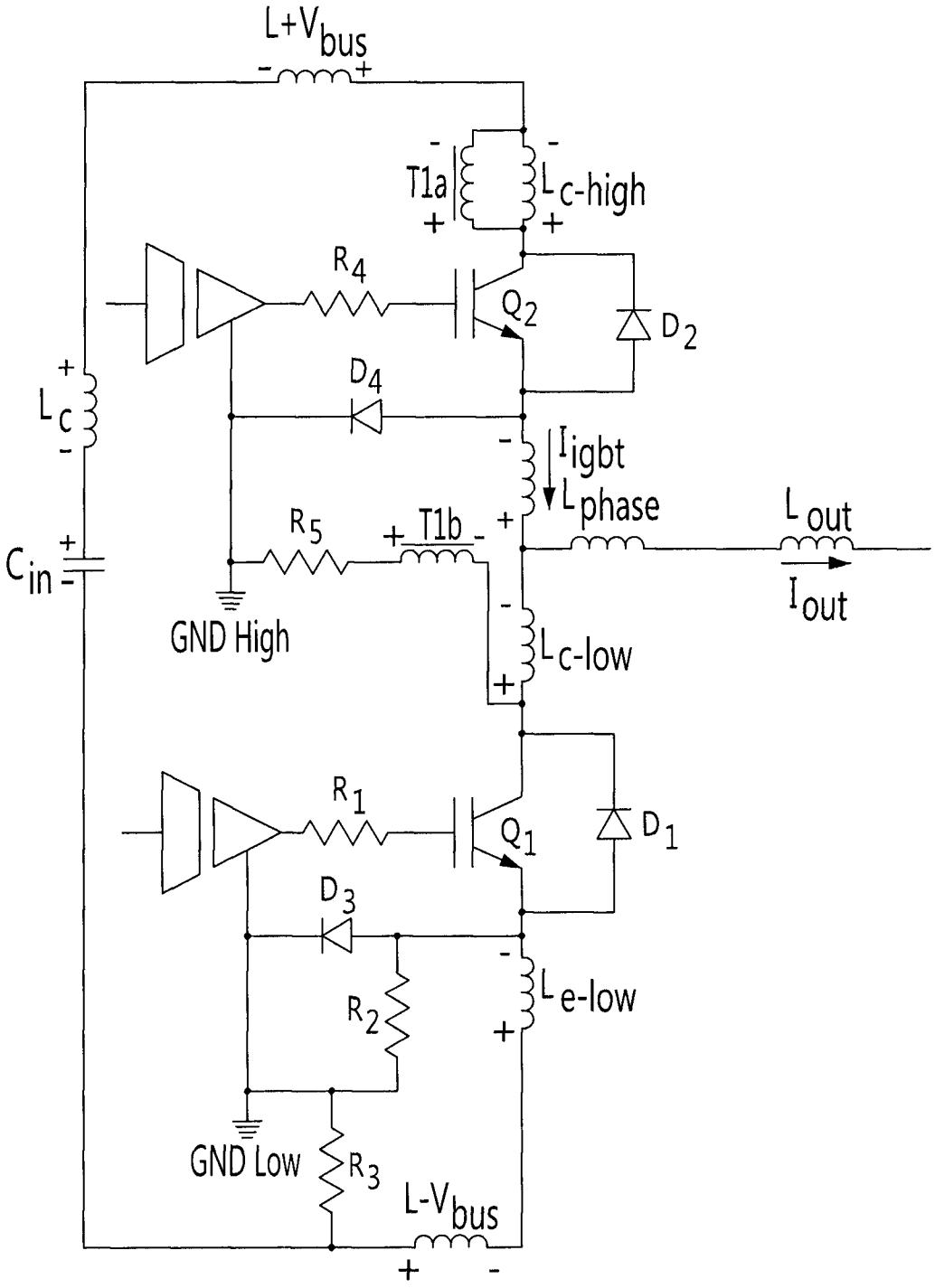


Fig. 5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Q2
D2
D4
Lc
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Lphase
Lout
R5
T1b
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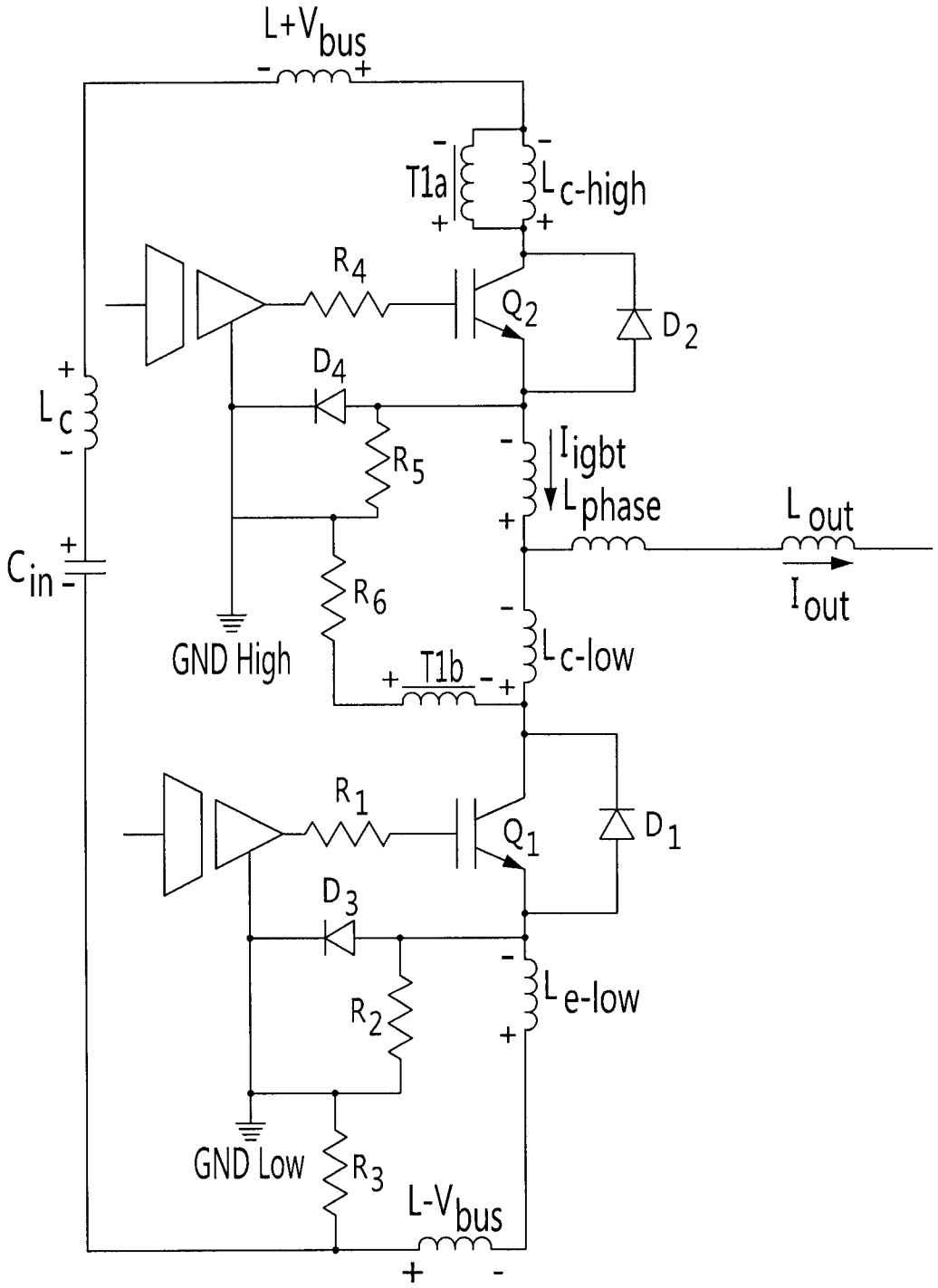
GND Low
R3
L-Vbus

Fig 6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D4
Lc
R5
Iigbt
Lphase
Lout
Iout
Cin
R6
GND High
T1b
Lc-low
R1
Q1
D1
D3
Le-low
R2
GND Low
R3
L-Vbus

Fig. 7

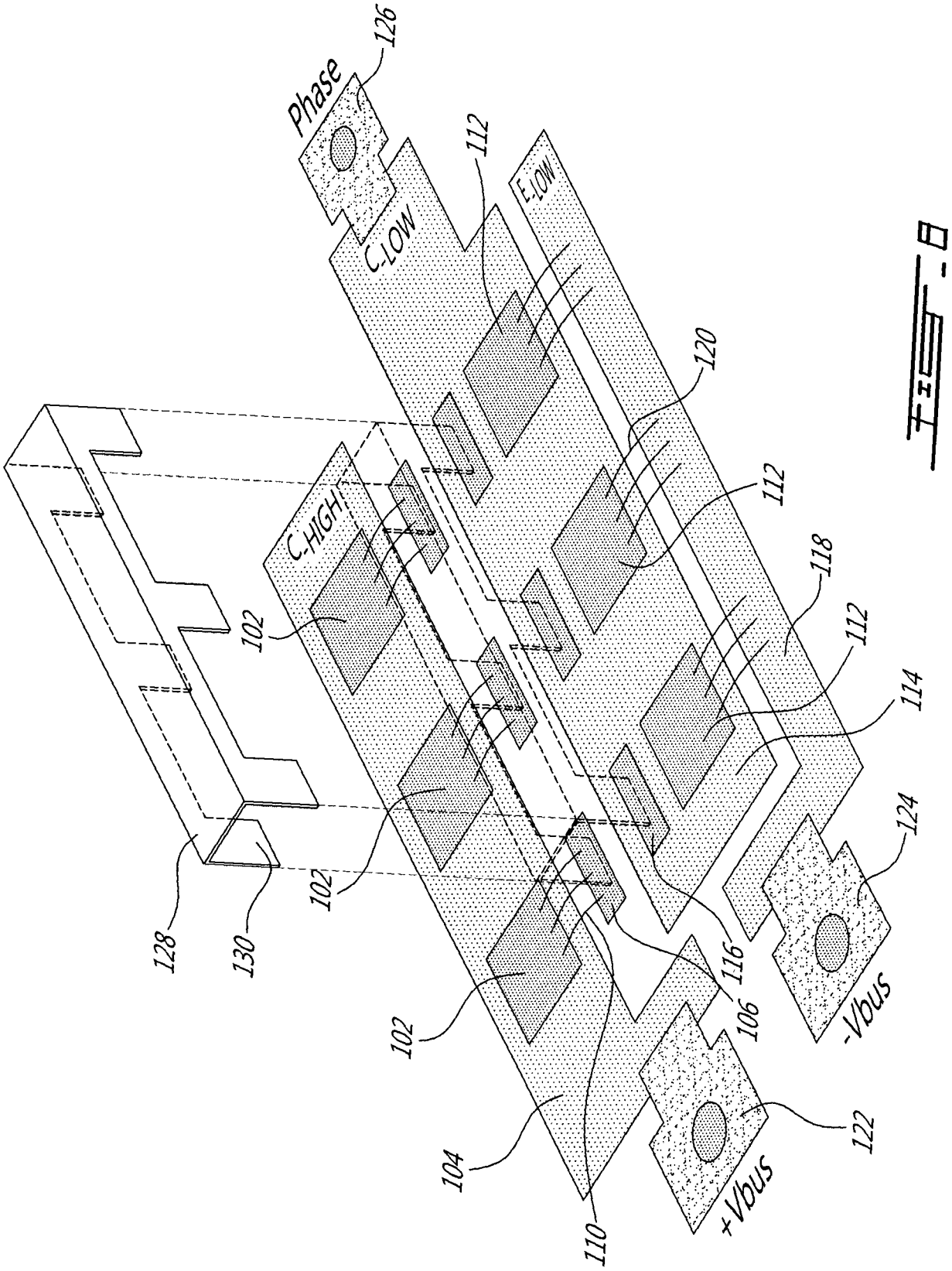

Phase
126
C_LOW
112
E_LOW
120
C_HIGH
102
118
112
114
124
128
130
116
106
-Vbus
104
122
+Vbus
110

Fig - 8

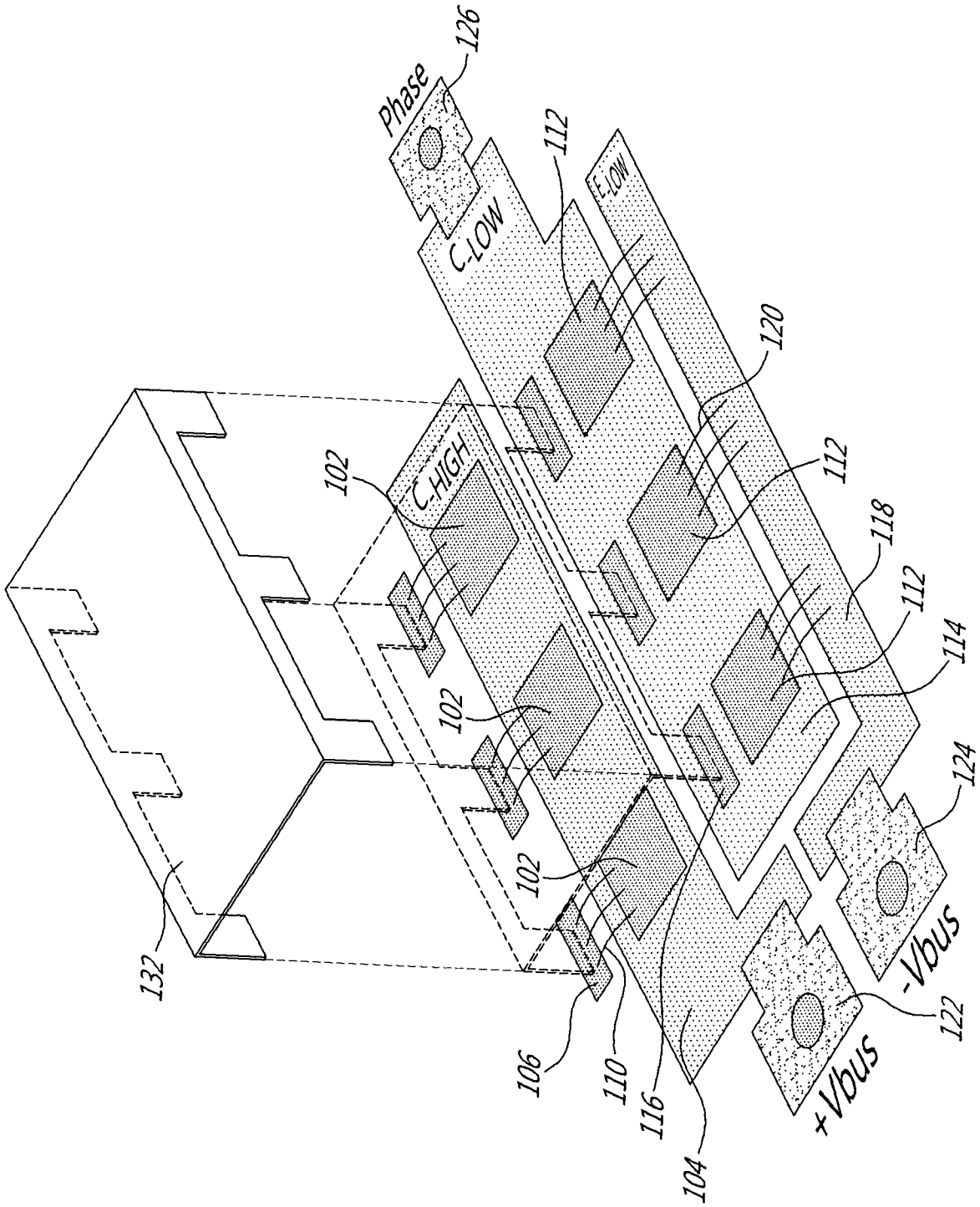
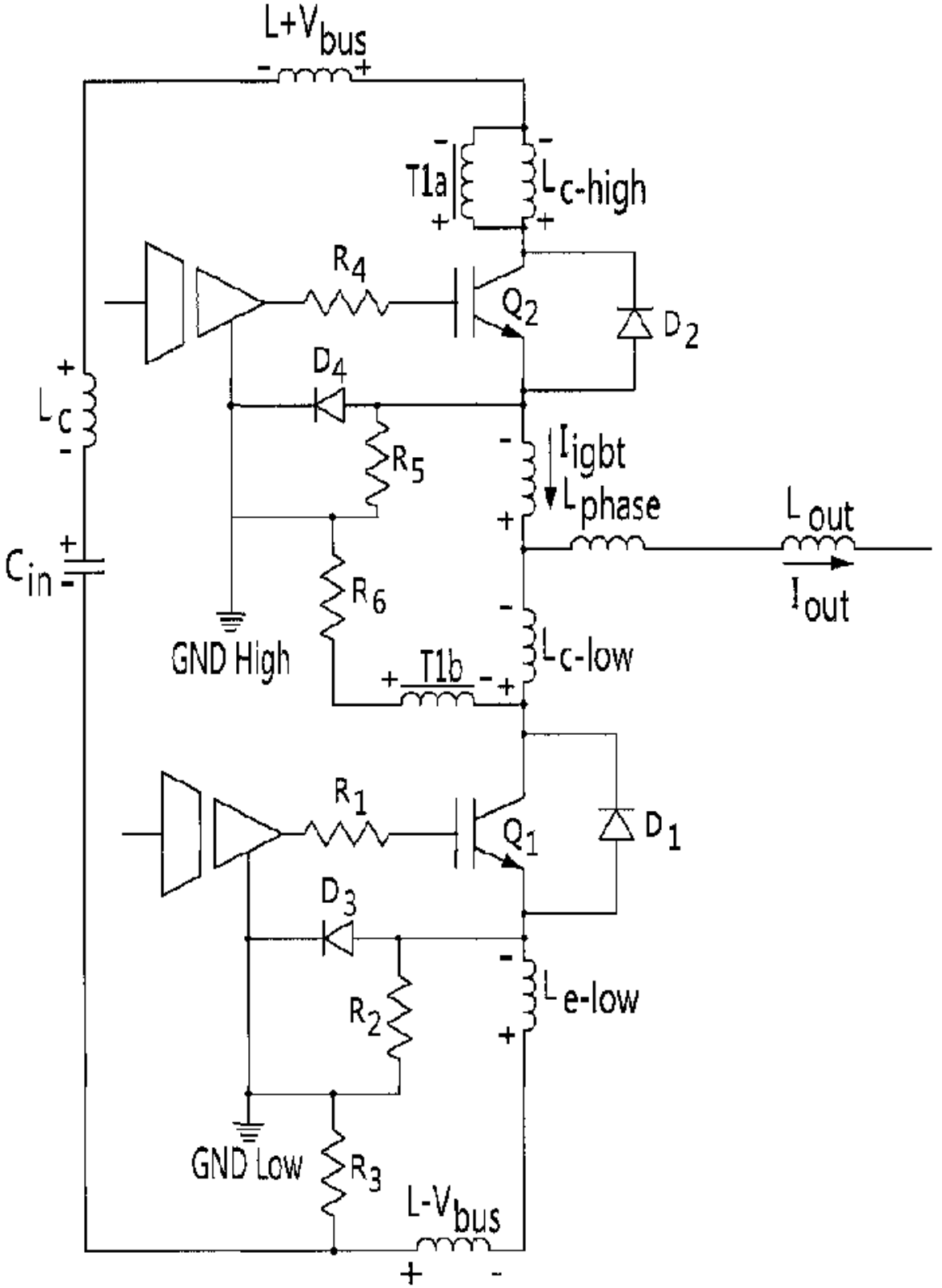

Phase
126
C_LOW
112
E_LOW
120
C_HIGH
102
112
118
112
114
102
124
102
-Vbus
132
122
+Vbus
106
110
116
104

Fig. 9


L+Vbus
T1a
Lc-high
R4
Q2
D2
D4
Lc
R5
Iigbt
Lphase
Lout
Iout
Cin
R6
GND High
T1b
Lc-low
R1
Q1
D1
D3
Le-low
R2
GND Low
R3
L-Vbus