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(54) **ELECTRIC COPPER PLATING LIQUID AND PROCESS FOR MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING SAME**

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(57) **ABSTRACT**

An object of the present invention is to improve the reliability and the yield of production of semiconductor integrated circuit devices by filling copper in the inside of features having a high aspect ratio for forming multi-layer interconnections composed of a plurality of interconnection layers which are connected to one another and to a copper electroplating bath suitable therefor. In the present invention, when the features are filled with copper, the use of a copper electroplating bath with an addition of cyanine dyes, for example, indolium compounds allows the copper plating to proceed preferentially from the bottoms of the features.

FIG. 1A

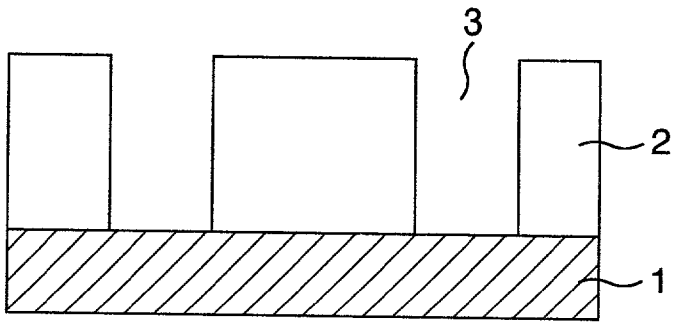


FIG. 1B

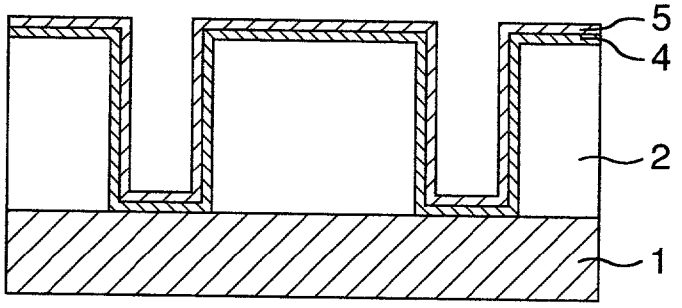


FIG. 1C

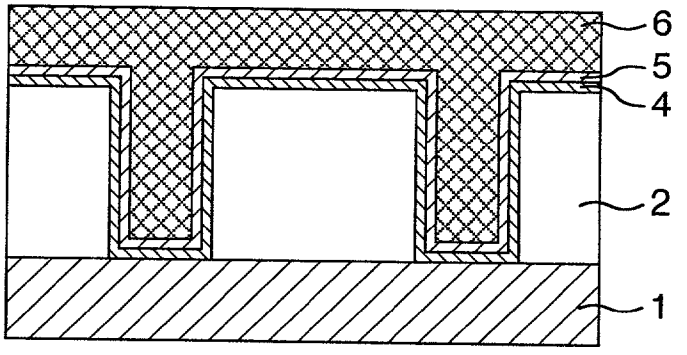


FIG. 1D

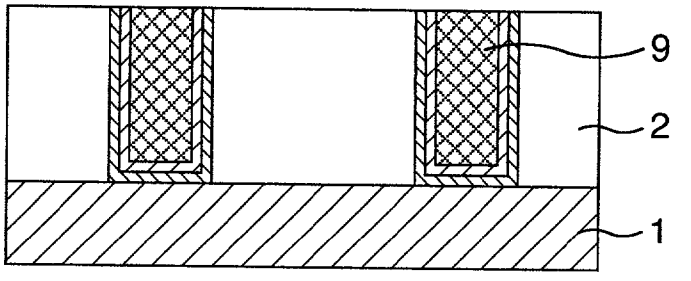


FIG. 2A

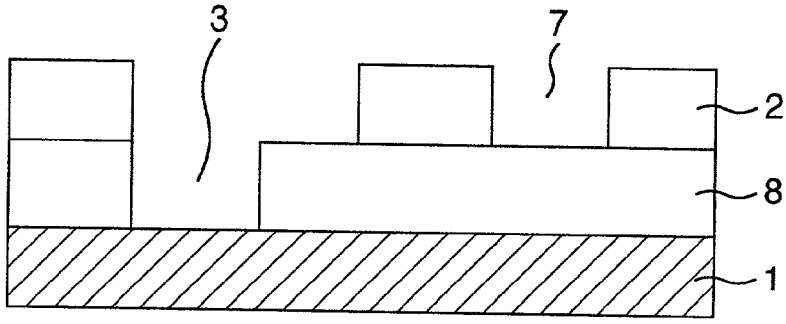


FIG. 2B

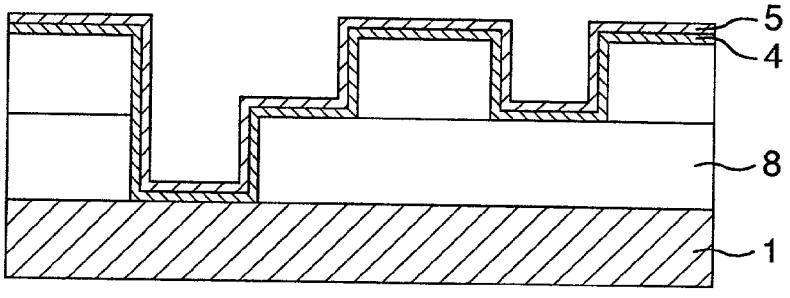


FIG. 2C

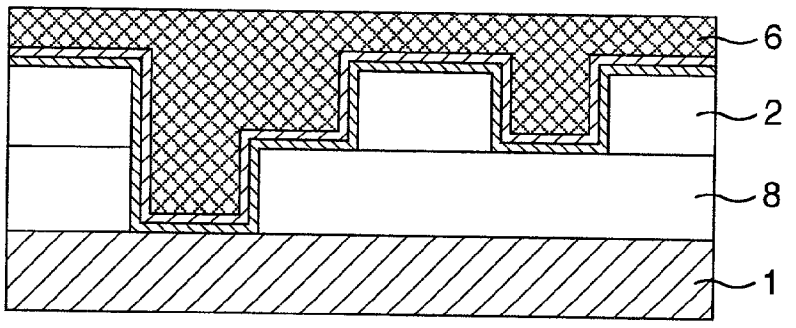


FIG. 2D

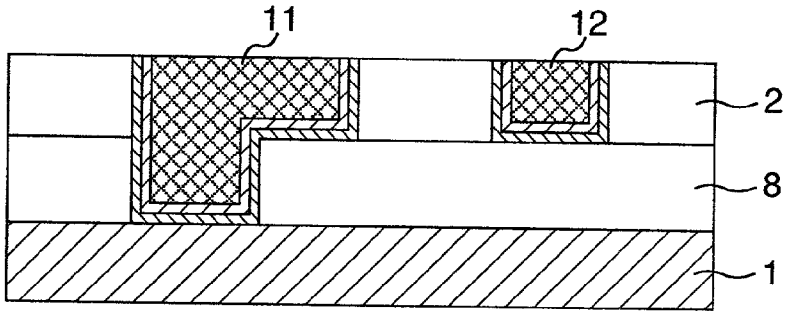


FIG. 3

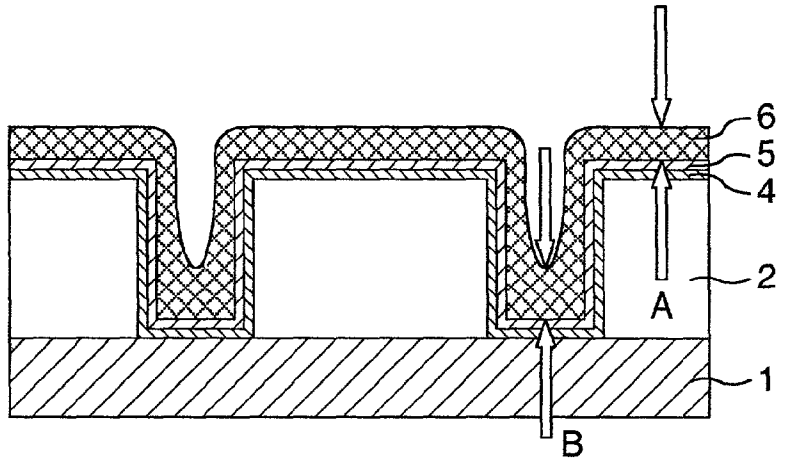


FIG. 4

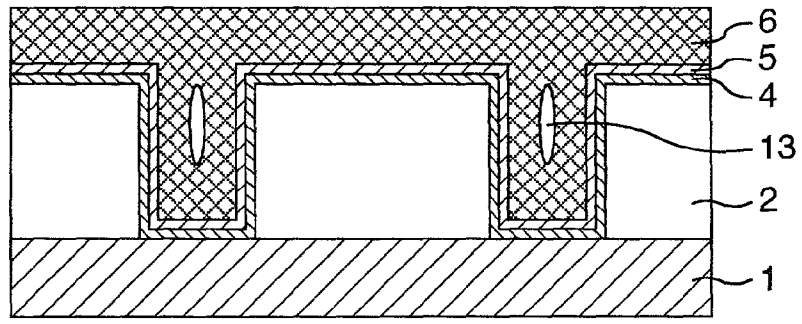
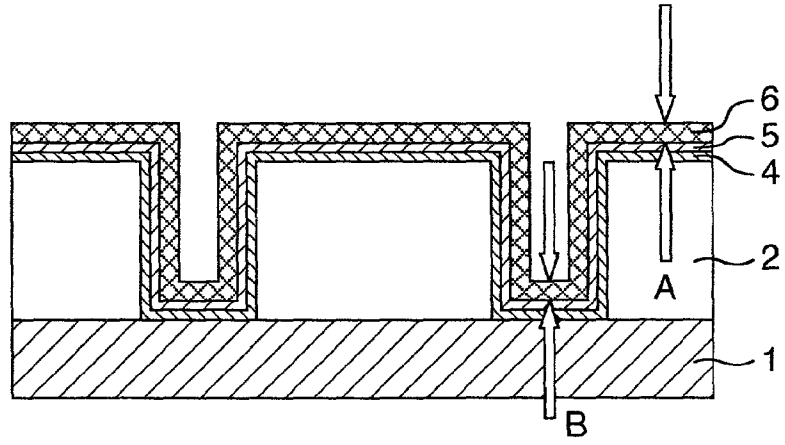


FIG. 5



ELECTRIC COPPER PLATING LIQUID AND PROCESS FOR MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING SAME

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a copper plating bath, more particularly, to a copper electroplating liquid to be used for filling copper in fine openings in insulating layers by electroplating, and a process for manufacturing a semiconductor integrated device with multi-layer interconnections formed using the same.

[0002] There have been conventionally used aluminum or aluminum-copper alloys as materials for use in interconnections in semiconductor devices. As interconnections are micronised with more highly integrated LSI, the delay of signal transmission due to an increase in resistance and capacitance of the interconnections and reduced reliability due to electromigration become a problem. In order to overcome this problem, there has been proposed a method of reducing the resistance of interconnections by making them with metals having a low resistance such as gold, silver and copper. Among them, copper is expected to be a substitute for aluminum and alloys thereof.

[0003] As opposed to aluminum, copper can not produce a compound having a high vapor pressure so that it is difficult to form fine patterns by dry etching. For this reason, there has been employed a technique (called as Damascene method) where trenches and vias are first formed in insulating layers in place corresponding to the patterns of interconnections, and then they are filled with copper.

[0004] Generally all the surfaces of a substrate including features therein are metallized and then excess metals are removed to form interconnections.

[0005] More practically, when interconnections are produced, a diffusion-inhibiting layer (barrier layer) and a copper seed layer are formed on the surfaces of an insulating interlayer having trenches and vias formed therein by sputtering and then copper is filled in the trenches and vias by electroplating with a seed layer being as an electron transmitting layer. Materials to be used for the barrier layer include high melting point metals such as tantalum, tungsten and the like, and alloys thereof and nitrides such as titanium nitride, tantalum nitride and the like.

[0006] Techniques for filling the features include physical vapor deposition (PVD) such as sputtering, chemical vapor deposition (CVD), and plating. The PVD method is poor in coverage with metals on the sides of the features making their aspect ratio higher (that is, making the features thinner and deeper), which may form voids in the filled metals. The CVD method is relatively good in coverage, but it suffers from high costs of source materials. The plating is lower in cost as compared with other methods and excellent in filling property. Therefore, it has attracted much interest. Particularly electroplating is excellent in filling property, provides a high throughput, and effective to mass production. Therefore, it is most promising as a method for filling features.

[0007] For example, Japanese Patent KOKAI No. Hei 11-26394 discloses a process for filling trenches by electroplating after forming an iodine coating layer on a seed layer.

[0008] Japanese Patent KOKAI No. Hei 11-97391 discloses a process for producing interconnections by electroplating with pulse current in a plating bath without additives.

[0009] Japanese Patent KOKAI No. Hei 11-310896 discloses a process for producing interconnections in a plating bath containing little support electrolyte.

[0010] Japanese Patent Kokai No. 2000-248397 discloses a process for filling trenches by adding a polymeric surfactant, a sulfur-based saturated organic compound and an organic dye compound to a plating bath.

[0011] As described above, though various processes have been studied to fill fine features with metals by using electroplating, each of them has a problem.

[0012] The process of Japanese Patent KOKAI No. Hei 11-26394 provides conformal deposit of metal by plating. If there are irregularities on the surface of a seed layer, the deposits on the raised sites may come to contact with adjacent deposits on the sides of the features as the plating proceeds, resulting in formation of voids. Even when the plated film has an appearance of a flat surface due to iodine, seam may be formed in the central portions of the features because the surface is not perfectly plat.

[0013] In the process of Japanese Patent KOKAI No. Hei 11-97391, the use of pulse current can make a diffusion layer thinner, which may allow uniform deposits on the fine features to be expected. However, the conformal deposition by this process may generate voids similarly to those as described above. It is difficult with the plating bath containing no additives to form flat films because the films to be deposited under plating grow reproducing the irregularities on the surface of the primer seed layer.

[0014] The process of Japanese Patent KOKAI No. Hei 11-310896 increases an amount of copper diffused into fine features by significantly reducing an amount of support electrolyte in a plating bath. However, even when sufficient amount of copper is supplied, conformal depositions occur in the features, resulting in formation of voids and seams.

[0015] In the process disclosed in Japanese Patent Kokai No. 2000-248397, the organic dye compound such as Absorber Dye ADI or Cy5 is added to the plating bath so as to attain levelling function which smoothes the copper surface. Absorber Dye ADI and Cy5 comprise an anionic compound having 2 or more of sulfonic groups. Such a compound is scarecely adsorbed on the surface in the plating step. Therefore, it is hard to grow plating preferentially from the bottoms, which is accomplished by a reaction of an additive described below.

[0016] Thus, it is difficult to fill completely the features having a high aspect ratio by the conventional electroplating process as described above. The interconnections having voids and seams therein suffer from increase of wiring resistivity, delay of the transmission of electric signals and the like. Therefore, there has been a need for a technique which allows such fine features to be completely filled.

[0017] As trenches were filled with copper by a bottom-up-filling technique, i.e., a technique of facilitating copper plating on the bottom of trenches as described in the report by Mr. Reid, titled "Copper Electrodeposition for IC interconnect Formation" in Advanced Metallization Conference

(ADMETA), Oct. 13, 1999, pp. 65-102, studies on its mechanism and plating baths suitable for it have been intensively made.

SUMMARY OF THE INVENTION

[0018] It is an object of the present invention to provide a copper electroplating bath suitable for filling copper in features having a high aspect ratio with high reproducibility.

[0019] It is another of the present invention to provide a copper electroplating bath suitable for filling copper in features having a high aspect ratio without generating voids and seams with high reproducibility.

[0020] It is still another of the present invention to provide a semiconductor integrated circuit device having a high interconnection density in the interconnection layers having a high electromigration resistance where fine features have been filled with copper, i.e., without existing voids and seams, using such a plating bath as above.

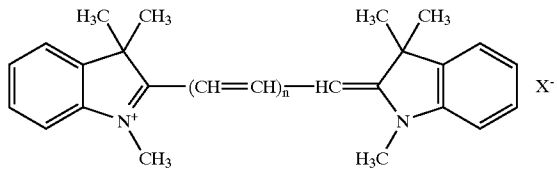
[0021] The present invention will be summarized under.

[0022] In the present invention, an additive is added to a copper electroplating bath, said additive suitable to allow copper plating to proceed preferentially from the bottoms of features such as trenches and vias having a high aspect ratio which have been formed on the surfaces of a substrate.

[0023] The copper electroplating bath of the present invention comprises a solution containing copper ions and electrolyte(s) with an addition of, for example, cyanine dye.

[0024] In an embodiment of the copper electroplating bath of the present invention, the solution containing copper ions and electrolyte(s) contains as an additive at least one of cyanine dyes represented by, for example, the following general formula (I):

(I)



[0025] where X^{31} is an anion, and n is 0, 1, 2, or 3 (abbreviated as n=0 to 3 hereunder).

[0026] In another embodiment of the copper electroplating bath according to the present invention, the solution containing copper ions and electrolyte(s) is characterized by having an indolium compound added thereto.

[0027] In a preferred embodiment, the copper electroplating bath may contain at least one or more of polyethers, organic sulfur compounds and halide ions as further additives.

[0028] The process for producing a semiconductor integrated circuit devices according to the present invention comprises providing an insulating layer having openings on the top of the major surface of a semiconductor wafer which has a plurality of circuit element areas formed therein, depositing a barrier layer and a seed layer on the bottom and the side surfaces of the openings and on the top surface of the insulating layer, and filling the inside of the openings with copper without forming any voids and seams by electroplating with the copper electroplating bath as described above to from a interconnection layer. The process is capable of producing a high packing density LSI having an excellent reliability with high reproducibility.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] **FIGS. 1A, 1B**, 1C, and 1D show a cross-sectional view of a major part of an interconnect structure at each step of the process for the production thereof in an Example according to the present invention, respectively.

[0030] **FIGS. 2A, 2B**, 2C, and 2D show a cross-sectional view of a major part of an interconnect structure at each step of the process for the production thereof in another Example according to the present invention, respectively.

[0031] **FIG. 3** shows a cross-sectional view of a major part of an interconnect structure showing how a copper film is allowed to grow by the plating according to the present invention.

[0032] **FIG. 4** shows a cross-sectional view of a major part of an interconnect structure in a Comparative Example to demonstrate the effect of the present invention.

[0033] **FIG. 5** shows a cross-sectional view of a major part of an interconnection structure showing how a copper film is allowed to grow by the plating in a Comparative Example to demonstrate the effect of the present invention.

[0034] In the drawings, each reference number designates a part as follows: **1**: Silicon substrate; **2**: Insulating layer; **3**: Via; **4**: Barrier layer; **5**: Seed layer; **6**: Copper electroplated layer; **7**: Trench; **8**: Insulating layer; **9**, **11** and **12**: Copper layer; **13**: Void.

DETAILED DESCRIPTION OF THE INVENTION

[0035] As described above, metals which may be used in filling fine features with a low resistance metal by electroplating include gold, silver and copper. These metals may diffuse into adjacent insulating layers and semiconductor layers to deteriorate characteristic properties of circuit elements. Therefore, the diffusion must be prevented by providing a barrier layer under the metal layer. Electroconductive materials which can function as barrier include metal nitrides such as titanium nitride, tungsten nitride, tantalum nitride, and high melting point metals such as tantalum and tungsten and alloys thereof. These barrier layers are also disposed sequentially to the surfaces of the insulating layers having the trenches and the vias as well as the inside of thereof.

[0036] The barrier layer which may be made of any one of metal nitrides and high melting point metals and alloys thereof has a relatively high resistance and may produce a relatively stable oxide on the surface, so that it is difficult to electroplate directly the surface of the barrier layer. For this reason, a seed layer as an electron transmitting layer, e.g., a copper film is further formed on the barrier layer using PVD, CVD, or electroless deposition process.

[0037] Next, according to the subject of the present invention, a copper is electroplated on the seed layers present even on the inner surfaces of the feature by copper electroplating to fill the inside of the feature with copper. The characteristics of the copper film are very sensitively depending upon the configuration of the seed layer and the thickness of the film.

[0038] For example, when the seed layer is discontinuous, the plating rate at the sites without any seed layer is very slow or produce no plating resulting in generation of voids. When the seed layer is not uniform in thickness or has irregularities on the surface, uniformity of the growing copper film is inhibited, that is, the thickness of copper film become not uniform during copper electroplating resulting in the formation of seams, i.e., seam like boundary in the copper film filling the inside of the feature.

[0039] The presence of such voids and seams may cause the confinement of plating bath components, air and moisture at the sites to reduce the reliability of the resulting semiconductor integrated circuit devices having highly packed fine interconnections. Therefore, the seed layer must be uniformly produced throughout the surfaces of the insulating layer and the inside of the feature. A non-negligible variation of the seed layer in the LSI having quite a lot of openings has an influence on the final proportion of good products, i.e., yield.

[0040] Even when a seed layer is formed throughout the surfaces, preferential growth of electroplated copper deposit in the openings of the feature may close off the feature. As a result, voids having plating bath remained therein are produced. When a copper grows conformally by electroplating, the plated film can not perfectly be flat so that voids and seams are inevitably formed in the central portion.

[0041] In order to fill the features with seamless copper, therefore, it is necessary to allow copper electroplating deposit to grow preferentially from the bottoms of the features. Moreover, as described above, it must be reproducibly conducted without being affected by fluctuation of the characteristics of the seed layer.

[0042] The present inventors have found that electroplating deposits can be grown preferentially from the bottoms of the features by using a specific additive with good reproducibility as described above. The additive is a material which suppresses the electroplating reaction and is consumed as the electroplating reaction proceeds. That is, the commencement of the electroplating reaction reduces the concentration of the additive on the surfaces where the reaction is taking place. If the diffusion rate of the additive is lower than the rate of the additive reaction, the diffusion of the additive controls the electroplating reaction. Therefore, an extent of the suppression of reaction depends on the amount of the additive to be supplied to the surfaces through diffusion.

[0043] For this reason, there may be a difference in the amount of the additive to be supplied through diffusion between the regions in the vicinity of the openings of the features and the bottoms of the features. The additive is smoothly supplied in the vicinity of the openings, resulting in the suppression of the electroplating reaction. On the other hand, inside the features, the additive tends to react into a material having no effect of suppressing the electroplating reaction before it reaches the bottoms, so that the amount of the additive is reduced in the bottoms. Therefore, the electroplating reaction at the bottoms is much less suppressed as compared with that around the openings. That is, less amount of the additive having an effect of suppressing the reaction is supplied to the bottoms, so that the electroplating proceeds preferentially from the bottoms.

[0044] If the additive has a very low rate of reaction, or if the rate of diffusion is very high, a sufficient amount of the additive may be supplied to the bottoms of the features. Therefore, the difference in suppression is reduced between the bottoms and the openings. If the additive has a very high rate of reaction, or if the rate of diffusion is very low, little supplement of the additive may be effected to the openings of the features. The difference in suppression is again reduced between the bottoms and the openings. Therefore, preferably the additive should be of a molecule which has a rate of diffusion and a rate of reaction in such appropriate ranges as producing a difference in concentration between the openings and the bottoms of the features. Consequently, this can be an extremely effective measure to the influence of the fluctuation of the characteristics of the aforementioned seed layer.

[0045] Materials useful for such an additive include 2-[(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-methyl]-1,3,3-trimethyl-3H-indolium perchlorate, 2-[3-(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-1-propenyl]-1,3,3-trimethyl-3H-indolium chloride, 2-[5-(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-1,3-pentadienyl]-1,3,3-trimethyl-3H-indolium iodide, and 2-[7-(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-1,3,5-heptatrienyl]-1,3,3-trimethyl-3H-indolium iodide. They should be preferably used in a concentration of about 1 to 15 mg/liter (which may be abbreviated as mg/L hereunder). The additive concentration outside this range may be effective as additive. If the concentration is lower than 1 mg/L, resulting effects may be insufficient, while if the concentration is higher than 15 mg/L, the concentration of impurities in the copper may possibly increased.

[0046] After the copper electroplating, excess portions of metal layers on the insulating layer (that is, the electroplated copper layer, the seed layer, and the barrier layer) are removed by CMP. At this point, since the uniformity in film thickness and the film flatness are required on the wafer, it is preferred to further add one or more of polyethers, organic sulfur compounds, and halide ions in addition of the aforementioned cyanine dyes to improve the thickness distribution on the wafer.

[0047] Such polyethers are preferably polyethylene glycols, polypropylene glycols, polyoxypropylene glycols having an average molecular weight of 1000 to 10,000.

[0048] The organic sulfur compounds are preferably 3-mercapto-1-propanesulfonic acid, 2-mercapto ethane sulfonic acid, bis(4-sulfobuthyl)disulfide, bis(3-sulfopropyl)disulfide, bis(2-sulfoethyl)disulfide, or bis(p-sulfophenyl)disulfide.

DESCRIPTION OF PREFERRED EMBODIMENTS

[0049] The following Examples demonstrate preferred embodiments of the present invention.

[0050] The copper electroplating bath according to the present invention is used in a range of 15 to 35° C. in order to avoid excessive decomposition of an additive. A concentration of copper ions of 0.2 mol/L or more is preferred and usually used in a range of current density of 0.2 to 3.0 A/dm^2 (square decimeter). When the copper electroplating is conducted, preferably the plating bath should be stirred with a pump or air, or the substrate should be rotated or vibrated in order to maintain the supply of the additive constant.

EXAMPLE 1

[0051] First, a composition of the copper electroplating bath and a process for electroplating copper on an interconnection substrate structure using the same according to the present invention and a method of evaluation for them with reference to **FIGS. 1A, 1B**, and **1**C.

[0052] i) Preparation of Interconnection Substrate Structure

[0053] In order to make it possible to evaluate characteristics of various plating baths as precisely as possible, basic samples of the interconnection substrate structure were commonly prepared as follows:

[0054] That is, as shown in **FIG. 1A**, an insulating layer 2 of SiO_2 having a thickness of 1.0 μm was formed on the surface of a silicon substrate of ϕ 200 mm, and etched by ordinary dry etching to from vias 3 having ϕ 0.25 μm and a depth of 1 μm.

[0055] Then, by sputtering, tantalum was deposited on the overall top surface to form a barrier layer **4** having a thickness of 50 nm and copper was deposited on the barrier layer to form a seed layer **5** having a thickness of 150 nm. The seed layer **5** was produced at a film formation rate of 200 to 400 nm/min using Ceraus ZX-1000, a long distance sputtering apparatus for sputtering copper (made by ULVAC Co.). **FIG. 1B** shows a cross-sectional view of the structure after the copper seed layer was formed.

[0056] ii) Process for Electroplating Copper

[0057] There were prepared various plating baths each having a composition as indicated in the following Table 1, and copper was electroplated on the top surface of the interconnection structure as shown in **FIG. 1B** to form an electroplated copper **6** as shown in **FIG. 1C**. The plated substrate structure obtained according to the procedure as described above was removed from the copper electroplating bath and washed with distilled water for 3 minutes.

TABLE 1

	Composition of Plating Bath					Plating
Sample No.	Copper Conc. (mol/L)	Sulfuric Acid Conc. (mol/L)	Hydrochloric Acid Conc. (mol/L)	Type of Additive	Additive Conc. (mol/L)	Condition Current Density (A/dm^2)
1	0.30	1.9	0	A-1	10	1.0
2	0.40	2.0	1.9×10^{-3}	A-3	8	2.5

TABLE 1-continued

	Composition of Plating Bath					Plating
Sample No.	Copper Conc. (mol/L)	Sulfuric Acid Conc. (mol/L)	Hydrochloric Acid Conc. (mol/L)	Type of Additive	Additive Conc. (mol/L)	Condition Current Density (A/dm^2)
3	0.80	1.0	0.9×10^{-3}	A-2	0.5	1.0
				B-1	100	
				C-1	30	
4	0.30	1.9	1.5×10^{-3}	A-4	20	2.0
				B-2	50	
				C-4	30	
5	0.26	1.9	1.9×10^{-3}	A-2	1	0.2
				B-2	80	
				C-3	15	
6	0.30	1.9	1.9×10^{-3}	A-2	10	1.5
				B-1	40	
				C-3	20	
7	0.80	1.0	1.6×10^{-3}	A-2	15	3.0
				B-3	40	
				C-3	10	
8	0.40	1.9	1.9×10^{-3}	A-1	8	1.0
				B-4	20	
				C-2	10	
9	0.30	1.9	0	—	—	1.0

[0058] Sample Nos. 1 to 8 in Table 1 indicate copper electroplating baths according to the present invention, and Sample No. 9 was indicates a copper electroplating bath outside the present invention prepared for comparison.

[0059] Various signs described in the column "Type of Additive" designate the following chemical materials:

[0060] A-1: 2-[(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-methyl]-1,3,3-trimethyl-3H-indolium perchlorate.

[0061] A-2: 2-[3-(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-1-propenyl]-1,3,3-trimethyl-3H-indolium chloride.

[0062] A-3: 2-[5-(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-1,3-pentadienyl]-1,3,3-trimethyl-3H-indolium iodide.

[0063] A-4: 2-[7-(1,3-Dihydro-1,3,3-trimethyl-2H-indol-2-ylidene)-1,3,5-heptatrienyl]-1,3,3-trimethyl-3H-indolium iodide.

[0064] B-1: Polyethylene glycol (an average molecular weight of 3000).

[0065] B-2: Polyethylene glycol (an average molecular weight of 1000).

[0066] B-3: Polypropylene glycol (an average molecular weight of 3000).

[0067] B-4: Polypropylene glycol (an average molecular weight of 1000).

[0068] C-1: 3-mercapto-1-propanesulfonic acid.

[0069] C-2: 2-mercapto ethane sulfonic acid.

[0070] C-3: bis(3-sulfopropyl)disulfide.

[0071] C-4: bis (2-sulfoethyl)disulfide.

[0072] Each electroplating was conducted at a current density as indicated in Table 1 for a period of time capable of providing a charge corresponding to the formation of a film thickness of 1.0 μm. When the process of growth of film deposit was to be observed, the electroplating was conducted for a period of time capable of providing a charge corresponding to the formation of a film thickness of 0.03 μm.

[0073] The temperature was at 24° C. and the total amount of liquid was 20 liter in a bath. As anode electrode, phosphorus-containing copper was used. The electroplating bath was circulated through a filter at a rate of 15 liter/min with an external pump.

[0074] iii) Evaluation of Electroplated Copper Film

[0075] The cross-section of the plated film was observed by a scanning electron microscope (SEM) where the substrate structure after plated (**FIG. 1C**) was processed with FIB (Focused Ion Beam) and the cross-sections of 100 vias were observed. When the process of the growth of copper film to be plated was observed, in the cross-section of the major portion of the interconnection structure as shown in **FIG. 3**, the thickness of plated film (A) on the surface of the substrate on the way of plating and the thickness of plated film on the bottom of vias (B) were measured and the ratio of B/A was calculated. The uniformity in sheet resistance of plated copper film was evaluated based on measurements at 49 points by a four probe method of the resistivity measurement. Moreover, the test of electromigration resistance (EM resistance) was conducted in the following procedure: a direct current was passed through the interconnections prepared according to the present invention and the resistance was measured with time. The end of the lifetime was defined at the time when the resistance of the interconnections increased by 30%. Comparisons of the results obtained under various conditions were made. The high EM resistance of the copper interconnections improves the durability of the semiconductor devices themselves. These results are summarized in Table 2 under.

TABLE 2

	Plating Bath Composition		Plating Condition	Evaluation Items: Uniformity in plane of			
Sample No.	Type of Dyes	Conc. of Cyanine Dye (mg/L)	Current Density (A/dm^2)	Sheet Resistance (%)	B/A	Presence of boid	EM Resistance (a.u.)
1	A-1	10	1.0	13	2.1	No	1.4
2	A-3	8	2.5	17	3.0	No	1.5
3	A-2	0.5	1.0	3	2.8	No	4.2
4	A-4	20	2.0	5	3.2	No	5.0
5	A-2	1	0.2	4	5.1	No	5.2
6	A-2	10	1.5	4	4.5	No	6.1
7	A-2	15	3.0	5	5.3	No	4.9
8	A-1	8	1.0	4	6.1	No	5.4
9	—	—	1.0	21	1.0	Yes	1.0

[0076] The designations of the signs in the column "Type of Cyanine Dye" in Table 2 are the same as those in Table 1. They are reused for convenience. The B/A is the ratio of the film thickness on the bottoms of the features (B) to that on the surface (A).

[0077] The plating bath of Sample No. 9 (comparative) produced voids as described later, while those of Sample Nos. 1 to 8 (present invention) did not produced observable voids and seams after plating, because of the addition of cyanine dyes to the plating bath allowing the bottoms of the vias to be preferentially plated. Thus, good filling performance could be achieved. Moreover, the EM resistance of the interconnections was also improved. Therefore, it has been found that the semiconductor integrated circuit devices produced according to the present invention have an improved reliability.

[0078] Sample Nos. 3 to 8 contained a polyether, an organic sulfur compound and halide ions in addition to cyanine dye. It has been found that they achieved a good filling property as well as a good uniformity in film thickness on the plane of the substrate with good reproducibility as can be seen from the excellent uniformity in sheet resistance in a range of 3 to 5%. Moreover, the EM resistance of the interconnections was also improved. Therefore, it has been found that the semiconductor integrated circuit devices having an excellent reliability can be produced.

[0079] Sample Nos. 5 to 8 made it possible to further facilitate the growth of film to be preferentially plated on the bottoms (**FIG. 3**) by rendering the concentration of cyanine dye appropriate as can be seen from the high ratio of B/A in a range of 4.5 to 6.1.

[0080] In order to make the effects of the present invention more easily understandable, the present Example 1 will be described with reference to the comparison with the copper electroplating bath of Sample No. 9 (comparative) as shown in Table 1.

[0081] With the copper electroplating bath of Sample No. 9 shown on the bottom in Table 1 as a case of using none of the aforementioned additives which are characteristic of the present invention, copper was plated following to steps **1A**, **1B** and **1C** shown in the drawings.

[0082] The substrate structure after plated was processed with FIB in the same manner as above and the cross-sections of 100 vias were observed by SEM. As a result, voids were observed in the copper films in the holes indicating that there were produced portions not filled with copper in the vias as

shown in the cross-sectional view thereof in **FIG. 4**. Moreover, it was confirmed that some of voids became smaller into a seam like form.

[**0083**] Observation of the process of the growth of copper film to be plated revealed that all the vias have a uniform copper film grown inside the feature as shown in **FIG. 5** and that the electroplating did not proceed preferentially from the bottoms. In this case, the ratio of B/A was calculated to be 1.0.

[**0084**] The foregoing demonstrate the predominancy of the present invention that the vias can be perfectly filled with copper by allowing the electroplating to proceed preferentially from the bottoms thereof.

EXAMPLE 2

[**0085**] Next, the process for producing a semiconductor integrated circuit device having multi-layer interconnections by using the copper electroplating bath according to the present invention will be described with reference to **FIG. 1** again.

[**0086**] **FIG. 1** shows a cross-sectional view of a major part of a semiconductor integrated circuit device having a plurality of semiconductor circuit element areas formed therein (not shown) at each step of the process for the production of the device. It shows an example where the present invention is applied to fill the inside of the features for connecting a plurality of interconnection layers at different levels with copper by electroplating.

[**0087**] That is, in **FIG. 1A, a** substrate **1** has an interconnection layer (not shown) which is formed on an insulating layer coating the surface of a silicon wafer of ϕ 200 mm which has a plurality of semiconductor circuit element areas (not shown) formed, said interconnection layer being connected to said plurality of semiconductor circuit element areas. An insulating interlayer 2 of SiO_2 or the like having a thickness of 1 μm was deposited on the top surface of the substrate. Said interlayer has the bottom surface in contact with the top surface of said interconnection layer (that is, it terminates at the contact) and it was provided with vias **3** having such a high aspect ratio as having ϕ 0.25 μm and a depth of 1 μm for connecting between interconnection layers. At the bottoms of the vias, said interconnection layer is exposed.

[**0088**] Next, as described in Example 1 and as shown in **FIG. 1B, a** barrier layer **4** is deposited continuously on the top surface of the insulating layer **2** and a seed layer **5** is deposited on the barrier layer. The exposed portions of the surface of the interconnection layer at the bottoms of the holes are covered with the barrier layer **4** to be electrically connected.

[**0089**] Then as shown in **FIG. 1C, a** copper layer **6** is plated on the surface of the seed layer **5** using the copper electroplating bath according to the present invention as described above, to fill the vias **3** with the copper.

[**0090**] The substrate which was plated by the process as described above was removed from the copper electroplating bath and washed with distilled water for 3 minutes. Then it was processed with FIB and the cross-sections of 100 vias were observed by SEM. As a result, it was found that voids or seams were not observed and the vias **3** were perfectly filled with copper.

[**0091**] Next, as shown in **FIG. 1**D, chemical and mechanical polishing was effected to remove the metal **6** deposited by the electroplating. The chemical mechanical polishing was performed by using a chemical mechanical polishing apparatus, CMP Apparatus AVANT Model 1472 (made by SpeedFam-IPEC Co.) with alumina dispersion grains containing 1 to 2% hydrogen peroxide and a pad (IC-1000 made by Rodel Co.). The polishing was conducted to reach the insulating layer under a pressure of 150 g/cm^2. As a result, no separation occurred at each boundary. The conductive layers consisting of barrier layer **4**, seed layer **5**, and electroplated metal layer **6** were separated by the chemical mechanical polishing to obtain an interconnect structure.

[**0092**] Then, on the flat surface, an insulating layer (not shown) of SiN or the like was coated to prevent the diffusion of copper, and in addition an insulating layer (not shown) of SiO_2 or the like is deposited. The insulating film (SiO_2 film) and the insulating layer (SiN layer) on the aforementioned filled copper film may be selectively removed by dry etching to form an interconnection structure having a plurality of vias as shown in **FIG. 1A**.

[**0093**] Moreover, on the thus obtained interconnection structure, the steps shown in **FIGS. 1B, 1C** and **1**D may be repeated on the to produce a semiconductor integrated circuit device having multi-layer fine pattern interconnection structure.

[**0094**] The semiconductor integrated circuit devices produced as described above according to the present invention have neither void, nor seam in the copper film filled in the vias **3** which are the key to the construction of the multilayer fine pattern interconnection system. Therefore, the semiconductor integrated circuit devices having a highly reliable multi-layer interconnection structure can be reproducibly produced at high yield.

EXAMPLE 3

[**0095**] **FIG. 2** is for explaining the process for production of a semiconductor integrated circuit device having a plurality of semiconductor circuit element areas (not shown) formed therein. It shows an example where the present invention is applied to fill the inside of features for forming interlayer connections connecting a plurality of interconnection layers at different levels, or therebetween, with copper, respectively. **FIGS. 2A, 2B, 2**C and **2**D show a cross-sectional view of a major part of the device at each step of the process for producing the device.

[**0096**] As shown in **FIG. 2A, a** substrate **1** has first interconnection layer (not shown) on an insulating layer which is coated on the silicon wafer of ϕ 200 mm which has a plurality of semiconductor circuit element areas (not shown) formed therein in the same manner as in Example 2, said first interconnection layer being connected to said plurality of semiconductor circuit element areas. Insulating interlayers **8** and **2** of SiO_2 or the like, each having a thickness of 0.5 μm were deposited on the top surface of the substrate.

[**0097**] In these insulating interlayers, there is provided vias **3**, for connecting between interconnection layers, having a stairs type cross-section through the insulating layers **8** and **2** and having a high aspect ratio which consists of a via having ϕ 0.25 μm and a depth of 1 μm and having the

bottom in contact with the top surface of said first interconnection layer to expose the top surface therein, and a trench or via having ϕ 0.25 μm and a depth of 0.5 μm terminating at the surface of the insulating layer **8**, both vias being in conjunction with each other to form said stairs type. At a location apart from the vias, there is also provided in the insulating layer **2** a trench **7**, for forming narrow and long interconnection extending on the surface of the insulating layer **2**, having a high aspect ratio such as width 0.25 μm and a depth of 0.5 μm and having the bottom on the insulating layer **8**. Thus, the provision in the insulating layers of the narrow and long trench **7** for forming interconnection, a plurality of openings having different depths, one of which is a continuous opening having a different depth differentiates this Example from Example 2 described above.

[**0098**] The thus produced interconnect structure is provided with a barrier layer **4** and a seed layer **5** (**FIG. 2B**) as in Example 2, and further a copper layer **6** is plated on the seed layer **5** using the copper electroplating bath of the present invention (**FIG. 2C**). The metal layers on the surface of the insulating layer **2** were removed by a CMP technique to produce a flat insulating surface at the same level as the surfaces of the copper layers **11** and **12** which were filled in the features **3** and **7** (**FIG. 2D**).

[**0099**] Similarly to Example 2, the substrate after the step shown in **FIG. 2C** was completed was removed from the copper electroplating bath as a sample and processed with FIB. The cross-sections of 100 vias **3** and 100 trenches **7** were observed by SEM. As a result, it was found that neither void, nor seam was observed and the openings were perfectly filled with copper.

[**0100**] As a result of observations on the process of the growth of plated films within a short period of plating time, all the features had a higher film thickness at the bottom than that at the corner of the features. It has been found, therefore, that plated copper 6 were deposited proceeding preferentially from the bottoms as described with reference to **FIG. 3**. Moreover, it was confirmed that the plated copper **6** were deposited preferentially from the deepest bottoms of the features. Slight irregularities appeared to be produced on the surfaces of the interconnection structure as a whole. It was confirmed that they have no problem as they could be made flat by CMP to form flat major surfaces with good reproducibility as shown in **FIG. 2D**.

[**0101**] It has been found from the foregoing that even when there are a plurality of features having different depths, or a plurality of features having different opening diameters, or features having a sequential stairs type bottom as shown in **FIG. 2A**, they can be filled reproducibly with copper at a high yield without generating either void or seam as in Example 2.

[**0102**] Large scale integrated circuits (LSIs) will be required to load an increasingly larger number of complicated circuit function blocks on one semiconductor substrate. Such LSIs will require a multi-layer fine pattern interconnection structure which is produced with copper layers filled by plating in a plurality of features having different depths and shapes as described in the present Example 3 in relation to the process of production and the configuration of circuits. Application of the present invention allows high reliability LSIs to be produced in large scale at a high yield.

[**0103**] According to the present invention, the inside of features can be reproducibly filled with copper without apertures such as voids and seams by allowing copper plating to proceed preferentially from the bottoms of the features. The possibility of forming fine vias and trenches not having any apertures such as voids and seams can improve the reliability of high density semiconductor integrated circuit devices having fine interconnections filled with copper and the yield of the production thereof.

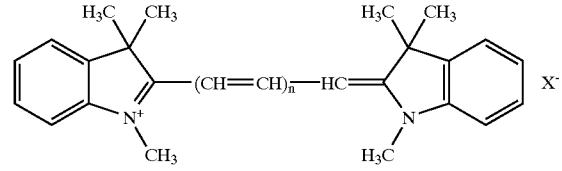
[**0104**] The following embodiments are disclosed in relation to the above description:

[**0105**] (1) A copper electroplating bath comprising a solution containing copper ions and electrolyte(s) with an addition of cyanine dye(s).

[**0106**] (2) A copper electroplating bath comprising a solution containing copper ions and electrolyte(s) with an addition of indolium compound(s).

[**0107**] (3) A copper electroplating bath comprising a solution containing copper ions and electrolyte(s) with an addition of at least one of the compounds represented by the following general formula (I):

(I)



[**0108**] where X^- is an anion, and n is 0, 1, 2, or 3.

[**0109**] (4) The copper electroplating bath according to above items (1) to (3), wherein comprising said copper electroplating bath with a further addition of one or more of polyethers, organic sulfur compounds and halide ions.

[**0110**] (5) The copper electroplating bath according to above items (1) to (4), wherein at least one or more of said cyanine dyes, indolium compounds and the compounds of the general formula (I) is added at a concentration of 1 to 15 mg/L.

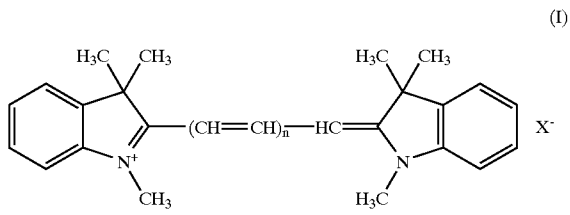
[**0111**] (6) A process for producing a semiconductor integrated circuit device characterized in that said process comprising providing an insulating layer having features on the top of the major surface of a semiconductor wafer which has a plurality of circuit element areas formed, depositing a barrier metal layer and a seed metal layer on the bottoms and the side surfaces of said features and on the top surface of said insulating layer, and filling the inside of said features with copper by electroplating with the copper electroplating bath according to any one of above items (1) to (5).

What is claimed is:

1. A copper electroplating bath comprising a solution containing copper ions and at least one of electrolytes with an addition of at least one of cyanine dyes.

2. A copper electroplating bath comprising a solution containing copper ions and at least one of electrolytes with an addition of at least one of indolium compounds.

3. A copper electroplating bath comprising a solution containing copper ions and at least one of electrolytes with an addition of at least one of the compounds represented by the following general formula (I):



(I)

where X^- is an anion, and n is 0, 1, 2, or 3.

4. The copper electroplating bath according to claim 1, wherein one or more of polyethers, organic sulfur compounds and halide ions is further added to said copper electroplating bath.

5. The copper electroplating bath according to claim 2, wherein one or more of polyethers, organic sulfur compounds and halide ions is further added to said copper electroplating bath.

6. The copper electroplating bath according to claim 3, wherein one or more of polyethers, organic sulfur compounds and halide ions is further added to said copper electroplating bath.

7. The copper electroplating bath according to claim 1, wherein at least one or more of said cyanine dyes is added at a concentration of 1 to 15 mg/L.

8. The copper electroplating bath according to claim 2, wherein at least one or more of said indolium compounds is added at a concentration of 1 to 15 mg/L.

9. The copper electroplating bath according to claim 3, wherein at least one or more of the compounds of the general formula (I) is added at a concentration of 1 to 15 mg/L.

10. A process for producing a semiconductor integrated circuit device comprising providing an insulating layer having features on the top of the major surface of a semiconductor wafer which has a plurality of circuit element areas formed, depositing a barrier metal layer and a seed metal layer on the bottoms and the side surfaces of said features and on the top surface of said insulating layer, and filling the inside of said features with copper by electroplating with the copper electroplating bath according to claim 1.

11. A process for producing a semiconductor integrated circuit device comprising providing an insulating layer having features on the top of the major surface of a semiconductor wafer which has a plurality of circuit element areas formed, depositing a barrier metal layer and a seed metal layer on the bottoms and the side surfaces of said features and on the top surface of said insulating layer, and filling the inside of said features with copper by electroplating with the copper electroplating bath according to claim 2.

12. A process for producing a semiconductor integrated circuit device comprising providing an insulating layer having features on the top of the major surface of a semiconductor wafer which has a plurality of circuit element areas formed, depositing a barrier metal layer and a seed metal layer on the bottoms and the side surfaces of said features and on the top surface of said insulating layer, and filling the inside of said features with copper by electroplating with the copper electroplating bath according to claim 3.

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