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(54) ELECTRONIC TIMEPIECE

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese Company of 3—4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic timepieces.

The present invention seeks (a) to provide a logical control of an electronic timepiece, (b) to reduce the cost in assembling the timepiece, (c) to produce a timepiece which is easily repaired by performing the logical control by means of an external physical signal, (d) to produce a highly accurate and highly reliable temperature compensated timepiece, (e) to construct a logical circuit for temperature compensation using a small number of active elements so that the circuit can be integrated in a small area, (f) to realise a small and inexpensive electronic timepiece, (g) to produce a high precision electronic timepiece which has a relatively low power consumption and uses a vibrator whose temperature variation is large and a low frequency band, and (h) to produce a miniaturised high precision electronic timepiece employing a micro-miniaturised vibrator which is produced at moderate cost by a chemical etching technique.

According to the present invention there is provided an electronic timepiece including two oscillator circuits each having a piezo-electric oscillator, and connected to produce time standard signals, each oscillator circuit including a variable capacitor for setting the nominal frequency of the time standard signal produced thereby, the capacitors being interlocked for variation as a unit.

The electronic timepiece may include a memory circuit for memorizing a signal which is representative of a function of the difference between the frequencies of the time standard signals.

The electronic timepiece may, additionally or alternatively, include a detecting circuit for detecting the difference between the frequencies of the time standard signals,

a frequency divider circuit, and a pulse adding circuit or a pulse eliminating circuit connected to be controlled by the detecting circuit and connected in series with the divider circuit.

The electronic timepiece may include a programmable counter.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:—

Figure 1 is a block diagram of a conventional electronic timepiece;

Figure 2 is a block diagram of one embodiment of an electronic timepiece according to the present invention;

Figure 3 is a circuit diagram of a second embodiment of an electronic timepiece according to the present invention; and

Figure 4 is a circuit diagram of another embodiment of an electronic timepiece according to the present invention;

Figure 1 illustrates a conventional electronic timepiece. This electronic timepiece has an oscillator circuit comprising a piezo-electric oscillator 1 whose output is connected to an inverter 2 which functions as an amplifier, a phase control resistor 3, a bias resistor 4, and capacitors 5, 6 for controlling the frequency of the output signal from the oscillator circuit. Generally, a high-precision electronic timepiece can be achieved by using, for example, a temperature variable capacitor as the capacitor 6 to compensate for the temperature characteristics of the piezo-electric oscillator 1. A time standard signal produced from the oscillator circuit is frequency divided by a divider circuit 7 which, in turn, drives a display device 8. A construction such as that illustrated in Figure 1 may be employed in both watches and stop-watches. The conventional electronic timepiece illustrated in Figure 1 has the following defects:

(1) It is remarkable difficult to arrange that the temperature characteristics of the piezo-electric oscillator 1 can be completely compensated by means of a temperature variable capacitor and this is an obstacle to obtaining a high precision electronic timepiece.

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65
70
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80
85
90
95
100

(2) Whilst piezo-electric oscillators having good temperature characteristics are known, such piezo-electric oscillators vibrate in a comparatively high frequency band, so that the electronic timepiece has to have a high capacity battery to supply sufficient electrical power to drive it. However, high capacity batteries are of relatively large size and the volume available to house the battery of this type in an electronic timepiece is limited.

Figure 2 is a block diagram of an embodiment of an electronic timepiece according to the present invention having piezo-electric oscillators 9, 10 each of which is connected in an oscillator circuit of similar construction to that shown in Figure 1. Interlocked trimmer capacitors 11 are connected in both oscillator circuits for variation as a unit so that the nominal frequencies, which are substantially equal, of the time standard signals produced by the oscillator circuits are variable together. Capacitors 12, 13 in the oscillator circuits control the frequency difference between the piezo-electric oscillators.

Although both piezo-electric oscillators will have different frequency/temperature characteristics, a circuit 14 detects the difference in the frequency of the time standard signals from the oscillator circuits. The output of the circuit 14 is fed *via* a memory circuit 15 to a pulse adding or eliminating circuit 16 which produces an output signal which is combined with the time standard signal from the piezo-electric oscillator 10. The output from the circuit 16 is fed to a frequency divider circuit 17 which drives a display device 18. Thus, the electronic timepiece displays the time indication to a high degree of precision and substantially independently of temperature. The memory circuit 15 may, if desired, be omitted from the arrangement illustrated in figure 2.

Figure 3 is a circuit diagram of part of embodiment of an electronic timepiece according to the present invention. Each of the two terminals 19 receives a time standard signal from an oscillator circuit and corresponds to the two inputs of the circuit 14 of Figure 2. One of the terminals 19 is connected to a flip-flop frequency divider circuit 20 having a plurality of stages, and a delay circuit 21 consisting of, for example, a shift register. The other terminal is connected to a flip-flop frequency divider circuit 22 having a plurality of stages and a delay circuit 23 which may be a shift register. The delay circuits 21, 23 produce relatively narrow width pulses which are fed to one terminal of respective AND circuits 24, 25. The output signal from the divider circuit 22, half-period shifted (180° out of phase) from the output of the AND circuit 25 by the delay circuit 23, is fed to one input of an AND circuit 27 through a delay circuit 26, the

other input of the AND circuit 27 being constituted by the output signal from the divider circuit 22. The output signals from the AND circuits 24, 25 are fed to set and reset terminals of a flip-flop circuit 30 after having passed respective AND circuits 28, 29. The output of the flip-flop circuit 30 inverts each time the phase of the output of the AND circuit 24 is half-period shifted (180° out of phase) from the output of the divider circuit 22 and so the difference in frequency of the time standard signals applied to the terminals 19 is detected. The output signal from the flip-flop circuit 30 is applied to one terminal of an AND circuit 32, the other terminal of which receives the output signal after it has been delayed by delay circuit 31, which may be a shift register. The AND circuit 32 produces a pulse signal of relatively narrow period which is used to set a flip-flop circuit 35, and to reset a counter 38 which can be formed on either the same substrate as the circuitry described above or on a separate substrate.

A comparatively high speed clock pulse 37 is fed to the counter 38 which, together with an inverter 39 and an AND circuit 40 constitutes a timer. The clock pulse controlled by this timer is fed to a counter 44. The counter 44 is reset to zero by a comparator 43 in the same state as a counter 34. A flip-flop circuit 48 is also reset by the comparator 43, and a pulse is added by an OR circuit 50 which is controlled by an inverter 45, an AND circuit 46, and an inverter 47. The input to an AND circuit 46 from a flip-flop circuit 49 is inverted with respect to the input signal applied to the OR circuit 50 from the flip-flop circuit 49. Although the counter 38 produces an output signal after a definite period and is clamped at a high level, the counter 34 and the flip-flop circuit 35 are reset at the same time by a pulse from a delay circuit 41 and an AND circuit 42. A low level output from the flip-flop circuit 35 is inverted by an inverter 36 and is fed to an AND circuit 33 with a comparatively slow clock pulse 53. The output of the AND circuit 33 is fed to the counter 34 until the next pulse is produced from the AND circuit 32. The counter 34 acts as a memory circuit to memorise a final state while the flip-flop circuit 35 is set by the output from the AND circuit 32. The output of the OR circuit 50 is connected to a frequency divider circuit 51 which drives a display device 52.

The arrangement illustrated in figure 3 compensates for second order effects due to the temperature characteristics of the piezo-electric oscillators. The counter 34 memorizes the period approximated to the first order effect of temperature. The product of the frequency of the signal at the output of the AND circuit 32 and the pulse

adding rate which is repeated at a definite frequency by the counter 38 represents the second order effect due to temperature. Thus extremely precise temperature correction is achieved even with piezo-electric oscillators which vibrate in a relatively low frequency band. Moreover inaccuracies caused by the combination of elements with different characteristics, such as temperature variable capacitors can be compensated. It is, of course, possible to compensate the third order effects due to temperature in a similar manner.

In the circuit illustrated in Figure 3, the flip-flop circuit 35 is reset and the counter 38 is set by the output of the AND circuit 32 which has a definite period, the difference between the frequencies of the outputs of the oscillator circuits approximating to the second order effects of temperature. However, the components indicated by reference numerals 33 to 44 can be omitted and the output of the AND circuit 32 connected to reset inputs of the inverter 45 and the flip-flop circuit 48.

Figure 4 illustrates another embodiment of an electric timepiece according to the present invention. Reference numerals 54, 55, 56 represent output signals from the AND circuit 32, the AND circuit 25, and the flip-flop circuit 49, in Figure 3. A counter 57 adds a fixed number-pulse each time the counter 57 is controlled by an inverter 58 and the AND circuit 59 and an OR circuit 60, and is reset by the signal 54. A counter 61 is operated by a proper clockpulse 73 and is reset by the signal 54. A comparator group 62 including counters provides output signals to inputs of and OR circuit 63. A counter 64 is reset by the output of the OR circuits 63, and eliminates a pulse when controlled by inverters 65, 66, and AND circuit 67 a delay circuit 69, an inverter 68, and an AND circuit 70. The output of the AND circuit 70 is fed to a divider circuit 71 which drives a display device 72. Temperature compensation is effected by this circuitry. Moreover, the combination of the circuitry of Figure 4 and the circuitry illustrated in Figure 3 which is controlled by an output

of the comparator group 62 effects complicated function compensation.

As will be appreciated in the above discussion, temperature compensation is effected by means of the difference in the frequency of two piezo-electric oscillators. The interlocking trimmer capacitors vary the nominal value of the frequencies.

An electronic timepiece according to the present invention can be produced easily by using low power MOS—IC whose accumulation rate is high and it can keep time precisely and be powered by a miniaturized low power electric cell or battery.

WHAT WE CLAIM IS:—

1. An electronic timepiece including two oscillator circuits each having a piezo-electric oscillator, and connected to produce time standard signals, each oscillator circuit including a variable capacitor for setting the nominal frequency of the time standard signal produced thereby, the capacitors being interlocked for variation as a unit.

2. An electronic timepiece as claimed in claim 1 including a memory circuit for memorizing a signal which is representative of a function of the difference between the frequencies of the time standard signals.

3. An electronic timepiece as claimed in claim 1 or 2 including a detecting circuit for detecting the difference between the frequencies of the time standard signals, a frequency divider circuit, and a pulse adding circuit or a pulse eliminating circuit connected to be controlled by the detecting circuit and connected in series with the divider circuit.

4. An electronic timepiece as claimed in any preceding claim including a programmable counter.

5. An electronic timepiece substantially as herein described with reference to and as shown in Figures 2 to 4 of the accompanying drawings.

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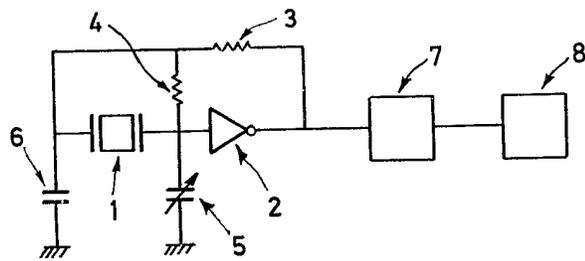


FIG. 1 .

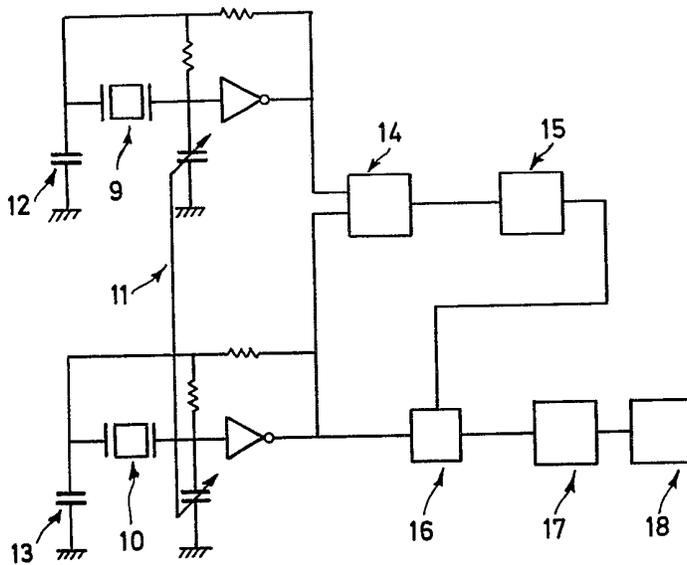
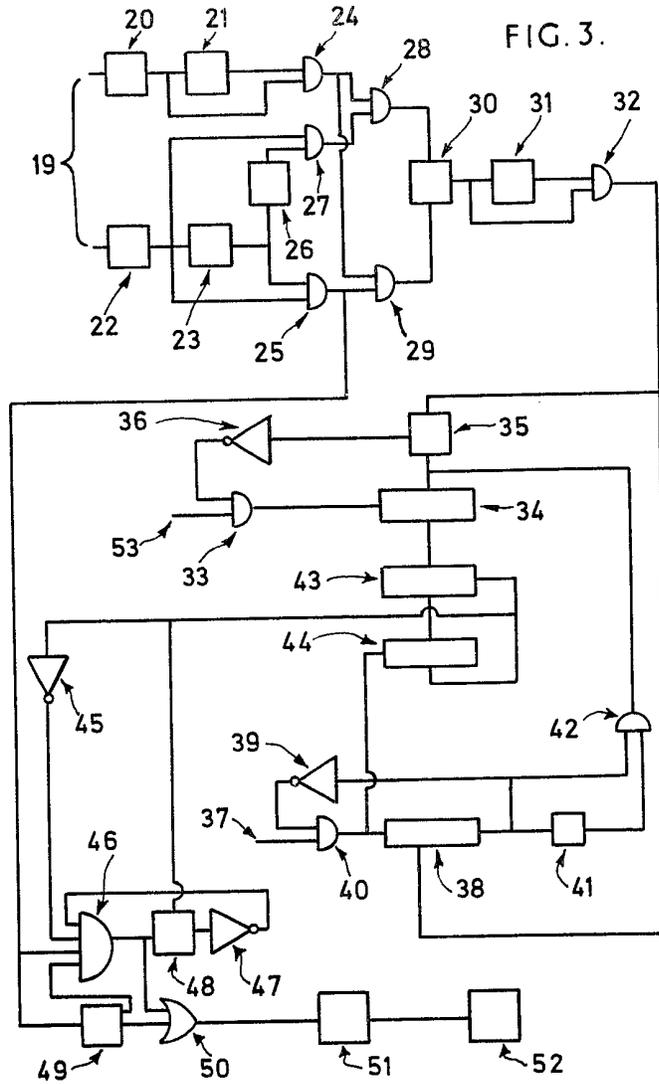


FIG. 2 .



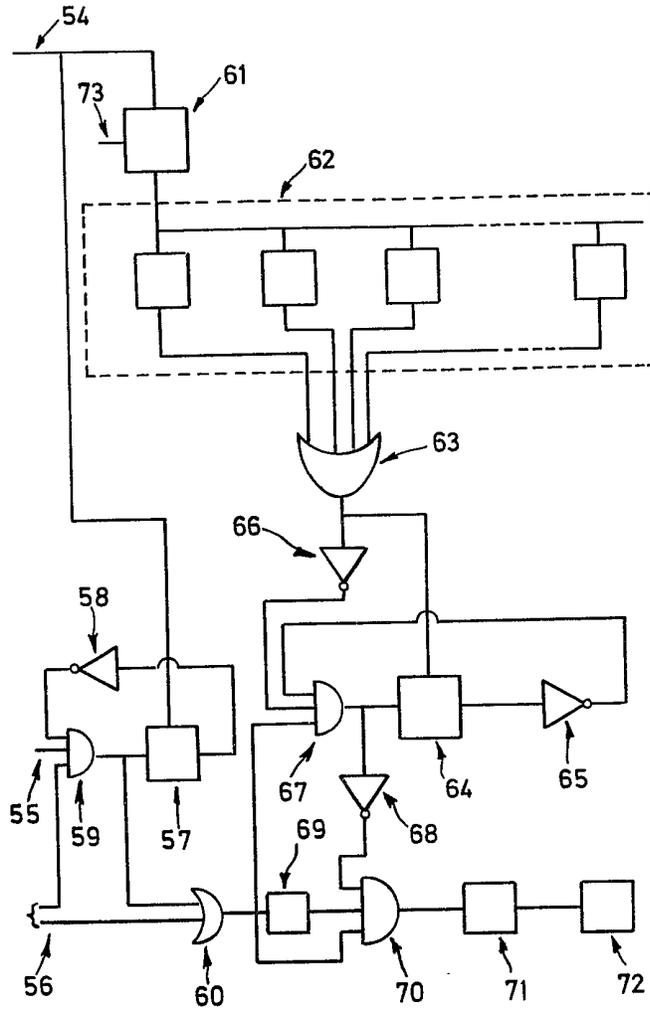


FIG. 4