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(54) **Title:** DISPLAY SUBSTRATE, PREPARATION METHOD THEREOF, AND DISPLAY PANEL COMPRISING DISPLAY SUBSTRATE

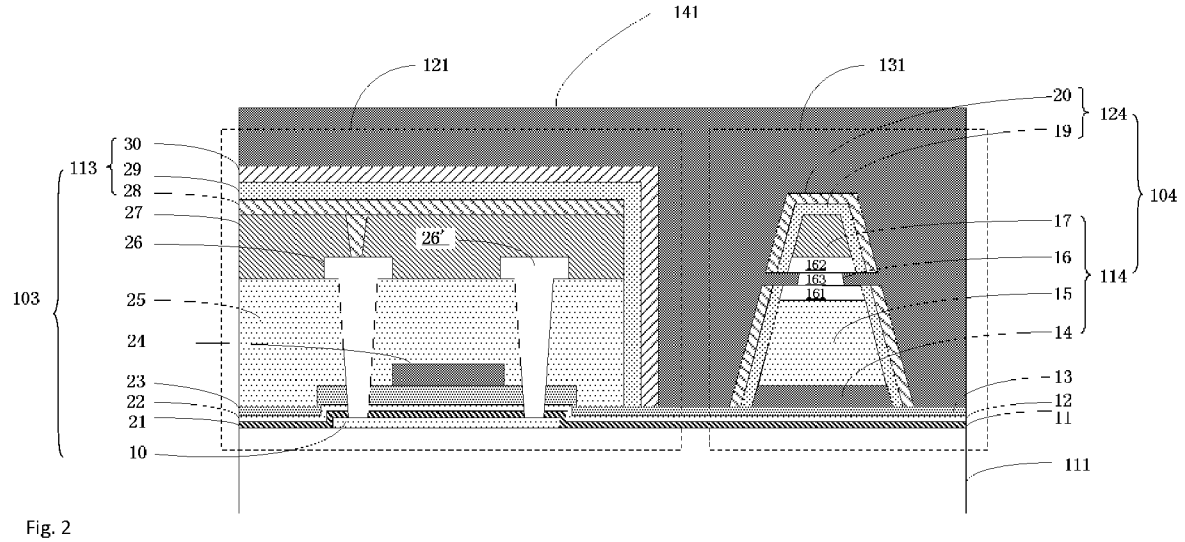


Fig. 2

(57) **Abstract:** Disclosed herein is a display substrate comprising: a support; a pixel on the support and with a thin-film transistor (TFT) therein; and a barrier on the support, surrounding the pixel, and separated from the pixel by a trench; wherein the barrier comprises a protrusion extending from the support and configured to retard invasion of moisture and oxygen into the pixel; wherein the protrusion comprises a layer coplanar with a layer of the TFT. Also disclosed herein are a display panel with this display substrate and a system with this display panel.

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DISPLAY SUBSTRATE, PREPARATION METHOD THEREOF, AND DISPLAY PANEL COMPRISING DISPLAY SUBSTRATE

Cross-Reference to Related Application

[1] This application claims priority to Chinese Patent Application No. 201811353169.X, filed on November 14, 2018, the contents of which are incorporated by reference in the entirety.

Technical Field

[2] The disclosure herein relates to the field of display technology, and more particularly to a display substrate, a preparation method thereof, and a display panel comprising the same.

Background

[3] With the development of the display technology, the organic light emitting diodes (OLEDs) display will gradually replace the liquid crystal displays (LCDs).

[4] With the development of the wearable technology, the stretchable OLED displays have become the future direction of development.

Summary

[5] Disclosed herein is a display substrate comprising: a support; a pixel on the support and with a thin-film transistor (TFT) therein; and a barrier on the support, surrounding the pixel, and separated from the pixel by a trench; wherein the barrier comprises a protrusion extending from the support and configured to retard invasion of moisture and oxygen into the pixel; wherein the protrusion comprises a layer coplanar with a layer of the TFT.

[6] According to an embodiment, the support comprises a plurality of islands and a plurality of bridges connecting the islands; wherein the pixel is on one of the islands.

[7] According to an embodiment, the barrier has a gap configured to accommodate wiring leading into the pixel from outside of the pixel.

[8] According to an embodiment, the protrusion comprises a layer of metal, a layer of dielectric, or any combination thereof.

[9] According to an embodiment, the barrier does not comprise any layer extending into the pixel.

[10] According to an embodiment, the protrusion comprises a recess into a sidewall of the protrusion.

[11] According to an embodiment, the recess is a volume defined by a first layer, a second layer and a third layer of the protrusion; wherein the second layer is sandwiched between the first layer and the third layer; wherein the first layer and the third layer extend to the sidewall but the second layer does not extend to the sidewall.

[12] According to an embodiment, the pixel and the barrier each comprise a layer of the same material.

[13] Disclosed herein is a display substrate comprising: a support; a pixel on the support and with a thin-film transistor (TFT) therein; and a barrier on the support and surrounding the pixel; wherein the barrier comprises a protrusion extending from the support and configured to retard invasion of moisture and oxygen into the pixel; wherein the protrusion comprises a recess into a sidewall of the protrusion; wherein the protrusion comprises a layer coplanar with a layer of the TFT.

[14] According to an embodiment, the support comprises a plurality of islands and a plurality of bridges connecting the islands; wherein the pixel is on one of the islands.

[15] According to an embodiment, the barrier has a gap configured to accommodate wiring leading into the pixel from outside of the pixel.

[16] According to an embodiment, the protrusion comprises a layer of metal, a layer of dielectric, or any combination thereof.

[17] According to an embodiment, the barrier does not comprise any layer extending into the pixel.

[18] According to an embodiment, the recess is a volume defined by a first layer, a second layer and a third layer of the protrusion; wherein the second layer is sandwiched between the first layer and the third layer; wherein the first layer and the third layer extend to the sidewall but the second layer does not extend to the sidewall.

[19] According to an embodiment, the pixel and the barrier each comprise a layer of the same material.

[20] Disclosed herein is a display panel, comprising any of the display substrates above, and an encapsulation layer over the pixel and the barrier.

[21] According to an embodiment, the display panel further comprises a coating at least partially covering the protrusion.

[22] According to an embodiment, the coating comprises a discontinuity separating two discontinuous portions of the coating.

[23] According to an embodiment, the discontinuity extends along an entire length of the barrier.

[24] Disclosed herein is a system comprising the display panel above, wherein the system is an e-book reader, a laptop computer, a computer monitor, an OLED panel, a mobile phone, a tablet computer, a television, a display screen, a digital photo frame, or a portable GPS system.

[25] Disclosed herein is a method of making a display substrate of a display panel, the method comprising: forming a barrier on a support; wherein the barrier surrounds a pixel on the support; wherein the barrier comprises a protrusion extending from the support and configured to retard invasion of moisture and oxygen into the pixel.

[26] According to an embodiment, the method further comprises forming an encapsulation layer over the pixel and the barrier.

[27] According to an embodiment, forming the barrier comprises forming a coating on the protrusion.

[28] According to an embodiment, forming the barrier comprises forming a recess into a sidewall of the protrusion.

[29] According to an embodiment, the pixel comprises a light emitter and a thin-film transistor (TFT); wherein forming the barrier comprises forming a layer of the barrier and a layer of the light emitter or of the TFT by depositing the same material and at the same time.

[30] According to an embodiment, the method further comprises disconnecting the layer of the barrier and the layer of the light emitter or of the TFT.

Brief Description of Figures

[31] FIG. 1A is a top view of a display substrate according to an embodiment of the disclosure;

[32] FIG. 1B is a sectional view of an island according to an embodiment of the disclosure;

[33] FIG. 1C is a top view of a barrier in an island according to an embodiment of the disclosure;

[34] FIG. 2 is a sectional view of an island in another embodiment of the disclosure;

[35] FIG. 3 is a flow chart of a method of forming an island of a display substrate of a display panel according to an embodiment of the disclosure; and

[36] FIGS. 4A- FIG. 4I show the structures obtained at each stage of forming a barrier according to embodiments of the disclosure.

Detailed Description

[37] In this disclosure, when a part is described as being between a first part and a second part, there may be or may not be an intermediate part between the part and the first or second part. When a part is described to be connected to another part, the part may be directly connected to the other part without an intermediate part, or may be indirectly connected to the other part with an intermediate part.

[38] Stretchable OLED displays tend to exhibit relatively poor display quality because moisture and oxygen invasion into the luminescent layer has a negative impact on the performance of the luminescent layer.

[39] FIG. 1A is a top view of a display substrate according to an embodiment of the disclosure. FIG. 1B is a sectional view of an island according to an embodiment of the disclosure. Specifically, FIG. 1B is a sectional view taken from line B-B' in FIG. 1A.

[40] As shown in FIG. 1A, the display substrate 100 comprises a plurality of islands 101 and a plurality of bridges 102 connecting the islands 101. The bridges 102 are used for wiring, and the arrangement of the bridges 102 enables the display substrate 100 to be stretchable. At least one of the plurality of islands 101 in the display substrate 100 may be the island 101 shown in FIG. 1B.

[41] As shown in FIG. 1B, the island 101 comprises a support 111 (for example, a flexible support of polyimide), a pixel area 121 on the support 111, and a barrier area 131 on the support 111 and surrounding the pixel area 121. FIG. 1B shows only a partial section of the barrier area 131. The pixel area 121 comprises at least one pixel 103, and the barrier area 131 comprises a barrier 104. The island 101 further comprises an encapsulation layer 141 over the pixel 103 and the barrier 104. For example, the encapsulation layer 141 may comprise alternating organic and inorganic layers. The encapsulation layer 141 may also fills the trench between the pixel 103 and the barrier 104.

[42] Optionally, the distance between the edge of the pixel area 121 and the edge of the island 101 can be 10 microns to 50 microns, such as 20 microns, 40 microns, etc.

[43] FIG. 1C is a top view of a barrier in the island according to an embodiment of the disclosure.

[44] As shown in FIG. 1C, in certain embodiments, the barrier 104 has a gap V for wiring into the pixel 103 and the gap may be arranged at the joints of the bridge 102 and the barrier 104. Optionally, the distance between the barrier 104 and the pixel area 121 can be 1 micron to 5 microns, such as 2 microns, 4 microns, etc. As an example, the distance between

the barrier 104 and the edge of the island 101 can be 3 microns to 15 microns, such as 5 microns, 10 microns, etc.

[45] In an embodiment, at least one island comprises a barrier surrounding the pixel area. The barrier can retard the invasion of the moisture and oxygen around the island into the pixel area, so as to reduce the adverse effect on the performance of the pixel in the pixel area, and thus improve the display quality of the display panel.

[46] In certain embodiments, as shown in FIG. 1B, the barrier 104 comprises a barrier body 114 and a coating 124 covering the barrier body 114. The barrier body 114 is a protrusion extending from the support 111. A lamination can be disposed between the barrier 104 and the support 111. For example, the lamination comprises a first dielectric layer 11, a metal layer 12, and a second dielectric layer 13 stacked sequentially in the direction away from the support 111. The first and second dielectric layers 11 and 13 may comprise silicon oxide layers (e.g. SiO_2), silicon nitride layers (e.g. SiN_x), or a lamination of silicon oxide layers and silicon nitride layers, with a thickness of 1000-5000 angstroms, e.g., 2000 angstroms, 3000 angstroms, etc.

[47] The barrier body 114 and the coating 124 are detailed as follows.

[48] In certain embodiments, in the direction away from the support 111 (that is, from bottom to top), the barrier body 114 comprises one or more of a first metal layer 14, a first insulation interlayer 15, a second metal layer 16, and a first flattening layer 17 superimposed sequentially. For example, in an embodiment, the barrier body 114 comprises a first metal layer 14, a first insulation interlayer 15, and a first flattening layer 17 superimposed from bottom to up. In another embodiment, the barrier body 114 comprises a first metal layer 14 and a second metal layer 16 superimposed from bottom to up. Optionally, the first metal layer 14 comprises Mo, Al, Ti or Cu layers with thickness ranging from 1000 angstroms to 5000 angstroms, such as 2000 angstroms, 4000 angstroms, etc. As an example, the materials of the first flattening layer 17 may include an organic material such as resins.

[49] In certain embodiments, in the direction away from the support 111 (that is, from bottom to top), the coating 124 comprises one or more of a first electrode layer 18, a first luminescent layer 19 and a second electrode layer 20 sequentially covering the barrier body 114. The coating 124 may cover the upper surface of the uppermost layer of the barrier body 114 and the sides of each layer of the barrier body 114.

[50] As an example, the first electrode layer 18 can be used as the material for OLED anode, such as a laminated layer comprising indium tin oxide (ITO) /Ag/ITO, the thickness of which can be 1000-5000 angstroms, for example, 2000 angstroms, 3000 angstroms, 4000

angstroms and so on. For example, the first luminescent layer 19 may comprise an organic luminescent material layer, and the first luminescent layer 19 may also comprise one or more of an electron transport layer, a hole transport layer, an electron injection layer, and a hole injection layer. The second electrode layer 20 can be used for OLED cathode materials, such as Mg-Ag alloy.

[51] In certain embodiments, as shown in FIG. 1B, the pixel 103 comprises a light emitter 113. The light emitter 113 comprises a third electrode layer 28 on one side of the support 111, a second luminescence layer 29 on one side of the third electrode layer 28 away from the support 111, and a fourth electrode layer 30 on one side of the second luminescence layer 29 away from the third electrode layer 28. The fourth electrode layer 30 in the pixel 103 is separated from the second electrode layer 20 in the barrier 104. Such a structure can better block the moisture and oxygen around the island 101 from entering the pixel area 121 through the second electrode layer 20, thus reducing the adverse effects on the performance of the pixel 103 and improving the display quality of the display panel.

[52] In certain embodiments, the second luminescence layer 29 can be separated from the first luminescence layer 19, and the third electrode layer 28 can be separated from the first electrode layer 18.

[53] In certain embodiments, the two layers of at least one of the following three groups are prepared using the same composition process: the third electrode layer 28 and the first electrode layer 18, the second luminescence layer 29 and the first luminescence layer 19, the fourth electrode layer 30 and the second electrode layer 20. For example, the third electrode layer 28 and the first electrode layer 18 are formed by patterning the same material layer using the same composition process.

[54] In certain embodiments, as shown in FIG. 1B, the pixel 103 comprises an active layer 10 on one side of the support 111, a gate layer 24 on one side of the active layer 10 away from the support 111, a second insulation interlayer 25 on one side of the gate layer 24 away from the active layer 10, a source 26 and a drain 26' running through the second insulation interlayer 25 and connected to the active layer 10, and a second flattening layer 27 on one side of the second insulation interlayer 25 away from the gate layer 24. In certain embodiments, the two layers of at least one of the following three groups are prepared using the same composition process: the first metal layer 14 and the gate layer 24, the first insulation interlayer 15 and the second insulation interlayer 25, the second metal layer 16 and source 26, the first flattening layer 17 and the second flattening layer 27.

[55] Furthermore, the pixel 103 may also comprise a dielectric layer 21, a metal layer 22, and a dielectric layer 23 stacked from bottom to top between the active layer 10 and the gate layer 24, respectively.

[56] Some layers in the pixel 103 constitute driving transistors, storage capacitors and other components in the pixel 103. For example, the drive transistors comprise an active layer 10, a dielectric layer 21 (as gate dielectric layer), a gate layer 24, a source 26 and a drain 26'. For example, the storage capacitors comprise a metal layer 22, a dielectric layer 23 and a gate layer 24.

[57] FIG. 2 is a sectional view of the island in another embodiment of the disclosure. The differences between FIG. 2 and FIG. 1 are described below. Other relevant points can refer to the above descriptions.

[58] As shown in FIG. 2, the barrier body 114 comprises a second metal layer 16. The second metal layer 16 comprises a first layer 161, a second layer 162, and a third layer 163 located between the first layer 161 and the second layer 162. The first layer 161 and the second layer 162 may be a Ti layer, and the third layer 163 may be an Al layer.

[59] The projections of the first layer 161, the second layer 162 and the third layer 163 on the support 111 are a first projection, a second projection and a third projection, respectively. Here, the first projection and the second projection cover the third projection, and the area of the first projection and the second projection is larger than the area of the third projection. In other words, at least one side of the third layer 163 is closer to the center of the third layer 163 than the side of the first layer 161 and the second layer 162. Namely, the barrier body 114 has a recess into the sidewall of the barrier body 114. The coating 142 thus may have a discontinuity at the recess, the discontinuity separating two discontinuous portions of the coating 142. The discontinuity may extend along an entire length of the barrier 104.

[60] Furthermore, as shown in FIG. 2, the coating 124 comprises the first luminescent layer 19 covering the barrier body 114 and the second electrode layer 20 covering the first luminescent layer 19, excluding the first electrode layer 18.

[61] Suppose the part of the barrier body 114 located on the side of the third layer 163 away from the support 111 is a first part, and the part of the barrier body 114 located on the side of third layer 163 close to the support 111 is a second part. The area of the second electrode layer 20 covering the first part is spaced from the area covering at least one side of the second part.

[62] Herein, the area of the second electrode layer 20 covering the second part comprises two areas covering two sides of the second part (that is, the left and right areas below the third layer 163). The area of the second electrode layer 20 covering the first part is spaced from at least one of the two areas. FIG. 2 shows the area of the second electrode layer 20 covering the first part is spaced from both the two areas.

[63] In aforesaid embodiments, the second electrode layer 20 in the barrier is discontinuous, and is divided into several separated areas, thus blocking the travel path of the moisture and oxygen. Even if the moisture and oxygen around the island enter the second electrode layer 20, it is difficult for the moisture and oxygen to enter the pixel 103 of the pixel area 121 through the second electrode layer 20. Such a structure can further improve the display quality of the display panel.

[64] The disclosure also provides a method of preparing the display substrate. The method comprises forming a plurality of islands connected by bridges. At least one island can be formed according to the flow chat shown in FIG. 3.

[65] FIG. 3 is a flow chart of a method of forming an island of a display substrate of a display panel according to an embodiment of the disclosure.

[66] In 302, providing a support, for example, a flexible support.

[67] In 304, forming a pixel area on the support, and a barrier area on the support and surrounding the pixel area. The pixel area comprises a pixel, and the barrier area comprises a barrier surrounding the pixel area.

[68] In certain embodiments, different processes can be used to form the pixels and the barriers. For example, a second pixel and barrier can be formed following the formation of the first pixel and barrier.

[69] In certain embodiments, the barrier may be formed in the process of forming a pixel.

[70] In 306, forming an encapsulation layer over the pixel and the barrier.

[71] In an embodiment, the island comprises a barrier surrounding the pixel area. The barrier can retard the invasion of the moisture and oxygen around the island into the pixel area, so as to reduce the adverse effect on the performance of the pixel in the pixel area, and thus improve the display quality of the display panel.

[72] The following describes the process of forming barriers in accordance with certain embodiments of the disclosure.

[73] First, forming a barrier body. The barrier body comprises, in the direction away from the support, one or more of a first metal layer, a first insulation interlayer, a second metal layer, and a first flattening layer superimposed sequentially.

[74] In certain embodiments of the disclosure, the projection areas of the first metal layer, the first insulation interlayer, the second metal layer, and the first flattening layer on the support increases gradually. For example, the barrier body is trapezoid. For example, the angle between the side of the trapezoid and the surface of the support is less than 70 degrees, such as 65 degrees, 60 degrees, 50 degrees, etc. Such a structure is conducive to the formation of the lamination.

[75] Second, forming a coating. The coating comprises, in the direction away from the support, one or more of a first electrode layer, a first luminescent layer and a second electrode layer sequentially covering the barrier body.

[76] In certain embodiments of the disclosure, the coating is formed as follows: in the direction away from the support, sequentially forming the first electrode layer, the first luminescent layer and the second electrode layer covering the barrier body.

[77] In certain embodiments of the disclosure, the second metal layer comprises a first layer, a second layer, and a third layer located between the first layer and the second layer. In this case, the coating is formed as follows: forming the first electrode layer covering the surface of the barrier body; performing an etching process to remove the first electrode layer and an exposed part of the third layer; and forming the first luminescent layer covering the surface of the barrier body and the second electrode layer covering the first luminescent layer. Herein, the part of the barrier body located on the side of the third layer away from the barrier area is a first part, and the part of the barrier body located on the side of third layer close to the barrier area is a second part. The area of the second electrode layer covering the first part is spaced from the area covering at least one side of the second part.

[78] FIG. 4A- FIG. 4I show the structures obtained at each stage of forming a barrier according to embodiments of the disclosure.

[79] First, as shown in FIG. 4A, forming an active layer 10 configured to drive the transistors on the support 111, for example, polycrystalline silicon layer or amorphous silicon layer or the like.

[80] In certain embodiments, a buffer layer may be formed on the support 111 prior to the formation of the active layer 10, for example, a lamination of a silicon oxide layer and a silicon nitride layer.

[81] Second, as shown in FIG. 4B, sequentially forming a first dielectric material layer, a first metal material layer and a second dielectric material layer on the support 111.

[82] The first dielectric material layer, the first metal material layer and the second dielectric material layer in the barrier area 131 are the first dielectric layer 11, the metal layer 12, and the second dielectric layer 13, respectively. The first dielectric material layer, the first metal material layer and the second dielectric material layer in the pixel area 121 are the dielectric layer 21, the metal layer 22, and the dielectric layer 23, respectively.

[83] Further, as shown in FIG. 4C, forming a first metal layer on the second dielectric layer 13 and a gate layer 24 on the dielectric layer 23. Here the metal layer 22, the dielectric layer 23 and the gate layer 24 constitute a storage capacitor.

[84] For example, a second metal material layer, such as Mo, Al, Ti or Cu, can be deposited on the structure shown in FIG. 4B. And then, the deposited second metal material layer is patterned to yield the first metal layer 14 and the gate layer 24.

[85] As shown in FIG. 4D, forming a first insulation interlayer 15 on the first metal layer 14 and the second insulation interlayer 25 with an opening 251 extending to the active layer 10.

[86] For example, the insulation material layer can be deposited on the structure shown in FIG. 4C, and the deposited insulation material layer can be patterned to obtain the first insulation interlayer 15 and the second insulation interlayer 25. The insulation material layer may include, for example, a lamination comprising a silicon nitride layer and a silicon oxide layer.

[87] As shown in FIG. 4E, forming, on the first insulation interlayer 15, a second metal layer 16, and a source 26 and a drain 26' configure to fill the opening 251.

[88] For example, a third metal material layer can be deposited on the structure shown in FIG. 4D, and the deposited third metal material layer can be patterned to obtain the second metal layer 16, the source 26 and the drain 26'. The third metal material layer can include Ti/Al/Ti lamination, etc.

[89] As shown in FIG. 4F, forming a first flattening layer 17 on the second metal layer 16 and a second flattening layer 27 on the second insulation interlayer 25. The second flattening layer 27 comprises an opening 271 extending to the source 26 and the drain 26'.

[90] For example, a flattening material layer can be deposited on the structure shown in Fig. 4F and patterned to obtain the first flattening layer 17 and the second flattening layer 27. The flattening material layer may include, for example, a resin material layer.

[91] To facilitate the subsequent description, the lamination comprising the first metal layer 14, the first insulation interlayer 15, the second metal layer 16 and the first flattening layer 17 is called a barrier body 114.

[92] As shown in FIG. 4G, forming a first electrode layer 18 covering the surface of the barrier body 114 and a third electrode layer 28 on the first flattening layer 17.

[93] In certain embodiments, the third electrode layer 28 can fill the opening 271. In other embodiments, the opening 271 can be filled with a conductive material to form a connector connected to a source 26 or drain 26'.

[94] As shown in FIG. 4H, forming a first luminescent layer 19 covering the first electrode layer 18 and the second luminescent layer 29 covering the third electrode layer 28. In certain embodiments, the first luminescent layer 19 can be separated from the second luminescent layer 29.

[95] For example, a luminescent material layer can be deposited on the structure shown in FIG. 4G, and then the luminescent material layer is patterned to form the first luminescent layer 19 and the second luminescent layer 29 which are spaced apart. For example, by controlling the distance between the barrier body 114 and the pixel area, the deposited luminescent material layer can automatically crack into the first luminescent layer 19 and the second luminescent layer 29 when the luminescent material layer is deposited on the structure shown in FIG. 4G.

[96] As shown in FIG. 4I, forming a second electrode layer 20 covering the first luminescent layer 19 and a fourth electrode layer 30 covering the second luminescent layer 29.

[97] Here, the lamination comprising the first electrode layer 18, the first luminescent layer 19 and the second electrode layer 20 is called a coating 124.

[98] The barrier 104 can be obtained by the processes shown in FIG. 4A- FIG. 4I. In the process of forming the pixel 103, the barrier 104 can be formed at the same time, which simplifies the operation and saves the cost.

[99] The manufacturing process of the above barrier is only one example and is not intended to limit the disclosure.

[100] The disclosure also provides a display system which comprises a display panel of any of the above-mentioned embodiments. In certain embodiments, the system may comprise, for example, a product or component with display function such as a mobile terminal, a television, a display screen, a tablet computer, a digital photo frame, a portable GPS, an electronic paper, etc.

[101] While various aspects and embodiments have been disclosed herein, other aspects and embodiments will be apparent to those skilled in the art. The various aspects and embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

What is claimed is:

1. A display substrate, comprising:

a support;

a pixel on the support and with a thin-film transistor (TFT) therein; and

a barrier on the support, surrounding the pixel, and separated from the pixel by a trench;

wherein the barrier comprises a protrusion extending from the support and configured to retard invasion of moisture and oxygen into the pixel;

wherein the protrusion comprises a layer coplanar with a layer of the TFT.

2. The display substrate of claim 1,

wherein the support comprises a plurality of islands and a plurality of bridges connecting the islands;

wherein the pixel is on one of the islands.

3. The display substrate of any one of claims 1-2, wherein the barrier has a gap configured to accommodate wiring leading into the pixel from outside of the pixel.

4. The display substrate of any one of claims 1-3, wherein the protrusion comprises a layer of metal, a layer of dielectric, or any combination thereof.

5. The display substrate of any one of claims 1-4, wherein the barrier does not comprise any layer extending into the pixel.

6. The display substrate of any one of claims 1-5, wherein the protrusion comprises a recess into a sidewall of the protrusion.

7. The display substrate of claim 6, wherein the recess is a volume defined by a first layer, a second layer and a third layer of the protrusion; wherein the second layer is sandwiched between the first layer and the third layer; wherein the first layer and the third layer extend to the sidewall but the second layer does not extend to the sidewall.

8. The display substrate of any one of claims 1-7, wherein the pixel and the barrier each comprise a layer of the same material.

9. A display substrate comprising:

a support;

a pixel on the support and with a thin-film transistor (TFT) therein; and

a barrier on the support and surrounding the pixel;

wherein the barrier comprises a protrusion extending from the support and configured to retard invasion of moisture and oxygen into the pixel;

wherein the protrusion comprises a recess into a sidewall of the protrusion;

wherein the protrusion comprises a layer coplanar with a layer of the TFT.

10. The display substrate of claim 9,

wherein the support comprises a plurality of islands and a plurality of bridges connecting the islands;

wherein the pixel is on one of the islands.

11. The display substrate of any one of claims 9-10, wherein the barrier has a gap configured to accommodate wiring leading into the pixel from outside of the pixel.

12. The display substrate of any one of claims 9-11, wherein the protrusion comprises a layer of metal, a layer of dielectric, or any combination thereof.

13. The display substrate of any one of claims 9-12, wherein the barrier does not comprise any layer extending into the pixel.

14. The display substrate of any one of claims 9-13, wherein the recess is a volume defined by a first layer, a second layer and a third layer of the protrusion; wherein the second layer is sandwiched between the first layer and the third layer; wherein the first layer and the third layer extend to the sidewall but the second layer does not extend to the sidewall.

15. The display substrate of any one of claims 9-14, wherein the pixel and the barrier each comprise a layer of the same material.

16. A display panel, comprising the display substrate of any one of claims 1-15, and an encapsulation layer over the pixel and the barrier.

17. The display panel of claim 16, further comprising a coating at least partially covering the protrusion.

18. The display panel of claim 17, wherein the coating comprises a discontinuity separating two discontinuous portions of the coating.

19. The display panel of claim 18, wherein the discontinuity extends along an entire length of the barrier.

20. A system comprising the display panel of any one of claims 16-19, wherein the system is an e-book reader, a laptop computer, a computer monitor, an OLED panel, a mobile phone, a tablet computer, a television, a display screen, a digital photo frame, or a portable GPS system.

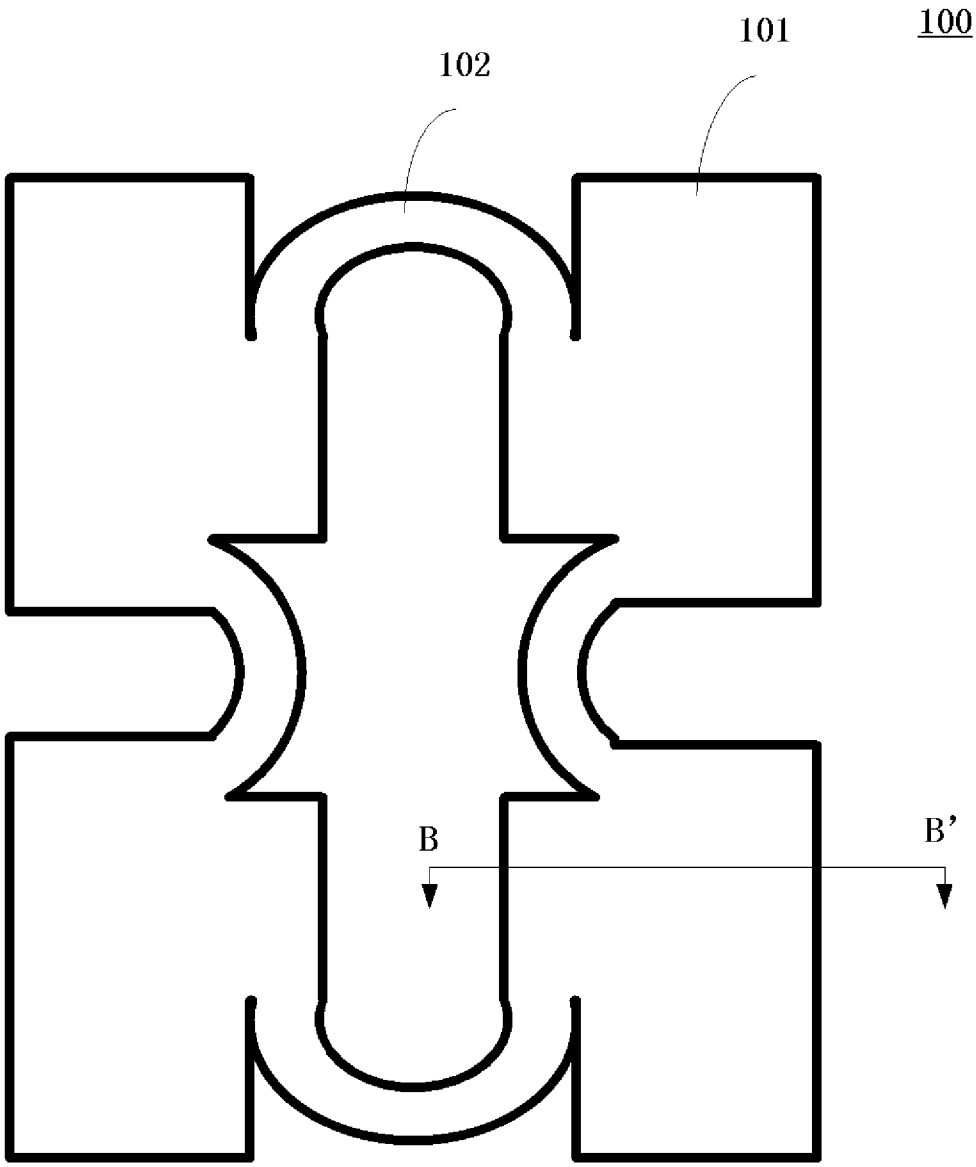


Fig. 1A

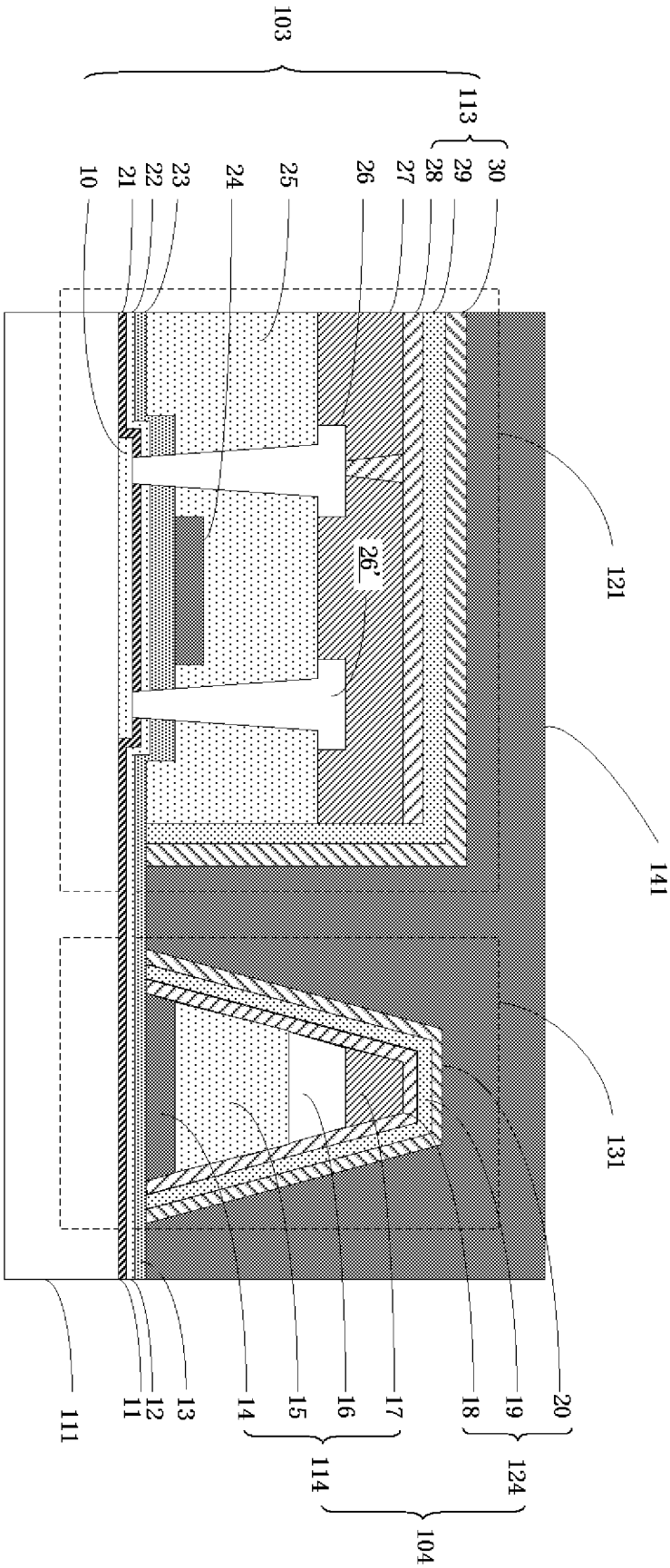

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Fig. 1B

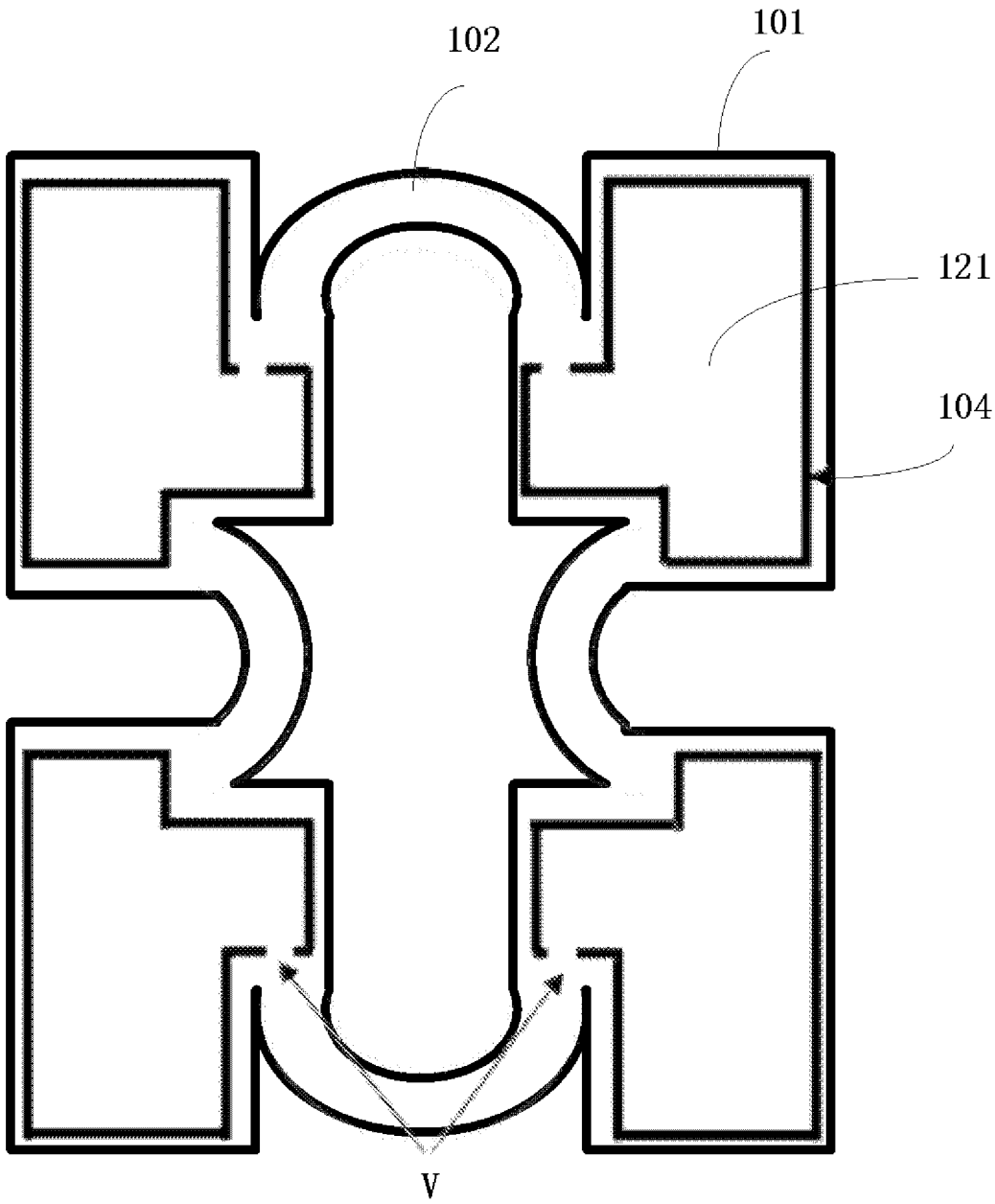


Fig. 1C

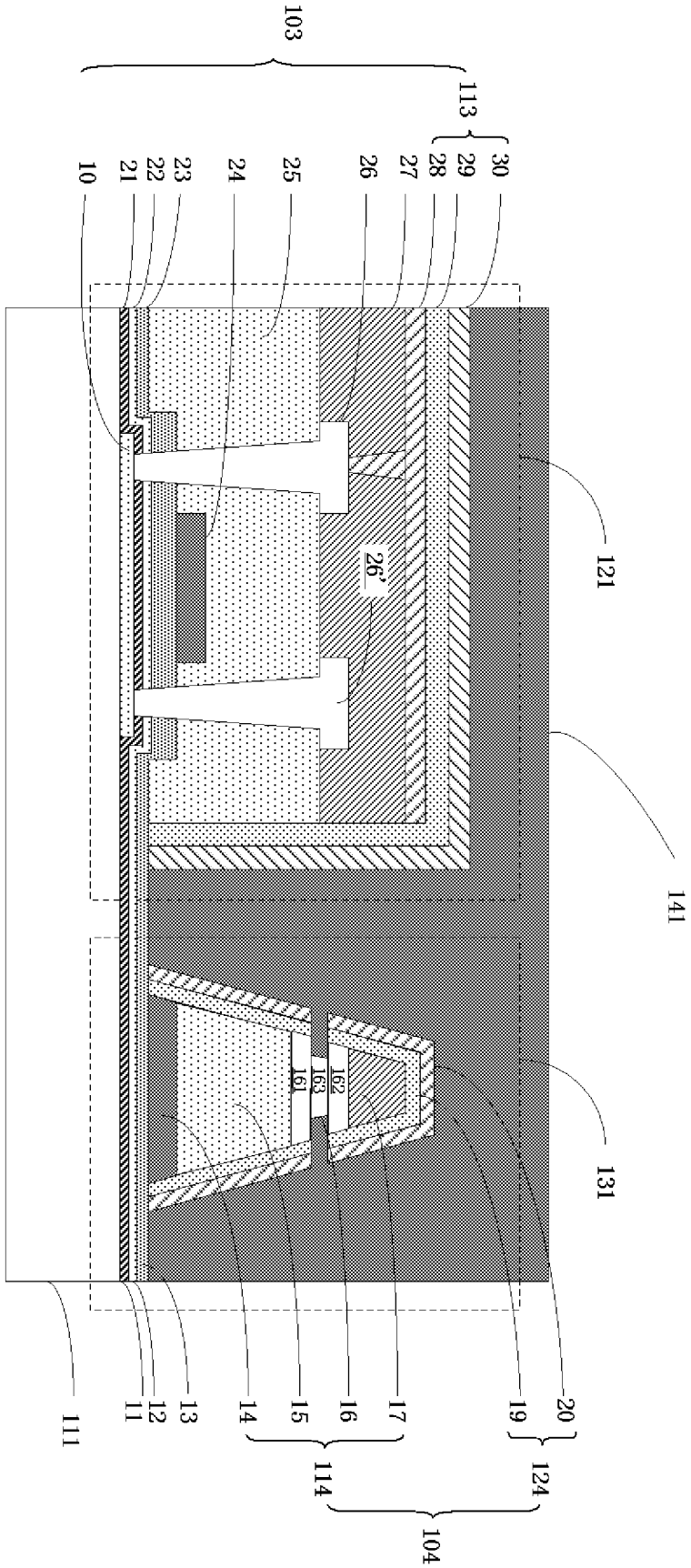

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Fig. 2

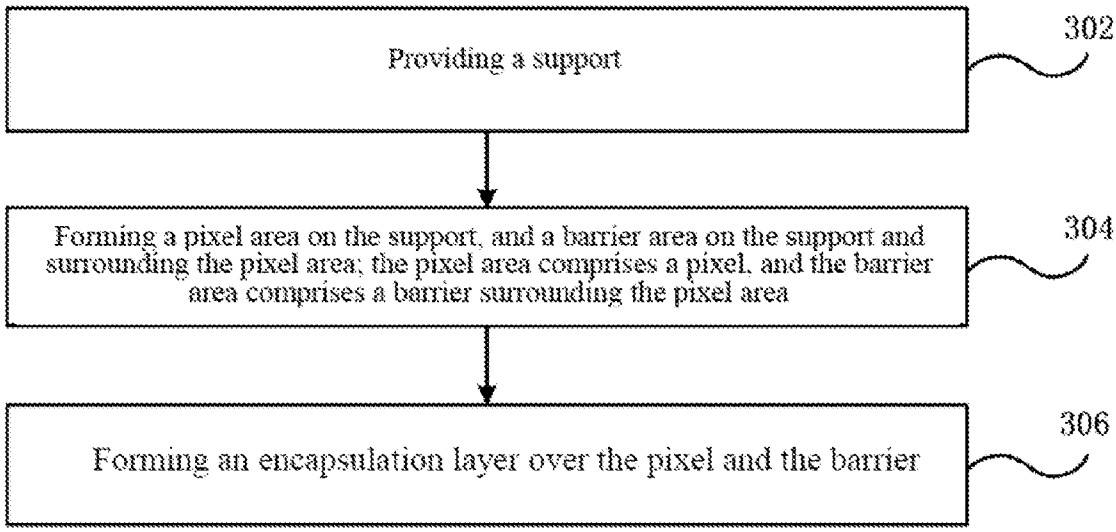


Fig. 3



Fig. 4A

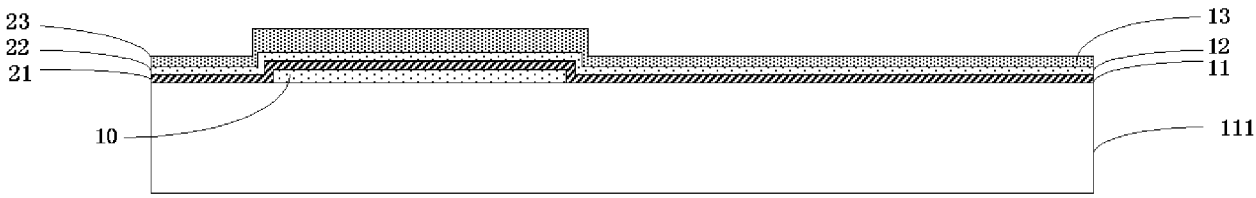


Fig. 4B

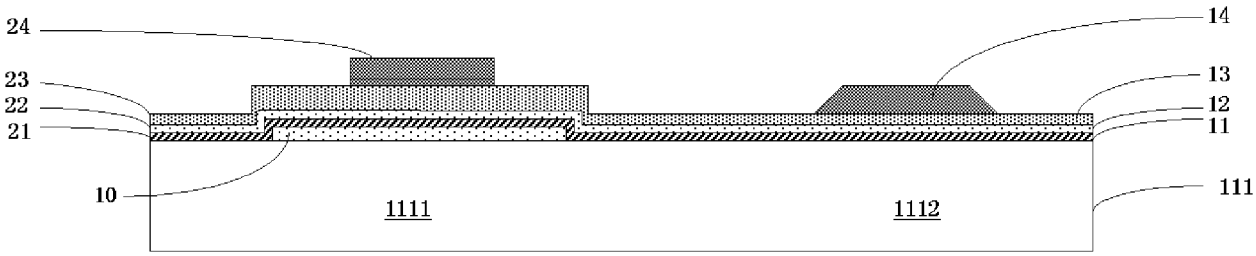


Fig. 4C

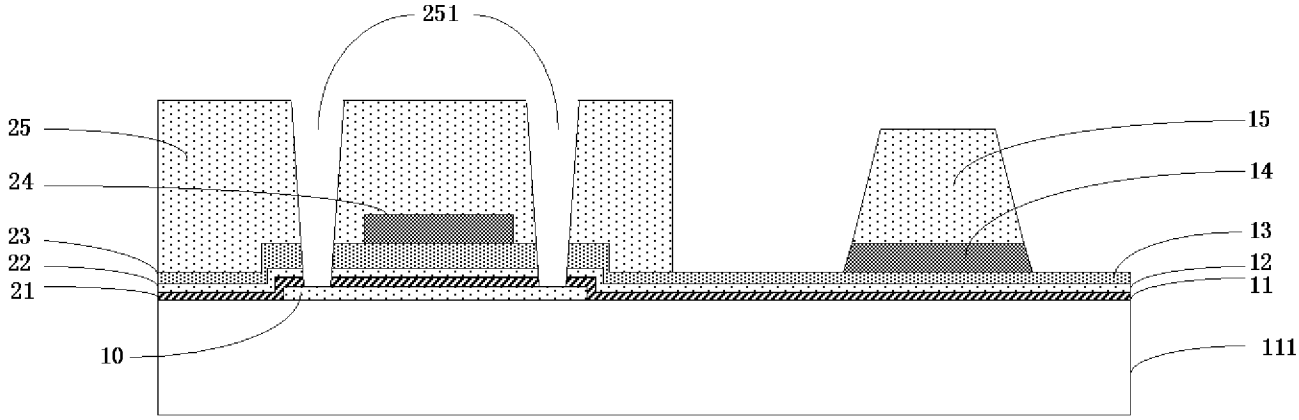


Fig. 4D

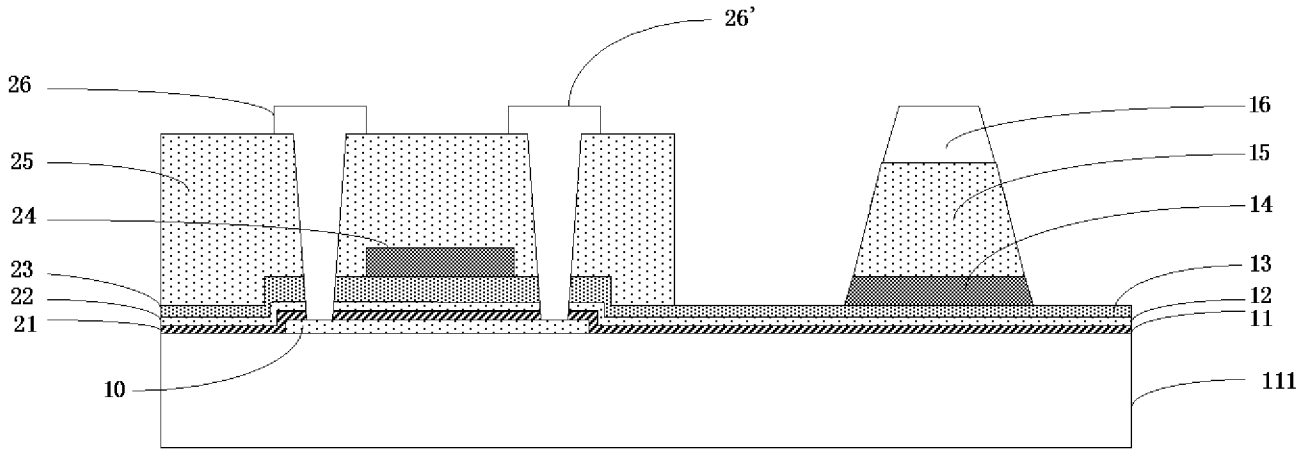


Fig. 4E

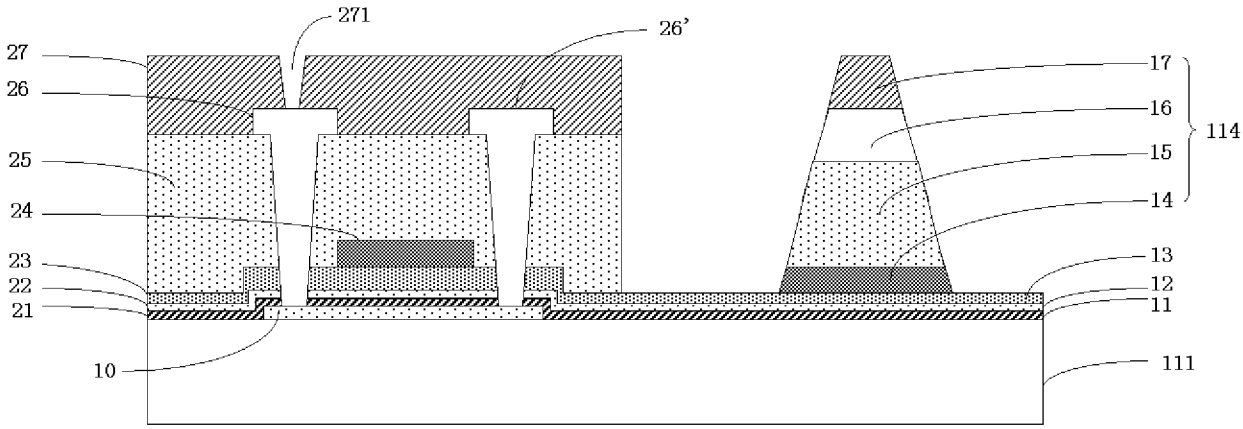


Fig. 4F

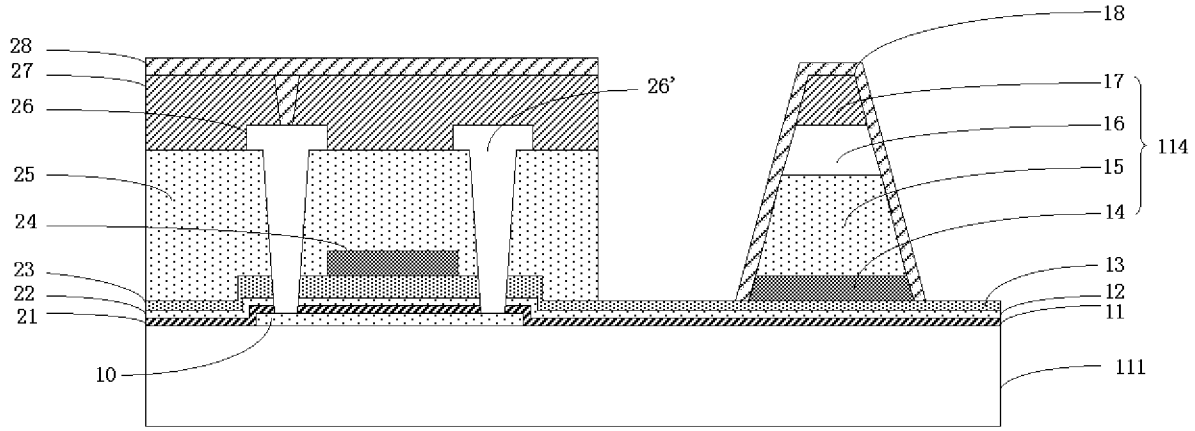


Fig. 4G

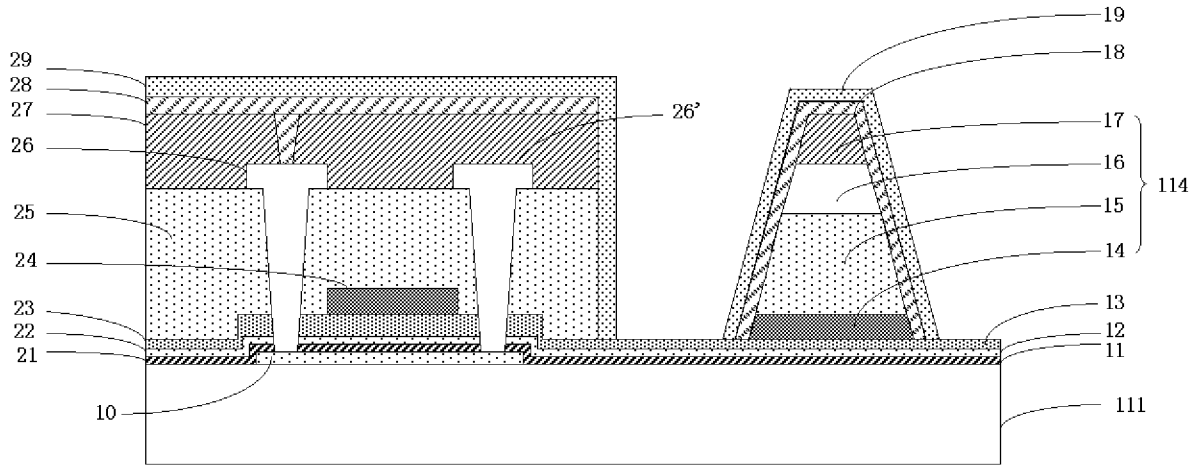


Fig. 4H

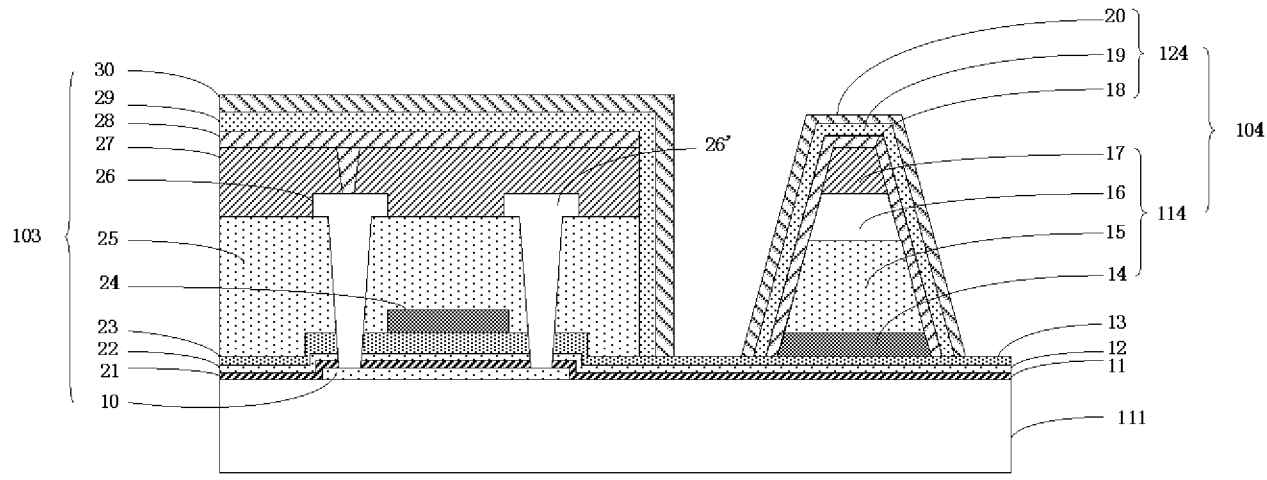


Fig. 4I

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/081006

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, IEEE, CNPAT, CNKI:display, substrat+, panel, support, pixel, TFT, thin film transistor, barrier, trench, protrusion, moistur +, oxygen, coplanar, island, bridg+, gap, metal, dielectric, recess, sidewall

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 108777258 A (SHANGHAI TIANMA MICROELECTRONICS CO., LTD.) 09 November 2018 (2018-11-09) description, paragraphs [0042]-[0088] and figures 1-2, 5-19	1, 4-5, 8, 16-17, 20
Y	CN 108777258 A (SHANGHAI TIANMA MICROELECTRONICS CO., LTD.) 09 November 2018 (2018-11-09) description, paragraphs [0042]-[0088] and figures 1-2, 5-19	2
Y	CN 108511621 A (BOE TECHNOLOGY GROUP CO., LTD.) 07 September 2018 (2018-09-07) description, paragraphs [0047]-[0048] and figures 2(a)-2(d)	2
X	CN 105390525 A (SAMSUNG DISPLAY CO., LTD.) 09 March 2016 (2016-03-09) description, paragraphs [0221]-[0403] and figures 24-28	1, 4-5, 8, 16-17, 20
A	CN 107026244 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 08 August 2017 (2017-08-08) the whole document	1-20
A	US 2002185967 A1 (FRIEND, RICHARD HENRY) 12 December 2002 (2002-12-12) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01 August 2019	**12 August 2019**

Name and mailing address of the ISA/CN	Authorized officer
National Intellectual Property Administration, PRC **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing** **100088** **China**	**WANG,Guangjun**
Facsimile No. **(86-10)62019451**	Telephone No. **86-(10)-53961225**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2019/081006

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	108777258	A	09 November 2018	None			
CN	108511621	A	07 September 2018	None			
CN	105390525	A	09 March 2016	US	2016064691	A1	03 March 2016
				KR	101667800	B1	20 October 2016
				EP	2991130	A1	02 March 2016
				KR	20160027489	A	10 March 2016
				US	10319944	B2	11 June 2019
				KR	101789238	B1	21 November 2017
				KR	20160123270	A	25 October 2016
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				JP	2017134402	A	03 August 2017
US	2002185967	A1	12 December 2002	US	6580212	B2	17 June 2003
				WO	9912398	A1	11 March 1999
				GB	9718516	D0	05 November 1997