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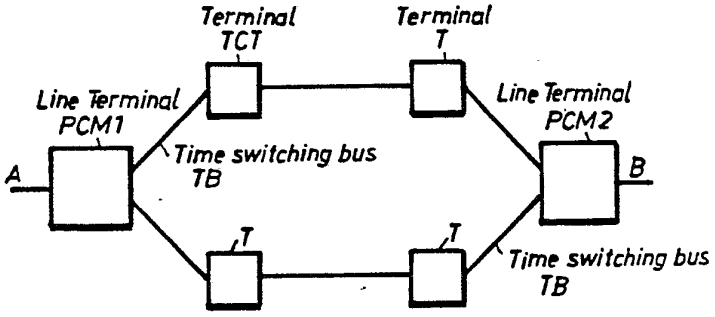
(54) Title: METHOD AND APPARATUS FOR THROUGH-CONNECTION TESTING IN A DIGITAL TELECOMMUNICATION NETWORK

(57) Abstract



Method and apparatus in duplex transmission of digital information between subscribers connected to terminals associated with each other in a telecommunication network of the time multiplex type in which information is transmitted in the form of binary words in specially assigned time slots, of carrying out with the aid of parity check, during traffic in progress, through-connection testing for checking that a correct connection has been set up after a switching path has been established. The through-connection check is started and detected in the same station (terminal). After detected correct parity, which is done with the aid of a parity check means (M1) and a comparison circuit (OR), there is generated a parity bit with intentional incorrect polarity for sending on the line towards the next station. Generation of desired parity is done with the aid of an apparatus including a local processor (MP), a control memory (CM), a counter (TR) and said comparison circuit. All stations along a switching path are of equal value and contain the same means. A central processor assigns one of the stations (TCT), at the setting up of a connection, to be the control station for the through-connection test. The control bit with intentionally incorrect parity is switched straight through remaining switching points and is looped in the line terminal (PCM2) where information from the B subscriber is received. The loop connection is carried out with the aid of a parity check circuit (M2) for extracting the parity bit from the terminal side, and a further parity check circuit (M3) for the loop formation itself and feeding out the parity bit back towards the TCT station. A check is made in the latter that it is the intentionally erroneous parity bit which is detected, and if this is the case the correct parity is sent, subsequent to which it is awaited that the correct parity will traverse the switching path and once again be detected in the TCT station. After this detection, a signal is sent to the central processor that the through-connection test is completed, after which this control is broken off and normal parity monitoring takes over, the latter not being embraced by the invention, however.

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METHOD AND APPARATUS FOR THROUGH-CONNECTION TESTING IN A DIGITAL TELECOMMUNICATION NETWORK

TECHNICAL FIELD

The invention relates to a method and apparatus in a telecommunication system for checking, with the aid of so-called through-connection testing, the establishment and existence of a duplex connection for transmitting digital information in a time division multiplexed bus network, to which subscribers are connected via line terminals.

BACKGROUND ART

A method is disclosed, e g in the Swedish Patent 7410475-3, for through-connection testing in a digital exchange in a telecommunication system. The method is characterized by erroneous parity intentionally being introduced into the digital character flow to an input on an exchange, after steps have been taken to set up a connection between the input and a given output at the exchange, subsequent to which said output is scanned with respect to erroneous parity, and that information relating to the result of said scanning indicating erroneous or correctly established connection, is transmitted to a central control unit.

DISCLOSURE OF INVENTION

The problem with the known method is that it is entirely under the control of a central control unit controlling all activity relating to the through-connection test, resulting in substantial time delay and complicated hardware. Neither is the method utilizable in a larger switching network with a larger number of exchanges or terminals. The test is limited solely to the exchange. The method is based on parity being checked on the receive side under control of the central processor and established on the send side also under control of the central processor. It is thus necessary to take active steps both on the send and receive side of a connection.

The method and apparatus in accordance with the invention, which solves said

problems, is characterized by the claims and is utilizable in a multiprocessor system, and is not under the control of any central processor. The through-connection test in accordance with the invention is based on that monitoring to ensure that a connection has been set up and exists, is checked one and the same terminal, i e the terminal transmitting the through-connection test also has the task of detecting it. This means that all other terminals along the path of the connection, e g processors and the PCM line terminals, only pass along the test message without taking any further steps. The embodiment of this invention is also based on an erroneous parity bit being added to the data samples. It is indeed possible to use other testing signals than erroneous parity, e g a particular check word or a particular check bit. The invention thus permits monitoring that a correct connection has been established in a duplex connection in a digital bus system. The through-connection test (TCT) for both halves of a duplex connection is initiated, and the result is checked at the same point (terminal) of the connection. A parity bit of intentionally wrong polarity is sent together with the speech sample and, as mentioned, the generation of the parity bit and the check of its polarity is performed in the same terminal (processor). In a multiprocessor system initiation and testing can thus be assigned to one and the same processor, which is not possible in the prior art.

BRIEF DESCRIPTION OF DRAWINGS

The apparatus in accordance with the invention is described in detail below with the aid of an embodiment, and with reference to the appended drawing, whereon

Figure 1 is a traffic path diagram illustrating the establishment of a connection where the apparatus in accordance with the invention is incorporated,

Figure 2 depicts a terminal in the switching network with the apparatus in accordance with the invention drawn in as a block diagram,

Figure 3 is a block diagram of a terminal for carrying out the through-connection test.

MODE FOR CARRYING OUT THE INVENTION

As will be seen from Figure 1, a digital switching network of the kind discussed contains a plurality of terminals T, which are digital, processor-controlled

exchanges, one of said terminals denoted TCT being appointed to carry out the through-connection test in the network. The terminals T are connected to each other via time multiplexed buses TSB (Time Switch Bus).Subscriber-connected PCM line terminals PCM 1 and PCM 2 are also connected to the terminals T. In the line terminals are carried out, inter alia, analogue/digital conversion and digital/analogue conversion respectively from and to the line outside the digital network structure.

A duplex connection can be considered as set up between two subscribers in directions A to B and B to A. The actual setting up of the connection in the time multiplexed stage is not accounted for, since this is known in the prior art. A normal parity check is made in a manner known per se in the TCT station for ensuring that a switching path has been set up at all. If any connection point is incorrect, erroneous parity is obtained, indicating such as non-operated switching points, i e switches which has not been set up. The switch causes erroneous parity when it is not activated.

When correct parity is established, i e a correct connection has been set up through the network, the through-connection check is carried out by intentionally generating erroneous (inverted) parity from that terminal (selector point) TCT which has been assigned by a central processor CP (not shown) at the setting up instant for carrying out the through-connection test. For said test it is only in the TCT-terminal that correct parity is awaited. All other switching points in the established connection are switched through, whether parity is correct or erroneous, i e outgoing parity is the same as incoming parity. The intentionally generated erroneous parity bit is taken round the whole switching path and returns as input data to the TCT station, where it is detected. When it has been detected, correct parity is sent to the network. Correct parity is then awaited, for ensuring that all registers along the switching path are emptied of erroneous parity. The central processor is then informed that the connection is correctly set up. A microprocessor MP in the TCT station can decide whether correct or incorrect parity shall be sent. Odd parity is said to be correct parity. For detected erroneous parity (not intentionally generated) correct parity is sent. For a disapproved through-connection test, the central processor makes a new setting up attempt. An alarm is given for repeated unsuccessful connection attempts. The TCT station is usually

the station which is situated closest to the A subscriber.

The intentionally applied erroneous parity is tied the whole time to given channels through the different stations along the switching path. The advantage of this is that no switch can be incorrectly operated without this being discovered at the through-connection test.

Figure 2 illustrates the parts applicable to the invention incorporated in a line terminal, e g PCM 2.

In transmitting a call in a direction from the subscriber A to the subscriber B, binary information is received in series form from the switching terminals on an input to a series parallel converter SP2 of the 74LS395 type in the line terminal PCM 2. Since it is a question of a time division system the speech information is transmitted in the form of samples each comprising eight bits and a parity bit. After conversion to parallel form, the speech samples and the parity bit are applied to the inputs on a parallel/series converter PS 2 of the 74LS395 type for further dispatch on a line L1, e g to the subscriber B. Said signals from the output on the converter SP2 are also applied to the inputs on a modulo-2 adder M2 of the 74LS280 type, in which a parity check takes place in a known manner, i e a check whether the parity is odd or even, and in conformity therewith a parity bit is sent to the input of a modulo-2 adder M3 of the 74LS280 type. The speech samples from the subscriber B are applied to the input on a series/parallel converter SP3 in the line terminal PCM 2. After conversion, the signals are supplied in parallel form to the inputs on a parallel/series converter PS3 for transmission on the time bus TB, and also to further inputs on said modulo-2 adder M3, on the output of which a parity bit is sent answering to the parity bit and speech sample from the subscriber B supplied to the inputs. Speech samples from the subscriber B thus depart from the converter PS3 with a parity bit inserted in the line circuit, said parity bit being obtained without information exchange with, and control from some common central processor, but only by a simple loop connection process. Outgoing parity has the same polarity as incoming parity.

In Figure 3 are shown the necessary circuits included in the terminal TCT for carrying out the through-connection test, said terminal being selected to

control said test at the setting up of the connection. Such circuits are also included in remaining terminals T, since all terminals are equal.

A 74LS395-type series/parallel converter SP1 receives the speech sample with the parity bit from the time bus TB on its input. The binary speech samples are forwarded to a parallel/series converter PS1 of the type 74LS395 for feeding out to the line in series form. The speech samples from the output on the converter SP1 are furthermore applied to the inputs of a modulo-2 adder M1 of the type 74LS280, while the parity bit from the bus is supplied to a first data input on a data selector DS of the type 74LS153. A signal at a constant level, e g corresponding to a logical one, is applied to an input on the modulo-2 adder. The parity signal formed by the addition is sent from a first output of the modulo-2 adder M1 to a second input on the data selector DS. The inverted parity bit is sent from a second output on the adder to a third input on the data selector. The signal from said first parity output on the adder M1 is compared in an exclusive-OR gate, denoted by OR, of the type 74LS882 with the parity bit obtained from the converter SP1. If needed, the result of the comparison can be read in a local processor MP, this being a microprocessor made by MOTOROLA with the number M6801. At the start of a through-connection test the microprocessor MP is given an order from the unillustrated central processor CP to carry out said through-connection test, said microprocessor then writing into a control memory CM, of the type 2148 made by Intel, that the correct parity shall be sent, i e the value 01 corresponding to odd parity. A condition counter TR of the type 74LS161 is set to zero simultaneously by the microprocessor. The task of the condition counter is to control the reaction of the microprocessor to the incoming parities. Control signals are sent from two outputs on the control memory to the corresponding control inputs PC0 and PC1 on the data selector DS. For PC0 = 0 and PC1 = 1 odd parity is sent via the input 5-output 1 of the data selector to the input on the parallel/series converter PS1. This parity signal is sent through the network and received on the input of the TCT station. For equality between the compared parity signals, the circuit OR sends a logical zero signal meaning correct parity and, providing that the condition counter TR is at 0, results in that the microprocessor steps the counter TR one step and changes the control word in the memory CM, which thereby sends intentionally erroneous parity (even parity) corresponding to the logical signal 10. When the control inputs are activated by the signal 10

even parity is sent via the input 6 to the converter PS1 from the data selector.

For difference between the compared parity signals, the circuit OR sends a logical one signal resulting in that, providing that the condition counter TR is at one, the microprocessor MP steps the counter one step and changes the control word in the memory CM to correct parity, i e odd (01), which is sent out on the bus via the data selector. When this correct parity is once again detected, and providing that the condition counter TR is at position 2, the microprocessor steps the counter a further step (3) and sends a control signal to the central processor denoting that the through-connection test is completed. The value 3 on the condition counter signifies that regard will no longer be taken to incoming parities.

In a terminal T, not designated as a control terminal for the through-connection test, the condition counter TR is put in the position 3 at the setting-up instant and the control memory CM is charged with the value 00, incoming parity thus being fed via the input 4-output 1 of the data selector DS to the input on the parallel/series converter PS1 and to the line.

CLAIMS

1 A method, in duplex transmission of digital information between subscribers connected to terminals associated with each other via a telecommunication network of the time multiplex type in which the information is transferred in the form of binary words in specially assigned time slots, of carrying out through- connection test during traffic in progress, with the aid of parity check for checking that a correct connection has been set up after a switching path has been established, characterized in that the through-connection test is started and detected in one and the same station (TCT), a check bit of erroneous parity being arranged to be intentionally sent, after detected correct parity, together with each of a plurality of word samples from a given station (TCT) in the switching network said station being chosen at the setting up of the connection, and in that said control bit in passing through other stations is dispatched unaltered to the next switching point in the network, and in that a parity check of said control bit is carried out in said given station (TCT) from which correct parity is generated and sent after approved parity control, i e for received intentionally erroneous parity.

2 Apparatus for carrying out the method as claimed in claim 1, in duplex transmission of digital information between subscribers connected to terminals associated with each other via a telecommunication network of the time multiplex type in which the information is transferred in the form of binary words in specially assigned time slots, of carrying out through-connection test during traffic in progress, with the aid of parity check for checking that a correct connection has been set up after a switching path has been established, characterized in that

a station (TCT), in the established switching path, for sending and receiving through-connection test information, contains a first parity check means (M1), provided with inputs and outputs, for parity-checking binary information coming in from a line (TB), the resulting control signal being sent uninverted on one output thereof and inverted on another output thereof to respectively a second and a third data input on a data selector (DS) to the first input of which the parity information is supplied directly from said line (TB),

a local processor (MP) controlling via a control memory (CM) the selection of output information from the data selector so that the latter in response to the

value of signals from the control memory to control inputs (PC0, PC1), sends signals on an output corresponding to one of said three inputs,
a comparison circuit (OR) for comparing between incoming parity from the line and calculated, uninverted parity, from said first parity check means (M1), the comparison result being applied to the input of said local processor,
a condition counter (TR) which is stepped forward by said processor in response to signals from the comparator (OR), the condition signal from the counter and the result from the comparator constituting control information for selecting information in the control memory (CM),
and that a second parity check means (M2) in a line terminal (PCM2) controls incoming information in one direction of the duplex connection to form a parity bit which is supplied to a third parity check means (M3), which also receives binary words from the other direction of the duplex connection and feeds the parity bit generated after the parity check further to the next switching point in a direction towards the TCT station.

3 Apparatus as claimed in claim 2, characterized in that the data selector (DS) sends correct (odd) parity on reception of the control signals PC0=0 and PC1=1, inverted (even) parity on reception of the signals 10, and on reception of the control signals 00 sends parity incoming from the line without alteration to the next switching point.

4 Apparatus as claimed in claim 2, characterized in that said parity check means (M1, M2, M3) comprise modulo-2 adders.

5 Apparatus as claimed in claim 2, characterized in that said comparator circuit (OR) is an exclusive-OR circuit.

Fig. 1

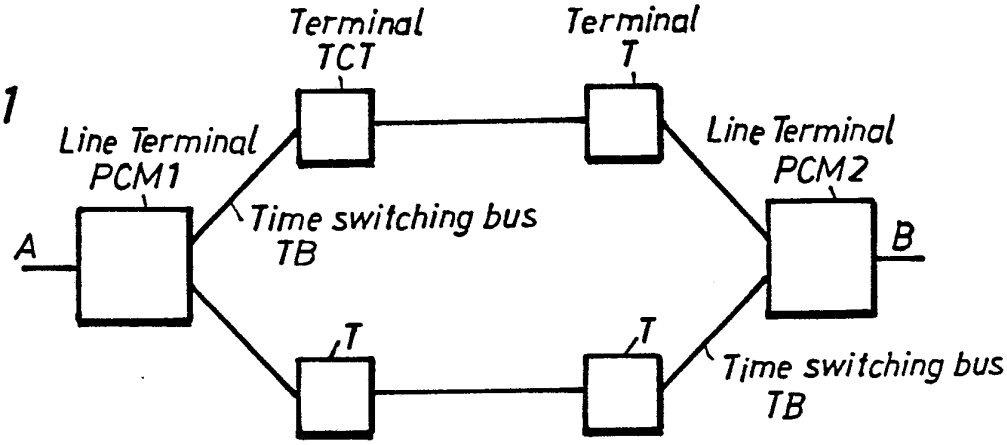


Fig. 2

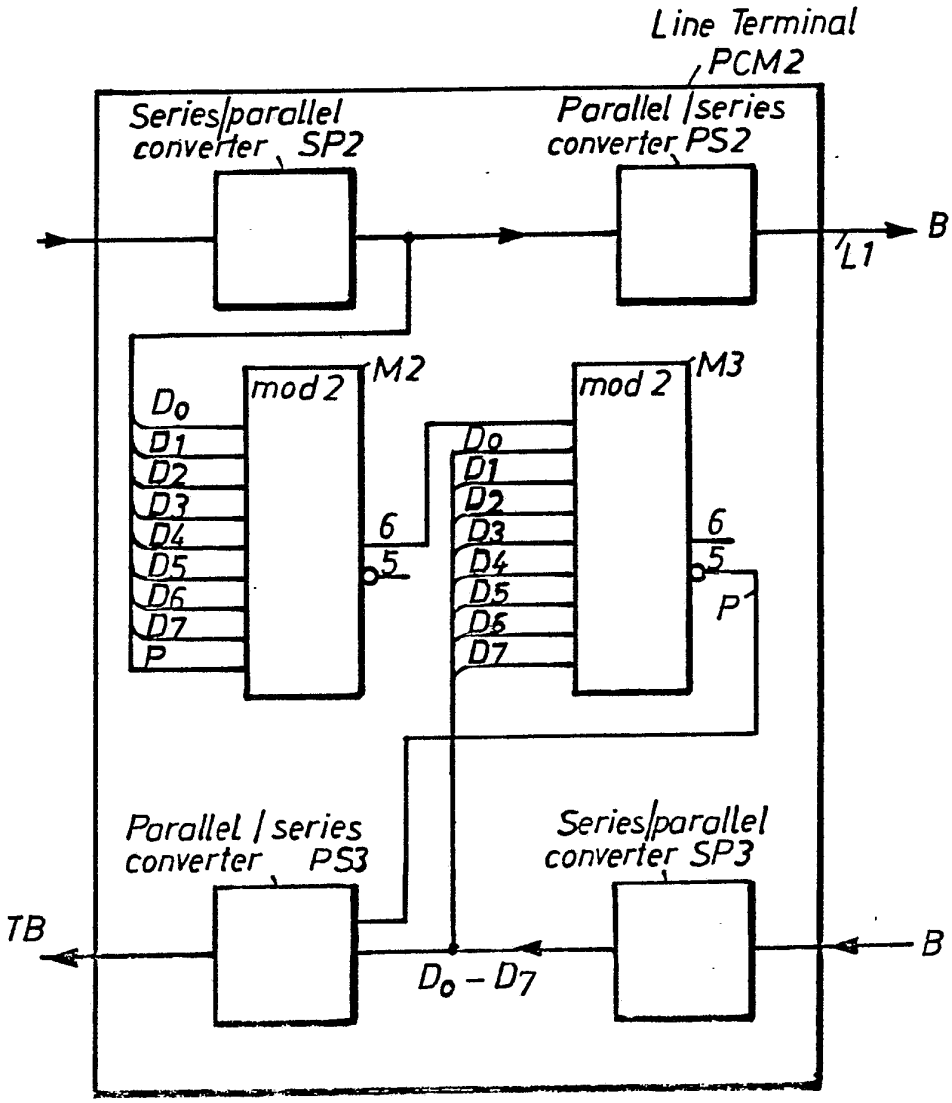
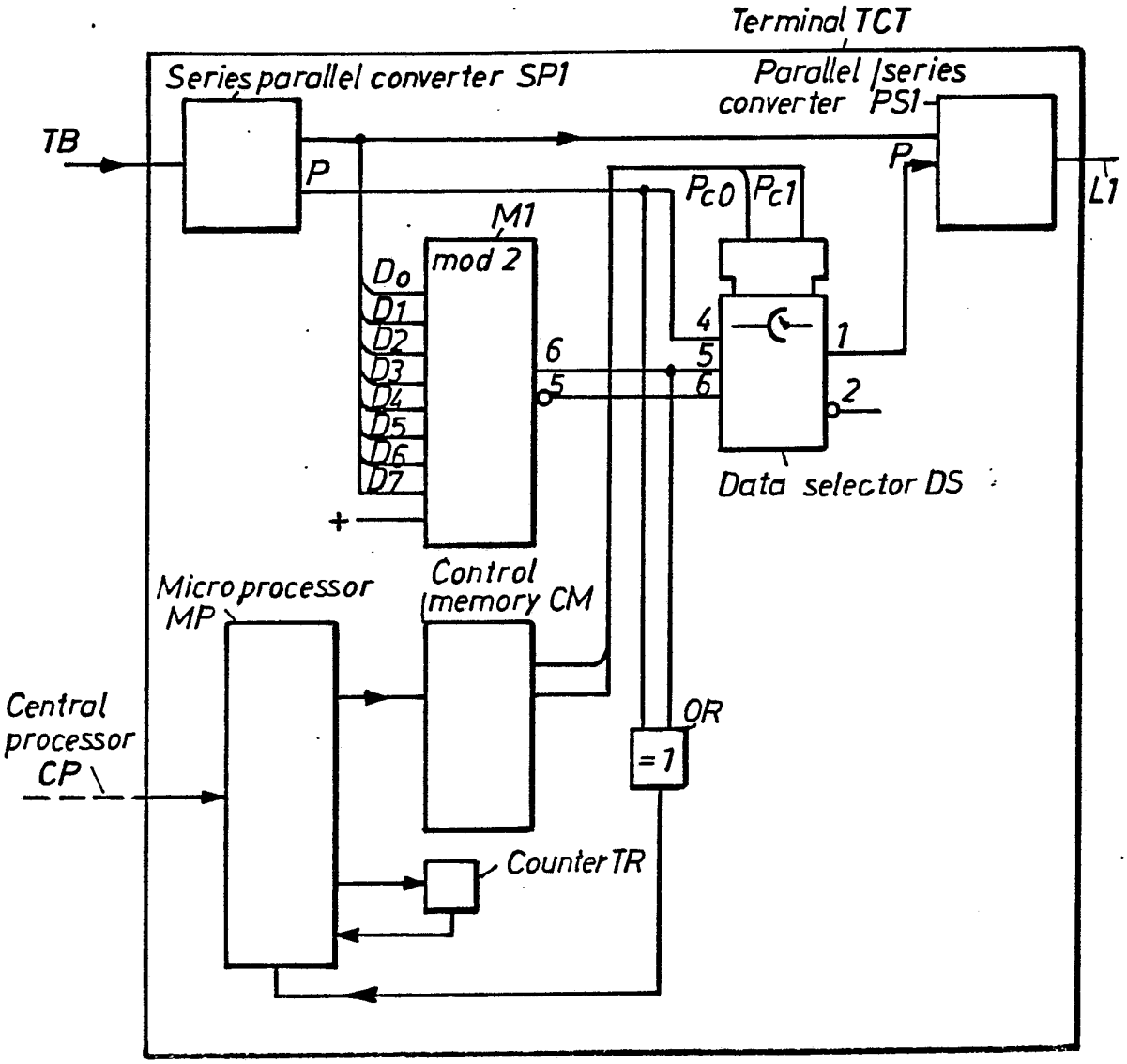


Fig. 3



INTERNATIONAL SEARCH REPORT

International Application No PCT/SE83/00195

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC 3

H 04 J 3/14, H 04 M 3/22

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC 3	H 04 J 3/14, H 04 M 3/22-3/28, H 04 Q 1/22, 1/24
National Cl	21a3:68/30
US Cl	179:15, 175.2, 175.21

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

SE, DK, NO, FI classes as above

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category [6]	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A , 3 823 269 (SAITO) 9 July 1974 see abstract	1-5
A	US, A , 4 048 445 (GHISLER) 13 September 1977 see abstract	1-5
A	US, A, 4 149 038 (PITRODA ET AL) 10 April 1979	1-5
A	Ericsson Review, Volume 55, No. 4, issued December 1978, (Stockholm) B Ericsson and S Roos, "Digital gruppväljare i AXE 10-systemet", pages 140-147, see figure 8.	1-5

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IV. CERTIFICATION

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