(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 March 2010 (18.03.2010)

PCT

(10) International Publication Number
WO 2010/029079 A1

(51) International Patent Classification:
H04J 3/06 (2006.01) *H04H 60/04* (2008.01)

(21) International Application Number:
PCT/EP2009/061641

(22) International Filing Date:
8 September 2009 (08.09.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10 2008 046 914.9
12 September 2008 (12.09.2008) DE

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: METHOD FOR SYNCHRONIZING A RECEIVER AND A TRANSMITTER IN A COMMUNICATION SYSTEM, AND TRANSMITTING STATION AND RECEIVING STATION ADAPTED FOR USE IN THE METHOD ACCORDING TO THE INVENTION

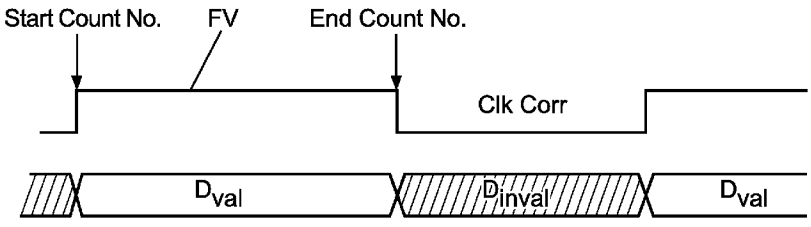


Fig. 3

(57) Abstract: The method is used for synchronizing a transmitter (1) and a receiver (K0). The transmitter and the receiver operate at a first (f_A) or a third (f_B) clock frequency, respectively. The data generated by the transmitter (1) and the receiver (K_0) are transmitted in sections via a transmission link. The transmission link is operated in both directions at a second clock frequency (f_{prot}). The method comprises a step of clock synchronization between the transmitter and the receiver. To this end, an equalization method is used in which a transmission path (TXP) and a receiver path (RXP) respectively perform a clock cycle counting method, which comprises the following steps: the duration of a FRAME_VALID signal (DV), indicating a particular data transmission phase, in clock cycles of the first or the second clock frequency is ascertained in the transmission path; the duration of the FRAME_VALID signal (FV), indicating a particular data transmission phase, in clock cycles of the third or the second clock frequency is ascertained using a second counter (Z1', Z2') in the receiver path; the clock cycle numbers (ΔTX, ΔRX) respectively ascertained by the two counters are compared; the frequency difference between the operating clock (CLK_SRC) of the transmitter (1) and the operating clock (CLK_DEST) of the receiver (2) is equalized on the basis of the comparison result.

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METHOD FOR SYNCHRONIZING A RECEIVER AND A TRANSMITTER IN A COMMUNICATION SYSTEM, AND TRANSMITTING STATION AND RECEIVING STATION ADAPTED FOR USE IN THE METHOD ACCORDING TO THE INVENTION

Technical Field

The invention relates to a method for synchronizing a receiver and a transmitter in a communication system in which the transmitter and the receiver interchange data via a transmission link. The invention also relates to a transmitting station and a receiving station adapted for use in the method according to the invention.

Background of the Invention

Need for methods for clock synchronization between individual data sources using packet-oriented protocols exists with a view to the film business, for example, where a typical scenario is that of random use of a number of different sources of digital data, such as cameras, microphones or other storage media for real-time streams.

From the point of view of post-production/finishing, all cameras should have the same local time. If a network transmission protocol is being used, it is possible to implement a possible method for interchanging the correct time with appropriate accuracy, as described in IEEE Standard 1588 (IEEE = Institute of Electrical and Electronic Engineers). If data from different data sources are being processed and transmitted by a central server, however, the data streams need to be handled in the form of a time-division multiplex. To prevent data losses, each of the data sources needs to be

synchronized not only with the exact time but also with frequency information in order to achieve approximately the same clock frequency as in the server in each data source. That is to say that the sources need to be synchronized to the clock frequency and/or time of the central server.

The synchronization of a plurality of sources, such as cameras in a film studio, has to date been implemented by a Genlock (Generator Lock) signal. Genlock is a method which requires an extra line and which cannot be used for packet-oriented protocols such as Ethernet or Infiniband.

A further difficulty with a packet-oriented protocol is that the clock frequency (f_{prot}) of the transmission system is asynchronous with respect to the original reference frequency (f_B) of the source or (f_A) of the central server.

In this case, the exact clock frequency information is lost as a result of a change of the clock domains when embedded data are transmitted by protocol, which means that the frequency information cannot be interchanged directly between the transmitter and the plurality of receiver ends.

The object of the present invention is thus to propose a new method for clock synchronization and, by extension, for time synchronization which allows the previously described drawbacks to be overcome. Appropriately designed receiving and transmitting stations are also at the focal point of the invention.

Invention

This object is achieved by a method having the features of Claim 1 and by a transmitting station having the features according to Claim 9 and also by a receiving station having the features of Claim 14. Advantageous embodiments of the invention are defined in further claims.

The method is used for clock synchronization between a transmitting station and a receiving station in a communication system in which the transmitter and the receiver interchange data via a transmission link. In this case, the data are respectively transmitted from the transmitting station to the receiving station, or in the opposite direction, via a respective transmission link, at least sections of which are routed through a protocol clock domain, during transmission phases interrupted by pauses. The transmitting station operates at a first clock frequency. The data transmission takes place at a second clock frequency, also called the protocol clock frequency. The receiving station operates at a third clock frequency. An equalization method for equalizing the frequency difference between the operating clocks of the two communication partners is performed. In the course of the equalization method, a transmission path and a receiver path respectively perform a clock cycle counting method, which comprises the following steps:

- the duration of a FRAME_VALID signal (FV), indicating a particular data transmission phase, in clock cycles of the first or the second clock frequency is ascertained using a first counter (Z1, Z2) in the transmission path;
- the duration of the FRAME_VALID signal (FV), indicating a particular data transmission phase, in clock cycles of the

third or the second clock frequency is ascertained using a second counter (Z1', Z2') in the receiver path;

- the clock cycle numbers (ΔTX, ΔRX) respectively ascertained by the two counters are compared;
- the frequency difference between the operating clock of the transmitter (1) and the operating clock of the receiver (2) is equalized on the basis of the comparison result.

In this case, the clock cycle numbers respectively counted by the two counters are compared with one another, and the comparison result is taken as a basis for prompting the equalization of the frequency difference.

The FRAME_VALID signal is provided internally, for example, in each Ethernet interface and therein in the MAC layer. By way of example, a level may have been set to a relatively high value ("high") on the basis of a reference potential so as thereby to indicate that data are being transmitted, while the level is accordingly set to a relatively low value ("low") so as thereby to indicate that no data are being sent. Self-evidently, the converse case is also conceivable, i.e. that the level is set to a relatively low value so as thereby to indicate that data are being transmitted. In this text, the term "transition edge of the "FRAME_VALID" signal" covers the terms "positive edge of the "FRAME_VALID" signal" and "negative edge of the "FRAME_VALID" signal".

The name of the signal is not meant to be limiting. In principle, it is also possible to use any other suitable transmission phase indicator signal, which carries information about the duration of a real/valid transmission phase in

contrast to a phase in which no data or what are known as filler data are transmitted, instead of the "FRAME_VALID" signal. The phase in which no data or filler data are transmitted is also referred to as an idle state. In this connection, it is important that during this transmission phase indicator signal the clock frequency (f_{prot}) of the transmission system is not modified or corrected in the transmitter or receiver. This occurs only during the idle state. Hence, the duration of the transmission phase indicator signal is a reference time in the transmitter and the receiver. Therefore, only this time is used in order to measure a possible clock offset between the source or the central server.

The fact that the method involves utilization of the clock from the transmission protocol and of a signal which is present in each communication interface along the transmission path means that it is possible to achieve synchronization between two stations which are far apart, even if there are yet other intermediate stations between them.

Various embodiments of the method according to the invention are disclosed in the patent application. At one time, the duration of the FRAME_VALID signal is ascertained by capturing clock edges of the clock signal at the first clock frequency and converting an appropriate clock edge signal to a transmission protocol clock domain, wherein the converted clock edge signal is used as an enable signal for a counter clocked on the basis of the second clock frequency (f_{prot}) and the counter readings of the counter are captured when the transition edges of the FRAME_VALID signal are recognized, and

the difference is used to determine the duration of the FRAME_VALID signal. This is done in the transmission path. A similar thing is done in the reception path, except that the clock edges of the clock signal at the third clock frequency are captured.

A further refinement relates to the solution that the transmission path ascertains the duration by converting the FRAME_VALID signal to the clock domain for the first clock frequency, wherein the converted FRAME_VALID signal is used as an enable signal for the counter clocked on the basis of the first clock frequency and the counter readings of the counter are captured when the transition edges of the FRAME_VALID signal are recognized, and the difference is used to determine the duration of the FRAME_VALID signal; and wherein the reception path ascertains the duration by converting the FRAME_VALID signal to the clock domain for the third clock frequency, wherein the converted FRAME_VALID signal is used as an enable signal for the counter clocked on the basis of the third clock frequency and the counter readings of the counter are captured when the transition edges of the FRAME_VALID signal are recognized, and the difference is used to determine the duration of the FRAME_VALID signal. An implementation based on this solution affords the advantage that the counters are operated with a continuous enable signal and the operating clock of the station is used and not the clock of the transmission protocol. They can therefore run more slowly, which also affords advantages in respect of accuracy.

In one refinement of the method according to the invention, the equalization method is performed for each pair of

communication partners in a communication system. It is thus possible to equalize frequency differences between a plurality of stations which are synchronized to a central clock frequency together. If the stations supply data for one and the same project then all stations relate to the same clock frequency and no errors arise in respect of different time bases. This is advantageous particularly in the case of video post-production in video studios.

If additionally time synchronization is also performed on the basis of IEEE Standard 1588, for example, the time code for the video data in the various stations is also correct, and it is possible for the cut editing to be performed on the basis of the time code and from any editing positions.

The aforementioned step of synchronizing the time of the at least one peripheral unit to the time of the central unit is performed once particularly whenever the relevant peripheral unit is restarted.

The invention allows regeneration of frequency or timing information from a data source to a plurality of terminals, too, in the case of packet-oriented protocols.

The invention can also be used - even if changes occur in the clock domain - in networks or for individual direct connections.

The invention affords a high level of accuracy, which is of crucial importance when transmitting real-time data, such as video, audio or high-speed measurement data.

The invention does not require an additional signal line.

Further advantages and details of the invention are described below with reference to the appended drawings.

Brief Description of the Drawings:

In the drawings:

Figure 1 shows a schematic illustration to clarify the basic setup of a communication system;

Figure 2 shows a basic block diagram with a protocol frame to illustrate a data transmission between the communication partners in a pair of communication partners in the communication system from Figure 1;

Figure 3 shows a timing diagram to illustrate the processes on the physical layer;

Figure 4 shows a block diagram of a first electronic device in a transmission path;

Figure 5a shows a block diagram of a first electronic device in a reception path;

Figure 5b shows a block diagram of an evaluation unit which also generates control signals for readjusting the clock frequency which is to be synchronized;

Figure 6 shows a flowchart for a comparison method taking place in the evaluation unit;

Figure 7 shows a block diagram of a second electronic device in a transmission path; and

Figure 8 shows a block diagram of a second electronic device in a reception path.

Detailed Description of the Invention

Figure 1 shows a schematic illustration to clarify the basic setup of a communication system KS which, by way of example, is part of the technical equipment of a film studio and comprises a server 1 which is central to the communication system KS and cameras K_0, K_1, ..., K_{n-1} which are peripheral to the communication system.

The central server 1 is operated at a central clock frequency f_A, while the individual cameras K_0, K_1, ..., K_{n-1} are respectively operated at a different peripheral clock frequency.

A pair of communication partners respectively comprises the central server 1 as one communication partner and a respective one of the cameras K_0, K_1, ..., K_{n-1} as the other communication partner, which means that the number of pairs of communication partners in the communication system matches the number of cameras K_0, K_1, ..., K_{n-1}.

The peripheral cameras K_0, K_1,..., K_{n-1} respectively produce a data stream, comprising real-time-critical camera data, in

sync with their respective associated peripheral clock frequency. The user data are sent from the individual cameras to the central server 1 in transmission phases by transmission link, respectively routed through a protocol clock domain. The transmission rate is assumed to be high, which means that it is also possible for pauses between the transmission phases to occur in which no user data are transmitted. The protocol clock domain has a protocol clock frequency. Generally, the protocol clock frequency f_{prot} is asynchronous with respect to the original reference frequency of the data source or with respect to the central server 1.

The individual cameras K_0, K_1, ... K_{n-1} are synchronized to the time of the central server 1 by means of time synchronization based on IEEE Standard 1588. This synchronization method is also called the precision time protocol PTP. An algorithm is used to ascertain that appliance among the participating appliances which indicates that it has the most exact time. Next, this appliance (Grandmaster Clock) distributes the time to the other appliances (Slave Clocks), wherein the signal delays are compensated for. The compensation is based on the assumption that the forward and return paths for synchronization messages in the network, averaged over a plurality of steps, have the same delay.

The time synchronization needs to be performed in order to respectively obtain the correct time stamp for each receiver.

The synchronization paths SP_0, SP_1, ... SP_{n-1}, along which the synchronization data containing clock-frequency and time information are transmitted from the central server 1 to the

individual cameras K_0, K_1, ..., K_{n-1}, are oriented in a first direction, indicated by first arrows P, which runs from the server 1 to the cameras K_0, K_1,...., K_{n-1}. By contrast, the data paths DP_0, DP_1,...., DP_{n-1}, along which the camera data are transmitted from the individual cameras K_0, K_1, ..., K_{n-1} to the central server 1, are oriented in a second direction, indicated by arrows P', which is opposite to the first direction. It is thus advantageously possible to perform synchronization and user-data transportation independently of one another if a bidirectional link is set up, such as for a 10-gigabit Ethernet link.

Each camera K_0, K_1, ..., K_{n-1} is provided with a clock control device which can be used to alter the operating clock of the respective camera K_0, K_1, ..., K_{n-1}.

By way of example, the clock control devices are respectively in the form of a phase locked loop (PLL) or a delay locked loop (DLL).

For each of the pairs of communication partners, a separate equalization method is performed for equalizing the frequency difference between the operating clocks of the two communication partners in the respective pair of communication partners.

However, since the equalization methods performed for each of the pairs of communication partners match in terms of basic flow, it is sufficient for the text below to describe the equalization method by way of example merely using the example of the first pair of communication partners formed from the

central server 1 and the first camera K_0 with reference to Figures 2 to 6 in order to avoid mere repetition.

Figure 2 shows a basic block diagram with a protocol frame PF for illustrating a data transmission in the synchronization path between the central server 1 and the first camera K_0. The data $D_0....D_{n-1}$ packed in a protocol frame PF are transmitted from the central server 1 within a first clock domain DA to the first camera K_0 within a third clock domain DB via a packet-oriented transmission link within a second clock domain DProt. A data word comprises the data bits $D_0....D_{n-1}$ and has the data word length n. A data packet may be made up of one or more data words. As described, the data packets relate to data for synchronization, particularly the clock cycle numbers, for which the extraction and use are explained in more detail below. Camera remote control data are also transmitted in this way. In addition, it is also possible for intercom data to be transmitted to the camera in this way. These are audio data, e.g. for direction instructions to the cameraman.

The synchronous data stream is transmitted from the central server 1 to the first camera K_0 using a packet-oriented protocol which has an at least approximately fixed data rate of 1 GBit/s or 10 GBit/s, e.g. using the Ethernet or Infiniband protocol. In respect of a protocol layer, for example the MAC (Medium Access Control) layer, the use of a fixed data rate (e.g. 1 Gb/s or 10 Gb/s) internally results in a fixed data word length and clock frequency. By way of example, in the case of a 10 Gb Ethernet protocol (XGE) based on IEEE Standard 802.3ae, it is possible to use a data word length of 64 bits at 156.25 MHz. A plurality of data words can

be combined into a packet of variable length. Data packets are transmitted in a protocol frame, with header information, such as a preamble and address information, and a trailer with an error checksum at the end.

The first clock frequency f_A in the first clock domain DA is produced by a first clock source CLK_SRC. The second clock frequency f_{prot} in the second clock domain is produced by a second clock source CLK_PROT, and the third clock frequency f_B in the third clock domain is produced by a third clock source CLK_DEST.

The first clock frequency f_A and the third clock frequency f_B are nominally the same. However, the use of two local oscillators results in small differences, which are permitted to be no more than +/- 100 ppm in the case of a 10-Gigabit Ethernet transmission, for example.

As already described above, the operating clock - controlled by the clock control device - of the first camera K_0 can be varied.

The first camera K_0 produces a data stream which is in sync with the first clock frequency f_B.

In a first step of the synchronization method, the server 1 embeds not only conventional data but also novel clock cycle numbers into the protocol frame PF.

Clock cycle numbers need to be periodically repeated at certain intervals. Clock cycle numbers can be transmitted in a

manner multiplexed with other data or else separately in a protocol frame.

To achieve a situation in which the value of the clock frequency f_B matches the value of the original frequency f_A, the method according to the invention involves the performance of a synchronization method, described in more detail further below, in order to reduce the influence of clock jitter and migration effects, e.g. effects of temperature.

In respect of the processes which are illustrated in the timing diagram shown in Figure 3 and which take place during the transmission of the data stream produced by the server 1 on the Ethernet MAC layer, it is possible to distinguish between firstly a "valid" time period, in which embedded data (for example the data words with the bits $D_0 \ldots D_{n-1}$ in each clock cycle of the second clock frequency f_{prot}) are transmitted and therefore a FRAME_VALID signal has the value 1 ("FRAME_VALID"=1), and secondly an "invalid" time period, in which no data to be transported are available and therefore the FRAME_VALID signal has the value 0 ("FRAME_VALID"=0). The FRAME_VALID signal is in sync with the second clock domain or clock frequency f_{prot}. In the case of the Ethernet bus protocol, data packets of up to eight bytes per clock cycle are transmitted in sync with the clock frequency f_{prot}. In order to prescribe the length of a transmission frame in bytes for the transmitter, a "byte mask" needs to be indicated in addition to the data. In the case of eight bytes, eight bits are used, for example, each bit masking a byte as valid or invalid. The FRAME_VALID signal can be generated directly from one of these masking bits, since it corresponds to the time

length of the Ethernet data packet at the transmitter and receiver ends.

The receiver regenerates the masking bits internally in the MAC layer by evaluating the applied data. The receiver-end FRAME_VALID signal should be produced from the same bit as at the transmitter end. The transmitter and receiver ends then have the same time reference available. If the application does not supply any data which are to be transported, arbitrary filler data can be embedded in the case of 10 Gigabit Ethernet, e.g. between a preamble 0x"D5555555555555FB" or an end byte 0x"FD" and invalid data bytes 0x"07", besides the synchronization information. From this valid frame, it is possible to reconstruct the FRAME_VALID signal at the receiver end.

During the transmission of the valid data from the server 1, the second clock frequency f_{prot} will also become the reference frequency for the source data from the camera K_0.

The subsequently described production of the specific clock cycle numbers is effected using a first electronic device E1, shown as a block diagram in Figure 4, in a transmitter path TXP, first variant. A first circuit of the first electronic device E1 examines the duration for which the value of the FRAME_VALID signal is equal to 1 for clock cycles of the first clock frequency f_A. In this regard, an edge capture detector FD is used to capture the rising (positive) edges of the clock signal at the first clock frequency f_A, and a corresponding edge signal is transformed to the second clock domain of the reference clock at the clock frequency f_{prot} in an inherently

known manner using a first and a second flip flop F1, F2. The flip flops are preferably edge-triggered D-type flip flops. The aforementioned edge signal is used as an enable signal for a counter Z1 which is clocked at the second clock frequency f_{prot}. Under the triggering of an edge detector FDB for both edges of the FRAME_VALID signal FV shown in Figure 2, the start and end counter readings of the counter Z1 are obtained at the output of the first counter Z1.

A first accumulator A connected downstream of the counter Z1 ascertains a first clock cycle number ΔTX as the difference between the captured counter readings at the end and the start of the "FRAME_VALID" signal. To this end, a subtractor SUB1 and a third flip flop F3 are provided. Clock cycle number data identifying the first clock cycle number ΔTX are embedded into the start or the end of one of the subsequent protocol frames which follow the protocol frame that is currently being transmitted and are sent to the camera K_0.

To this end, the first clock cycle number ΔTX is registered using a fourth flip flop F4 upon the next valid protocol frame (for example upon the next positive edge of the "FRAME_VALID" signal, i.e. upon the subsequent protocol frame).

In a receiver path RXP, first variant, a second electronic device E2 shown as a block diagram in Figure 5a is used to ascertain a second clock cycle number ΔRX when valid data are received. The second electronic device E2 matches the first electronic device E1 in terms of basic design and basic manner of operation, which is why to avoid mere repetition a detailed description of the second electronic device E2 is subsequently

dispensed with. While the circuit E1 for the frequency synchronization is integrated in the server 1 at the transmission end, the circuit E2 in the exemplary embodiment described is accommodated in the camera K_0, that is to say at the reception end. The circuit E2 is used to determine the length of the FRAME_VALID signal recovered in the Ethernet interface in clock units of the camera clock at the frequency f_B.

The second electronic device E2 in turn comprises a plurality of flip flops F1', F2', F3', a plurality of edge capture detectors FD', a second counter Z1', an accumulator A' and an edge detector FDB'.

The second clock cycle number ΔRX is ascertained in a similar manner to the ascertainment of the first clock cycle number ΔTX, which is why to avoid mere repetition a detailed description of the ascertainment of ΔRX is subsequently dispensed with.

Figure 5b shows a coarse block diagram of an evaluation unit in which the ascertained clock cycle numbers ΔTX and ΔRX are compared and control signals for correcting the clock frequency which is to be synchronized are generated. The block shown performs a comparison method, the flow of which is shown as a flowchart in Figure 6.

If the result in step S1 is positive, the comparison and control electronics continue the comparison method in step S2. If the result in step S1 is negative, on the other hand, the comparison and control electronics return to the starting

point SP of the comparison method. The test in step S1 is intended to express that it is important not to ascertain the clock cycle number difference during the FRAME_VALID signal in the central server 1, because in this phase there may still be no consistent measurement results available for the clock cycle numbers.

In step S2, the comparison and control electronics calculate a clock cycle number difference by subtracting the first clock cycle number ΔTX from the second clock cycle number ΔRX.

In step S3, the comparison and control electronics check whether the clock cycle number difference calculated in step S2 is equal to zero.

If the result of the check in step S3 is that the clock cycle number difference is equal to zero, the comparison and control electronics return to the starting point SP of the comparison method.

If the result of the check in step S3 is that the clock cycle number difference is not equal to zero, on the other hand, the comparison and control electronics move to step S4.

In step S4, the comparison and control electronics check whether the clock cycle number difference is less than zero. If the result of the check in step S4 is that the clock cycle number difference is less than zero, the comparison and control electronics move to step S5.

If the result of the check in step S4 is that the clock cycle number difference is not less than zero, however, the comparison electronics move to step S6.

In step S5, the comparison and control electronics prompt the clock control device 3 to be used to increase the third clock frequency f_B of the third clock domain DB.

In step S6, the comparison and control electronics prompt the clock control device 3 to be used to reduce the third clock frequency f_B of the third clock domain DB.

Figure 7 shows a block diagram of a second electronic device E3 in a transmission path. Figure 8 shows a block diagram of a second electronic device E4 in a reception path. The third electronic device and the fourth electronic device are used for an alternative solution to the previously described solution.

Figure 7 can be compared with Figure 4. In this case, identical components have been denoted by the same reference symbols throughout the two block diagrams. An important difference relates to the manner of operation of the counter Z2. This is operated at the operating clock CLK_SRC in the transmitting station. In this case, the frequency f_A is lower than in Figure 4. By way of example, the protocol clock frequency for 10 GBE is 156.25 MHz. By contrast, the operating clock in the station is typically lower than half the protocol frequency. The FRAME_VALID signal FV is converted to the clock domain at the first clock frequency f_A by means of the two flip flops F5 and F6. This converted FRAME_VALID signal is

used as an enable signal for the counter Z2. The counter readings are captured as in the example shown in Figure 4 upon the occurrence of the rising and falling edges of the FRAME_VALID signal FV. In contrast to Figure 4, the clock cycle number capture is not performed using an accumulator. Instead, two flip flops F7 and F8 are used which buffer-store the counter readings upon the rising edge of the FRAME_VALID signal and the falling edge of the FRAME_VALID signal. A downstream subtraction circuit SUB2 calculates the difference between the two counter readings. This difference is transferred to the flip flop F9 one operating clock cycle later and is available at the output as a clock cycle number ΔTX. All the components downstream of the counter Z2 are operated at the clock CLK_prot of the data transmission protocol.

Figure 8 shows the circuit, corresponding to Figure 6, for the reception path RXP. It can be compared with Figure 5a. The basic design of the structure is identical. As shown, the operating clock CLK_DIST of the receiving station at the clock frequency f_B is used at the input of this circuit.

In respect of an application in the network, the data transmission link from a data source to a data sink can be routed through a number of network nodes, each of which can be considered either as a transmitter or as a receiver. In the respective receiver, the clock frequency of the protocol layer f_{prot} can be corrected or resynchronized (clock correction) in order to receive synchronous protocols. This is done only in the phase in which the FRAME_VALID signal FV indicates the

inactive state. It is thus possible to achieve synchronization over the entire transmission link.

The frequency f_{prot} of the transmission protocol is the reference frequency. The duration of the FRAME_VALID signal is the reference duration which is used in each node in order to obtain the clock cycle numbers. This also applies to the receiver at the end node, that is to say the previously described synchronization method can also be applied within a network architecture having numerous network nodes.

The invention can be used for all kinds of transmitted data where a clock normally needs to be considered, such as data from various sensors. The invention can be used to resynchronize application clock cycles to a plurality of receivers in packet-oriented protocols so long as a fixed data rate for providing the application data and a fixed transmission rate are used.

In particular, the use of the invention affords advantages where it is necessary to transmit real-time data, that is to say especially multimedia data such as audio or video data streams.

Examples of other appliances between which the synchronization can take place in the manner of the invention are encoders and decoders for audio and/or video data streams, DSL routers and personal computers, streaming clients and digital receivers, such as set top boxes or what are known as IRD (Integrated Receiver Decoder) appliances, which are digital TV sets with an integrated set top box. The list is not conclusive.

In order to make use of the theoretically also conceivable transmission phase for the synchronization, in which no valid data are transmitted, it would be necessary to define a section therein in which no clock correction for the protocol clock frequency f_{prot} is permitted. It would also be possible to use a certain signal section within the valid data transmission phase as a reference, that is to say half or another fraction of this phase, for example.

Patent Claims

1. Method for synchronizing a receiver (K_0) and a transmitter (1), which is operated at a first clock frequency (f_A) and whose data are transmitted to the receiver (2), which is operated at a third clock frequency (f_B), via a data transmission link at a second clock frequency (f_{prot}), wherein the transmitter end sends the data during transmission phases interrupted by pauses, characterized in that a transmission path (TXP) and a receiver path (RXP) respectively perform a clock cycle counting method, which comprises the following steps:

- the duration of a FRAME_VALID signal (FV), indicating a particular data transmission phase, in clock cycles of the first or the second clock frequency is ascertained using a first counter (Z1, Z2) in the transmission path;
- the duration of the FRAME_VALID signal (FV), indicating a particular data transmission phase, in clock cycles of the third or the second clock frequency is ascertained using a second counter (Z1', Z2') in the receiver path;
- the clock cycle numbers (ΔTX, ΔRX) respectively ascertained by the two counters are compared;
- the frequency difference between the operating clock of the transmitter (1) and the operating clock of the receiver (2) is equalized on the basis of the comparison result.

2. Method according to Claim 1, wherein the transmission path (TXP) ascertains the duration of the FRAME_VALID signal (FV) by capturing clock edges of the clock signal at the first clock frequency (f_A) and converting an appropriate clock edge

signal to a transmission protocol clock domain (DProt), wherein the converted clock edge signal is used as an enable signal for the counter (Z1) clocked on the basis of the second clock frequency (f_{prot}) and the counter readings of the counter (Z1) are captured when the transition edges of the FRAME_VALID signal (FV) are recognized, and the difference is used to determine the duration of the FRAME_VALID signal (FV); and wherein the reception path (RXP) ascertains the duration by capturing clock edges of the clock signal at the third clock frequency (f_B) and converting an appropriate clock edge signal to a transmission protocol clock domain (DProt), wherein the converted clock edge signal is used as an enable signal for the counter (Z1') clocked on the basis of the second clock frequency (f_{prot}) and the counter readings of the counter (Z1') are captured when the transition edges of the FRAME_VALID signal (FV) are recognized, and the difference is used to determine the duration of the FRAME_VALID signal (FV).

3. Method according to Claim 1, wherein the transmission path (TXP) ascertains the duration by converting the FRAME_VALID signal (FV) to the clock domain (DA) for the first clock frequency (f_A), wherein the converted FRAME_VALID signal (FV) is used as an enable signal for the counter (Z2) clocked on the basis of the first clock frequency (f_A) and the counter readings of the counter (Z2) are captured when the transition edges of the FRAME_VALID signal (FV) are recognized, and the difference is used to determine the duration of the FRAME_VALID signal (FV); and wherein the reception path (RXP) ascertains the duration by converting the FRAME_VALID signal (FV) to the clock domain (DB) for the third clock frequency

(f_B), wherein the converted FRAME_VALID signal (FV) is used as an enable signal for the counter (Z2') clocked on the basis of the third clock frequency (f_B) and the counter readings of the counter (Z2') are captured when the transition edges of the FRAME_VALID signal (FV) are recognized, and the difference is used to determine the duration of the FRAME_VALID signal (FV).

4. Method according to one of the preceding claims, wherein a data record which characterizes the duration of the FRAME_VALID signal (FV), as ascertained in the transmission path (TXP) as a clock cycle number (ΔTX) using the first counter (Z1, Z2), is transmitted to the receiver (K_0) using one of the protocol frames which chronologically succeed the currently transmitted protocol frame, and the comparison is performed at the receiver end.

5. Method according to one of the preceding claims, wherein the means for equalizing the frequency difference between the operating clock (CLK_SRC) of the transmitter (1) and the operating clock (CLK_DEST) of the receiver (K_0) comprise a phase locked loop or a delay locked loop.

6. Method according to one of the preceding claims, wherein the second clock frequency (f_B) is increased if the result of the comparison of the clock cycle numbers (ΔTX, ΔRX) is that the ascertained clock cycle number at the transmission end (ΔTX) is greater than at the reception end (ΔRX), and wherein the clock frequency (f_B) is reduced if the result of the comparison is that the ascertained clock cycle number at the

transmission end (ΔTX) is less than at the reception end (ΔRX).

7. Method according to one of the preceding claims, wherein the synchronization method is performed for a respective pair of communication partners in a communication system (KS) which has a central unit (1) operated at a central clock frequency and a plurality of peripheral units (K_0,...., K_{n-1}) operated at a respective peripheral clock frequency, wherein the communication partners in each pair of communication partners or in at least a number of the pairs of communication partners are connected to one another by means of a packet-oriented data transmission protocol.

8. Method according to Claim 7, wherein time synchronisation based on IEEE Standard 1588 is performed between the communication partners in addition to the clock synchronisation method.

9. Transmitting station for use in the method according to one of the preceding claims, which performs data generation at a first clock frequency, having data transmission means which are used to supply the data generated in the transmitting station at the first clock frequency (f_A) to a data transmission link, wherein the data transmission means operate at a second clock frequency (f_{prot}), characterized in that the transmitting station has a first counter (Z1, Z2) which ascertains the duration of a FRAME_VALID signal (FV), indicating a particular data transmission phase, in clock cycles of the first or the second clock frequency, and in that

the data transmission means likewise send the ascertained clock cycle number (ΔTX) to the data transmission link.

10. Transmitting station according to Claim 9, having means which capture the duration of the clock edges of the clock signal at the first clock frequency (f_A) in the transmission path (TXP) and convert an appropriate clock edge signal to a transmission protocol clock domain (DProt), wherein the converted clock edge signal is used as an enable signal for the counter (Z1) clocked on the basis of the second clock frequency (f_{prot}) and the counter readings of the counter (Z1) are captured when the transition edges of the FRAME_VALID signal (FV) are recognized, and the difference is used to determine the duration of the FRAME_VALID signal (FV).

11. Transmitting station according to Claim 9, having means which convert the FRAME_VALID signal (FV) to the clock domain (DA) for the first clock frequency (f_A) in the transmission path (TXP) and use the converted FRAME_VALID signal (FV) as an enable signal for the counter (Z2) clocked on the basis of the first clock frequency (f_A) and capture the counter readings of the counter (Z2) when the transition edges of the FRAME_VALID signal (FV) are recognized and use the difference to determine the duration of the FRAME_VALID signal (FV).

12. Transmitting station according to one of Claims 9 to 11, characterized in that the data transmission means send a data record which characterizes the duration of the FRAME_VALID signal (FV), as ascertained in the transmission path (TXP) as a clock cycle number (ΔTX) using the first counter (Z1, Z2),

to the receiver (K_0) using one of the protocol frames which chronologically succeed the currently transmitted protocol frame.

13. Transmitting station according to one of Claims 9 to 12, characterized in that additionally time synchronization means are provided which perform time synchronization based on IEEE Standard 1588.

14. Receiving station for use in the method according to one of Claims 1 to 8 which performs data processing at a third clock frequency (f_B), having data reception means which are used for receiving the data transmitted via the transmission link and operate at the second clock frequency, characterized in that the receiving station has a second counter (Z1', Z2') which ascertains the duration of a FRAME_VALID signal (FV), indicating a particular data transmission phase, in clock cycles of the third or the second clock frequency, in that the receiving station has comparison means which are designed to compare the clock cycle number (ΔRX) counted by the second counter (Z1', Z2') with a clock cycle number (ΔTX) which is ascertained in a transmitting station and received from the transmission link, and in that the receiving station has adjusting means which are designed to take the comparison result as a basis for equalizing the frequency difference between the operating clock (CLK_SRC) of the transmitting station (1) and the operating clock (CLK_DEST) of the receiving station (2).

15. Receiving station according to Claim 14, having means which capture the duration of the clock edges of the clock signal at the third clock frequency (f_B) in the reception path (RXP) and convert an appropriate clock edge signal to a transmission protocol clock domain (DProt), wherein the converted clock edge signal is used as an enable signal for the counter (Z1') clocked on the basis of the second clock frequency (f_{prot}) and the counter readings of the counter (Z1') are captured when the transition edges of the FRAME_VALID signal (FV) are recognized, and the difference is used to determine the duration of the FRAME_VALID signal (FV).

16. Receiving station according to Claim 14, having means which convert the FRAME_VALID signal (FV) to the clock domain (DB) for the third clock frequency (FV) in the reception path (RXP) and use the converted FRAME_VALID signal (f_B) as an enable signal for the counter (Z2') clocked on the basis of the third clock frequency (f_B) and capture the counter readings of the counter (Z2') when the transition edges of the FRAME_VALID signal (FV) are recognized and use the difference to determine the duration of the FRAME_VALID signal (FV).

17. Receiving station according to one of Claims 14 to 16, characterized in that the adjusting means comprise a phase locked loop or a delay locked loop.

18. Receiving station according to one of Claims 14 to 17, wherein the adjusting means increase the third clock frequency (f_B) if the result of the comparison of the clock cycle numbers (ΔTX, ΔRX) is that the ascertained clock cycle number

at the transmission end (ΔTX) is greater than at the reception end (ΔRX), and reduce the clock frequency (f_B) if the result of the comparison is that the ascertained clock cycle number at the transmission end (ΔTX) is less than at the reception end (ΔRX).

19. Receiving station according to one of Claims 14 to 18, characterized in that additionally time synchronization means are provided which can perform time synchronization on the basis of IEEE Standard 1588.

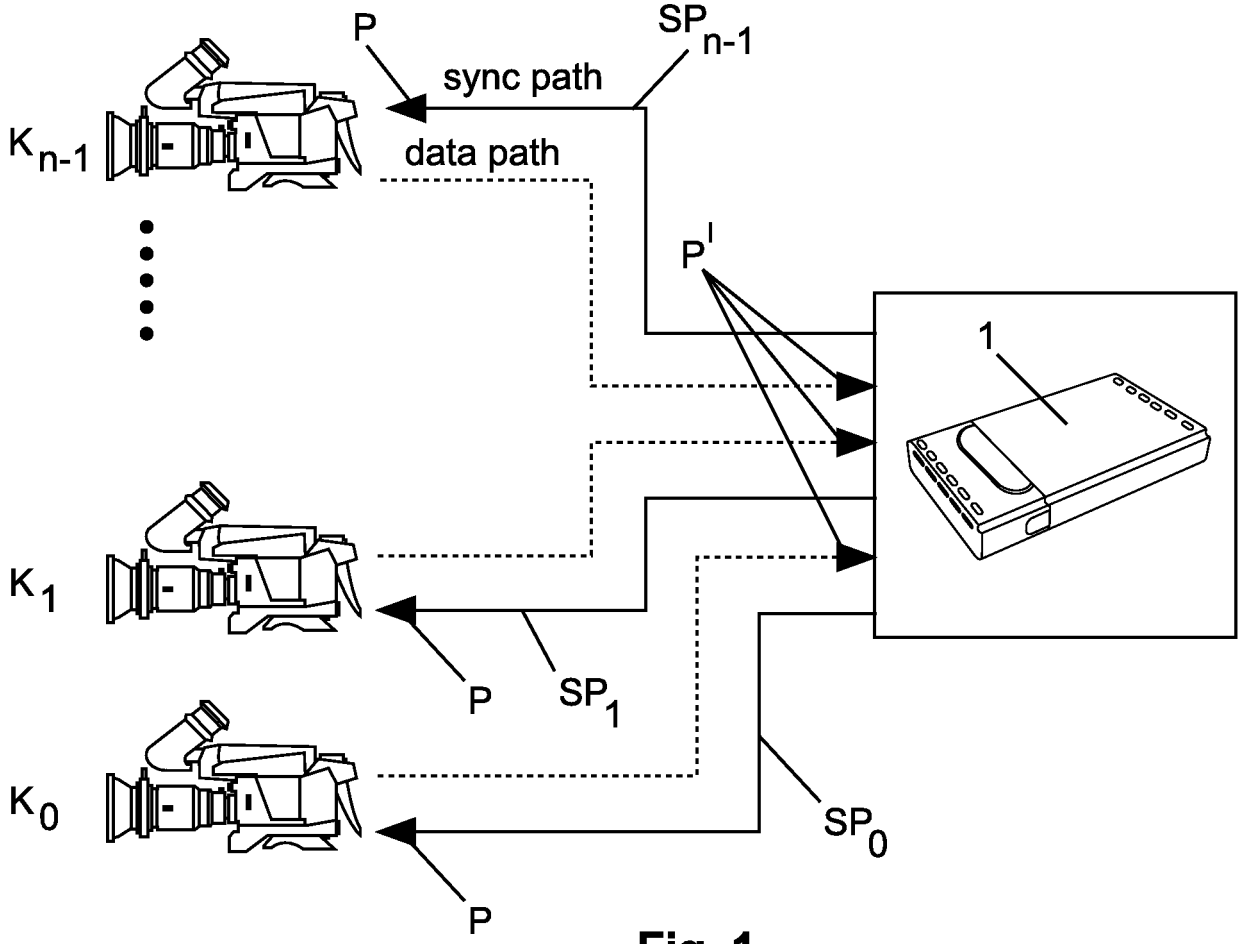

P
SP n-1
sync path
data path
K n-1
P'
1
K 1
P
SP 1
K 0
SP 0
P

Fig. 1

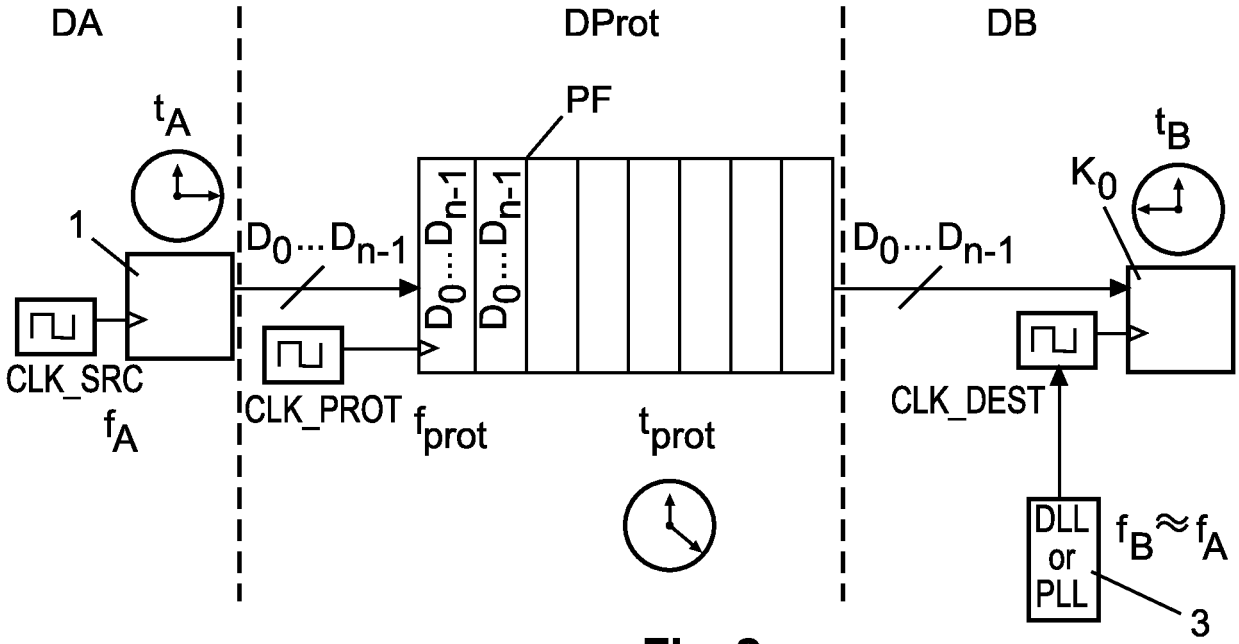

DA
DProt
DB
t A
PF
t B
K 0
1
D0...Dn-1
D0...Dn-1
D0...Dn-1
D0...Dn-1
CLK_SRC
f A
CLK_PROT
f prot
t prot
CLK_DEST
DLL
or
PLL
f B ≈ f A
3

Fig. 2

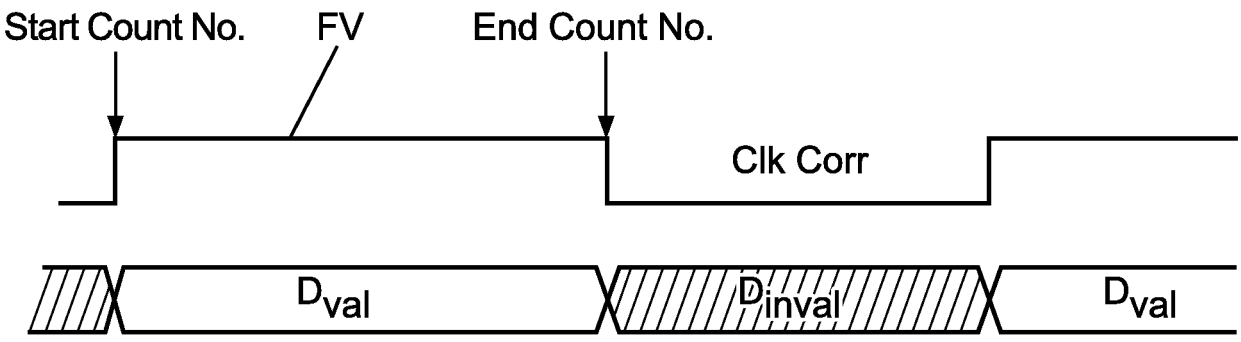

Start Count No.
FV
End Count No.
Clk Corr
Dval
Dinval
Dval

Fig. 3

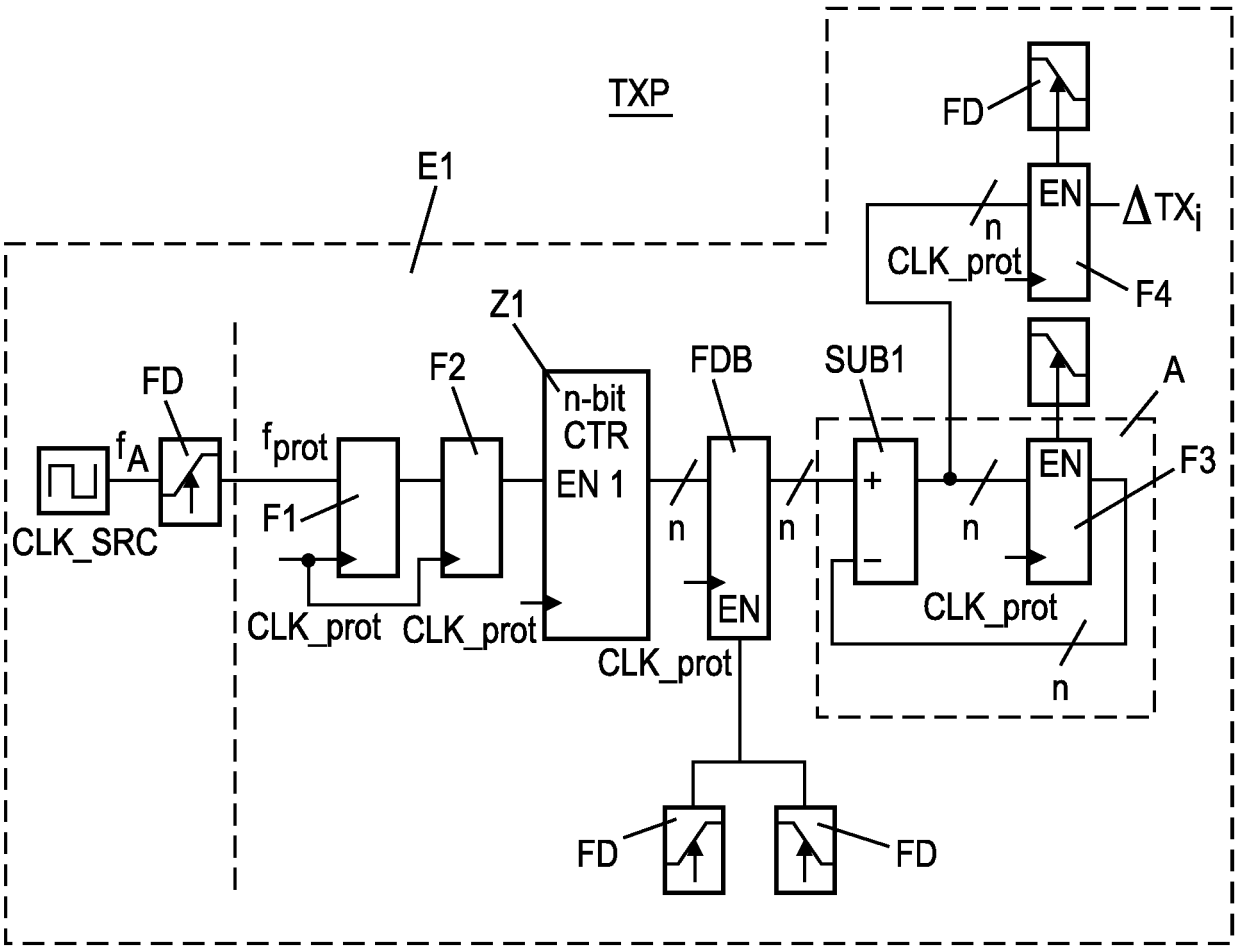

TXP
E1
FD
EN
ΔTXi
n
CLK_prot
F4
Z1
FD
F2
n-bit
CTR
EN 1
FDB
SUB1
A
fA
fprot
F1
CLK_SRC
CLK_prot
CLK_prot
CLK_prot
n
n
n
EN
EN
F3
CLK_prot
n
FD
FD

Fig. 4

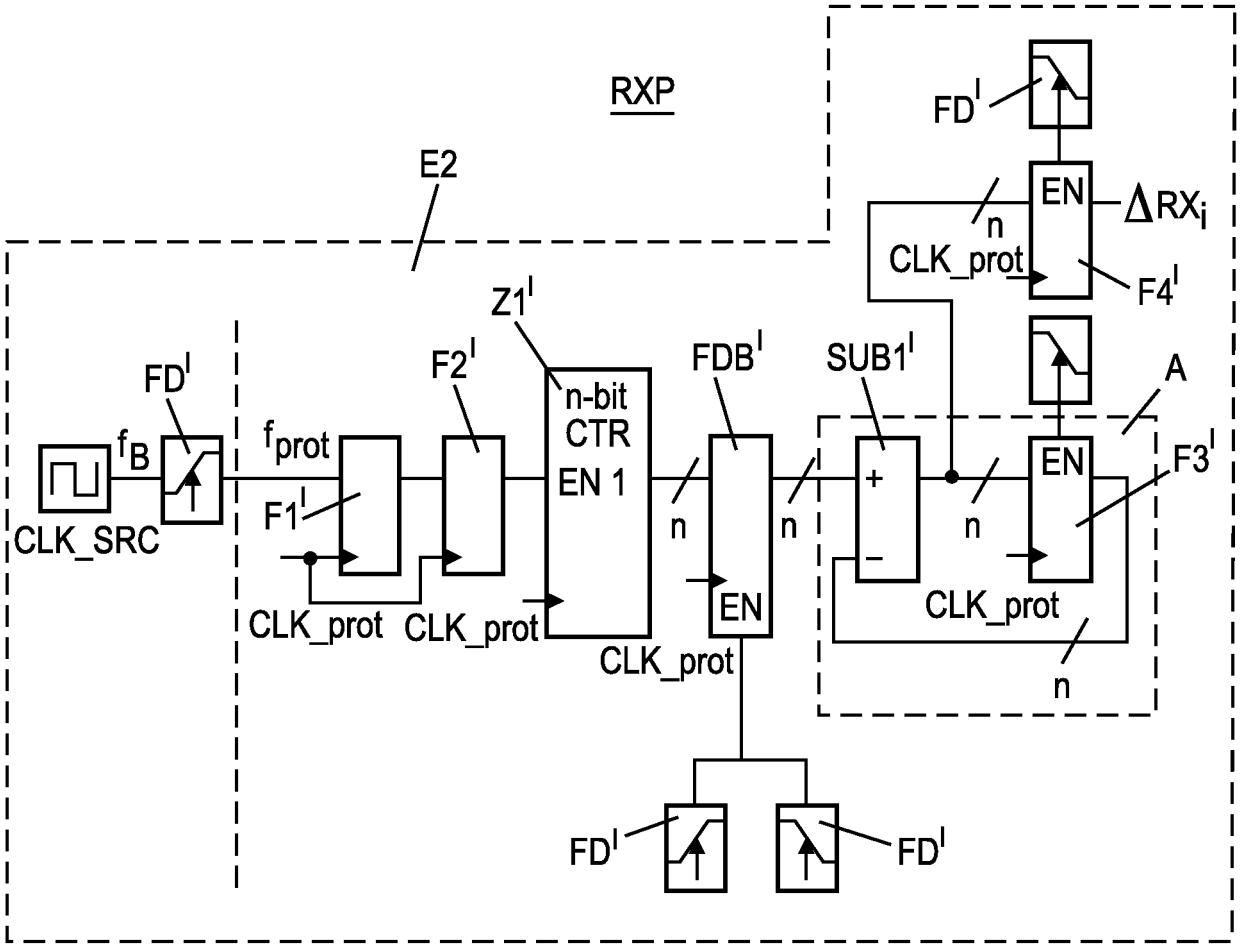

RXP
E2
FD
EN
ΔRXi
n
CLK_prot
F4
Z1
FD
F2
n-bit
CTR
EN 1
FDB
SUB1
A
fB
fprot
F1
CLK_SRC
CLK_prot
CLK_prot
CLK_prot
EN
+
−
EN
F3
n
n
n
n
CLK_prot
n
FD
FD

Fig. 5a

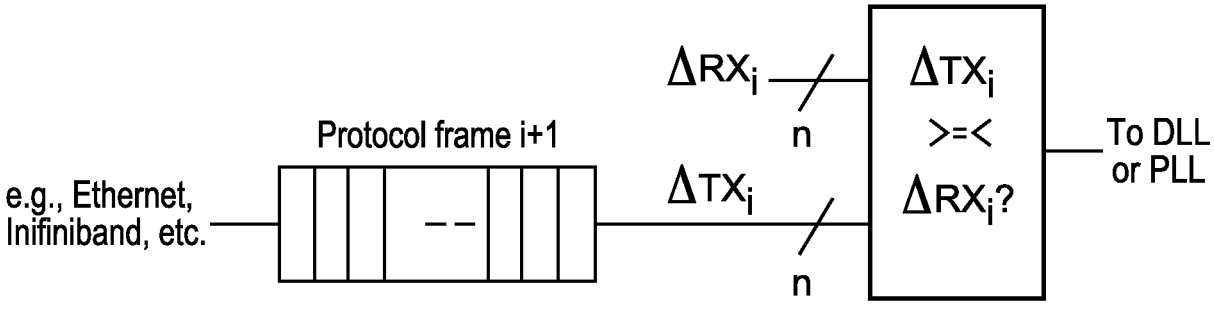

ΔRXi
n
ΔTXi
>=<
ΔRXi?
To DLL
or PLL
Protocol frame i+1
e.g., Ethernet,
Inifiniband, etc.
ΔTXi
n

Fig. 5b

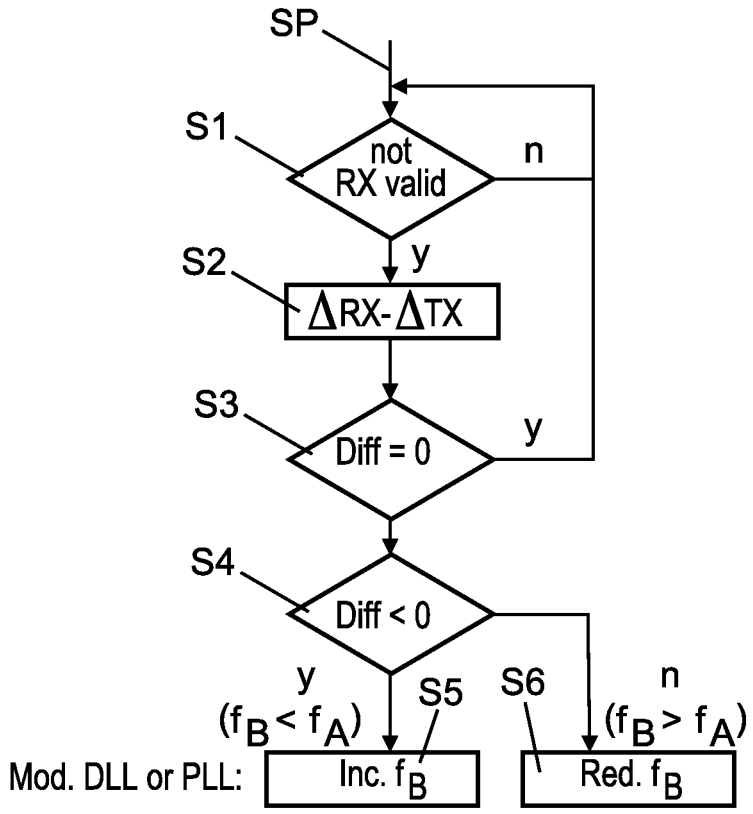

SP
S1
not
RX valid
n
y
S2
ΔRX-ΔTX
S3
Diff = 0
y
S4
Diff < 0
y
(fB< fA)
S5
S6
n
(fB> fA)
Mod. DLL or PLL:
Inc. fB
Red. fB

Fig. 6

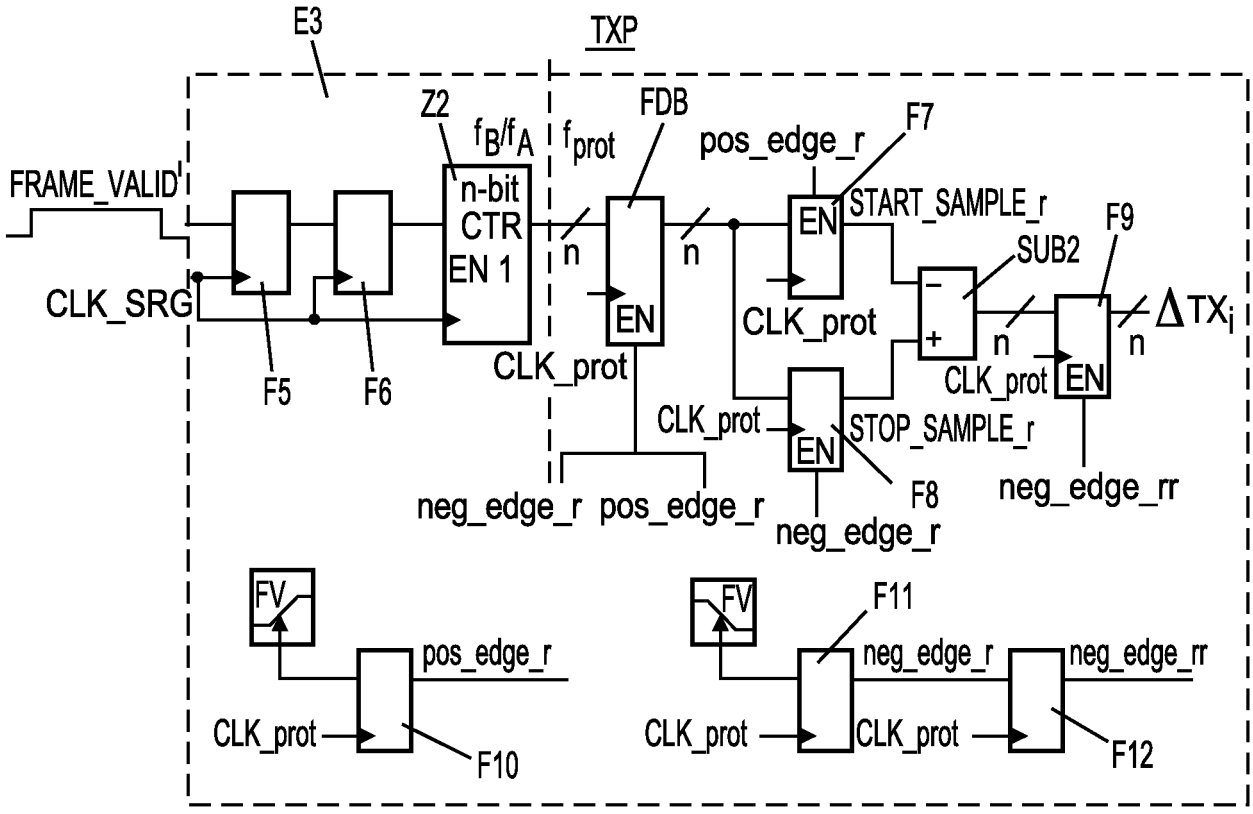

E3
TXP
Z2
fB/fA
fprot
FDB
pos_edge_r
F7
FRAME_VALID
n-bit
CTR
EN 1
START_SAMPLE_r
SUB2
F9
CLK_SRG
n
n
EN
CLK_prot
ΔTXi
F5
F6
CLK_prot
CLK_prot
EN
CLK_prot
EN
STOP_SAMPLE_r
F8
neg_edge_rr
neg_edge_r
pos_edge_r
neg_edge_r
FV
FV
F11
pos_edge_r
neg_edge_r
neg_edge_rr
CLK_prot
F10
CLK_prot
CLK_prot
F12

Fig. 7

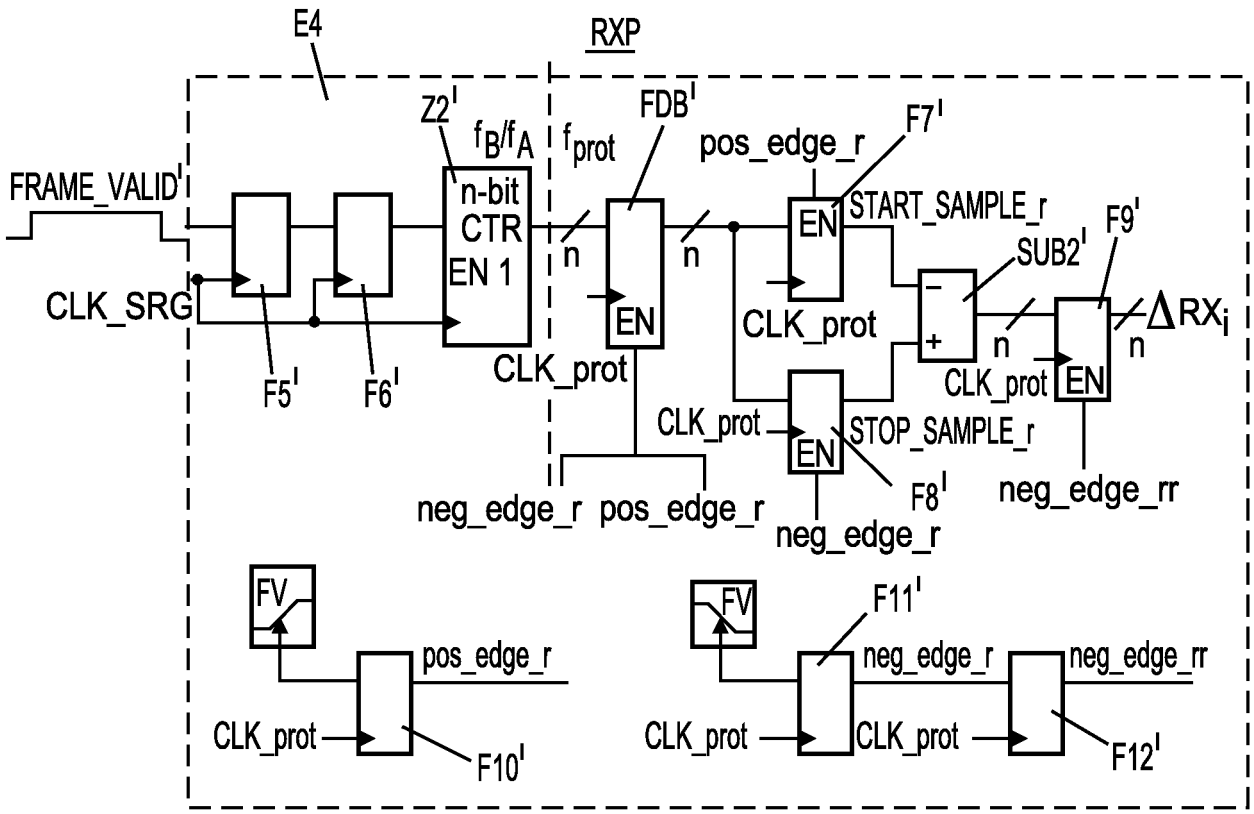

E4
RXP
Z2'
f_B/f_A
f_{prot}
FDB'
pos_edge_r
F7'
FRAME_VALID'
n-bit
CTR
EN 1
EN
START_SAMPLE_r
F9'
SUB2'
CLK_SRG
n
n
CLK_prot
F5'
F6'
CLK_prot
CLK_prot
n
n
ΔRX_i
CLK_prot
EN
CLK_prot
STOP_SAMPLE_r
F8'
neg_edge_r
pos_edge_r
neg_edge_r
neg_edge_rr
FV
FV
F11'
pos_edge_r
neg_edge_r
neg_edge_rr
CLK_prot
CLK_prot
CLK_prot
F10'
F12'

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/061641

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04J3/06 H04H60/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04J H04H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 339 182 A2 (SONY UK LTD [GB]) 27 August 2003 (2003-08-27) abstract paragraph [0001] paragraph [0008] paragraph [0013] - paragraph [0014] paragraph [0021] - paragraph [0025] paragraph [0040] figures 1,5	1-19
X	US 2008/019398 A1 (GENOSSAR MICHAEL [IL] ET AL) 24 January 2008 (2008-01-24) paragraph [0001] paragraph [0123] paragraph [0165] - paragraph [0166] figures 4,5	1-19

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
3 December 2009	10/12/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Fax: (+31–70) 340–3016	Marongiu, M

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/061641

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Information on patent family members

International application No
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