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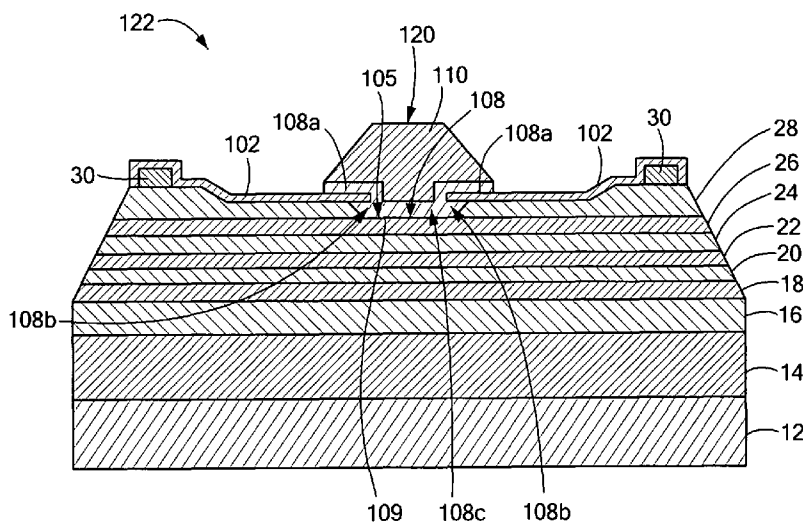
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(54) Title: ATOMIC LAYER DEPOSITION IN THE FORMATION OF GATE STRUCTURES FOR III-V SEMICONDUCTOR



(57) Abstract: A semiconductor structure having a recess (105) and a dielectric film (102) is disposed on and in contact with the semiconductor. The dielectric film has an aperture (104) therein. Portions of the dielectric film are disposed adjacent to the aperture and overhang underlying portions of the recess. An electric contact (108) has first portions (108a) thereof disposed on said adjacent portions of the dielectric film, second portions (108b) disposed on said underlying portions of the recess, with portions of the dielectric film being disposed between said first portion of the electric contact and the second portions of the electric contact, and third portions of the electric contact being disposed on and in contact with a bottom portion (109) of the recess in the semiconductor structure. The electric contact is formed by atomic layer deposition of an electrically conductive material over the dielectric film and through the aperture in such dielectric film.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER  
INV. H01L21/335 H01L21/285

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)  
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	figure 2c	3-7,9-18
Y	JESSEN G H ET AL: "Gate optimization of AlGaIn/GaN HEMTs using WSi, Ir, Pd, and Ni Schottky contacts" GAAS IC SYMPOSIUM. 25TH. ANNUAL IEEE GALLIUM ARSENIDE INTEGRATED CIRCUIT SYMPOSIUM. TECHNICAL DIGEST 2003. SAN DIEGO, CA, NOV. 9 - 12, 2003, GAAS IC SYMPOSIUM - IEEE GALLIUM ARSENIDE INTEGRATED CIRCUIT SYMPOSIUM, NEW YORK, NY : IEEE, US, 9 November 2003 (2003-11-09), pages 277-279, XP010673675 ISBN: 0-7803-7833-4 the whole document	3-6,9-18

Further documents are listed in the continuation of Box C.  See patent family annex.

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	paragraph [0019] - paragraph [0030]; figures 1A-1H	1-6,8-18
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