



(51) International Patent Classification:

H01L 31/0392 (2006.01) *H01L 31/077* (2012.01)
H01L 31/036 (2006.01) *H01L 31/18* (2006.01)

(21) International Application Number:

PCT/US2016/024120

(22) International Filing Date:

24 March 2016 (24.03.2016)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

14/672,072 27 March 2015 (27.03.2015) US

(71) Applicant: **SUNPOWER CORPORATION** [US/US]; 77
Rio Robles, San Jose, California 95134 (US).(72) Inventors: **RIM, Seung Bum**; 1618 Sand Hill Road, Apt.
319, Palo Alto, California 94304 (US). **SMITH, David D.**;
426 North Milton Avenue, Campbell, California 95008
(US). **JOHNSON, Michael C.**; 832 Oak Street, Alameda,
California 94501 (US). **SIMMONS, Christine Bourdet**;
846 Schiele Avenue, San Jose, California 95126 (US).(74) Agents: **VINCENT, Lester J.** et al.; **BLAKELY SOKO-**
LOFF TAYLOR & ZAFMAN LLP, 1279 Oakmead Park-
way, Sunnyvale, California 94085 (US).

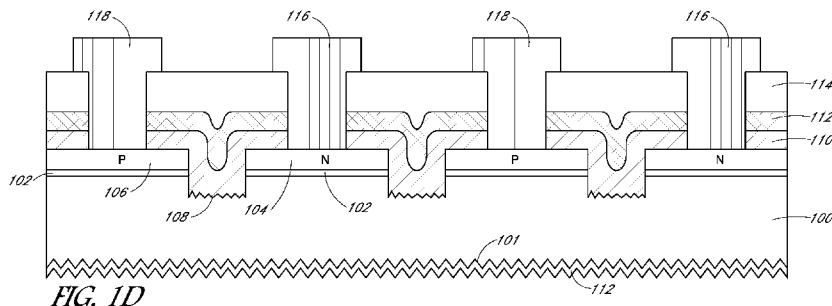
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) Title: PASSIVATION LAYER FOR SOLAR CELLS



(57) Abstract: Methods of fabricating solar cells having passivation layers, and the resulting solar cells, are described. In an example, a solar cell includes a substrate having a first surface and a second surface. A plurality of emitter regions is disposed on the first surface of the substrate and spaced apart from one another. An amorphous silicon passivation layer is disposed on each of the plurality of emitter regions and between each of the plurality of emitter regions, directly on an exposed portion of the first surface of the substrate.

PASSIVATION LAYER FOR SOLAR CELLS

TECHNICAL FIELD

[0001] Embodiments of the present disclosure are in the field of renewable energy and, in particular, methods of fabricating solar cells having passivation layers, and the resulting solar cells.

BACKGROUND

[0002] Photovoltaic cells, commonly known as solar cells, are well known devices for direct conversion of solar radiation into electrical energy. Generally, solar cells are fabricated on a semiconductor wafer or substrate using semiconductor processing techniques to form a p-n junction near a surface of the substrate. Solar radiation impinging on the surface of, and entering into, the substrate creates electron and hole pairs in the bulk of the substrate. The electron and hole pairs migrate to p-doped and n-doped regions in the substrate, thereby generating a voltage differential between the doped regions. The doped regions are connected to conductive regions on the solar cell to direct an electrical current from the cell to an external circuit coupled thereto.

[0003] Efficiency is an important characteristic of a solar cell as it is directly related to the capability of the solar cell to generate power. Likewise, efficiency in producing solar cells is directly related to the cost effectiveness of such solar cells. Accordingly, techniques for increasing the efficiency of solar cells, or techniques for increasing the efficiency in the manufacture of solar cells, are generally desirable. Some embodiments of the present disclosure allow for increased solar cell manufacture efficiency by providing novel processes for fabricating solar cell structures. Some embodiments of the present disclosure allow for increased solar cell efficiency by providing novel solar cell structures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figures 1A-1D illustrate cross-sectional views of various stages in the fabrication of a solar cell, in accordance with an embodiment of the present disclosure, wherein:

[0005] Figure 1A illustrates a cross-sectional view of a stage in solar cell fabrication involving forming a plurality of emitter regions on a first surface of a substrate;

[0006] Figure 1B illustrates a cross-sectional view of the structure of Figure 1A following forming an amorphous silicon passivation layer over each of the plurality of emitter regions and between each of the plurality of emitter regions;

[0007] Figure 1C illustrates a cross-sectional view of the structure of Figure 1B following forming a silicon nitride layer on the amorphous silicon passivation layer; and

[0008] Figure 1D illustrates a cross-sectional view of the structure of Figure 1C following forming a plurality of conductive contacts to the plurality of emitter regions.

[0009] Figures 2A-2B illustrate cross-sectional views of various stages in the fabrication of a solar cell, in accordance with another embodiment of the present disclosure, wherein:

[0010] Figure 2A illustrates a cross-sectional view of a stage in solar cell fabrication involving forming a plurality of emitter regions on a first surface of a substrate and forming a dielectric layer on each of the plurality of emitter regions and between each of the plurality of emitter regions; and

[0011] Figure 2B illustrates a cross-sectional view of the structure of Figure 2A following forming a plurality of conductive contacts to the plurality of emitter regions.

[0012] Figure 3 is a flowchart listing operations in a method of fabricating a solar cell as corresponding to Figures 1A-1D or 2A-2B, in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0013] The following detailed description is merely illustrative in nature and is not intended to limit the embodiments of the subject matter or the application and uses of such embodiments. As used herein, the word “exemplary” means “serving as an example, instance, or illustration.” Any implementation described herein as exemplary is not necessarily to be construed as preferred or advantageous over other implementations. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.

[0014] This specification includes references to “one embodiment” or “an embodiment.” The appearances of the phrases “in one embodiment” or “in an embodiment” do not necessarily refer to the same embodiment. Particular features, structures, or characteristics may be combined in any suitable manner consistent with this disclosure.

[0015] Terminology. The following paragraphs provide definitions and/or context for terms found in this disclosure (including the appended claims):

[0016] “Comprising.” This term is open-ended. As used in the appended claims, this term does not foreclose additional structure or steps.

[0017] “Configured To.” Various units or components may be described or claimed as “configured to” perform a task or tasks. In such contexts, “configured to” is used to connote structure by indicating that the units/components include structure that performs those task or tasks during operation. As such, the unit/component can be said to be configured to perform the task even when the specified unit/component is not currently operational (e.g., is not on/active). Reciting that a unit/circuit/component is “configured to” perform one or more tasks is expressly intended not to invoke 35 U.S.C. §112, sixth paragraph, for that unit/component.

[0018] “First,” “Second,” etc. As used herein, these terms are used as labels for nouns that they precede, and do not imply any type of ordering (e.g., spatial, temporal, logical, etc.). For example, reference to a “first” solar cell does not necessarily imply that this solar cell is the

first solar cell in a sequence; instead the term “first” is used to differentiate this solar cell from another solar cell (e.g., a “second” solar cell).

[0019] “Coupled” – The following description refers to elements or nodes or features being “coupled” together. As used herein, unless expressly stated otherwise, “coupled” means that one element/node/feature is directly or indirectly joined to (or directly or indirectly communicates with) another element/node/feature, and not necessarily mechanically.

[0020] “Inhibit” – As used herein, inhibit is used to describe a reducing or minimizing effect. When a component or feature is described as inhibiting an action, motion, or condition it may completely prevent the result or outcome or future state completely. Additionally, “inhibit” can also refer to a reduction or lessening of the outcome, performance, and/or effect which might otherwise occur. Accordingly, when a component, element, or feature is referred to as inhibiting a result or state, it need not completely prevent or eliminate the result or state.

[0021] In addition, certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, and “below” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, “side”, “outboard”, and “inboard” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

[0022] Methods of fabricating solar cells having passivation layers, and the resulting solar cells, are described herein. In the following description, numerous specific details are set forth, such as specific process flow operations, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known fabrication techniques, such as lithography and patterning techniques,

are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the figures are illustrative representations and are not necessarily drawn to scale.

[0023] Disclosed herein are solar cells. In one embodiment, a solar cell includes a substrate having a first surface and a second surface. A plurality of emitter regions is disposed on the first surface of the substrate and spaced apart from one another. An amorphous silicon passivation layer is disposed on each of the plurality of emitter regions and between each of the plurality of emitter regions, directly on an exposed portion of the first surface of the substrate.

[0024] In another embodiment, a solar cell includes a substrate having a first surface and a second surface. A plurality of emitter regions is disposed on the first surface of the substrate and spaced apart from one another. A dielectric layer is disposed on each of the plurality of emitter regions and between each of the plurality of emitter regions, directly on an exposed portion of the first surface of the substrate. An amorphous silicon passivation layer is disposed on the dielectric layer.

[0025] Also disclosed herein are methods of fabricating solar cells. In one embodiment, a method of fabricating a solar cell involves forming a plurality of emitter regions on a first surface of a substrate, each of the plurality of emitter regions spaced apart from one another. The method also involves forming an amorphous silicon passivation layer over each of the plurality of emitter regions and between each of the plurality of emitter regions.

[0026] One or more embodiments described herein are directed to methods of fabricating solar cells with multilayer passivation of polysilicon emitters of the solar cells. In one such embodiment, the passivation of a polysilicon/tunnel oxide/Si interface is improved by using an amorphous silicon (a-Si) or a-Si and silicon nitride (SiN) layer structure formed on top of polysilicon emitter regions. The passivation layers or passivation layer stacks described herein may be fabricated without the use of new tooling or manufacturing arrangements.

[0027] To provide context, a polysilicon/tunnel oxide/Si interface provides for very low saturation current density (J_0) to enable solar cells to exhibit high efficiency. However, options for achieving a low J_0 have been limited thus far. For example, the use of new tunnel oxide materials such as a nitride oxide or the use of nitridation has been employed to suppress out-diffusion. However, the use of such materials and processes often require expensive new processing or new tool development, and the method may be limited to use of boron-doped polycrystalline silicon emitter regions. In a particular example, P-poly J_0 has been limited at 6fA/cm^2 with state of the art processing, while N-poly J_0 is close to 1fA/cm^2 . P-poly J_0 reduction will result in efficiency improvement, but such reduction has not been achievable to date.

[0028] Addressing one or more of the above issues, in an embodiment, passivation of a polysilicon emitter is enhanced by implementing a multilayer structure deposited thereon. In one such embodiment, an a-Si layer is included in a bottom anti-reflective coating (BARC) stack to improve passivation quality of polysilicon emitter regions below the stack.

[0029] In an exemplary process flow, Figures 1A-1D illustrate cross-sectional views of various stages in the fabrication of a solar cell, in accordance with an embodiment of the present disclosure. Figure 3 is a flowchart 300 listing operations in a method of fabricating a solar cell as corresponding to Figures 1A-1D, in accordance with an embodiment of the present disclosure.

[0030] Referring to Figure 1A and corresponding operation 302 of flowchart 300, a plurality of alternating N-type and P-type semiconductor regions are formed above a substrate. In particular, a substrate 100 has disposed there above N-type semiconductor regions 104 and P-type semiconductor regions 106 disposed on a thin dielectric material 102 as an intervening material between the N-type semiconductor regions 104 or P-type semiconductor regions 106, respectively, and the substrate 100. The substrate 100 has a light-receiving surface 101 opposite a back surface above which the N-type semiconductor regions 104 and P-type

semiconductor regions 106 are formed. In an embodiment, as depicted in Figure 1A, each of the plurality of emitter regions 104 and 106 is spaced apart from one another.

[0031] In an embodiment, the substrate 100 is a monocrystalline silicon substrate, such as a bulk single crystalline N-type doped silicon substrate. It is to be appreciated, however, that substrate 100 may be a layer, such as a multi-crystalline silicon layer, disposed on a global solar cell substrate. In an embodiment, the thin dielectric layer 102 is a tunneling silicon oxide layer having a thickness of approximately 2 nanometers or less. In one such embodiment, the term “tunneling dielectric layer” refers to a very thin dielectric layer, through which electrical conduction can be achieved. The conduction may be due to quantum tunneling and/or the presence of small regions of direct physical connection through thin spots in the dielectric layer. In one embodiment, the tunneling dielectric layer is or includes a thin silicon oxide layer.

[0032] In an embodiment, the alternating N-type and P-type semiconductor regions 104 and 106, respectively, are polycrystalline silicon regions formed by, e.g., using a plasma-enhanced chemical vapor deposition (PECVD) process. In one such embodiment, the N-type polycrystalline silicon emitter regions 104 are doped with an N-type impurity, such as phosphorus. The P-type polycrystalline silicon emitter regions 106 are doped with a P-type impurity, such as boron. As is depicted in Figure 1A, the alternating N-type and P-type semiconductor regions 104 and 106 may have trenches 108 formed there between, the trenches 108 extending partially into the substrate 100.

[0033] In an embodiment, the light receiving surface 101 is a texturized light-receiving surface, as is depicted in Figure 1A. In one embodiment, a hydroxide-based wet etchant is employed to texturize the light receiving surface 101 of the substrate 100 and, possibly, the trench 108 surfaces as is also depicted in Figure 1A. It is to be appreciated that the timing of the texturizing of the light receiving surface may vary. For example, the texturizing may be performed before or after the formation of the thin dielectric layer 102. In an embodiment, a

texturized surface may be one which has a regular or an irregular shaped surface for scattering incoming light, decreasing the amount of light reflected off of the light receiving surface 101 of the solar cell. Referring again to Figure 1A, additional embodiments can include formation of a passivation and/or anti-reflective coating (ARC) layers (shown collectively as layer 112) on the light-receiving surface 101. It is to be appreciated that the timing of the formation of passivation and/or ARC layers may also vary.

[0034] Referring to Figure 1B and corresponding operation 306 of flowchart 300, the method also involves forming an amorphous silicon passivation layer 110 over each of the plurality of emitter regions 104 and 106, and between each of the plurality of emitter regions 104 and 106.

[0035] In an embodiment, as is depicted in Figure 1B, a portion of the amorphous silicon passivation layer 110 is formed directly on an exposed portion 108 of the first surface of the substrate 100. In an embodiment, the amorphous silicon passivation layer 110 is formed by depositing amorphous silicon via plasma-enhanced chemical vapor deposition (PECVD). In one such embodiment, the PECVD process is performed at a temperature below approximately 400 degrees Celsius.

[0036] In an embodiment, the amorphous silicon passivation layer 110 is an amorphous intrinsic silicon layer. In one such embodiment, a total composition of the amorphous intrinsic silicon layer has a total hydrogen concentration approximately in the range of 5-30 atomic % of total film composition. In one embodiment, the amorphous intrinsic silicon layer has a thickness approximately in the range of 3 – 15 nanometers. In an embodiment, either during formation the amorphous silicon passivation layer 110, or at a subsequent processing operation such as during annealing operation 310 described below, the method involves driving hydrogen from the amorphous silicon passivation layer 110 to an interface of the plurality of emitter regions 104 and 106 and the substrate 100.

[0037] Referring to Figure 1C and corresponding optional operation 308 of flowchart 300, the method of fabricating a solar cell involves forming a silicon nitride layer 112 on the amorphous silicon passivation layer 110. The silicon nitride layer may be included to provide at least some level of reflective or light-trapping attributes above the emitter regions 104 and 106. It is to be appreciated that other dielectrics may be suitable in place of silicon nitride. For example, other embodiments may involve the use of silicon oxynitride or silicon oxide for layer 112 described herein.

[0038] In an embodiment, referring to optional operation 310 of flowchart 300, the substrate 100 (and, hence, the amorphous silicon passivation layer 110) is thermally annealed. In one such embodiment, the thermal annealing is performed at a temperature approximately in the range of 300-550 degrees Celsius. In an embodiment, the thermal annealing is performed subsequent to forming the silicon nitride layer 112 (if present) on the amorphous silicon passivation layer 110.

[0039] Referring to Figure 1D and corresponding optional operation 312 of flowchart 300, conductive contacts 116 and 118 are fabricated to contact the N-type 104 and P-type 106 doped polycrystalline silicon emitter regions, respectively. In an embodiment, the contacts 116 and 118 are fabricated by first depositing and patterning an insulating layer 114 to have openings and then forming one or more conductive layers in the openings. As is also depicted in Figure 1D, the contact openings are also formed through the amorphous silicon passivation layer 110 and, if present, the silicon nitride layer 112 in order to expose the N-type 104 and P-type 106 doped polycrystalline silicon emitter regions.

[0040] In an embodiment, the conductive contacts 116 and 118 include metal and are formed by a deposition, lithographic, and etch approach or, alternatively, a printing process. In an exemplary embodiment, a metal seed layer is formed on the exposed portions of the P-type emitter regions 106 and on the N-type emitter regions 104. A metal layer is then plated on the metal seed layer to form conductive contacts 116 and 118, respectively, for the P-type emitter

regions 106 and the N-type emitter regions 124. In an embodiment, the metal seed layer is an aluminum-based metal seed layer, and the metal layer is a copper layer.

[0041] With reference again to Figure 1D, in a first embodiment, a finalized solar cell includes a substrate 100 having a first surface and a second surface 101. A plurality of emitter regions 104 and 106 is disposed on the first surface of the substrate 100 and spaced apart from one another. An amorphous silicon passivation layer 110 is disposed on each of the plurality of emitter regions 104 and 106, and between each of the plurality of emitter regions 104 and 106. The amorphous silicon passivation layer 110 is disposed directly on an exposed portion 108 of the first surface of the substrate 100.

[0042] In an embodiment, the substrate 100 is a lightly doped N-type monocrystalline substrate having a phosphorous doping concentration approximately in the range of $1\text{E}14\text{-}1\text{E}16$ atoms/ cm^3 at the exposed portion 108 of the first surface of the substrate 100. In one such embodiment, the amorphous silicon passivation layer 110 is an amorphous intrinsic silicon layer. In a particular such embodiment, a total composition of the amorphous intrinsic silicon layer has a total hydrogen concentration approximately in the range of 5-30 atomic % of total film composition. In another particular such embodiment, the amorphous intrinsic silicon layer has a thickness approximately in the range of 3 – 15 nanometers.

[0043] Referring again to Figure 1D, in an embodiment, each of the plurality of emitter regions 104 and 106 is separated from one another by a plurality of trenches 108 disposed in the first surface of the substrate 100. In one such embodiment, the amorphous silicon passivation layer 110 is disposed in the plurality of trenches 108, as is depicted in Figure 1D. In an embodiment, the solar cell further includes a silicon nitride layer 112 disposed on the amorphous silicon passivation layer 110, as is also depicted in Figure 1D. In one such embodiment, the silicon nitride layer 112 has a thickness approximately in the range of 30 – 100 nanometers. In an embodiment, the solar cell further includes a plurality of conductive contacts 116 and 118 electrically connected to corresponding ones of the plurality of emitter

regions 104 and 106. The plurality of conductive contacts 116 and 118 is formed through the silicon nitride layer 112 (if present) and the amorphous silicon passivation layer 110, as is depicted in Figure 1D.

[0044] In an embodiment, the solar cell of Figure 1D is a back contact solar cell, as is depicted in Figure 1D. Accordingly, the surface 101 is a light-receiving surface of the substrate 100, and the plurality of emitter regions 104 and 106 is a plurality of alternating N-type and P-type polycrystalline silicon emitter regions, each disposed on a thin dielectric layer 102 disposed a back surface of the substrate 100. In another embodiment, not depicted in Figure 1D, the solar cell is a front contact solar cell having one type (N- or P-) of emitter region on surface 101 of substrate 100, and the other type of emitter region on the opposing surface of substrate 100. In the latter embodiment, a second amorphous silicon passivation layer may be included as a passivation layer such that both types of emitter regions have an accompanying passivation layer on their respective sides of substrate 100.

[0045] In another exemplary process flow, Figures 2A-2B illustrate cross-sectional views of various stages in the fabrication of a solar cell, in accordance with an embodiment of the present disclosure. Figure 3 is a flowchart 300 listing operations in a method of fabricating a solar cell as corresponding to Figures 2A-2B, in accordance with an embodiment of the present disclosure.

[0046] Referring to Figure 2A, using the structure described in association with Figure 1A as a starting point, and to corresponding operation 304 of flowchart 300, a dielectric layer (202 and 204) is formed on each of the plurality of emitter regions 104 and 106 (see dielectric layer portions 204) and between each of the plurality of emitter regions 104 and 106, directly on an exposed portion 108 of the first surface of the substrate 100 (see dielectric layer portions 202). In an embodiment, one or both of dielectric layer portions 202 and 204 is formed in an oxidation process and is a thin oxide layer. In another embodiment, one or both of dielectric

layer portions 202 and 204 is formed in a deposition process and is a thin silicon nitride layer or silicon oxynitride layer.

[0047] Referring to Figure 2B and corresponding operation 306 of flowchart 300, the method also involves forming an amorphous silicon passivation layer 110 over each of the plurality of emitter regions 104 and 106, and between each of the plurality of emitter regions 104 and 106. As depicted in Figure 2B, in an embodiment, the amorphous silicon passivation layer 110 is formed directly on the dielectric layer (combination of 202 and 204).

[0048] In an embodiment, the amorphous silicon passivation layer 110 is formed by depositing amorphous silicon via plasma-enhanced chemical vapor deposition (PECVD). In one such embodiment, the PECVD process is performed at a temperature below approximately 400 degrees Celsius. In an embodiment, the amorphous silicon passivation layer 110 is a layer such as, but not limited to, an amorphous intrinsic silicon layer, an amorphous N-type silicon layer, or an amorphous P-type silicon layer. In one such embodiment, a total composition of the amorphous silicon passivation layer has a total hydrogen concentration approximately in the range of 5-30 atomic % of total film composition. In one embodiment, the amorphous silicon passivation layer 110 has a thickness approximately in the range of 3 – 15 nanometers. In an embodiment, either during formation the amorphous silicon passivation layer 110, or at a subsequent processing operation such as during annealing operation 310 described below, the method involves driving hydrogen from the amorphous silicon passivation layer 110 to an interface of the plurality of emitter regions 104 and 106 and the substrate 100.

[0049] Referring again to Figure 2B and corresponding optional operation 308 of flowchart 300, the method of fabricating a solar cell involves forming a silicon nitride layer 112 on the amorphous silicon passivation layer 110. The silicon nitride layer may be included to provide at least some level of reflective or light trapping attributes above the emitter regions 104 and 106.

[0050] In an embodiment, referring to optional operation 310 of flowchart 300, the substrate 100 (and, hence, the amorphous silicon passivation layer 110) is thermally annealed. In one such embodiment, the thermal annealing is performed at a temperature approximately in the range of 300-550 degrees Celsius. In an embodiment, the thermal annealing is performed subsequent to forming the silicon nitride layer 112 (if present) on the amorphous silicon passivation layer 110.

[0051] Referring again to Figure 2B and corresponding optional operation 312 of flowchart 300, conductive contacts 116 and 118 are fabricated to contact the N-type 104 and P-type 106 doped polycrystalline silicon emitter regions, respectively. In an embodiment, the contacts 116 and 118 are fabricated by first depositing and patterning an insulating layer 114 to have openings and then forming one or more conductive layers in the openings. As is also depicted in Figure 2B, the contact openings are also formed through the amorphous silicon passivation layer 110 and, if present, the silicon nitride layer 112. Furthermore, the contact openings are also formed through the dielectric layer 204 in order to expose the N-type 104 and P-type 106 doped polycrystalline silicon emitter regions. The conductive contacts of Figure 2B may be fabricated in a similar manner as described in association with conductive contacts 116 and 118 of Figure 1D.

[0052] With reference again to Figure 2B, in a second embodiment, a finalized solar cell includes a substrate 100 having a first surface and a second surface 101. A plurality of emitter regions 104 and 106 is disposed on the first surface of the substrate 100 and spaced apart from one another. A dielectric layer (combination of 202 and 204) is disposed on each of the plurality of emitter regions (dielectric layer 204 disposed on each of emitter regions 104 and 106), and between each of the plurality of emitter regions 104 and 106, directly on an exposed portion 108 of the first surface of the substrate 100 (dielectric layer 202 disposed directly on region 108 of substrate 100). An amorphous silicon passivation layer 110 is disposed on the dielectric layer 202/204.

[0053] In an embodiment, the substrate 100 is an N-type monocrystalline substrate having a phosphorous doping concentration approximately in the range of $1\text{E}18\text{-}1\text{E}20$ atoms/cm³ at the exposed portion 108 of the first surface of the substrate 100. In one such embodiment, the amorphous silicon passivation layer 110 is a layer such as, but not limited to, an amorphous intrinsic silicon layer, an amorphous N-type silicon layer, or an amorphous P-type silicon layer. In a particular such embodiment, a total composition of the amorphous silicon passivation layer 110 has a total hydrogen concentration approximately in the range of 5-30 atomic % of total film composition. In another particular such embodiment, the amorphous silicon passivation layer 110 has a thickness approximately in the range of 3 – 15 nanometers.

[0054] Referring again to Figure 2B, in an embodiment, each of the plurality of emitter regions 104 and 106 is separated from one another by a plurality of trenches 108 disposed in the first surface of the substrate 100. In one such embodiment, the portion 202 of the dielectric layer and the amorphous silicon passivation layer 110 are disposed in the plurality of trenches 108, as is depicted in Figure 2B. In an embodiment, the portion 202 of the dielectric layer is composed of silicon dioxide. In an embodiment, the solar cell further includes a silicon nitride layer 112 disposed on the amorphous silicon passivation layer 110, as is also depicted in Figure 2B. In one such embodiment, the silicon nitride layer 112 has a thickness approximately in the range of 30 – 100 nanometers. In an embodiment, the solar cell further includes a plurality of conductive contacts 116 and 118 electrically connected to corresponding ones of the plurality of emitter regions 104 and 106. The plurality of conductive contacts 116 and 118 is formed through the silicon nitride layer 112 (if present), through the amorphous silicon passivation layer 110, and through the portions 204 of the dielectric layer, as is depicted in Figure 2B.

[0055] In an embodiment, the solar cell of Figure 2B is a back contact solar cell, as is depicted in Figure 2B. Accordingly, the surface 101 is a light-receiving surface of the substrate 100, and the plurality of emitter regions 104 and 106 is a plurality of alternating N-type and P-

type polycrystalline silicon emitter regions, each disposed on a thin dielectric layer 102 disposed a back surface of the substrate 100. In another embodiment, not depicted in Figure 2B, the solar cell is a front contact solar cell having one type (N- or P-) of emitter region on surface 101 of substrate 100, and the other type of emitter region on the opposing surface of substrate 100. In the latter embodiment, a second amorphous silicon passivation layer may be included as a passivation layer such that both types of emitter regions have an accompanying passivation layer on their respective sides of substrate 100.

[0056] Although certain materials are described specifically with reference to above described embodiments, some materials may be readily substituted with others with other such embodiments remaining within the spirit and scope of embodiments of the present disclosure. For example, in an embodiment, a different material substrate, such as a group III-V material substrate, can be used instead of a silicon substrate. Additionally, although reference is made significantly to back contact solar cell arrangements, it is to be appreciated that approaches described herein may have application to front contact solar cells as well, examples of which are described briefly above. In other embodiments, the above described approaches can be applicable to manufacturing of other than solar cells. For example, manufacturing of light emitting diode (LEDs) may benefit from approaches described herein. Furthermore, it is to be appreciated that, where N+ and P+ type doping is described specifically, other embodiments contemplated include the opposite conductivity type, e.g., P+ and N+ type doping, respectively.

[0057] Thus, methods of fabricating solar cells having passivation layers, and the resulting solar cells, have been disclosed.

[0058] Although specific embodiments have been described above, these embodiments are not intended to limit the scope of the present disclosure, even where only a single embodiment is described with respect to a particular feature. Examples of features provided in the disclosure are intended to be illustrative rather than restrictive unless stated otherwise. The

above description is intended to cover such alternatives, modifications, and equivalents as would be apparent to a person skilled in the art having the benefit of this disclosure.

[0059] The scope of the present disclosure includes any feature or combination of features disclosed herein (either explicitly or implicitly), or any generalization thereof, whether or not it mitigates any or all of the problems addressed herein. Accordingly, new claims may be formulated during prosecution of this application (or an application claiming priority thereto) to any such combination of features. In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the appended claims.

CLAIMS

What is claimed is:

1. A solar cell, comprising:
 - a substrate having a first surface and a second surface;
 - a plurality of emitter regions disposed on the first surface of the substrate and spaced apart from one another;
 - an amorphous silicon passivation layer disposed on each of the plurality of emitter regions and between each of the plurality of emitter regions, directly on an exposed portion of the first surface of the substrate.
2. The solar cell of claim 1, wherein the substrate is a lightly doped N-type monocrystalline substrate having a phosphorous doping concentration approximately in the range of $1\text{E}14\text{--}1\text{E}16$ atoms/cm³ at the exposed portion of the first surface of the substrate.
3. The solar cell of claim 2, wherein the amorphous silicon passivation layer is an amorphous intrinsic silicon layer.
4. The solar cell of claim 3, wherein a total composition of the amorphous intrinsic silicon layer has a total hydrogen concentration approximately in the range of 5-30 atomic % of total film composition.
5. The solar cell of claim 3, wherein the amorphous intrinsic silicon layer has a thickness approximately in the range of 3 – 15 nanometers.
6. The solar cell of claim 1, further comprising:

a silicon nitride layer disposed on the amorphous silicon passivation layer, the silicon nitride layer having a thickness approximately in the range of 30 – 100 nanometers.

7. The solar cell of claim 6, further comprising:

a plurality of conductive contacts electrically connected to corresponding ones of the plurality of emitter regions, the plurality of conductive contacts formed through the silicon nitride layer and the amorphous silicon passivation layer.

8. The solar cell of claim 1, wherein the solar cell is a back contact solar cell, the first surface is a back surface of the substrate, the second surface is a light-receiving surface of the substrate, and the plurality of emitter regions is a plurality of alternating N-type and P-type polycrystalline silicon emitter regions, each disposed on a thin dielectric layer disposed on the first surface of the substrate.

9. The solar cell of claim 1, wherein the plurality of emitter regions is a plurality of N-type polycrystalline silicon emitter regions, the solar cell further comprising:

a plurality of P-type emitter regions disposed on the second surface of the substrate and spaced apart from one another;

a second amorphous silicon passivation layer disposed over each of the plurality of P-type emitter regions and between each of the plurality of P-type emitter regions, directly on an exposed portion of the second surface of the substrate.

10. The solar cell of claim 1, wherein each of the plurality of emitter regions is separated from one another by a plurality of trenches disposed in the first surface of the substrate, wherein the amorphous silicon passivation layer is disposed in the plurality of trenches.

11. A solar cell, comprising:

a substrate having a first surface and a second surface;

a plurality of emitter regions disposed on the first surface of the substrate and spaced apart from one another;

a dielectric layer disposed on each of the plurality of emitter regions and between each of the plurality of emitter regions, directly on an exposed portion of the first surface of the substrate; and

an amorphous silicon passivation layer disposed on the dielectric layer.

12. The solar cell of claim 11, wherein the substrate is an N-type monocrystalline substrate having a phosphorous doping concentration approximately in the range of $1\text{E}18\text{-}1\text{E}20$ atoms/cm³ at the exposed portion of the first surface of the substrate.

13. The solar cell of claim 12, wherein the amorphous silicon passivation layer is a layer selected from the group consisting of an amorphous intrinsic silicon layer, an amorphous N-type silicon layer, and an amorphous P-type silicon layer.

14. The solar cell of claim 13, wherein a total composition of the amorphous silicon passivation layer has a total hydrogen concentration approximately in the range of 5-30 atomic % of total film composition.

15. The solar cell of claim 13, wherein the amorphous silicon passivation layer has a thickness approximately in the range of 3 – 15 nanometers.

16. The solar cell of claim 11, wherein the dielectric layer comprises a layer of silicon dioxide, the solar cell further comprising:

a silicon nitride layer disposed on the amorphous silicon passivation layer, the silicon nitride layer having a thickness approximately in the range of 30 – 100 nanometers.

17. The solar cell of claim 16, further comprising:

a plurality of conductive contacts electrically connected to corresponding ones of the plurality of emitter regions, the plurality of conductive contacts formed through the silicon nitride layer, the amorphous silicon passivation layer, and the dielectric layer.

18. The solar cell of claim 11, wherein the solar cell is a back contact solar cell, the first surface is a back surface of the substrate, the second surface is a light-receiving surface of the substrate, and the plurality of emitter regions is a plurality of alternating N-type and P-type polycrystalline silicon emitter regions, each disposed on a thin dielectric layer disposed on the first surface of the substrate.

19. The solar cell of claim 11, wherein the plurality of emitter regions is a plurality of N-type polycrystalline silicon emitter regions, the solar cell further comprising:

a plurality of P-type emitter regions disposed on the second surface of the substrate and spaced apart from one another;

a second dielectric layer disposed on each of the plurality of P-type emitter regions and between each of the plurality of P-type emitter regions, directly on an exposed portion of the second surface of the substrate; and

a second amorphous silicon passivation layer disposed on the second dielectric layer.

20. The solar cell of claim 11, wherein each of the plurality of emitter regions is separated from one another by a plurality of trenches disposed in the first surface of the substrate, wherein the dielectric layer and the amorphous silicon passivation layer are disposed in the plurality of trenches.

21. A method of fabricating a solar cell, the method comprising:
- forming a plurality of emitter regions on a first surface of a substrate, each of the plurality of emitter regions spaced apart from one another; and
- forming an amorphous silicon passivation layer over each of the plurality of emitter regions and between each of the plurality of emitter regions.
22. The method of claim 21, wherein forming the amorphous silicon passivation layer comprises forming a portion of the amorphous silicon passivation layer directly on an exposed portion of the first surface of the substrate.
23. The method of claim 21, further comprising:
- prior to forming the amorphous silicon passivation layer, forming a dielectric layer on each of the plurality of emitter regions and between each of the plurality of emitter regions directly on an exposed portion of the first surface of the substrate, wherein the amorphous silicon passivation layer is formed directly on the dielectric layer.
24. The method of claim 21, further comprising:
- forming a silicon nitride layer on the amorphous silicon passivation layer.
25. The method of claim 24, further comprising:
- subsequent to forming the silicon nitride layer on the amorphous silicon passivation layer, thermally annealing the amorphous silicon passivation layer at a temperature approximately in the range of 300-550 degrees Celsius.
26. The method of claim 21, further comprising:

driving hydrogen from the amorphous silicon passivation layer to an interface of the plurality of emitter regions and the substrate.

27. The method of claim 21, further comprising:

forming a plurality of conductive contacts to the plurality of emitter regions, through the amorphous silicon passivation layer.

28. The method of claim 21, wherein forming the amorphous silicon passivation layer comprises depositing amorphous silicon by plasma-enhanced chemical vapor deposition (PECVD) at a temperature below approximately 400 degrees Celsius.

29. A solar cell fabricated according to the method of claim 21.

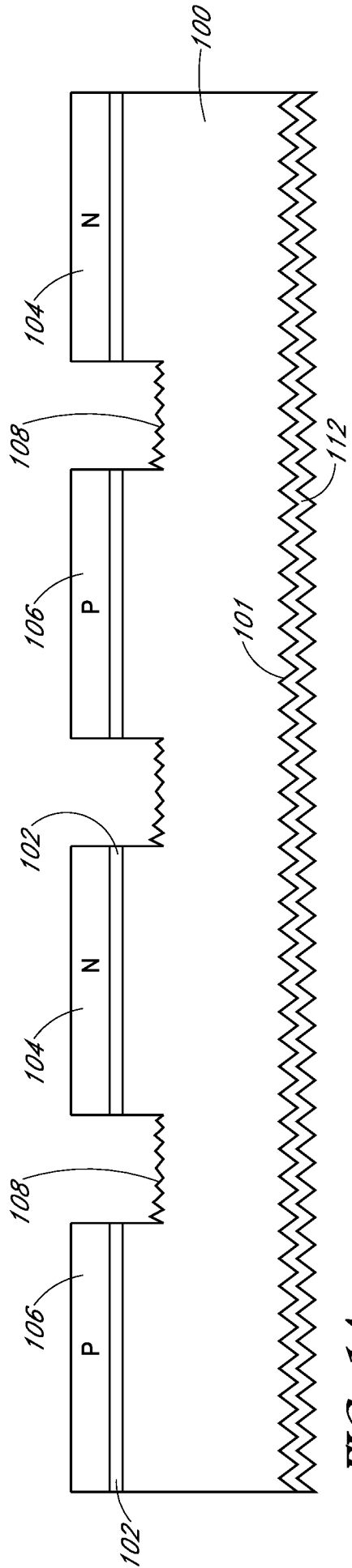


FIG. 1A

1/4

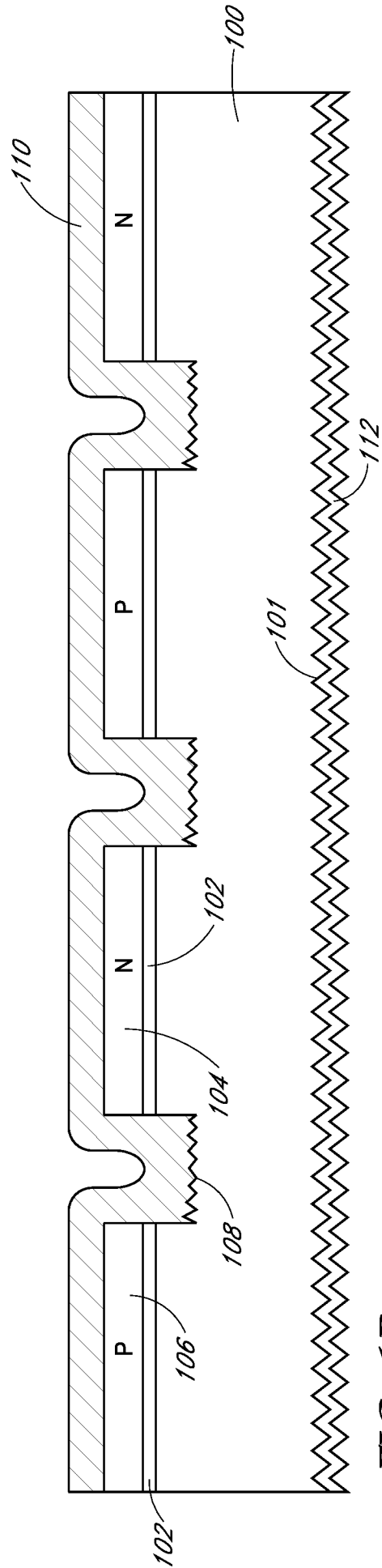


FIG. 1B

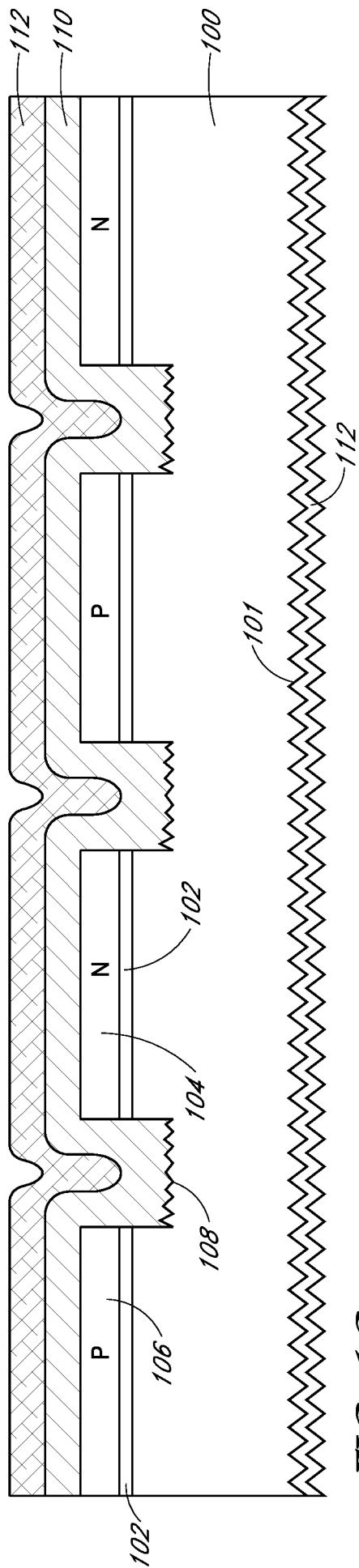


FIG. 1C

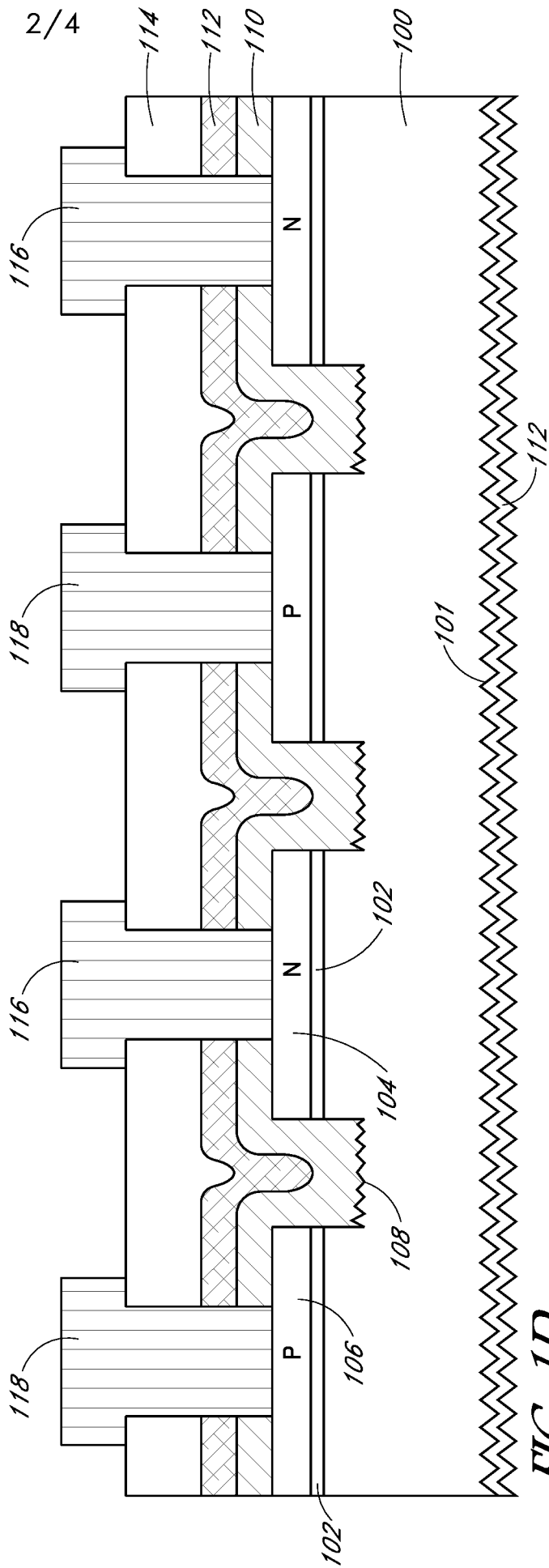
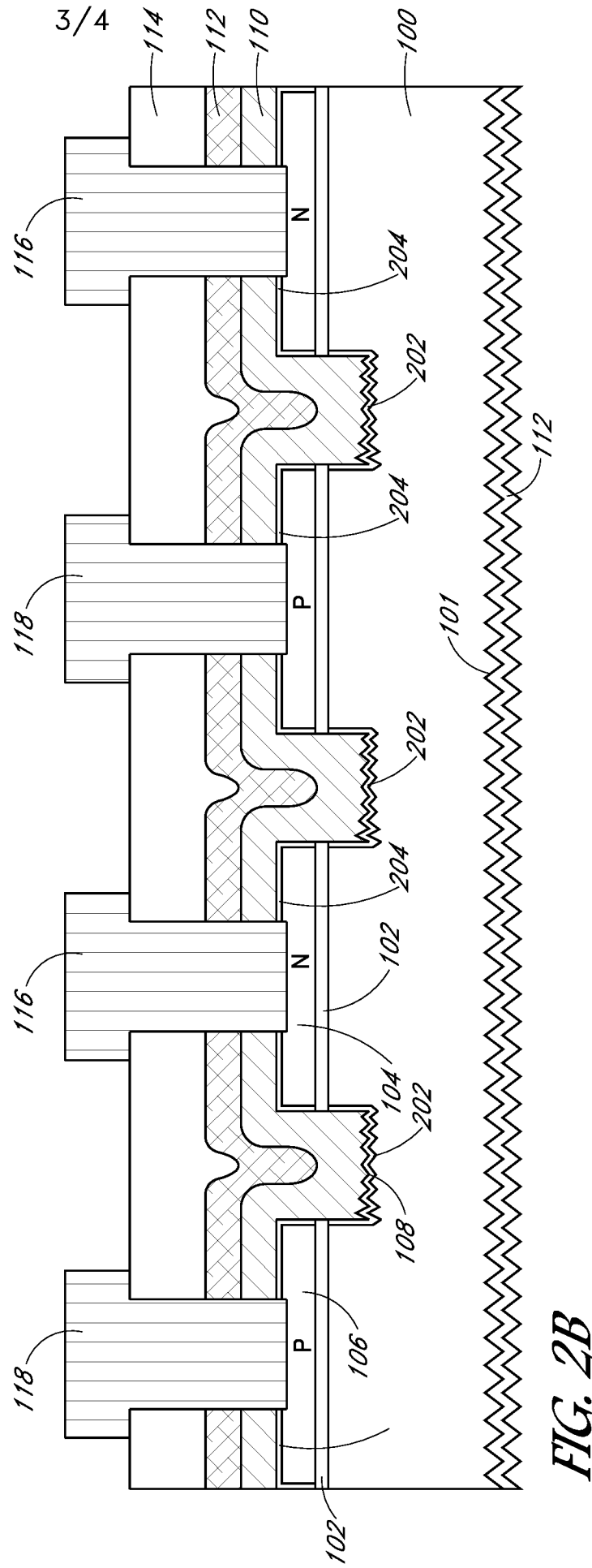
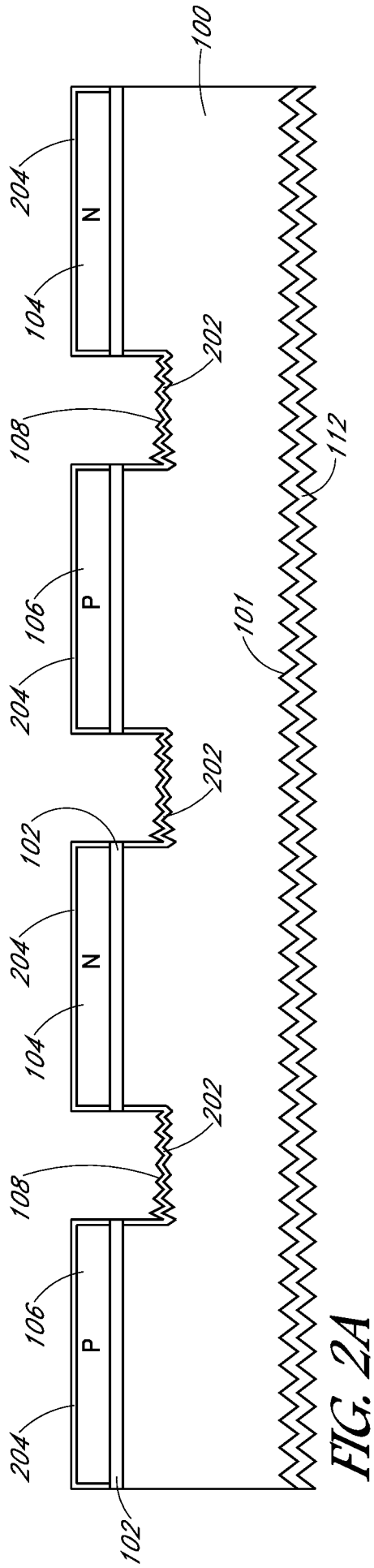
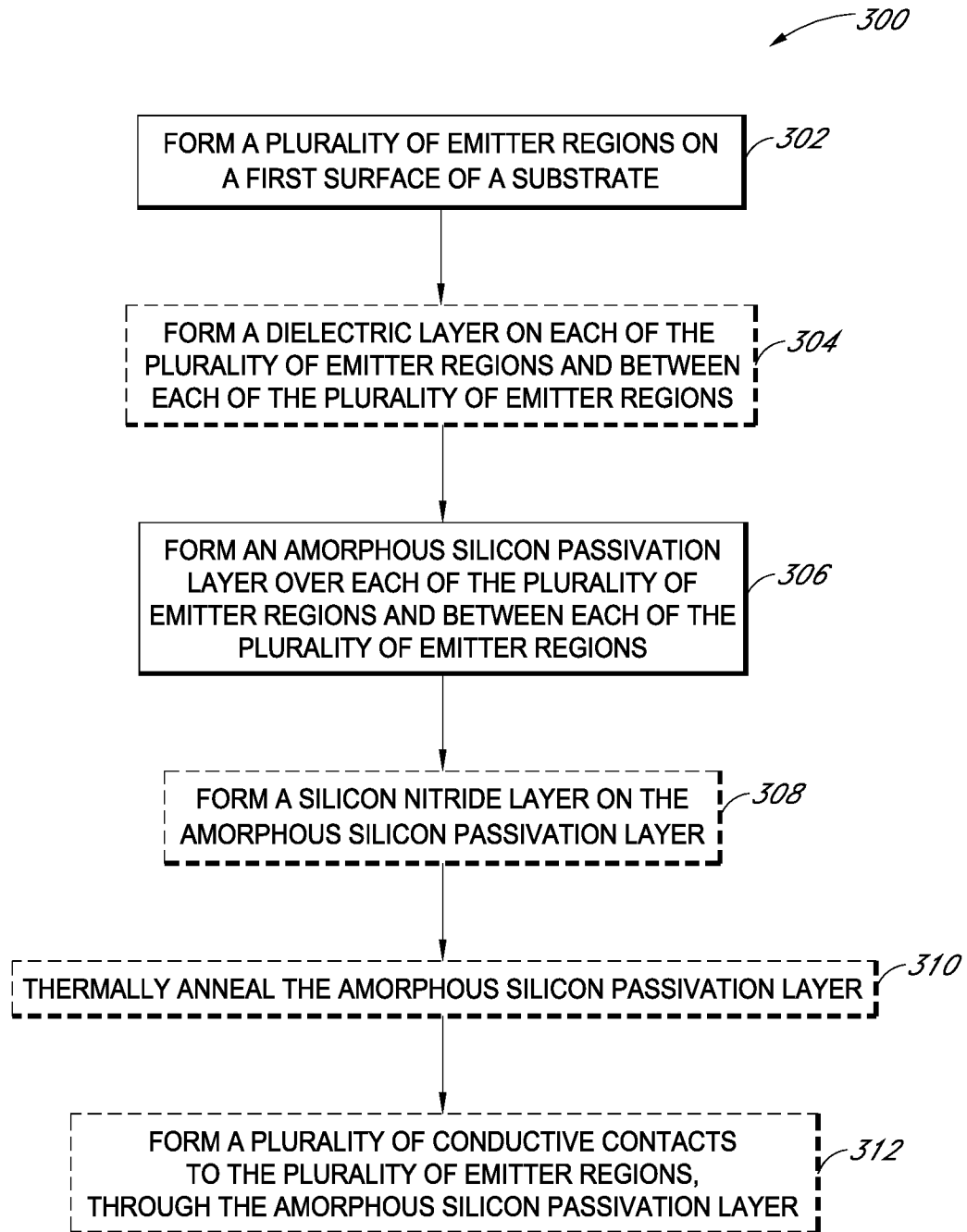


FIG. 1D



4/4

*FIG. 3*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/024120**A. CLASSIFICATION OF SUBJECT MATTER****H01L 31/0392(2006.01)i, H01L 31/036(2006.01)i, H01L 31/077(2012.01)i, H01L 31/18(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 31/0392; H01L 31/0216; H01L 31/0236; H01L 31/0352; H01L 31/04; H01L 31/18; H01L 31/072; H01L 31/042; H01L 31/036; H01L 31/077

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: emitter regions, amorphous silicon passivation layer, dielectric layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0240029 A1 (DAVID D. SMITH) 19 September 2013 See paragraphs [0023], [0033]–[0038]; claims 1, 3; and figures 1, 8A, 9, 10.	1–10, 21, 22, 24–29
Y		11–20, 23
Y	WO 2013-096500 A1 (SUNPOWER CORPORATION) 27 June 2013 See paragraph [0017]; and figure 6.	11–20, 23
A	US 2012-0266951 A1 (BO LI et al.) 25 October 2012 See paragraphs [0029]–[0049]; and figures 2A–2I.	1–29
A	US 2014-0027875 A1 (SANYO ELECTRIC CO., LTD.) 30 January 2014 See paragraphs [0021]–[0066]; and figures 2–7.	1–29
A	US 2013-0186456 A1 (DAISUKE IDE et al.) 25 July 2013 See paragraphs [0034]–[0072]; and figures 3, 6.	1–29



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

29 August 2016 (29.08.2016)

Date of mailing of the international search report

30 August 2016 (30.08.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

KIM, Do Weon

Telephone No. +82-42-481-5560



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/024120

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013-0240029 A1	19/09/2013	AU 2009-257973 A1	17/12/2009
		AU 2009-257973 B2	02/04/2015
		AU 2009-257974 A1	17/12/2009
		AU 2009-257974 B2	22/01/2015
		CN 102057497 A	11/05/2011
		CN 102057497 B	12/06/2013
		CN 103325861 A	25/09/2013
		CN 202307920 U	04/07/2012
		CN 202930394 U	08/05/2013
		EP 2297788 A1	23/03/2011
		EP 2297788 A4	02/07/2014
		EP 2297789 A1	23/03/2011
		EP 2297789 A4	02/07/2014
		EP 2297789 B1	05/08/2015
		JP 05524194 B2	18/06/2014
		JP 05625167 B2	19/11/2014
		JP 05780565 B2	16/09/2015
		JP 05860101 B2	16/02/2016
		JP 2011-523230 A	04/08/2011
		JP 2011-523231 A	04/08/2011
		JP 2014-160843 A	04/09/2014
		JP 2014-212339 A	13/11/2014
		JP 2016-036056 A	17/03/2016
		KR 10-1466753 B1	01/12/2014
		KR 10-1492683 B1	12/02/2015
		KR 10-2011-0025826 A	11/03/2011
		KR 10-2011-0030561 A	23/03/2011
		US 2009-0308438 A1	17/12/2009
		US 2009-0308457 A1	17/12/2009
		US 2011-0003423 A1	06/01/2011
		US 2011-0059571 A1	10/03/2011
		US 2013-0237007 A1	12/09/2013
		US 2014-0224319 A1	14/08/2014
		US 2015-0155417 A1	04/06/2015
		US 2016-0071991 A1	10/03/2016
		US 7812250 B2	12/10/2010
		US 7851698 B2	14/12/2010
		US 8450134 B2	28/05/2013
		US 8460963 B2	11/06/2013
		US 8673673 B2	18/03/2014
		US 8772894 B2	08/07/2014
		US 8975717 B2	10/03/2015
		US 9231145 B2	05/01/2016
		WO 2009-151808 A1	17/12/2009
		WO 2009-151809 A1	17/12/2009
WO 2013-096500 A1	27/06/2013	AU 2012-358982 A1	03/07/2014
		AU 2012-358982 B2	07/05/2015
		AU 2015-210421 A1	03/09/2015

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/024120

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0266951 A1	25/10/2012	CN 104011881 A	27/08/2014
		CN 104011881 B	04/05/2016
		DE 112012005381 T5	04/09/2014
		JP 2015-505167 A	16/02/2015
		KR 10-2014-0106701 A	03/09/2014
		TW 201344931 A	01/11/2013
		US 2013-0164879 A1	27/06/2013
		US 8597970 B2	03/12/2013
		US 8679889 B2	25/03/2014
US 2014-0027875 A1	30/01/2014	CN 103493216 A	01/01/2014
		EP 2702614 A1	05/03/2014
		EP 2702614 A4	24/09/2014
		JP 2014-512701 A	22/05/2014
		KR 10-2014-0041494 A	04/04/2014
		TW 201304160 A	16/01/2013
		US 2014-0295608 A1	02/10/2014
		US 2015-0087100 A1	26/03/2015
		US 8802486 B2	12/08/2014
		US 8912038 B2	16/12/2014
		US 9147795 B2	29/09/2015
		WO 2012-148523 A1	01/11/2012
		JP 05842173 B2	13/01/2016
US 2013-0186456 A1	25/07/2013	US 9224905 B2	29/12/2015
		WO 2012-132836 A1	04/10/2012
		CN 102725858 A	10/10/2012
		CN 102725858 B	09/12/2015
		EP 2530729 A1	05/12/2012
		EP 2530729 A4	29/10/2014
		JP 05845445 B2	20/01/2016
		WO 2011-093329 A1	04/08/2011