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A. DI GIUGNO ET AL

3,559,208

DATA DISPLAY MEANS

Filed Feb. 27, 1967

3 Sheets-Sheet 1

FIG. 1

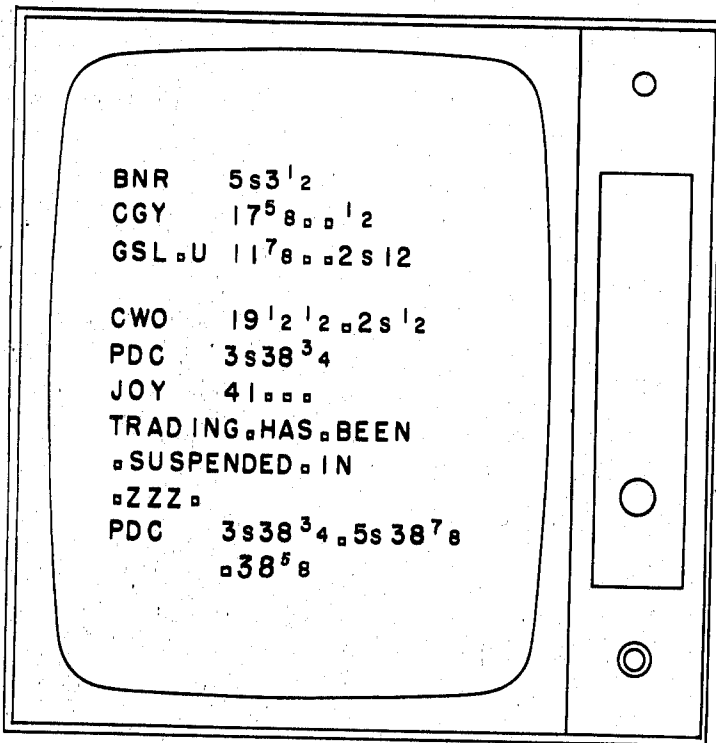
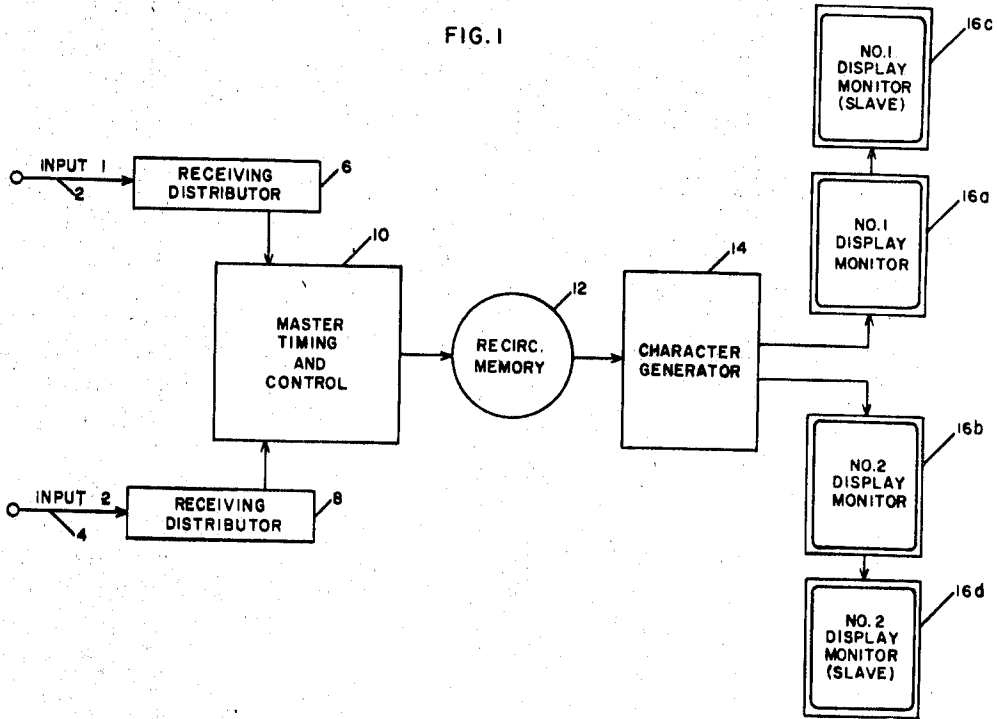


FIG. 2

DATA DISPLAY MEANS

Filed Feb. 27, 1967

3 Sheets-Sheet 2

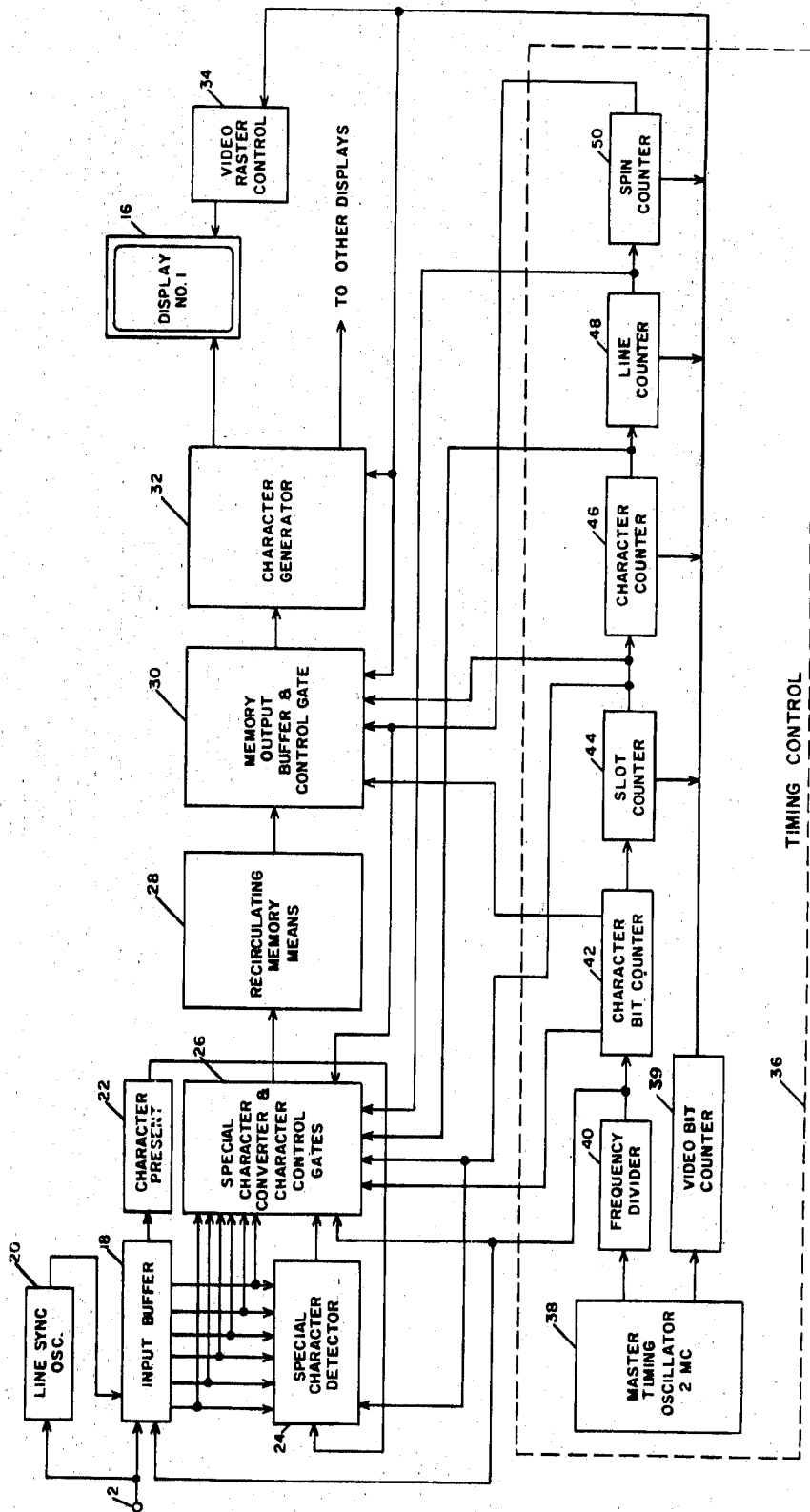
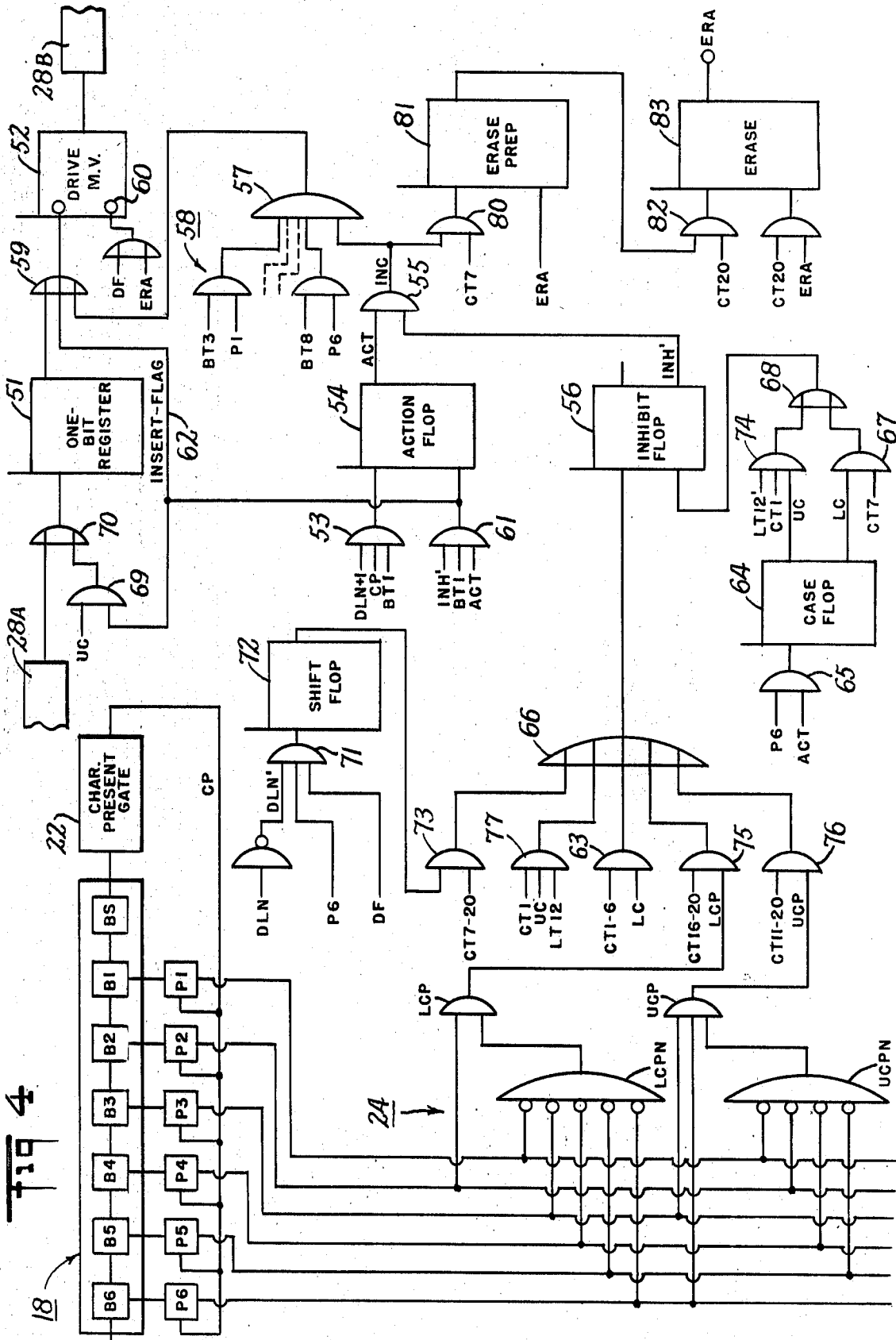


FIG. 3



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DATA DISPLAY MEANS

Angelo Di Giugno, Norwalk, Conn., and Joseph C. Marshall, Katonah, N.Y., assignors to The Bunker-Ramo Corporation, Stamford, Conn.
Continuation-in-part of application Ser. No. 548,127, May 6, 1966. This application Feb. 27, 1967, Ser. No. 618,730

Int. Cl. H04I 17/30

U.S. Cl. 340—324

31 Claims

ABSTRACT OF THE DISCLOSURE

An information display system for presenting graphic characters in a parallel line format and adapted (1) to receive a stream of coded electrical signals representing the graphic characters, (2) to segment the stream of signals into segregated groups of characters suitable for presentation on a single display line, and (3) to place each segregated group of characters on a corresponding line of a cathode-ray-tube display.

This application is a continuation-in-part of copending application Ser. No. 548,127, filed May 6, 1966, by Angelo Di Giugno and Joseph C. Marshall. The invention relates to data display means and methods, and more particularly to means and methods of displaying, in conventional graphic characters, data which has been transmitted in code form.

There are systems where coded data are transmitted, on a substantially continuous basis, from a central data distribution center to a number of remote receiving stations. At the receiving stations, the coded data are received, translated and reduced to some form of display. An example of such a system is the stock trading ticker information systems. In those systems, data relating to stock transactions are gathered at the stock exchange, coded and transmitted to ticker display devices at a great many remote stations. Conventionally, the remote receiving stations comprise printing units which translate the received coded data and print the results on a narrow strip of tape, the well-known ticker tape. These have long served the industry; however, they include an inherent undesirable limitation. Because the message is printed on tape, each receiving station can serve relatively few people, only two or three of whom can read the tape at one time.

There has long been a need for a means of displaying such data in a way where a large number of people can be simultaneously served by each output display device. There have been a number of efforts made to satisfy that need, none of them, however, being completely satisfactory. These have included mechanical display devices, which are often too slow in their response time, and projection devices wherein a printed ticker tape is optically projected onto a suitable screen. This presents a number of objections: time is lost in the mechanical conversion of the signals to the printer, the projection technique results in objectionable degradation of the image, the tape is not reusable, hence, soon collects in large quantities, and that system requires that the apparatus be serviced often with a fresh supply of paper tape and printing ink. There are other proposed systems which have been determined as being too costly or presenting a hard-to-follow display.

It is an object of the present invention to provide improved display means wherein a continuous stream of information is automatically separated into logical segments to be presented in the form of a series of corresponding successive parallel lines of graphical characters. A further object of the present invention is to provide an

improved display means as set forth wherein the presentation of old information is rapidly replaced by new information readily identifiable as such. Other objects, aspects and advantages of the invention will be pointed out in, or apparent from, the detailed description hereinafter.

In a preferred embodiment of the invention, there has been provided a display system wherein the information is presented in a predetermined number of successive parallel lines on the face of a cathode ray tube (CRT) such as is used in television receivers. The information is received in the form of a stream of signals representing a series of distinct information units, each such unit containing information concerning a single item or thing, such as the transactions relating to an identified security, or a text message concerning some matter of interest. The control circuitry is arranged to (1) separate the information into sequential segments, each of which advantageously may comprise an information unit or part thereof, and (2) present successive information segments on successive lines on the cathode ray tube until all of the predetermined number of lines have been occupied. Natural break points appear in the received information, for example at the end of words or at the end of the information concerning a single item. These natural break points may be detected and utilized, either alone or in conjunction with other information such as the point on a display line at which they occur, to segment the information.

In the embodiment disclosed, writing information into the last line results in the information in the first line being obliterated. The next information segment then is written into the first line, and simultaneously the old information in the second line is obliterated, and so on, through repetitive cycles, for successive lines. Thus, a blank line always separates the oldest data being displayed from the newest data being written. However, once data characters are written into any particular line, they remain stationary and easy to read until they are obliterated on the next cycle. Further, when the received data are of such nature as to permit of tabular presentation, such as stock transaction data, the information is presented in an easy-to-read tabular format.

A better understanding of the present invention may be had from the following detailed description when considered together with the accompanying drawings, in which:

FIG. 1 is a block diagram of the general arrangement of a display system embodying the present invention;

FIG. 2 is an illustrative representation of a display of information in accordance with the present invention;

FIG. 3 is a detailed diagram showing in substantial detail the interrelationship of the components comprising a display system in accordance with the present invention; and

FIG. 4 is a schematic diagram showing detailed aspects of the character detector and positioning control circuitry.

Referring now to the drawings in more detail, there is shown in FIG. 1 an arrangement for carrying out the present invention. As shown, there is a first input line 2 and a second input line 4, supplying information from a first and a second source of information, respectively. The information supplied from the first line 2 is applied as the input signal to a first input receiving distributor 6. Similarly, the information supplied from the second line 4 is applied as the input signal to a second input receiving distributor 8. There is also provided a master timing and control unit 10. This unit 10, first, provides timing control signals for the coordinating control of the rest of the apparatus, as will be more fully described hereinafter. Second, this unit 10 includes controlled gating and buffering means for processing the input signals applied thereto from the two receiving distributors 6 and 8.

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After the input signals have been processed in the master timing and control unit 10, the processed signals are stored in a recirculating memory unit 12. Under the control of the timing unit, character signals from the two input lines are alternated in the memory unit 12. The memory unit 12 may be any type of recirculating memory device; however, one form which has been found successful is a magneto-strictive delay line.

Again, under the control of the timing unit, the signals stored in the memory unit 12 are read out of the memory unit and applied as input signals to a character generator 14. Here the coded signals are converted into a different code form suitable for application to display means for presenting the characters represented by the coded signals. These signals are then supplied as input signals to a display means 16. While any of a number of different types of electrode-responsive display means are suitable for displaying the information, a preferred means is that including a cathode ray tube such as is used in television receivers. However, for the purpose of the present invention and as distinguished from television usage, the rectangular display area of the cathode ray tube is preferably arranged with its longer axis vertically disposed, as indicated in FIG. 2.

Even as there were two distinct sources of input information supplied to the master timing and control unit 10 and thence to the memory means 12, so there are illustrated two distinct display monitors 16a and 16b, respectively. The first display monitor 16a displays information received from the first input line 2 while the second display monitor displays information received from the second input line 4.

Another advantage of the present invention is that additional monitors 16c and 16d may be connected as slave monitors to display the same information as the primary monitor to which they are connected. These additional monitors considerably increase the number of people who can be served from one control unit with a minimal increase in cost.

In the system illustrated in FIG. 1, there are shown two input lines and, correspondingly, two output display monitors. A typical example of an application of the present invention is seen, as has been hereinbefore noted, in the display of information relating to transactions on the stock exchanges. For example, a continuous stream of information concerning the latest transactions in the trading of securities is provided by both the New York Stock Exchange and the American Stock Exchange. That information is distributed to subscribers' offices by telegraph or telephone lines. Since the two exchanges are distinct entities, the information emanating from these exchanges is separate and distinct, provided over separate wire service. Therefore, in the illustrated example, the information from the New York Stock Exchange may be received over the first input line 2 and displayed on the corresponding first display monitor 16a, while the information from the American Stock Exchange may be received over the second input line 4 and displayed on the corresponding second display monitor 16b.

While the input lines are separate and distinct as are the display monitors, the control unit, including the master timing and control means 10, the memory means 21 and the character generator 14, is singular and shared by the two input-output means.

In FIG. 2 there is shown a typical display of data received from one of the stock exchanges. In a specific embodiment of the present invention, the display area is divided into twelve successive horizontal data lines with each line divided into twenty character positions. In considering the display of information from the stock exchanges, the significance of the nature of the received signals is helpful. The characters represented by the received signals are of two basic types, the stock identifying characters known as upper case characters, and the characters descriptive of the transactions involving the identified security known as lower case characters. When printed out on conventional ticker tape, upper case and lower case

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characters are placed on different tracks of the tape, i.e. at different positions transversely of the tape. The received signals typically comprise six serial bits per character, with the sixth bit marked to indicate upper case and unmarked to indicate lower case.

In the disclosed system, the first character of a stock identifying code (upper case) is displayed in the upper left-hand corner of the CRT display area, with successive upper case characters being displayed in successive character positions in the top line. Usually no more than five character positions are required to display the stock-identifying symbols. The subsequent lower case characters representing transaction data respecting the identified stock are displayed on the same line as the stock identifying code but beginning at a predetermined indented position. Character position seven has been found to be a satisfactory position to display the first of the lower case characters, with subsequent lower case characters being displayed in successive character positions.

When the complete transaction relating to the identified stock has been posted in lower case symbols, the next signal received generally will be an upper case character, e.g. the start of another stock identifying code. Even though the line carrying the previous transaction has not been filled, the new upper case characters are displayed on the next line with the first of the new characters in the first character position of that line.

The combination of upper and lower case characters comprising a complete statement of transactions involving an identified stock may be considered an "information unit." The illustrated first line in FIG. 2 contains an information unit including the stock identifying symbol BNR and a single transaction of five hundred shares at 3½. In the second line, there is a multiple transaction posted in the form of an information unit including the identifying symbol CGY and two transactions, the first a block of 100 shares at 17¾ and another block of 100 shares at 17½. (The number 17, being common to both transactions, is simply omitted from the second posting for the sake of brevity.) Each of lines 1 and 2 contains only a single information unit; however, there may be occasions where more than one information unit may with advantage be placed on a single line.

It will be noted that periods may be included as visual separators between separate transactions involving an individual stock. The signals for these periods are lower case signals, i.e., the sixth (case) bit is unmarked. As will be noted hereinbelow, the received signals at times may contain upper case periods for certain special messages; however, their appearance on the display is the same as a lower case period.

In accordance with one aspect of the invention, the period character signals are detected and, when one occurs late in the line, the next set of data signals, even though a part of the same information unit, is displayed as a new segment on the next line in succession. In the preferred embodiment, for example, if a lower case period is detected at or after character position sixteen of any line, it is displayed in the next line, followed by the next lower case characters. However, as a lower case character, the period is displayed in the predetermined indented position, i.e., the seventh character position. This arrangement is shown in lines eleven and twelve of FIG. 2.

The eighth line of the display in FIG. 2 carries a textual message, all in upper case. Each word of the message is separated from the next succeeding word by an upper case period, as a visual separator. The period characters are detected and, if one occurs after a predetermined character position, for example at or after the eleventh character position, the period is displayed in the first character position of the next line with the characters of the next word in the immediately following character positions. This arrangement reduces the probability that a word of the textual message will be confusingly di-

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vided between two lines. The carry-over in the textual message situation differs from that of the lower case carry-over in that the carry-over portion of the textual message is displayed beginning at the first character position adjacent the left-hand margin of the display area instead of the indented position.

To summarize the immediately preceding description, the apparatus comprises control means which are responsive to certain predetermined characteristics of the received coded character signals and by recognition of such characteristics (shift from lower case to upper case, etc.) serves to identify the boundaries between unique sets of the received signals. The control means further includes means operable by such boundary identification to present on respective lines of the display groups of characters corresponding to the sets of coded signals which were segregated as separate entities as a result of the boundary identification.

As mentioned hereinabove, the lines of the display are written in sequence from top to bottom and, when the display area has been filled (either through line 11 or line 12, as will be explained), the cycle repeats, with the next information segment being placed in the top line. One of the problems with such a line sequence display is that of differentiating between old and new information. That is, the viewer frequently will wish to know what lines carries the latest information. In the disclosed embodiment of the present invention, such differentiation is achieved by causing the latest line written to be identified by a distinctive characteristic of the display.

Although there are various ways in which this can be done, the presently preferred arrangement is to provide a blank line immediately after the latest line. Thus, as a line of information is being written, the next line in the sequence is erased, indicating immediately and positively which line carries the latest data. If the line being written is the last (twelfth) line of the display, the top line is erased. Ordinarily, however, the twelfth line is unoccupied because it is reserved for carry-over from the eleventh line when the information being written is more than can be presented in a single line. This reserved use of the twelfth line minimizes the chance of dividing an information unit between the last and the first lines, which might be confusing to the viewer.

In FIG. 3, there is shown in substantially more detail, structure which embodies the present invention. In this illustrative embodiment, only one input line is shown; however, it will be understood that a second input may be accommodated by known multiplexing techniques. The input line 2, over which information signals are received, feeds into an input buffer 18. The input buffer 18 is represented by and included in the receiving distributor 6 of FIG. 1. The input buffer comprises a seven-bit shift register to accommodate a six-bit character code plus a start signal which is conventional for the transmission of such information.

In order to synchronize the shifting of the signals through the input buffer with the occurrence of the signals on the line, a line-synchronizing oscillator 20 is provided. See, for example, the disclosure of copending application Ser. No. 307,190, filed on Sept. 6, 1963, by Richard Windels et al. The line-synchronizing oscillator 20 may be a simple gated flip-flop. The oscillator 20 is keyed by the frequency of the signals on the line and provides, as an output, stepping pulses for the shift register 18. When the start pulse of a character code has been shifted into the last position of the shift register 18, a "character present" gate 22, when properly activated, produces a signal which signifies that a character is present in the buffer 18, ready to be processed out.

An important feature of the present invention is the provision of means for dividing the continuous stream of character signals on line 2 into separate information segments each suitable for placement on a separate line of the display. For this purpose, the control apparatus

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includes means to identify certain predetermined distinctive relationships between the nature of a received character and other conditions, including for example the case of the preceding character, and the position of the display being written (or next to be written in regular sequence). Analysis of each received character is initiated by the output of gate 22 which is applied as a control signal to a character detector 24 to which the outputs of the several bins of the register 18 also are connected. The character detector 24 comprises a plurality of gates arranged to respond to predetermined combinations of signals emanating from the bins of the input buffer 18, and serves to analyze the received character to determine where the character should be placed on the display.

Although various kinds of character analyzer apparatus are known and conventional in the electronics art, an example of one satisfactory arrangement is that shown in FIG. 4. There the seven bit bins of the input buffer 18 are shown as accommodating the "Start Bit," BS, and the six data bits, B1 to B6. When the Start Bit appears in the BS bin, indicating that a character is present in the buffer, a signal CP is produced at the output of the character-present gate 22. That output signal enables a plurality of parallel read gates P1 to P6 to read out in parallel the signals stored in the several bins of the input buffer 18.

In order to detect certain predetermined characters, leads from the several parallel gates P1 to P6 are coupled to a number of character AND gates, one such gate for each character to be detected. For example, one AND gate LCP (lower case period) detects the character represented by a bit in bin B2, but not in bins B1, B3, B4, B5 and B6, by virtue of a lead connected from P2 to the input of the AND gate together with the output of a NOR gate LCPN connected to gates P1, P3, P4, P5 and P6. A similar arrangement UCP and UCPN is shown for detecting an upper case period character represented by a bit only in bins B3 and B6.

Other character detector gates may of course be provided as required by particular applications. The specific detector circuits disclosed are intended to illustrate the nature of the functions performed to obtain the intended control of the display. It will be understood, of course, that the display system typically may include still other specific circuits to suit various special characteristics of the received data, such as circuits to detect the presence of fraction characters and the like. Such additional circuitry has not been shown herein in order to simplify the presentation and so aid in providing an understanding of the fundamental concepts of this invention.

Control signals derived from the character detector gates are applied to a special character converter and character control gate unit generally indicated in FIG. 3 by block 26, and details of which are illustrated in FIG. 4. The unit 26 includes a number of combinations of gate circuits and flip-flop registers which respond to signals derived from the input buffer 18, from the special character detector 24, from the output of the delay line 28, and from several timing signal sources. This control unit 26 serves primarily to determine the positioning on the CRT display of the characters which are received from input line 2, and particularly to segment the stream of received character data for presentation on separate lines of the CRT display.

Before proceeding with a detailed consideration of the operation of the character control unit 26, a brief review of the CRT display apparatus itself will first be presented to facilitate an understanding of the specific character control apparatus employed with the preferred embodiment of this invention. This CRT display apparatus is described fully in copending application Ser. No. 370,323, filed on May 26, 1964, by R. D. Belcher et al., and the disclosure of that application is hereby incorporated by reference into this application.

The heart of the display apparatus comprises the recirculating memory means 28 incorporating a magneto-

strictive delay line which carries all of the character data for controlling the presentation on the CRT display 16. This delay line recirculates ("spins") at a rapid rate (e.g. once every few milliseconds), and its output is fed through output control circuitry 30 to a character generator 32 (for details, see copending application Ser. No. 460,307 filed by E. M. Dean on June 1, 1965) which converts the character data read from the delay line into a form suitable for controlling the CRT display 16. If there are two or more sources of signals with corresponding display devices, the character data for the respective display devices may be interlaced in the delay line storage sequence, and the output control circuitry 30 arranged to cause the individual data presentations to be "painted" sequentially on the display devices during respective spins of the delay line.

Although the delay line 28 actually is a continuously functioning device in which a series of sequentially stored bits is constantly being circulated at a uniform speed, it may be considered as being subdivided into a series of so-called time "slots" each having a capacity (in the present embodiment) for storing eight bits carrying all of the information for defining a single character of the ultimate display. The first (leading) bit position of each slot is for the so-called "next character flag" and will be "marked" (logical one) in only one of the slots associated with a given display device to indicate to the control circuitry where the next received character is to be loaded in the delay line. When the flag bit position is marked, the next following bit indicates the "case" of the preceding character (i.e. whether the character is upper or lower case). The last six bits of a filled slot represent the basic character data, including the case-determining sixth bit of the received character code for use in generating the display code. After a character has been inserted in the slot which had carried the marked flag bit, the control circuitry normally advances the flag bit to the next slot in the sequence, so that the following character will be placed in that next slot.

The normal manipulation of the data bits in the delay line 28 is accomplished by control apparatus generally similar to that described in detail in the above-identified Windels et al. application, and reference should be made thereto where appropriate. As described in that application, the pulsing of the delay line is timed by counter circuitry 36 comprising a master oscillator 38 and a chain of counters 40-50. The first or "bit" counter 42 counts to eight, providing eight consecutive output pulses on eight respective output leads with each pulse lasting for the duration of the bit time.

These bit time pulses (BT) are used to gate the individual bits of each eight-bit "slot" into the delay line in proper position. Upon reaching a count of eight, the bit counter resets and furnishes a pulse to a slot counter 44. This counter provides a count equal to the number of display devices 16, e.g. it will count to two when a dual display arrangement is used such as shown in FIG. 1. The system can comprise a single display (as in FIG. 3), but the slot counter ordinarily will still be provided to assure proper timing relations for the particular CRT display disclosed herein.

The character counter 46 counts up to the number of character positions in each line of the CRT display 16, e.g. twenty, as in the preferred embodiment disclosed herein. The character counter resets after the end of the line, starting out the first character time pulse (CT1) at the instant the first bit time (BT1) is developed, and holding the character time pulse up during all eight bit times of the character. When the system includes a CRT data display of the type disclosed herein, the character counter is arranged to count beyond the number of character positions in the line in order to provide time for returning the beam to the next start position.

When the character counter resets, it simultaneously transmits a pulse to the line counter 48. This latter counter

provides a count of twelve, corresponding to the twelve lines in the CRT display. Resetting of the line counter also actuates a spin counter 50 so that, when the system includes more than one display device, the spin counter may indicate which of the display devices is to be fed data from the character generator 32.

When utilizing CRT display apparatus of the type disclosed in the above-referenced application Ser. No. 370,323, the display positions of the individual characters on the face of the CRT tube are determined by the slot positions of the characters in the delay line, and the slot position of any given character normally is determined, as described hereinabove, by the location of the "next character flag" at the time the character is inserted in the delay line. In carrying out the present invention with display apparatus of the type previously disclosed, the means for dividing the continuous stream of received signals into separate information segments for presentation on respective display lines will include control means for overriding or disabling the normal character-positioning action of the flag bit when the control functions require that the next character be placed in some position other than in the regular sequence.

To this end, the normal positioning action of the flag bit is disabled selectively in response to control signals indicating particular predetermined relationships between: (1) the nature of the character to be inserted in the delay line, e.g. whether it is upper or lower case, and whether it is a specific character such as a period, etc.; (2) certain precedent conditions, e.g. whether the immediately preceding character inserted in the delay line was upper or lower case; and (3) the current position of the "next character flag" bit. With the normal controlling function of the flag bit disabled, additional character positioning circuitry is activated to insert the character in a subsequent slot, and thereafter a new flag bit is placed in the next following slot to identify the location where the next character is to be stored in regular sequence in the delay line.

Returning now to the detailed circuitry shown in FIG. 4 for carrying out these operations, after a complete character has been detected by the character present gate 22, the equipment then must scan the delay line output to search for the "next character flag." The signals emerging from the delay line (identified herein as DLN) are examined with the aid of a one-bit storage register 51 which receives data bits from the delay line output 28A and, one bit time later, supplies those bits to a drive multivibrator 52 adapted to energize the sonic pulsing circuitry at the delay line input 28B.

In order to detect the next character flag, the output of the register 51 (identified herein as $DLN+1$) is coupled to an AND gate 53 together with the "character-present" signal (CP) from the input buffer 18, and the timing pulses BT1 from counter 42 identifying the first bit position for each slot. When the flag bit reaches the register 51, the output of gate 53 (DF) will go high to set a clocked Action flop 54, indicating that "action" respecting the delay line storage is to take place. The Action flop, like the other flops in the disclosed system is clocked by spike-like pulses at the end of each bit time, and thus sets at the end of BT1.

The set output (ACT) of Action flop 54 is directed to an AND gate 55, together with the reset output of Inhibit flop 56 (normally in reset condition), to produce an "insert-character" signal (INC) to initiate loading of the character from buffer 18 into the delay line 18. This delay line loading function can be performed in any conventional manner, illustratively by applying the INC signal to an AND gate 57 together with the signals from a series of AND gates 58 which time the buffer gates P1-P6 with respective bit counter signals BT3-BT8. By this means, the six bits of the waiting code character in buffer 18 are gated serially through AND gate 57 and an OR gate 59 to the input terminal of the delay line drive multi-

vibrator 52. Since the character bits are gated in by means of timing signals BT3-BT8, these data bits will occupy positions three through eight in the delay line slot in which the flag bit was detected.

Once the flag bit has been detected and loading action initiated, the flag bit should be erased because its function of identifying the next available slot has been performed. For this purpose, the output of AND gate 53 (DF) also is connected to a pulse-suppression terminal 60 of the drive multivibrator 52. Energization of this terminal 60 serves, in a conventional fashion, to prevent the transmission of any pulse to the delay line input 28B, and thus prevents the original flag bit from being recirculated through register 51 back into the delay line. This gate signal DF remains high only during the bit counter time BT1, and therefore does not interfere with the subsequent delivery of the waiting code character bits to the delay line during counter times B3-B8.

At the end of the character-load function, a signal is generated to reset the Action flop 54, and this resetting signal is used to insert a new flag bit in the first bit position of the next following slot. The resetting signal is generated by an AND gate 61 the output of which goes high during BT1 whenever the Action flop is set and the Inhibit flop 56 is reset (as it normally is, with exceptions to be described below). Thus, immediately after the sixth code character data bit has been loaded from buffer 18 into bit position eight in the originally marked slot, the output of AND gate 61 goes high. This signal resets the Action flop 54 and simultaneously is transmitted over a lead 62 to OR gate 59 to insert a new flag bit in the first bit position of the next following slot.

As explained hereinabove, when certain predetermined special conditions are detected, the normal positioning function of the next character flag is disabled and auxiliary character-positioning circuitry becomes operative to place the waiting code character into an advanced position the location of which is determined by the specific nature of the predetermined conditions detected. Turning now to these special conditions individually and in more detail, if a lower case character is detected when the flag bit is in slot one through six of any line, the waiting character is automatically placed in character position seven of that line. Detection of this condition is effected by an AND gate 63 which combines the CT1 through CT6 timing signals (from character counter 46) with the lower case lead (reset) of a Case flop 64.

Timing pulses CT1 through CT6 are generated when the delay line output is passing through character slots one through six of any line. Case flop 64 is controlled by an AND gate 65 to which is directed the sixth code character gate signal P6 and the set output of the Action flop 54. Thus, if P6 is low when the Action flop sets (indicating that a lower-case character is ready to be loaded), the Case flop will be placed in its reset condition with its lower-case lead high. Thereupon, AND gate 63 will transmit a corresponding high signal through an OR gate 66 to the set terminal of the Inhibit flop 56.

When the Inhibit flop 56 is set, its reset lead INH' goes high to close AND gate 55 and prevent loading of the waiting code character into the delay line. The Inhibit flop subsequently is reset by the output of an AND gate 67 which combines the reset lead from the Case flop 64 with character counter timing signal CT7, so that when the seventh character position of the display line is reached, a high signal is directed through an OR gate 68 to the reset terminal of the Inhibit flop. Resetting of this flop opens the AND gate 55 to permit the waiting code character bits P1-P6 to be inserted serially into the delay line.

As long as the Inhibit flop remains set to prevent loading of the character, the Action flop also remains set because the reset gate 62 receives the reset output INH' of the Inhibit flop. As soon as the Inhibit flop is reset, INH' goes high and the Action flop is reset at the next occur-

rence of bit counter timing signal BT1. This resetting signal also serves, as described hereinabove, as an "insert-flag" signal which is directed through lead 62 and OR gate 59 to the drive multivibrator 52 to enter a corresponding flag bit in the first bit position of the next following character slot.

The bit following the flag bit is used in this embodiment of the invention to indicate the case of the immediately preceding character, i.e. the character previously loaded into the delay line. This case marker bit is inserted by directing the insert-flag signal on lead 62 to an AND gate 69 with the set (upper case) lead from the Case flop 64. With the Case flop set, indicating that the character being loaded is upper case, the AND gate 69 will transmit through an OR gate 70 a "logical one" to the input of the one-bit register 51. Since this case marker bit is placed in the input of the register 51, whereas the flag bit is placed in the input of the delay line 28B, it will be evident that the case marker bit will be in bit position two, right behind the flag bit. If the previously loaded character was lower case, the output of AND gate 69 would be low and a logical zero would be inserted in the delay line, thus indicating that the preceding character was lower case.

Another special condition where the Inhibit flop is set is when there is a change of case from lower to upper in any character position after position seven. This condition is detected by an AND gate 71 to which is directed (1) the inverted delay line output DLN', (2) the output of gate P6 (high for an upper case character), and (3) the detect-flag lead DF. Whenever DF goes high to indicate that a flag bit has been detected in bit position one, the delay line output DLN will at that instant represent bit position two of the flag-marked slot, i.e. the case bit. Thus, if DLN is low (DLN' high) when DF goes high, bit position two is not marked in the slot carrying the flag bit, indicating, as explained hereinabove, that the preceding character in the delay line is lower case. If, at the same time, P6 is high (upper case character waiting to be stored), all of the inputs to AND gate 71 will be high, indicating that there has been a shift in case from lower to upper. The corresponding high output of AND gate 71 is used to set a Shift flop 72.

If the Shift flop 72 is set when the next character flag is detected in any slot from character position seven to the end of the display line, the normal character-locating function of the flag bit is disabled and the waiting upper case character is placed in the first position of the next succeeding line of the display (with the exception of line 12). For this purpose, the set output of the Shift flop is directed to an AND gate 73 together with the character count timing pulses CT7-20, and when the previously described conditions obtain, the high output of this AND gate 73 is directed through OR gate 66 to the set terminal of the Inhibit flop 56. The setting of this latter flop prevents the loading of the waiting character data in the normal sequence of the delay line, and maintains the Action flop 54 in set condition until an advanced position of the delay line is reached where the waiting character is to be loaded.

At the start of the next display line, a resetting AND gate 74 is energized by CT1 and the set (upper case) output lead of the Case flop 64. This AND gate also receives the inverted output of the twelfth count (LT12') produced by the line counter 48, so that the AND gate 74 will not produce a high output unless the delay line is operating in the storage regions corresponding to display lines 1-11. When the output of this gate 74 goes high, it transmits a corresponding signal through OR gate 68 to reset the Inhibit flop 56 and cause the waiting upper case character to be loaded into the delay line. As before, immediately after the entire waiting character has been loaded, the Action flop 54 is reset and a new flag bit is inserted in position one of the next succeeding slot, i.e. slot two. Thereafter, successive upper case characters are

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placed in the successive slot positions. If a lower case character appears at this time, it is advanced to the indented position seven as previously described, by virtue of the operation of AND gate 63.

If a lower case period is detected when the next character to be loaded would normally go into any of slot positions 16-20, the character-loading operation is suspended until the delay line slot corresponding to character position seven of the next display line is reached. To this end, the character counter outputs CT16-20 are coupled to an AND gate 75 together with a lead LCP (lower case period) derived from the character detector gate LCP previously described. Occurrence of a lower case period in these circumstances activates AND gate 75 which thereupon directs a signal to the set terminal of the Inhibit flop 56, and this flop functions, in the manner described hereinabove, to prevent loading of the waiting period character into the delay line. After the end of the line is reached, the character counter 46 will reset and, when it next reaches position seven, its output signal CT7 will energize AND gate 67 as described so as to reset the Inhibit flop 56. Thus, the waiting lower case period is loaded into the seventh slot for that display line. Successive lower case characters will be inserted in successive slots for the line.

If an upper case text message is being written and the visual word separator (upper case period) is detected when the next character to be inserted normally would go in position eleven or a subsequent position in the line, the normal character-locating function of the flag bit is disabled and the upper case period is inserted in the first character position of the next following line (except for line 12, as previously mentioned). For this purpose, the output of the upper case period detector gate UCP is directed to an AND gate 76 together with the character counter outputs CT11-20, so that when the stipulated conditions obtain, the output of AND gate 74 goes high and transmits through OR gate 76 a signal to set the Inhibit flop 56. Again, this Inhibit flop prevents the loading of the waiting period character until the character counter reaches the first character position of the next display line, whereupon AND gate 74 is energized by CT1 and the set (upper case) output of the Case flop so as to reset the Inhibit flop and cause loading of the waiting character. If the delay line is passing through the storage area for display line 12 at this time, AND gate 74 will be held closed by the logical zero signal on lead LT12', and thus the waiting character will be placed in the first character position of the top line of the display when LT12' goes high.

If an upper case text message reaches the end of a line of the display without coming to a period separator, the next character in the message is automatically placed in the first position of the next following line (except line 12). This result follows from the normal shifting of the flag bit because, if an upper case character is inserted in slot twenty of a line, the flag bit automatically will be shifted to the next succeeding slot which will be the first slot of the next following line. Thus, a subsequent upper case character will automatically be positioned in the first slot by the normal locating action of the flag bit. Such an upper case character will not be placed in the storage area for display line 12, because the timing signal LT12 is directed to an AND gate 77 (together with CT1 and the upper case signal from Case flop 64) to set the Inhibit flop 56. The Inhibit flop will thereafter be reset when the first line of the display is reached, by operation of the AND gate 74 as previously described, so that the waiting upper case character will appear in the top line of the display and not in the twelfth line.

If in writing a series of lower case characters, the end of the display line is reached without encountering a lower case period, the next following lower case character is automatically placed in the indented position (seven) of the following line. In more detail, when a lower case char-

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acter is inserted in slot twenty of a line, the resetting of the Action flop 54 automatically inserts a flag bit in the first slot of the next following line, and normally any following character would be expected to be loaded in that slot. However, if the following character is lower case, the operation of AND gate 63 will cause the Inhibit flop 56 to be set during the character counter times CT1-6, and thus the waiting lower case character will not be inserted in the delay line until slot seven of that display line is reached.

In display apparatus of the type used in the preferred embodiment, fractions may be portrayed as two successive small-sized numbers in respective adjacent character positions. Thus, when a fraction character is detected in the input buffer 18, the control circuitry would be arranged to generate two corresponding sets of six-bit character signals to be inserted in the next two slots of the delay line. If a fraction character is detected when slot position twenty is next to be filled, there would not be sufficient storage capacity to complete the fraction in that line. Thus, to accommodate a fraction character detected under those circumstances, the control circuitry may advantageously be arranged to set the Inhibit flop 56 until the seventh slot of the next line in the delay line is reached, and then to load the two fraction-characters in slots seven and eight for display together on that next line of the CRT. As before, the flag bit then would be inserted in the next empty slot, i.e. slot nine.

Once the display device 16 has been filled, as explained hereinabove, the cycle repeats, with the next segregated set of characters being presented in the top line in place of the original set of characters, and so forth. When, in such repeat cycle, a line of characters is being written, the next following line is blanked so as to identify the line having the latest information. With continued reference to FIG. 4, this result is achieved in this embodiment by combining the "insert-character" signal INC with character count CT7 at an AND gate 80 the output of which sets an Erase Prepare flop 81. The set output of the flop is combined with character count CT20 by an AND gate 82 which sets an Erase flop 83 when the delay line reaches the end of the line in which characters are being entered. The set output (ERA) of flop 83 is directed to the pulse suppression terminal 60 of the drive multivibrator 52, and erases all of the delay line bits from the delay line storage section corresponding to the display line following the line in which characters are being entered. Thus, this following line is completely blanked.

Setting of the Erase flop 83 resets the Erase Prepare flop 81, to prevent blanking of any lines beyond that desired. When the end of the blanked line is reached, the Erase flop is reset by character count CT20 which is combined with the set output ERA of the Erase flop. Thus the blanking circuitry is returned to normal condition.

Reverting now to FIG. 3, the character codes stored in the delay line 28 are read out into a memory output buffer and control gate means 30. Here, the signals are buffered and gated into proper channels to be applied to the character generator 32. Again, while any of a number of character generating means may be used, one form which has been successfully used is that described in detail and claimed in copending application Ser. No. 460,307, filed June 1, 1965, in the name of E. M. Dean for "Code Conversion Means." That application includes the reading of coded signals out of the memory means into the memory output buffer and control gates to produce, for a six-bit character code, an output signal on a selected one of sixty-four output leads coupled to the character generator 22.

In cathode ray tube character display means, one type of character formation is in the form of a five-by-seven dot matrix. Such character displays are used in on-line message composing instruments manufactured by The Bunker-Ramo Corporation. In such a display, the cathode ray beam is caused to execute a plurality of vertical

strokes of the height of the desired character with each vertical stroke divided into seven bit areas during which the beam may be allowed to impinge on the tube face. One additional bit time is needed to effect a retrace of the beam between strokes and one full eight-bit stroke is allowed to define a space between adjacent characters. Thus, there is needed in effect a forty-eight bit count to control the application of these character bits to the display means.

In the generation of the pulses to effect the five-by-seven dot pattern, the sixty-four individual character leads from the unit 30 (the sixty-four leads being illustrated herein as a single lead for simplicity) are applied to a diode matrix character generator as shown in the aforesaid Dean application. The resultant signals are then gated out of the character generator 32 as a series of pulses applied to a Z axis control of the cathode ray tube. This character generator converts the intermediate code, represented by the sixty-four individual lines, to a thirty-five bit character display code for the CRT.

The apparatus provides sequential scanning of the thirty-five input leads from the character generator 32, producing an output pulse in serial timed sequence for each marked data bit found on any one of the thirty-five input leads as it is being scanned. These serialized data bits may then be transmitted to the data display device 16 to effect a display of the coded characters. These pulses are applied to the cathode ray tube control element in timed relation to deflection signals applied to the tube control elements by a video raster control 34. The video raster control is, in turn, controlled by the timing control unit 36.

The timing control unit 36 includes the master timing oscillator 38 which produces a series of pulses at high frequency, for example, at two megacycles per second. That output is branched, and the signals in one branch divided by a frequency divider 40 to provide an input for the counter chains 42-50 already described. The other branch is applied as input to a video bit counter 39. The output of the video bit counter, an eight-stage shift register, produces the pulses which are used to time the output of the memory output buffer and control gate 30 and the character generator 32. The output pulses from the video bit counter 39 are also applied, along with control pulses from the slot counter 44, the character counter 46, the line counter 48 and the spin counter 50, as input control signals for the video raster control 34 as hereinabove mentioned.

The deflection pattern of the cathode ray beam in the display tube 16 is in the form, as previously noted, of a series of vertical strokes the height of the characters to be displayed. That pattern is repeated for each line of characters to be displayed with a horizontal retrace between lines and a vertical displacement. After the last line has been traced, the beam returns to again trace the first line, and so on. When there are two separate output displays, this sequence must be synchronized with the slot count as well as the character, line, spin and video bit count. A more detailed description of this type of character display, including the video raster control, is shown and claimed in copending application, Marshall et al., Ser. No. 460,117, filed June 1, 1965, for "Data Handling Apparatus."

While in the preferred embodiment of the invention, a CRT display device has been utilized and controlled, it is apparent that the teachings of this invention could be utilized to control other display devices as well. Thus, while the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and detail may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. Apparatus for displaying information in a parallel line format, comprising:

an electro-responsive image display means;
means for applying to said display means a sequential series of coded electrical signals representing information characters to be displayed on said display means;

analyzing means responsive to certain predetermined code combinations in said coded electrical signals representing information characters to be displayed for detecting and identifying natural break points between successive groups of said characters;

and control means normally operative to display successively received information characters in successive character positions on a line of said display means, said control means including means responsive at least in part to the detection of a natural break point by said break point identification means for displaying information characters following the detected predetermined code combination on a succeeding line of said display means.

2. Apparatus as claimed in claim 1, wherein said control means is operative, upon a predetermined number of lines being presented in succession on said image display means, to present the next group of characters in the first line of the display in place of the original group of characters presented in said first line, successive groups of characters thereafter received being placed in successive lines following said first line to replace the characters originally presented.

3. Apparatus as claimed in claim 2, wherein said control means includes means to present the information on said image display means with a distinctive characteristic identifying the latest line to be placed on the display means.

4. Apparatus as claimed in claim 3, wherein said apparatus includes means to provide a blank line following said latest line as said distinctive characteristic identifying the latest information.

5. Apparatus as claimed in claim 1, wherein the display lines of said image display means have a terminal position beyond which characters are not presented;

said control means including margin setting means for detecting the occurrence of at least a selected natural break point within a predetermined number of character positions from said terminal position, and line starting means responsive to a detection by said margin setting means for initiating a new display line.

6. Apparatus as claimed in claim 5, wherein said applied electrical signals represent first and second types of characters;

said margin setting means including means to detect a natural break point in said first type of characters normally to be presented within a first predetermined number of positions from said terminal position and to detect a natural break point in said second type of characters normally to be presented within a second predetermined number of positions from said terminal positions;

said line starting means being operable to initiate a new display line upon the detection of either of said natural break points in a position less than the corresponding predetermined number of positions from the terminal position.

7. Apparatus as claimed in claim 6, wherein said display lines normally start with characters of said first type followed by characters of said second type at a subsequent indented position;

said line starting means being arranged to start a new line at the normal start position when a natural break point in said first type of characters has been detected and to start a new line at an indented position when a natural break point in said second type of characters has been detected.

8. Apparatus as claimed in claim 7, wherein said first and second types of characters are upper and lower case characters respectively.

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9. Apparatus as claimed in claim 2, wherein said control means includes line starting means operable, in response to detection by said analyzing means of a certain code combination, to initiate the display of a new group of characters at a line position other than the next line position in the regular sequence.

10. Apparatus as claimed in claim 9, wherein said applied electrical signals represent first and second types of characters;

said analyzing means including means for detecting whether an applied signal represents a character of said first or said second type;

said line starting means being operable to initiate the new display line at a line position advanced beyond the next position in regular sequence upon detection of a signal of said first type, and to initiate the new display line at the next regular position upon detection of a signal of said second type.

11. Apparatus as claimed in claim 10 wherein said line starting means is operative, after completion of the next-to-last line of the display, to position the new group of characters in the first line of the display upon the detection of a natural break point in characters of said first type and to position the new group of characters in the last line of the display upon the detection of a natural break point in characters of the second type.

12. Apparatus as claimed in claim 11 wherein the display lines normally begin with characters of said first type to be followed by characters of said second type at an indented position;

said line starting means being operative to start the new group of characters in the first line at the normal beginning position when a natural break point in characters of said first type is detected and to start the new group of characters in the last line at said indented position when a natural break point in characters of said second type is detected.

13. Apparatus as claimed in claim 1, wherein said image display means comprises recirculating storage means adapted to store electrical signals for representing and developing the characters presented on the display, said storage means having a storage section for each line of the display with each section sub-divided into storage slots for respective characters of the corresponding line, the storage slot in which the next character is to be placed being identified by a flag signal;

means to detect said flag signal as the data in said storage means is recirculated;

character insertion means normally responsive to detection of said flag signal for effecting loading of a waiting character signal into the flag-identified slot;

said control means being operative, in response to the identification by said analyzing means of said predetermined code combination, to inhibit the normal functioning of said character insertion means to prevent loading of the waiting character signal until a subsequent part of said storage means is reached.

14. Apparatus as claimed in claim 13, including means to release the inhibition of said character insertion means when the storage means reaches a slot location corresponding to a predetermined indented position of a display line.

15. Apparatus as claimed in claim 14, wherein said signals comprise signals of first and second types, each display normally starting with signals of said first type and followed by signals of said second type at an indented position along the display line, said control means being operative to provide said inhibiting effect when a character of said second type is detected prior to said intended position, the inhibiting effect being released when the indented position is reached, whereby the waiting character is loaded into the storage means to be presented at said indented position.

16. Apparatus as claimed in claim 13, including means to release the inhibition of said character insertion means when the recirculating storage means reaches a further

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storage section corresponding to a subsequent display line.

17. Apparatus as claimed in claim 16, wherein said inhibiting action is initiated upon the detection of a natural break point within a predetermined number of character positions from the end of the storage section in which the flag signal appears.

18. Apparatus as claimed in claim 1, wherein said applied electrical signals represent first and second types of characters, the lines on said display means normally beginning with characters of said first type;

and character positioning means responsive to the detection of a character of said second type at any position within a predetermined number of character positions after the start of a display;

said character positioning means being operative to place such a detected character in a preselected indented position along said display line with subsequent characters thereafter.

19. Apparatus as claimed in claim 18, including means to detect a character of said first type normally to be placed in any position subsequent to said indented position;

said character positioning means being operative in response to such detection of a character of said first type to place the character in position to begin a new display line.

20. Apparatus as claimed in claim 1, wherein said electrical signals represent first and second types of characters;

said control means including means for starting a display line at a first position to present characters of said first type, and to present characters of said second type at a subsequent indented position and thereafter along said display line.

21. Apparatus as claimed in claim 20, wherein said control means includes means to start a display line at said indented position when the character to be placed at the beginning of a new line is of said second type.

22. Apparatus as claimed in claim 1, wherein said electrical signals represent first and second types of characters;

said analyzing means including means to determine whether a given signal represents one or the other type of character;

said control means including means responsive to the application of a signal representing a character of said first type immediately following a signal representing a character of said second type and operable thereby to start a fresh line on said display.

23. Apparatus as claimed in claim 22, wherein said image display means includes memory means in which is placed data indicating the type of the most recent character to be presented on the display;

said control means including means to compare the type data in said memory means with the type of an applied signal as determined by said analyzing means and operable in accordance with such determination to start a fresh line of the display when there has been a shift from said second type to said first type.

24. Apparatus as claimed in claim 23, wherein said memory means comprises part of a recirculating storage means carrying signals identifying all of the characters to be presented on said display;

the type data for each character being stored as a digital data bit along with the remaining data required to identify the character.

25. Apparatus as claimed in claim 1, including memory means to store certain characteristic features of applied character signals presented on said display means and means to identify the next character position in the normal sequence of progression along a display line;

said control means including character insertion means adapted to position a new character in a location advanced beyond the next character position in the

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normal sequence, said insertion means including means conjointly responsive to:

- (1) the nature of the new character as determined by said analyzing means,
- (2) precedent characteristic features stored in said memory means, and
- (3) the location of the next character position in the normal sequence.

26. Apparatus as claimed in claim 1, wherein said electro-responsive image display means is a cathode-ray-tube; and

circuit means coupled to said cathode-ray-tube responsive to coded electrical signals and arranged to produce control signals for generating corresponding graphic characters on the screen of said cathode-ray-tube.

27. Apparatus as claimed in claim 1, including converter means to receive the applied signals in transmission-coded format and to produce corresponding character signals to serve as control signals for the image display means.

28. Apparatus as claimed in claim 1, including first and second means for applying first and second streams of coded electrical signals from first and second information sources, respectively;

said display means including first and second display devices for presenting information derived from said sources, respectively;

said analyzing means being responsive to said first and second signals; and

said control means including means responsive to the output of said analyzing means and operable to control both of said display devices.

29. Apparatus as claimed in claim 28, wherein said

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analyzing and control means function on a time-shared basis to service both of said display devices.

30. Apparatus as claimed in claim 1, wherein said display means includes a plurality of separate display devices; and

means for presenting the information simultaneously on all of said display devices in said parallel line format.

31. A device of the type described in claim 1, wherein only a finite number of characters may be displayed on each line of said display means; and

wherein said control means includes:

means for determining if a detected natural break point is located within a predetermined number of character positions from the end of the display line, and means responsive to said natural break point being within said predetermined number of character positions from the end of the display line for terminating the display line.

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