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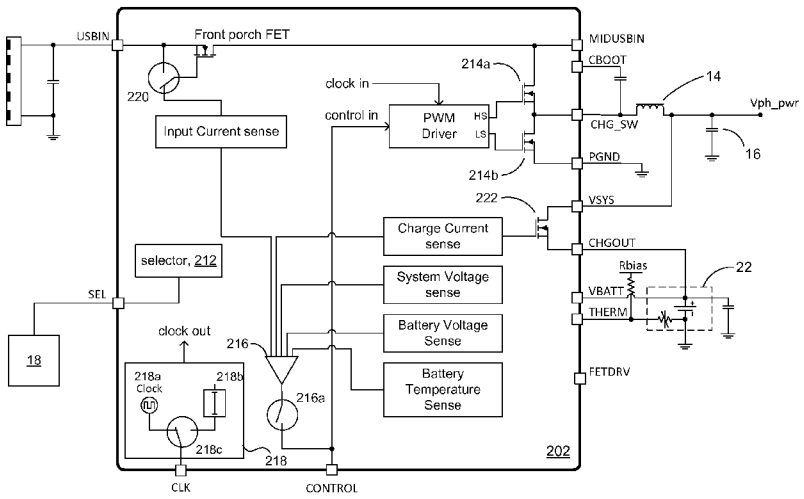

Fig. 2

(57) Abstract: A multi-phase charging circuit comprises a device that can be configured for master mode operation or slave mode operation. In master mode operation, the device generates a control signal and a clock signal to control operation of a switching circuit for generating charging current. In slave mode operation, the device receives externally generated control and clock signals to control operation of its switching circuit.

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MASTER-SLAVE MULTI-PHASE CHARGING

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present disclosure claims priority to U.S. App. No. 14/065,752 filed October 29, 2013 which, in turn, is entitled to and claims the benefit of the filing date of U.S. Provisional App. No. 61/827,443 filed May 24, 2013, the contents of all of which are incorporated herein by reference in their entirety for all purposes.

BACKGROUND

[0002] Unless otherwise indicated herein, the approaches described in this section are not prior art to the claims in this application and are not admitted to be prior art by inclusion in this section.

[0003] As mobile computing devices (e.g., smart phones, computer tablets, and the like) continue to be used more widely, the need for fast charging of batteries becomes more significant. Advancements in fast battery charging techniques are being hampered by the high temperatures that result during fast charge sequences. In most cases, the high temperatures are caused by high inductor temperatures, which can exceed the temperature of the charging circuit.

SUMMARY

[0004] The present disclosure describes a multi-phase charging circuit for operation in a multi-stage parallel configuration to perform battery charging. The multi-phase charging circuit may include selection circuitry to configure the circuit for "master" operation or for "slave" operation. In master configuration, the multi-phase charging circuit may generate clock and control signals to control operation of the charging circuitry in the master-configured circuit itself, and provide those signals to one or more slave-configured circuits as externally generated signals. In slave configuration, the multi-phase charging circuit may use an externally generated clock signal to synchronize operation of its charging circuitry with the master-configured circuit. In some embodiments, the master configured device may provide additional control signals to the control operation in the slave-configured circuits.

[0005] The following detailed description and accompanying drawings provide a better understanding of the nature and advantages of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] With respect to the discussion to follow and in particular to the drawings, it is stressed that the particulars shown represent examples for purposes of illustrative discussion, and are presented in the cause of providing a description of principles and conceptual aspects of the present disclosure. In this regard, no attempt is made to show implementation details beyond what is needed for a fundamental understanding of the present disclosure. The discussion to follow, in conjunction with the drawings, make apparent to those of skill in the art how embodiments in accordance with the present disclosure may be practiced. In the accompanying drawings:

[0007] Fig. 1 shows a printed circuit board (PCB) level embodiment of the present disclosure.

[0008] Figs. 1A and 1B show additional illustrative embodiments in accordance with the present disclosure.

[0009] Fig. 2 shows a general view of a charging circuit in accordance with the present disclosure.

[0010] Fig. 3 shows a single-phase configuration of a charging circuit in accordance with the present disclosure.

[0011] Figs. 4A and 4B show a dual-phase configuration of charging circuits in accordance with the present disclosure.

[0012] Figs. 5A, 5B, and 5C show a 3-phase configuration of charging circuits in accordance with the present disclosure.

[0013] Fig. 6 illustrates an example of an implementation of a master-only charging circuit in accordance with the present disclosure.

[0014] Fig. 7 illustrates an example of an implementation of a slave-only charging circuit in accordance with the present disclosure.

[0015] Figs. 8A, 8B, and 8C illustrate an embodiment for a dual-input master-slave configuration.

[0016] Fig. 9 illustrates an embodiment for a dual-input master.

DETAILED DESCRIPTION

[0017] In the following description, for purposes of explanation, numerous examples and specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be evident, however, to one skilled in the art that the present disclosure as expressed in the claims may include some or all of the features in these examples, alone or in combination with other features described below, and may further include modifications and equivalents of the features and concepts described herein.

[0018] Fig. 1 shows a portion of a printed circuit board (PCB) 10 populated with battery charging devices in accordance with the present disclosure. The PCB 10 may be a circuit board, for example, in a mobile computing device, a smart phone, and in general any electronic device. The PCB 10 may be populated with battery charging devices 102, 102a, 102b. It will be appreciated in the discussions to follow that fewer or more battery charging devices may be provided. Each of the battery charging devices 102, 102a, 102b may be embodied in any suitable integrated circuit (IC) packaging format (e.g., single in-line packaging, dual in-line packaging, surface mount devices, and so on) and interconnected on the PCB 10.

[0019] In some embodiments, the battery charging devices 102, 102a, 102b are identical devices that can be configured for different modes of operation. For example, device 102 may be configured for "master" mode operation, while devices 102a, 102b may be configured for "slave" mode operation. It will be understood that battery charging devices 102, 102a, 102b may include pins or terminals (not shown) that allow the devices to be interconnected on the PCB 10 using PCB traces, represented generally by 12.

[0020] In accordance with principles of the present disclosure, the battery charging devices 102, 102a, 102b may be connected to a battery 22 via a connection 24 (e.g., battery terminal) for coordinated charging of the battery by the battery charging devices. The battery 22 may comprise any known configuration of one or more cells (e.g., a single-cell configuration, a multi-cell, multi-stack configuration, etc.) and may be use any suitable chemistry that allows for recharging.

[0021] In some embodiments, the battery charging devices 102, 102a, 102b operate as buck converters, and in other embodiments the battery charging devices may comprise buck-boost converters. In some embodiments, the inductive component of the buck converter may be provided as external inductive elements 14 provided on the PCB 10. Accordingly, each

battery charging device 102, 102a, 102b may be connected to a corresponding external inductive element 14, such as an inductor. The inductive elements 14 are "external" in the sense that they are not part of the charging ICs that comprise the battery charging devices 102, 102a, 102b. In accordance with the present disclosure, the capacitive component of the buck converters may be provided as an external capacitive element 16 on the PCB 10 that can be shared by each battery charging device 102, 102a, 102b. The capacitive element 16 is "external" in the sense that it is not part of the charging ICs that comprise the battery charging devices 102, 102a, 102b.

[0022] Further in accordance with the present disclosure, each battery charging device 102, 102a, 102b may be connected to a corresponding external selection indicator 18 to configure the device for master or slave mode operation. Each selection indicator 18 is "external" in the sense that it is not part of the charging IC that comprises the device. In some embodiments, the selection indicator 18 may be a resistive element. For example, a connection to ground potential (e.g., approximately 0Ω) may serve to indicate the device (e.g., 102) should operate in master mode. A non-zero resistance value (e.g., 10KΩ, 100KΩ, etc.) may serve to indicate that the device (e.g., 102a, 102b) should operate in slave mode. More generally, in other embodiments, the selection indicator 18 may be a source of a suitable analog signal or digital signal that can serve to indicate to the device 102, 102a, 102b whether to operate in master mode or slave mode.

[0023] Power to the battery charging devices 102, 102a, 102b may be externally provided via any suitable connector 26. Merely as an example, the connector 26 may be a USB connector. Power from the VBUS line of a USB connector may be connected to device 102 (e.g., at a USBIN terminal), which may then distribute the power to the other devices 102a, 102b via a MIDUSBIN terminal. These and other terminals will be described in more detail below.

[0024] One of ordinary skill will appreciate that embodiments according to the present disclosure may include any electronic device. For example, Fig. 1A points out that the PCB 10 may be incorporated in any electronic device 50 to charge battery 22. Fig. 1B illustrates another configuration in which PCB 10 may be provided in a first electronic device 52 that has a connection 54 to a second electronic device 56 to charge battery 22 in the second electronic device. In some embodiments, the connection 54 may not be physical, for

example, wireless energy transfer from device 52 may be provided using magnetic induction circuitry (not shown).

[0025] The discussion will now turn to details of battery charging device 102 in accordance with some embodiments of the present disclosure. Fig. 2 shows a simplified schematic representation of the battery charging device 102. In some embodiments, the battery charging device 102 may comprise a charging IC 202. It will be appreciated that in some implementations, the design of the charging IC may be implemented on two or more ICs. For purposes of discussion, however, we can assume a single charging IC implementation without loss of generality.

[0026] The charging IC 202 may comprise circuitry to provide battery charging functionality in accordance with principles of the present disclosure. In some embodiments, for example, the battery charging functionality may be provided using a buck converter, or a buck-boost converter, and so on. Accordingly, the charging IC 202 may include a high-side FET 214a and a low-side FET 214b that can be configured in a buck converter topology in conjunction with inductive element 14 and capacitive element 16.

[0027] A pulse width modulated (PWM) driver circuit may produce gate drive signals (HS, LS) at its switching output to switch the gates of respective FETs 214a and 214b. The PWM driver circuit may receive a current-mode control signal at its control input and a clock signal at its clock input to control the switching of FETs 214a and 214b. Power (Vph_pwr) from the buck converter may be connected to charge the battery 22 through battery FET 222 via the VSYS and CHGOUT terminals of the charging IC 202. The battery FET 222 may serve to monitor the charge current (e.g., using a charge current sense circuit).

[0028] In accordance with principles of the present disclosure, the control signal may be internally generated within the charging IC 202 or externally provided to the charging IC. For example, a feedback compensation network comprising various feedback control loops and a comparator 216 may serve as a source of an internally generated control signal. In a particular embodiment, the feedback control loops may include an input current sense circuit (e.g., senses input current at USBIN), a charge current sense circuit (e.g., senses current at VSYS and CHGOUT terminals using battery FET 222), a system voltage sense circuit (e.g., senses voltage at VSYS terminal), a battery voltage sense circuit (e.g., senses battery voltage at VBATT terminal), and a battery temperature sense circuit (e.g., senses battery temperature at THERM terminal). In other embodiments, the feedback control loops may comprise fewer, or

additional, sense circuits. The comparator 216 may produce a reference that serves as the internally generated control signal.

[0029] The control signal produced by comparator 216 is "internal" in the sense that the control signal is generated by circuitry that comprise the charging IC 202. By comparison, a control signal is considered to be "externally" provided when the signal is received from a source external to the charging IC 202; e.g., via the CONTROL terminal of the charging IC. In some embodiments, a control selector 216a may be provided to select either the internal control signal generated by the comparator 216 or an externally generated control signal received on the CONTROL terminal to serve as the control signal for the PWM driver circuit.

[0030] In accordance with principles of the present disclosure, the clock signal may be internally generated within the charging IC 202 or externally provided to the charging IC. For example, the charging IC 202 may include a clock generator 218 to produce a clock signal (clock out). The clock generator 218 may include a clock generating circuit 218a and a delay element 218b. The clock generating circuit 218a may produce a clock signal that serves as an internally generated clock signal. The delay element 218b may receive an externally provided clock signal.

[0031] The clock signal produced by the clock generating circuit 218a is "internal" in the sense that the clock signal is generated by circuitry that comprise the charging IC 202, namely the clock generating circuit. By comparison, a clock signal is considered to be "externally" provided when the signal is received from a source external to the charging IC 202; e.g., via the CLK terminal of the charging IC. In some embodiments, a clock selector 218c may be provided to select either the internal clock signal generated by the clock generating circuit 218a or an external clock signal provided on the CLK terminal and delayed (phase shifted) by the delay element 218b to serve as the clock signal for the PWM driver circuit.

[0032] The charging IC 202 may include a selector circuit 212 to configure the charging IC to operate in "master" mode or "slave" mode according to the external selection indicator 18 provided on an SEL input of the charging IC. The selection indicator 18 may be a circuit, or a source of an analog signal (e.g., an analog signal generator) or a digital signal (e.g., digital logic). In some embodiments, for example, the selection indicator 18 may be an electrical connection to ground potential, either directly or through a resistive element. The selector circuit 212 may operate the control selector 216a and the clock selector 218c according to the

selection indicator 18. The selector circuit 212 may also operate a switch 220 to enable or disable sensing of the current input in accordance with the selection indicator 18.

[0033] In accordance with the present disclosure, the charging IC 202 may be configured as a single-phase standalone device, or used in a multi-phase configuration. The discussion will first describe a single-phase configuration. Fig. 3 illustrates an example of the charging IC 202 configured to operate as a standalone battery charger. The charging IC 202 may be configured using the SEL input to operate in master mode. In some embodiments, master mode operation in charging IC 202 may be designated by a selection indicator 18 that comprises a connection of the SEL input to ground potential. This convention for designating master mode operation will be used for the remainder of the disclosure with the understanding that, in other embodiments, other conventions may be adopted to indicate master mode operation.

[0034] In an embodiment, the selector 212 may be configured to respond to the presence of a ground connection at the SEL input by configuring the charging IC 202 for master mode operation. For example, the selector 212 may operate the control selector 216a in a first configuration to provide an internally generated control signal to the control input of the PWM driver circuit. The internally generated control signal is also provided to the CONTROL terminal of charging IC 202, which for the single-phase configuration shown in Fig. 3 is not relevant.

[0035] Similarly, the selector 212 may operate the clock selector 218c in a first configuration to provide an internally generated clock signal (e.g., via clock generating circuit 218a) to the clock input of the PWM driver circuit. The internally generated clock signal is also provided to the CLK terminal of charging IC 202, which for the single-phase configuration shown in Fig. 3 is not relevant. The selector 212 may also operate switch 220 to a configuration that enables input current sensing on the power input USBIN.

[0036] In operation, the master-mode configured charging IC 202 shown in Fig. 3 operates as a buck converter to charge battery 22. Feedback control to the PWM driver circuit is provided by the circuitry comprising the charging IC 202, and likewise, the clock signal to the circuit is provided from within the charging IC. The configuration is a "standalone" configuration in the sense that there is only one charging IC.

[0037] The discussion will now turn to a description of an example of a multi-phase configuration of the charging IC 202 in accordance with the present disclosure, and in

particular a dual-phase configuration. In a dual-phase configuration, two charging ICs 202 are connected and operate together to charge a battery 22. One of the charging ICs 202 may be configured as a master device and the other as a slave device. Figs. 4A and 4B show an example of charging ICs 202a and 202b configured to operate respectively as a master device and as a slave device. The charging ICs 202a, 202b are connected together at connections A, B, C, D, E, F, and G. The resulting current flow is illustrated in Figs. 4A and 4B as flow 422.

[0038] The charging IC 202a shown in Fig. 4A is configured for master mode operation as described in Fig. 3. In accordance with the present disclosure, the control signal generated by the comparator 216 in charging IC 202a is provided as an externally generated control signal 402 (e.g., via the CONTROL terminal), in addition to serving as an internally generated control signal for the PWM driver circuit in the charging IC. Similarly, the clock signal generated by the clock generator 218 is provided as an externally generated clock signal 404 (e.g., via the CLK terminal), in addition to serving as an internally generated clock signal for the PWM driver circuit in the charging IC 202a.

[0039] Referring to Fig. 4B, the charging IC 202b is configured for slave mode operation. The charging IC 202b may be configured using the SEL input to operate in slave mode. In some embodiments, slave mode operation may be designated by a selection indicator 18 that comprises a resistive element. This convention for designating slave mode operation will be used for the remainder of the disclosure with the understanding that, in other embodiments, other conventions may be adopted to indicate salve mode operation. In a particular embodiment, for example, a 10K resistor may be used to indicate slave mode operation. It will be appreciated, of course, that another resistance value may be used. The selector 212 may be configured to respond to the detection of a 10KΩ resistance at the SEL input by configuring the charging IC 202b for slave mode operation.

[0040] In slave mode operation, the selector 212 may operate the control selector 216a in a second configuration to receive the externally generated control signal 402 that is received on the CONTROL terminal of the charging IC 202b. The control selector 216a provides the externally generated control signal 402 to the control input of the PWM driver circuit. Operation of the control selector 216a in the second configuration disconnects or otherwise effectively disables the feedback network in charging IC 202b from the PWM driver circuit. This "disconnection" is emphasized in the figure by illustrating the elements of the feedback network in charging IC 202b using broken grayed out lines.

[0041] The selector 212 in charging IC 202b may also operate the clock selector 218c in a second configuration to receive the externally generated clock signal 404 on the CLK terminal. The clock selector 218c provides the externally generated clock signal 404 to the delay element 218b. The clock signal that is provided to the PWM driver circuit comes from the delay element 218b, thus disconnecting or otherwise effectively disabling the clock generating circuit 218a in the charging IC 202b.

[0042] Switch 220 may be configured (e.g., by selector 212) to disable current sensing at the USBIN terminal of charging IC 202b. Power to the high- and low- side FETs 214a, 214b may be provided by the MIDUSBIN terminal via connection B. Similarly, charge current sensing in the slave-configured charging IC 202b may be disabled by disabling its battery FET 222.

[0043] As can be appreciated from the foregoing description, operation of the PWM driver circuit in the slave-mode charging IC 202b is controlled by the control signal and clock signal that is generated in the master-mode charging IC 202a and provided to the slave-mode charging IC 202b respectively as externally generated control and clock signals 402, 404. From the point of view of the slave-mode charging IC 202b, the control and clock signals generated in the master-mode charging IC 202a are deemed to be "externally generated."

[0044] The master-mode charging IC 202a may synchronize with the slave-mode charging IC 202b by asserting a signal on the FETDRV terminal. For example, when the master-mode charging IC 202a pulls the FETDRV terminal LO, the PWM driver circuit in the slave-mode charging IC 202b is disabled. When the master-mode charging IC 202a pull the FETDRV terminal HI, the PWM driver circuit in the slave-mode charging IC 202b begins switching. In some embodiments, the FETDRV terminal may be used by the master-mode charging IC 202a to initiate switching in the slave-mode charging IC 202b after the input current rises above a threshold level, in order to balance light-load and heavy-load efficiency. For example, switching losses at light load can outweigh the decreased conduction losses, which can be avoided by not enabling the slave-mode charging IC 202b right away. After enablement, the slave-mode charging IC 202b will operate in synchrony with the clock signal from the master-mode charging IC 202a. Control of the PWM driver circuit in the slave-mode charging IC 202b will be provided by the control signal from the master-mode charging IC 202a, thus allowing the master to set the charge current limit, input current limit, etc.

[0045] In accordance with the present disclosure, the delay element 218b may be configured (e.g., by selector 212) to provide a selectable phase shift that is suitable for dual-phase operation. For example, the delay element 218b may provide a 180° phase shift of the externally generated clock signal 404. Accordingly, the clock signal that is provided to the clock input of the PWM driver circuit in the slave-mode charging IC 202b is 180° out of phase relative to the clock signal in the master-mode charging IC 202a. Consequently, the charging cycle of the master-mode charging IC 202a will be 180° out of phase relative to the charging cycle of the slave-mode charging IC 202b. For example, when the high-side FET 214a is ON in the master device, the high-side FET in the slave device is OFF, and vice-versa.

[0046] The discussion will now turn to a description of a 3-phase configuration of the charging IC 202 in accordance with the present disclosure. In a 3-phase configuration, three charging ICs 202 are connected and operate together to charge a battery 22. One of the charging ICs 202 may be configured as a master device and the other two as slave devices. Figs. 5A-5C show an example charging ICs 202a, 202b, and 202c configured to operate respectively as a master device, a first slave device, and a second slave device. The charging ICs 202a, 202b, 202c are connected at connections A1, B1, C1, D1, E1, F1, and G1 and connections A2, B2, C2, D2, E2, F2, and G2.

[0047] The master device in Fig. 5A is configured as explained in connection with Fig. 4A. The first and second slave devices (Figs. 5B and 5C) are configured as explained in connection with Fig. 4B. In 3-phase operation, the delay elements 218b in the first and second slave devices may be configured to provide 120° and 240° phase shifts, respectively, of the externally generated clock signal 404 as the clock input for the respective PWM driver circuits. For example, the selection indicator 18 in the first slave device of Fig. 5B may be a 100K resistor to indicate 120° phase shift, and similarly, the selection indicator 18 in the second slave device of Fig. 5C may be a 1M resistor to indicated 240° phase shift. It will be appreciated, of course, that other resistance values may be used. In operation, the charging cycle of the master device (Fig. 5A) will be 120° out of phase relative to the charging cycle of the first slave device (Fig. 5B) and 240° out of phase relative to the charging cycle of the second slave device (Fig. 5C).

[0048] It will be appreciated that, more generally, N-phase operation may be provided using N charging ICs (one master device and (N-1) slave devices) and connecting them in

accordance with the examples shown in the figures. Each of the (N-1) slave devices receives from the master device the externally generated control signal 402 and the externally generated clock signal 404. In some embodiments, the m^{th} slave device may be configured (e.g., using a suitable selection indicator 18) to provide an $m\times(360\div N)°$ phase shift (e.g., using the delay element 218b) of the externally generated clock signal 404 as the clock input for its PWM driver circuit. In some embodiments, the quantity $(m\div N)$ is an integral multiple of 360.

[0049] The discussion will now turn to another embodiment of charging ICs in accordance with the present disclosure. In some embodiments, a charging IC may be implemented as a master-only device. In other words, the charging IC always operates in master mode and is not configurable to operate as a slave device. Fig. 6, for example, shows a charging IC 602 comprising, among other components, a feedback network comprising several sensor components (e.g., input current sense, charge current sense, etc.) that feed into a comparator 616. The comparator output generates an internally generated control signal that feeds into the control input of the PWM driver circuit and which serves as an externally generated control signal 622 that is output at the CONTROL terminal. The charging IC 602 further comprises a clock 618 that generates a clock signal that generates an internally generated clock signal, which feeds into the clock in of the PWM driver circuit, and which serves as an externally generated clock signal 624 that is output at the CLK terminal. This particular embodiment of charging IC always uses its internally generated control and clock signals and always outputs those signals as respective externally generated control and clock signals. As such, the charging IC 602 can omit selector 212, selectors 216a, 218b, and 220, and the delay element 218b in order to realize a smaller, lower cost device.

[0050] In some embodiments, a charging IC may be implemented as a slave-only device. Fig. 7, for example, shows a charging IC 702 comprising a PWM drive circuit having a control input that receives only an externally generated control signal 722 (e.g., from the CONTROL terminal). The PWM driver circuit, furthermore, has a clock input that receives only an externally generated clock signal 724 (e.g., from the CLK terminal). The selector 712 serves to configure a delay element 718 to provide phase shifting of the externally generated clock signal 724 according to the selection indicator 18. For example, the delay element 718 may be configured to provide an $m\times(360\div(M+1))°$ phase shift of the externally generated clock signal depending on what is connected to the selector 712, where m identifies the charging IC 702 as being the m^{th} slave device among a total of M slave devices.

[0051] The charging IC 702 is "slave-only" in the sense that it does not generate its control and clock signals internally, but rather obtains them from a source external to the charging IC. Since the control signal and clock signal are always externally generated, the slave-only charging IC 702 can omit the circuitry comprising the feedback network and the clock. Likewise, the slave-only charging IC 702 can omit the input FET and battery FET, since the device does not need to sense the input current. This can be advantageous in terms of a smaller device and/or a lower cost device, especially since the input and battery FETs are power FETs which can occupy significant areas on the die.

[0052] In some embodiments, the slave-only charging IC 702 may include additional circuitry to enhance performance. Though not illustrated, for example, a slave-only charging IC may include inductor current sense circuitry for peak current limiting. As another example, a slave-only charging IC may additionally include a thermal loop to ensure the junction temperature does not exceed a maximum operating limit.

[0053] The discussion will now turn to a description of a dual-input two-phase master-slave configuration. Referring to Figs. 8A, 8B, and 8C, a charging IC in accordance with the present disclosure may further include a FETCRTL terminal. Fig. 8A shows the charging IC 802a configured as a dual-input master. In a particular embodiment, for example, the dual-input master configuration may be indicated with a selection indicator 18 that comprises a 100KΩ resistor. Fig. 8B shows the charging IC 802b configured as a dual-input slave, operating in slave mode. Fig. 8C shows the charging IC 802b operating in master mode. In a particular embodiment, the dual-input slave configuration may be indicated using a selection indicator 18 that comprises a 200KΩ resistor. The configuration is "dual-input" in the sense that there are two voltage inputs. A first voltage input (e.g., USBIN) may be connected to the dual-input master 802a and a second voltage input (e.g., DCIN) may be connected to the dual-input slave 802b via a DCIN FET 812, as illustrated in Figs. 8A-8C for example.

[0054] In operation, when there is a voltage on USBIN terminal of the dual-input master 802a, the dual-input configured charging ICs 802a and 802b operate in a master/slave mode as explained above. For example, the dual-input master 802a generates a feedback control signal 802 that is used by the master and provided to the slave (Fig. 8B) via the CONTROL terminal. Likewise, the dual-input master 802a generates a clock signal 804 that is used by the master and provided to the slave via the CLK terminal. The dual-input slave 802b shown in Fig. 8B uses the externally provided control signal 802 and clock signal 804 to control its

PWM driver circuit. In addition, the dual-input master 802a asserts FETCTRL (e.g., goes high-z) to turn OFF the DCIN FET 812 that is connected to the dual-input slave 802b. This serves to electrically isolate the DCIN voltage source (if present) from the USBIN (DCIN) terminal of the dual-input slave 802b. The dual-input master 820a asserts FETDRV (e.g., pulls HIGH) to signal the dual-input slave 802b to operate in slave mode.

[0055] When there is no voltage on the USBIN terminal of the dual-input master 802a, the master does not perform battery charging. The dual-input master 802a will assert FETCTRL (e.g., goes LOW) to turn ON the DCIN FET 812 to allow current flow from the DCIN voltage source. The dual-input slave 802b operates in master mode to perform battery charging using the DCIN input provided on its USBIN terminal. This master operating mode of the dual-input slave 802b is illustrated in Fig. 8C. Notably, the dual-input slave 802b does not receive an external control signal or clock signal on its CONTROL and CLK terminals, since the dual-input master 802a is not performing battery charging. Instead, the dual-input slave 802b generates its own control and clock signals and performs battery charging from DCIN in master mode.

[0056] The discussion will now turn to a description of a multi-phase master-slave configuration using, as the master device, a charging IC of the present disclosure configured for two voltage source inputs. Fig. 9 illustrates a dual-input charging IC 902 configured with a charging IC 904 configured for slave mode operation. The bounding box 900 is used to indicate that device 904 and a portion of device 902 are configured as illustrated in Figs. 4A and 4B. In some embodiments, the device 902 may be configured to always operate in master mode. The device 904 may be configured with a selection indicator comprising a 1kΩ resistor to indicate that the slave may operate in on-the-go (OTG) mode.

[0057] In operation, when charging from USBIN, the devices 902, 904 may operate in master/slave mode to provide multi-phase charging of the battery 22 as explained in the foregoing embodiments. However, when device 902 is charging from DCIN, the device 904 may be signaled to operate in OTG mode. For example, device 904 may include interface circuitry (not shown) to receive a command via the Inter-Integrated Circuit (I^2C) communication protocol. It will be appreciated, of course, that any other suitable signaling may be used.

[0058] In OTG mode, the device 904 provides power from the battery 22 directly to the USBIN terminal. Fig. 9 illustrates the two different current flows 912, 914 in this "OTG"

mode of operation. Flow 912 represents charging current from the dual-input charging IC 902 to charge battery 22. Flow 914 represents current from battery 22 to the USBIN terminal of device 902. It is noted that though control and clock signals from device 902 may be provided on its respective CONTROL and CLK terminals, the signals are not used by the device 904 in OTG mode.

Advantages and Technical Effect

[0059] Charging circuitry in accordance with the present disclosure allow for the paralleling of multiple battery chargers. Each battery charger is connected to its own inductive element, thus creating an opportunity for improved thermal performance by allowing for the use of smaller inductors. In addition, the smaller inductors allows for smaller packaging footprints. Multiple battery chargers allow for current sharing, thus distributing the power load among the battery chargers. Since each battery charger operates out of phase relative to the other battery chargers, the battery "sees" a charging current that has reduced ripple.

[0060] Another advantage of embodiments according to the present disclosure is flexibility in system design. Each battery charger may be used in a single phase standalone configuration, or in a multi-phase configuration of two or more devices.

[0061] Additional flexibility can be realized by incorporating a master device in larger a power management IC. A particular user may then design a multi-phase configuration by simply adding one or more slave-configured devices to their system.

[0062] The above description illustrates various embodiments of the present disclosure along with examples of how aspects of the particular embodiments may be implemented. The above examples should not be deemed to be the only embodiments, and are presented to illustrate the flexibility and advantages of the particular embodiments as defined by the following claims. Based on the above disclosure and the following claims, other arrangements, embodiments, implementations and equivalents may be employed without departing from the scope of the present disclosure as defined by the claims.

[0063] We claim the following:

1. A circuit for a battery charger, the circuit comprising:

a switching circuit having a control input, a clock input, and a switching output configured to connect to an inductive element;

a charging terminal configured to electrically connect the inductive element to a battery terminal to provide power to charge a battery connected to the battery terminal;

a control terminal;

a clock terminal;

a control selector configured to operate in a first configuration that provides an internally generated control signal to the control terminal and the control input of the switching circuit, and to operate in a second configuration that provides an externally generated control signal received on the control terminal to the control input of the switching circuit; and

a clock selector configured to operate in a first configuration that provides an internally generated clock signal to the clock terminal and the clock input of the switching circuit, and to operate in a second configuration that provides an externally generated clock signal received on the clock terminal to the clock input of the switching circuit.

2. The circuit of claim 1 further comprising a first FET and a second FET connected to the switching output of the switching circuit, the first FET being connected to the second FET, the first FET and the second FET being switched ON and OFF by the switching circuit in accordance with control signal received on the control input and a clock signal received on the clock input.

3. The circuit of claim 1 further comprising a delay element that can be selectively connected by the clock selector between the clock input and the clock terminal to provide an externally generated clock signal received on the clock terminal to the clock input.

4. The circuit of claim 3 wherein the delay element is configured to provide a selectable phase shift of the externally generated clock signal.

5. The circuit of claim 1 further comprising a clock signal generator to generate the internally generated clock signal; and a delay element,

wherein the clock selector, when operating in the first configuration, connects the clock signal generator to the clock terminal and the clock input of the switching circuit,

wherein the clock selector, when operating in the second configuration, connects the delay element between the clock input and the clock terminal to provide an externally generated clock signal received on the clock terminal to the clock input.

6. The circuit of claim 5 wherein the delay element is configured to produce a phase shift of the externally generated clock signal.

7. The circuit of claim 1 further comprising a control signal generator to generate the internally generated control signal,

wherein the control selector, when operating in the first configuration, connects the control signal generator to the control terminal and the control input of the switching circuit,

wherein the control selector, when operating in the second configuration, connects the control terminal to the control input to provide an externally generated control signal received on the control terminal to the control input.

8. The circuit of claim 1 further comprising a selector input configured to connect to an external selection indicator, wherein the control selector and the clock selector operate in the first or second configuration depending on the selection indicator.

9. The circuit of claim 8 wherein the delay element is configured to produce a phase shift of the externally generated clock signal depending on the selection indicator.

10. The circuit of claim 8 wherein the external selection indicator is a digital signal.

11. The circuit of claim 8 wherein the external selection indicator is an analog signal.

12. The circuit of claim 8 wherein the external selection indicator comprises one or more resistor elements.

13. A charging circuit comprising:

a control terminal;

a clock terminal;

a high-side FET and a low-side FET;

a PWM driver for driving the high-side FET and the low-side FET;

feedback circuitry comprising a plurality of control loops, the feedback circuitry generating a control signal;

a clock module comprising a clock generator and a delay element, the clock module generating a clock signal that is provided to the PWM driver; and

a selection module to configure the charging circuit in a first configuration or a second configuration,

wherein in the first configuration, the control signal is provided to the PWM driver and to the control terminal, and the clock signal is generated from the clock generator,

wherein in the second configuration, an externally generated control signal received on the control terminal is provided to the PWM driver, an externally generated clock signal received on the clock terminal is provided to the delay element, and the clock signal is an output of the delay element.

14. The charging circuit of claim 13 wherein the delay element provides a selectable phase shift.

15. The charging circuit of claim 13 wherein in the first configuration, the clock signal is not generated from the delay element, wherein in the second configuration, the clock signal is not generated from the clock generator.

16. The charging circuit of claim 13 wherein in the first configuration, the control signal generated by the feedback circuitry and provided on the control terminal serves as an externally generated control signal.

17. The charging circuit of claim 13 wherein in the first configuration, the clock signal generated by the clock module and provided on the clock terminal serves as an externally generated clock signal.

18. A charging circuit comprising:

a PWM driver for driving a high side FET and a LOW side FET;

a delay element;

a first input pin connected to the PWM driver provide the PWM driver with an externally provided control signal received on the first input pin; and

a second input pin connected to the delay element to provide the delay element with an externally provided clock signal received on the second input pin, wherein the delay element delays the clock signal to produce a delayed clock signal which is provided to the PWM driver.

19. The charging circuit of claim 18 wherein the control signal to the PWM driver is provided only by the externally provided control signal.

20. The charging circuit of claim 18 wherein the clock signal to the PWM driver originates only from the externally provided clock signal.

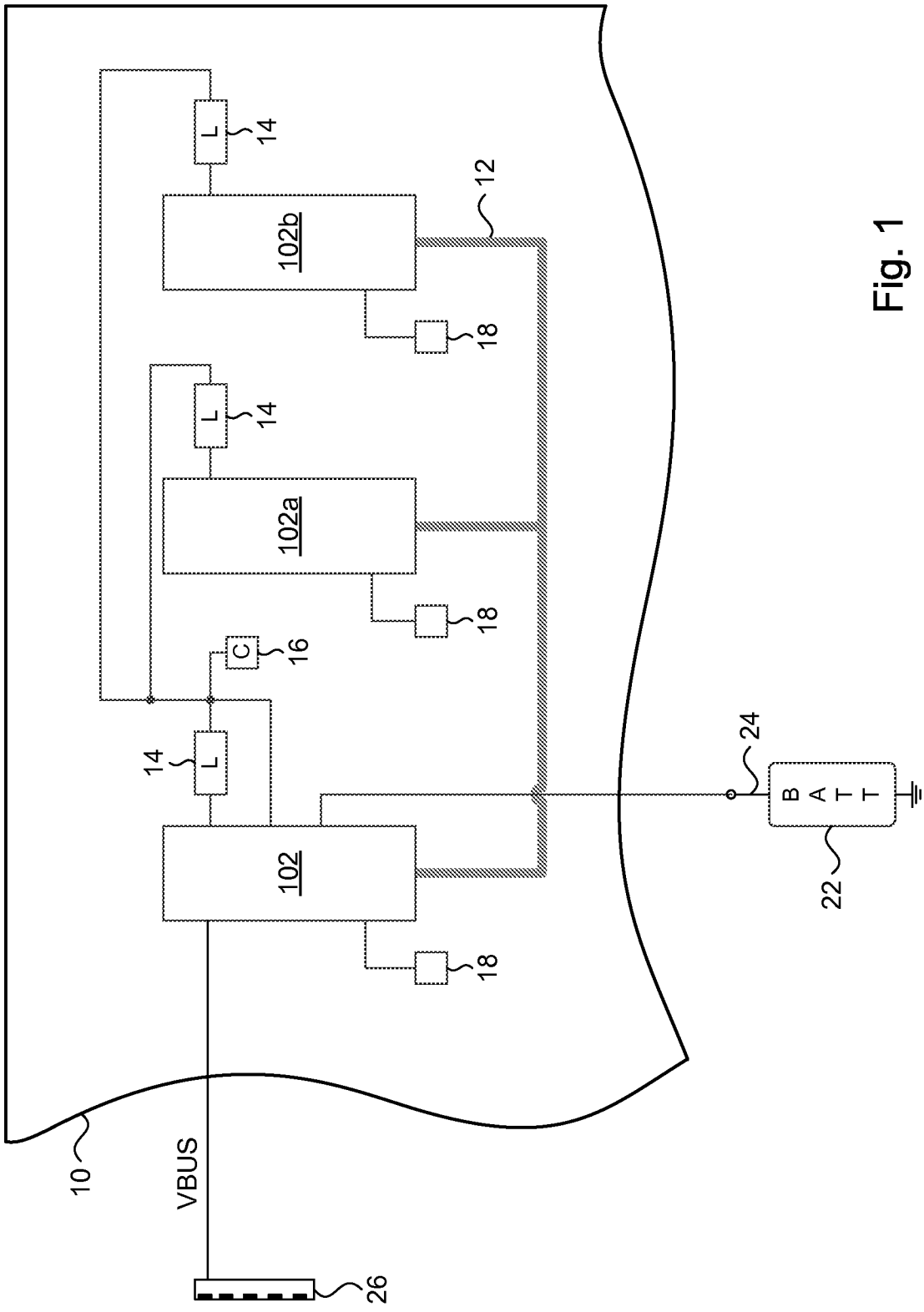

Fig. 1

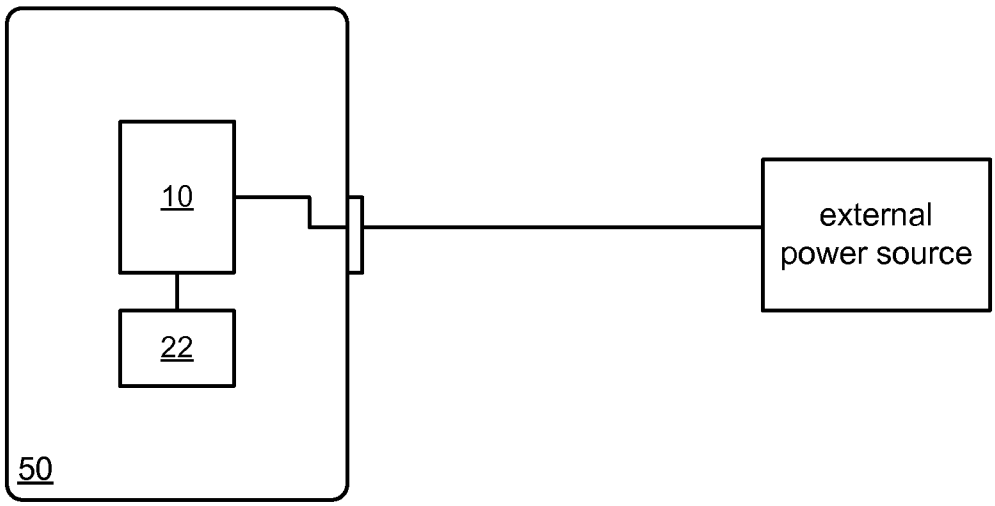
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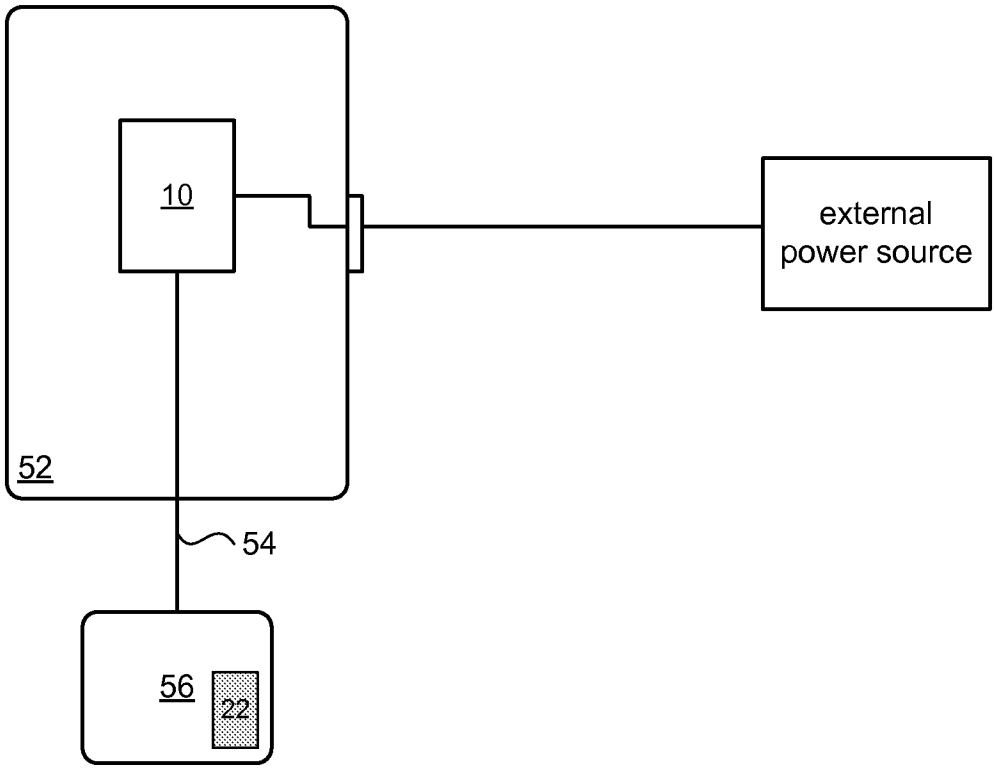
Fig. 1A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22
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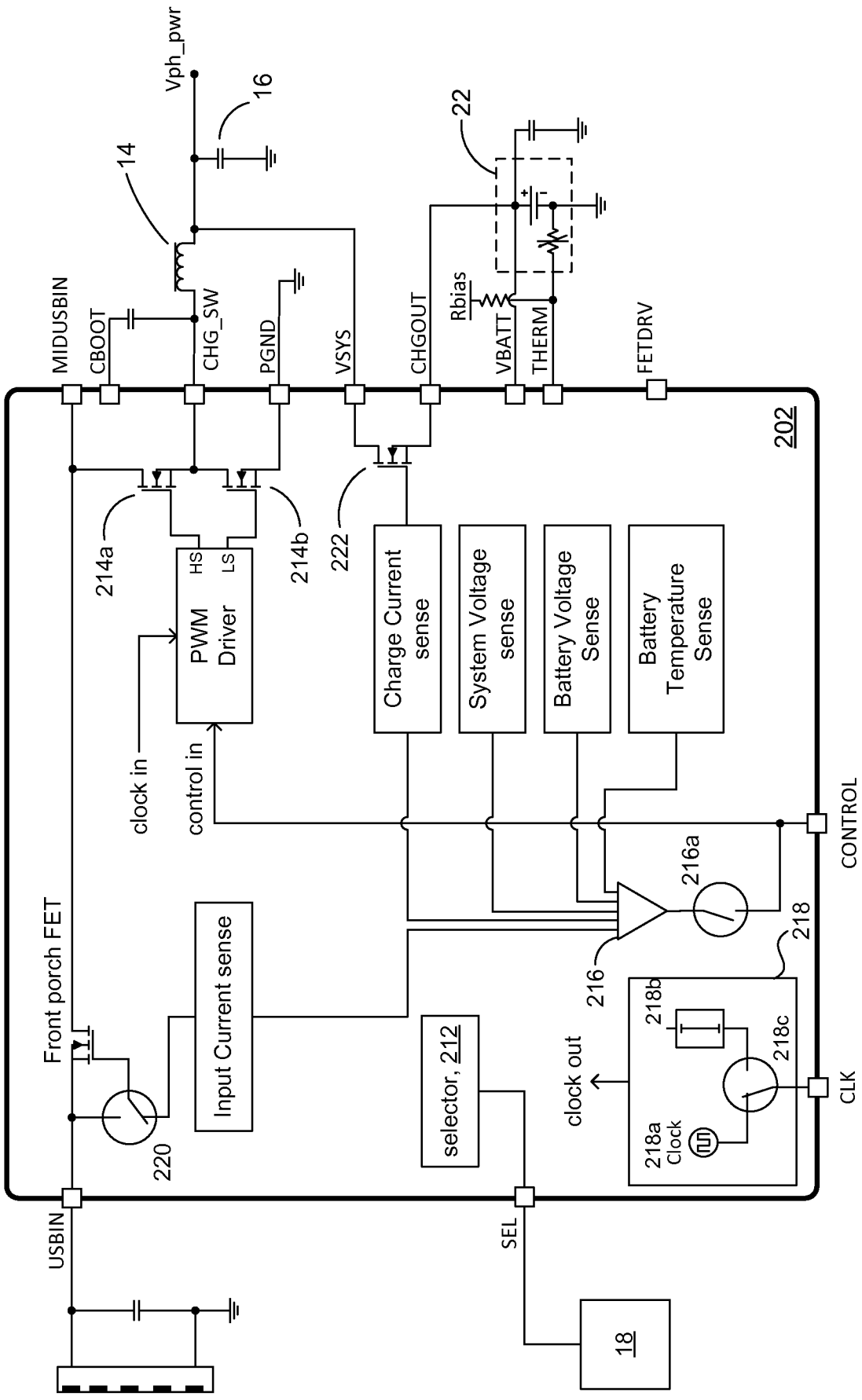
power source

Fig. 1B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214a
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222
HS
LS
PWM Driver
Charge Current sense
System Voltage sense
Battery Voltage Sense
Battery Temperature Sense
clock in
control in
CONTROL
216a
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218b
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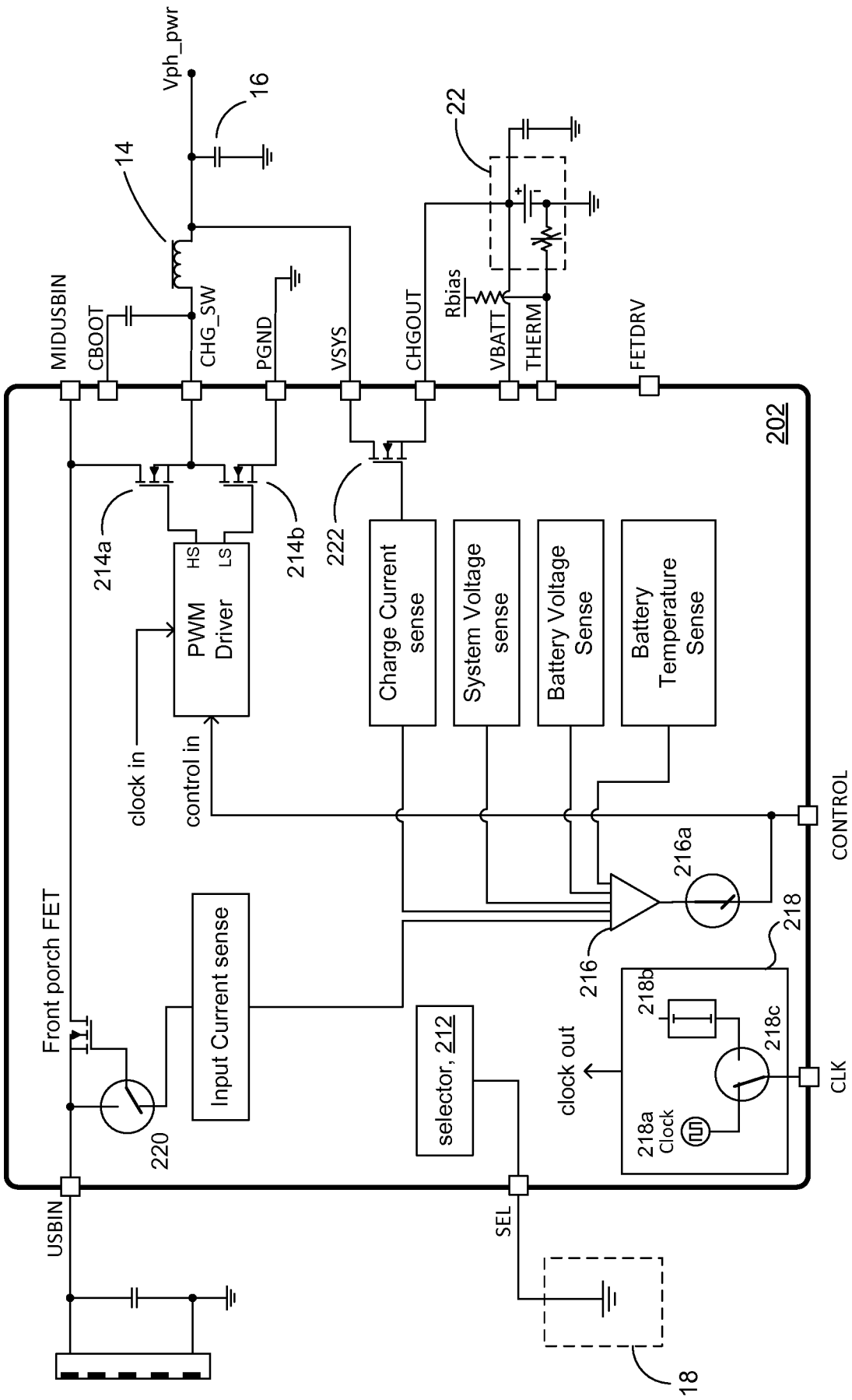
CLK
clock out
Front porch FET
Input Current sense
220
selector, 212
USBIN
SEL
18

Fig. 2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Charge Current sense
System Voltage sense
Battery Voltage Sense
Battery Temperature Sense
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control in
CONTROL
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SEL
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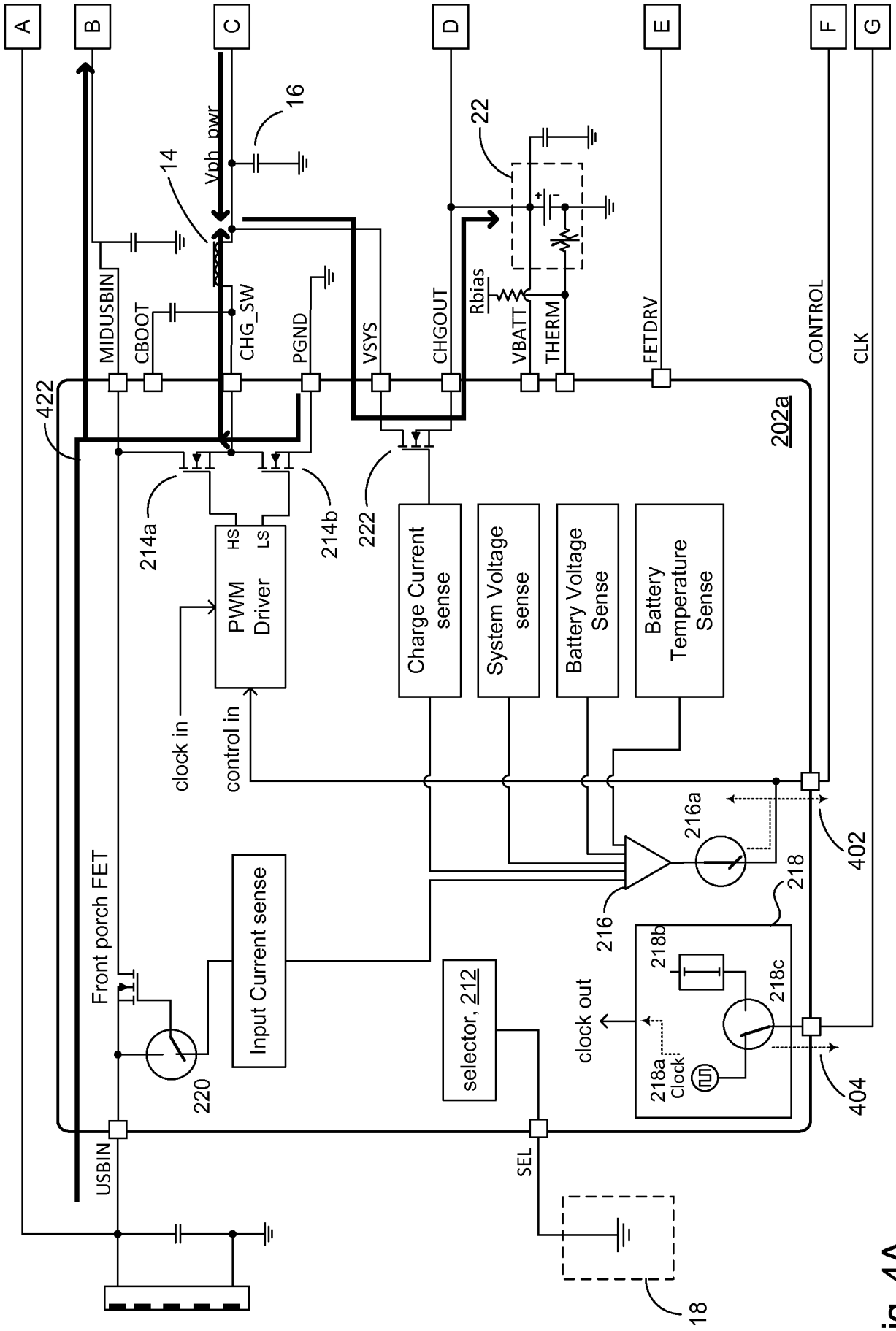
Fig. 3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VBATT
THERM
FETDRV
CONTROL
CLK
422
202a
214a
214b
222
HS
LS
PWM Driver
clock in
control in
Charge Current sense
System Voltage sense
Battery Voltage Sense
Battery Temperature Sense
216a
402
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Clock
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Front porch FET
Input Current sense
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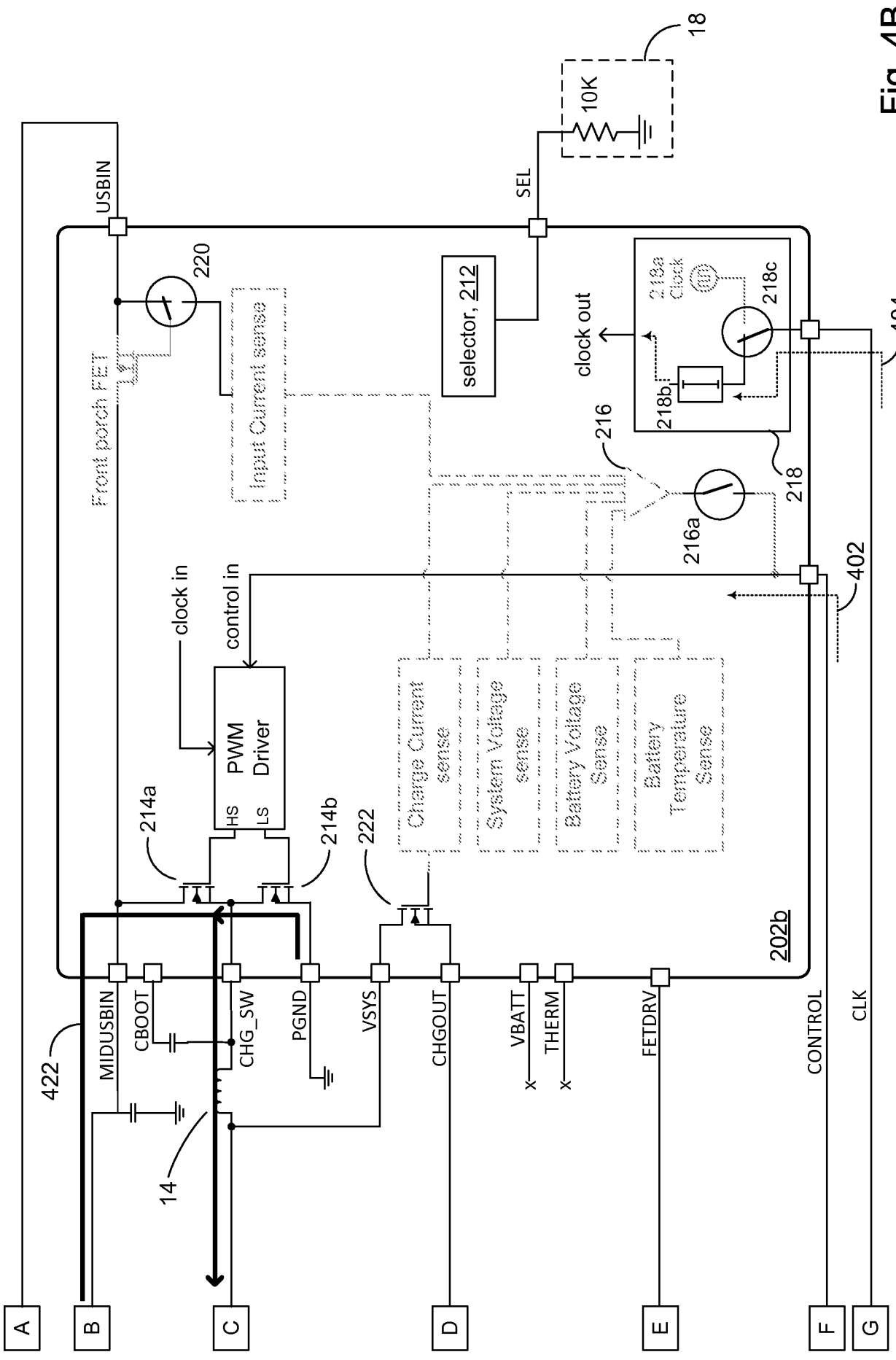
selector, 212
clock out
USBIN
SEL
18

Fig. 4A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Front porch FET
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clock in
control in
402
PWM Driver
HS
LS
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214b
222
Charge Current sense
System Voltage sense
Battery Voltage Sense
Battery Temperature Sense
202b
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CBOOT
CHG_SW
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THERM
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CONTROL
CLK
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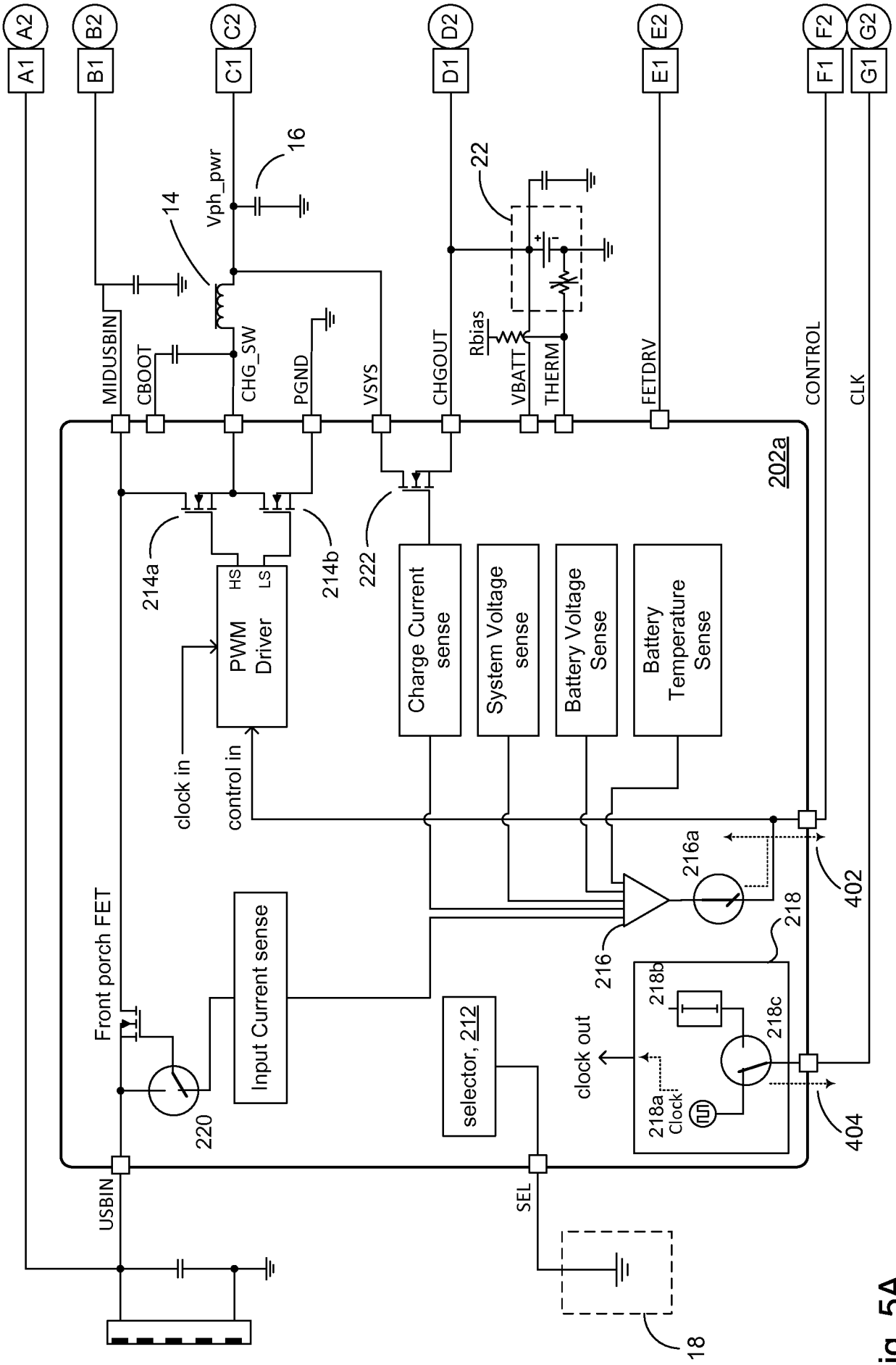
D
E
F
G

Fig. 4B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THERM
FETDRV
CONTROL
CLK
Vph_pwr
16
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202a
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214b
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HS
LS
PWM Driver
clock in
control in
Charge Current sense
System Voltage sense
Battery Voltage Sense
Battery Temperature Sense
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Front porch FET
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SEL
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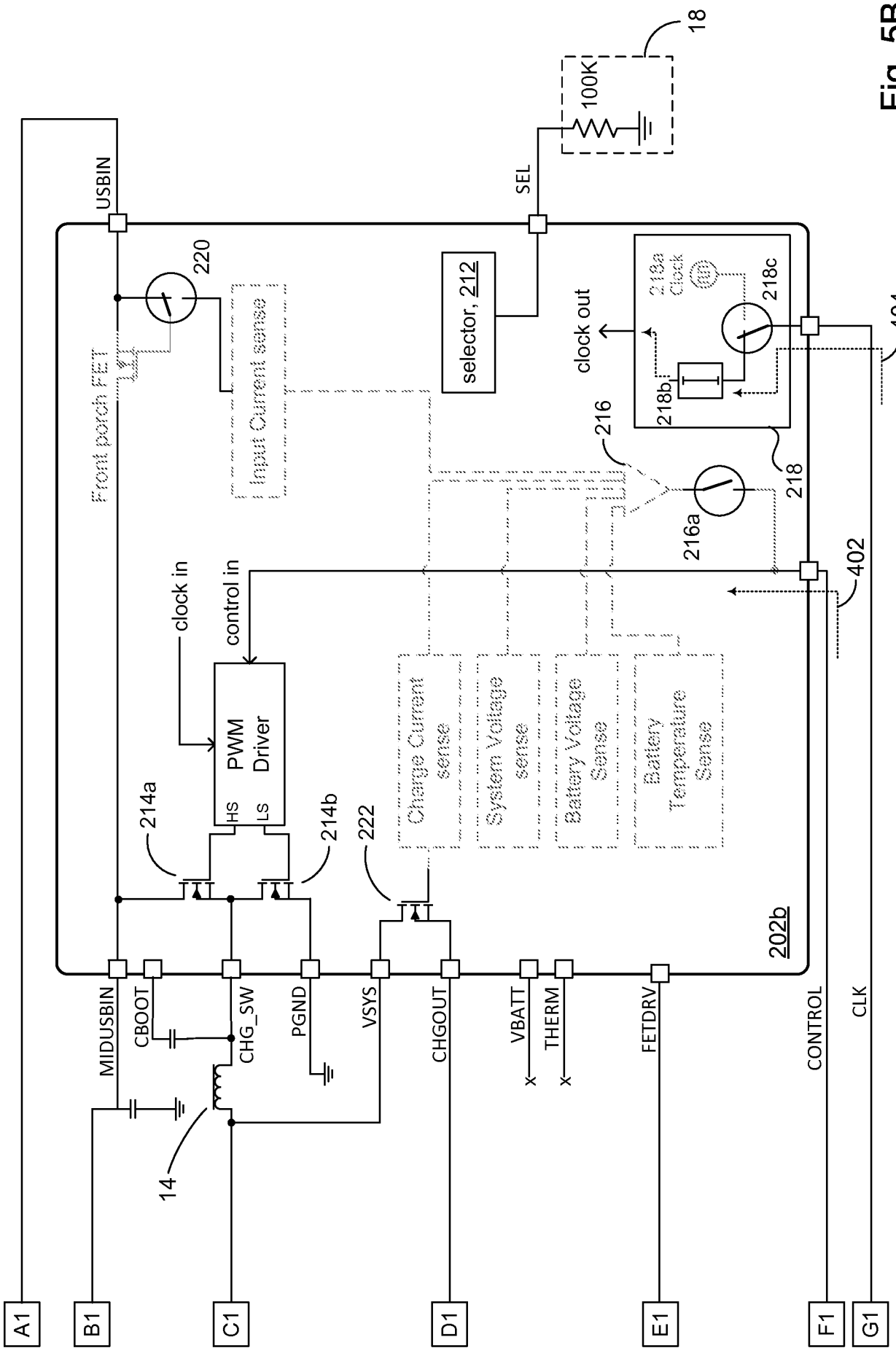
Fig. 5A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THERM
FETDRV
CONTROL
CLK
14
220
Front porch FET
Input Current sense
selector, 212
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100K
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clock out
218a Clock
218b
218c
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216a
218
404
402
clock in
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System Voltage sense
Battery Voltage Sense
Battery Temperature Sense
202b

Fig. 5B

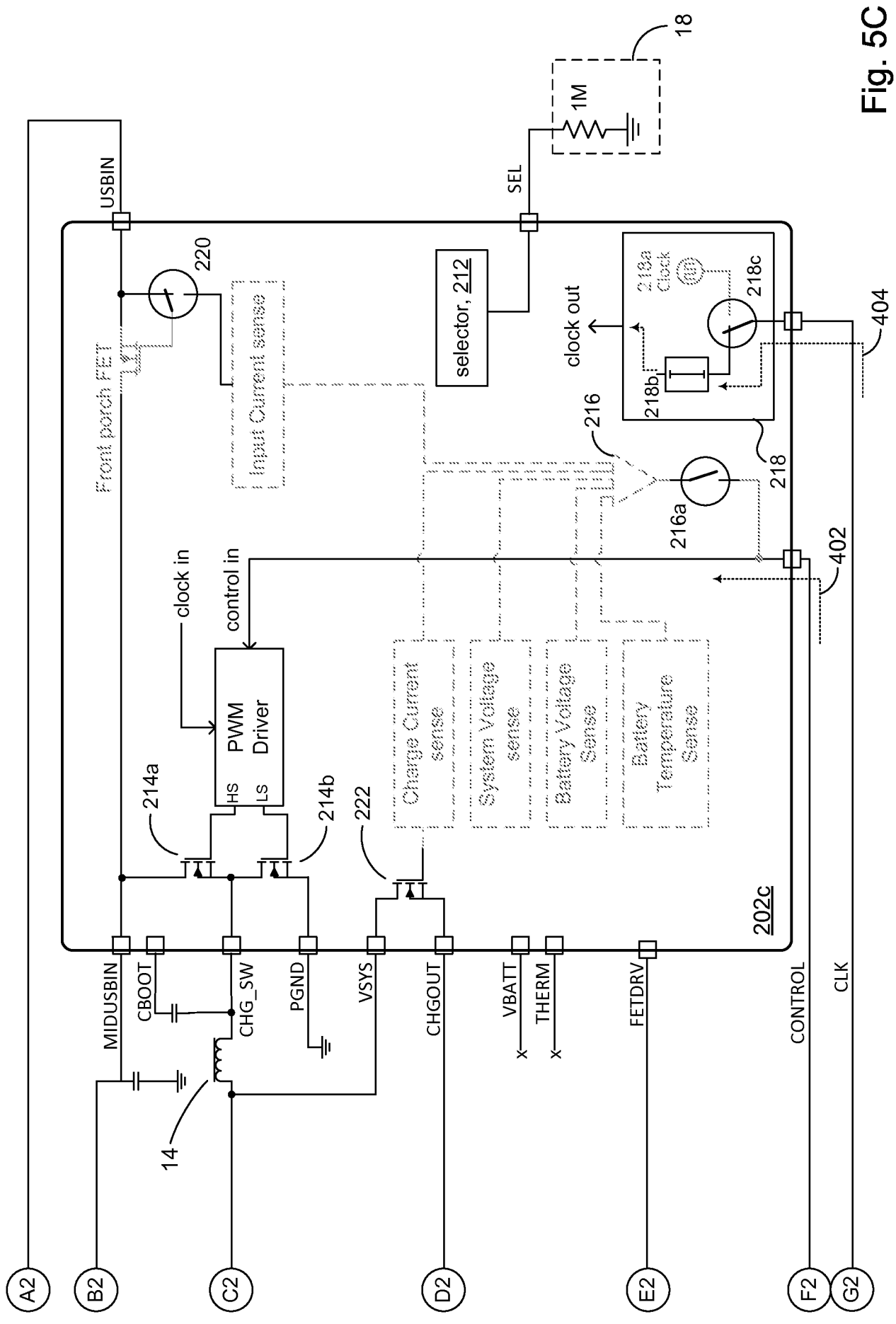
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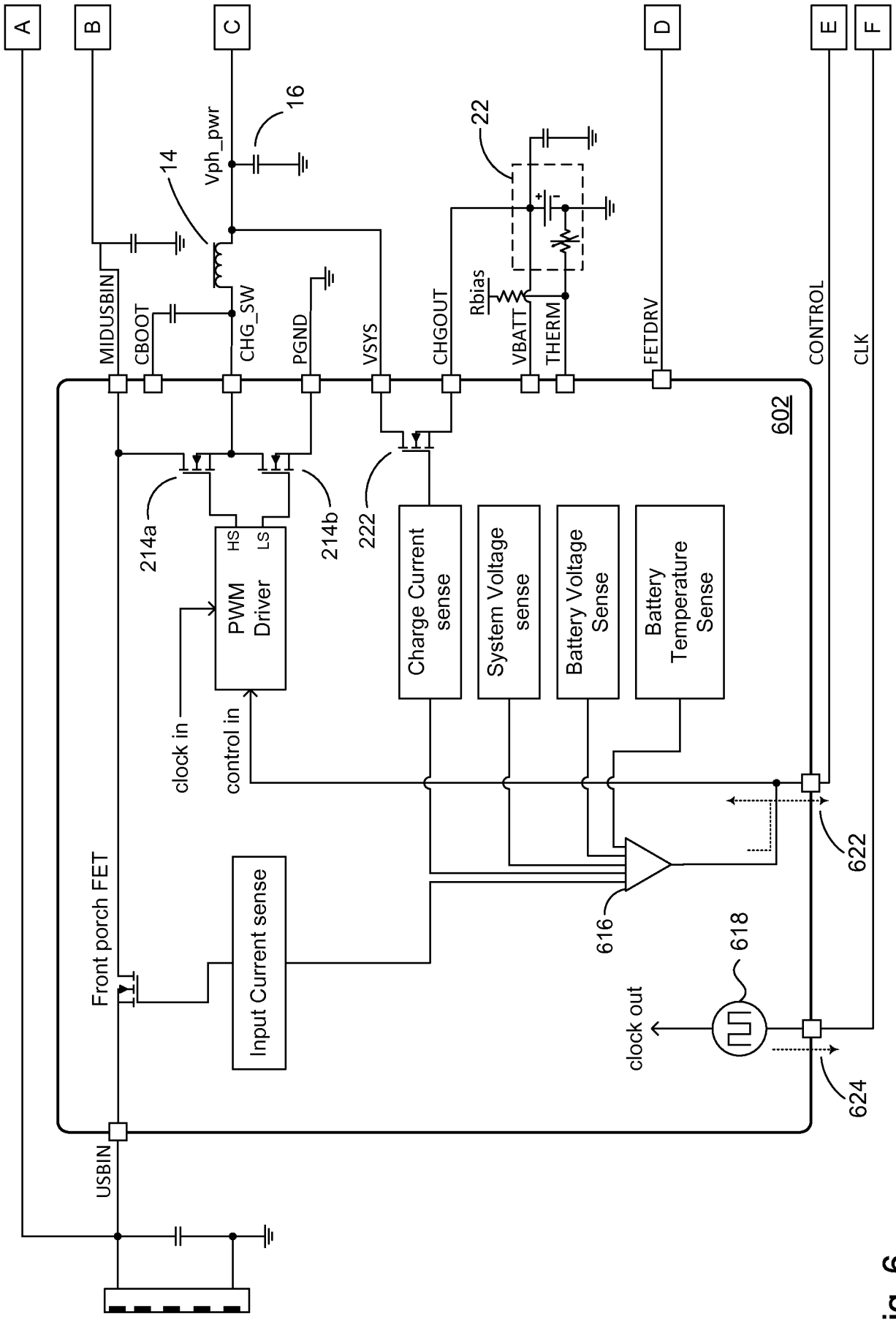
Fig. 5C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LS
PWM Driver
clock in
control in
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Battery Temperature Sense
Front porch FET
Input Current sense
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618
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624
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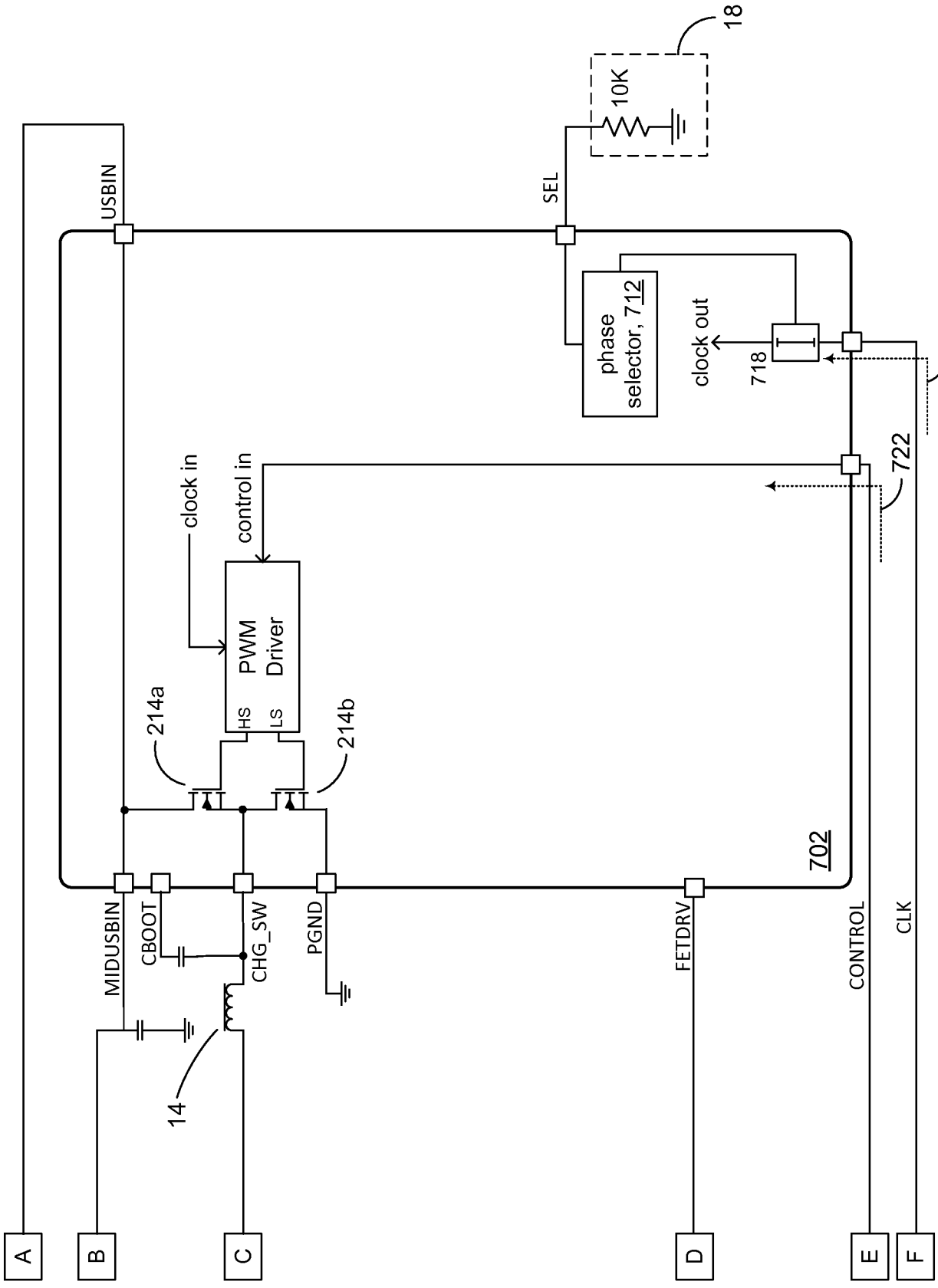
USBIN

Fig. 6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phase selector, 712
clock out
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724
722
702

Fig. 7

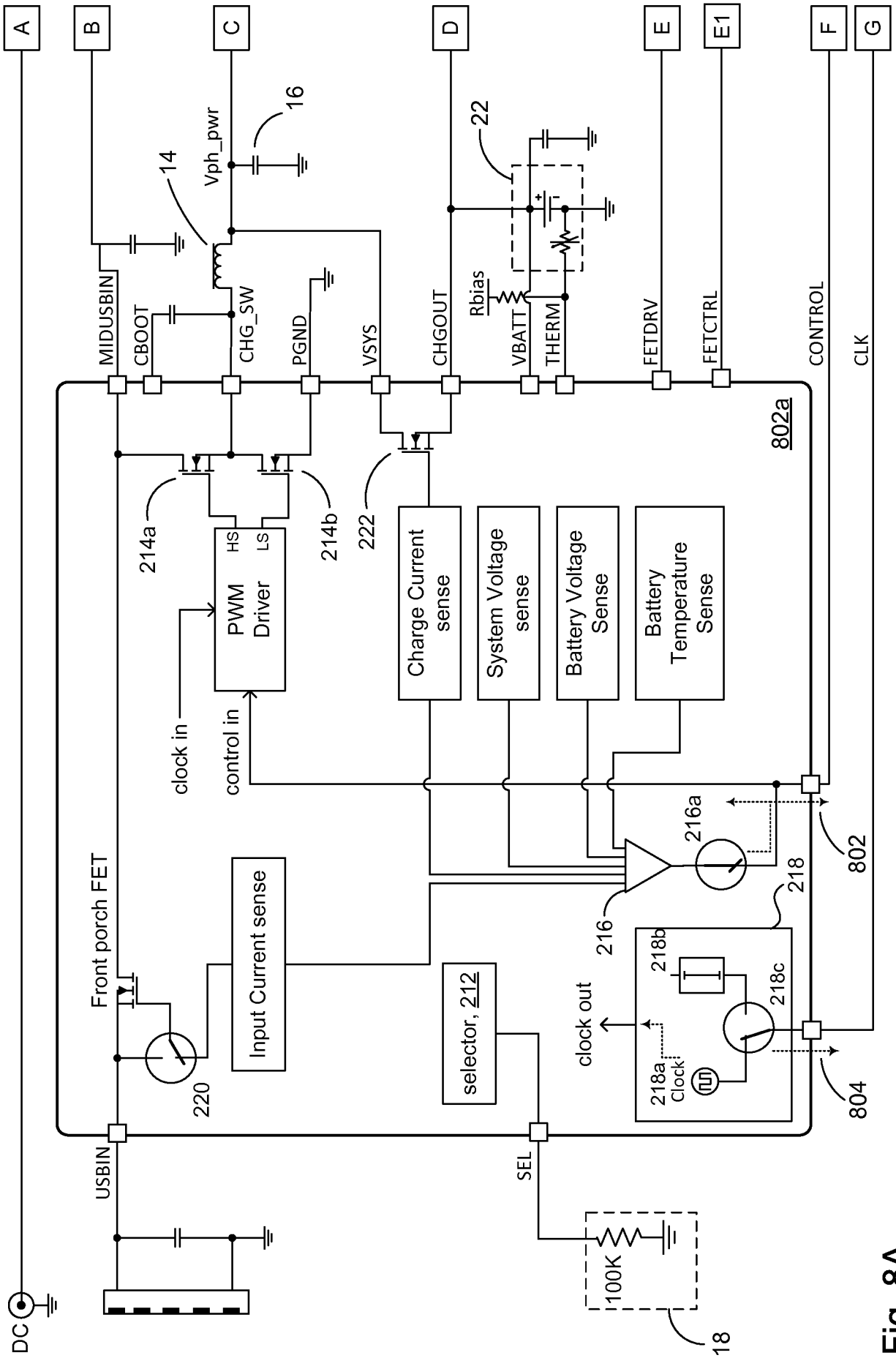
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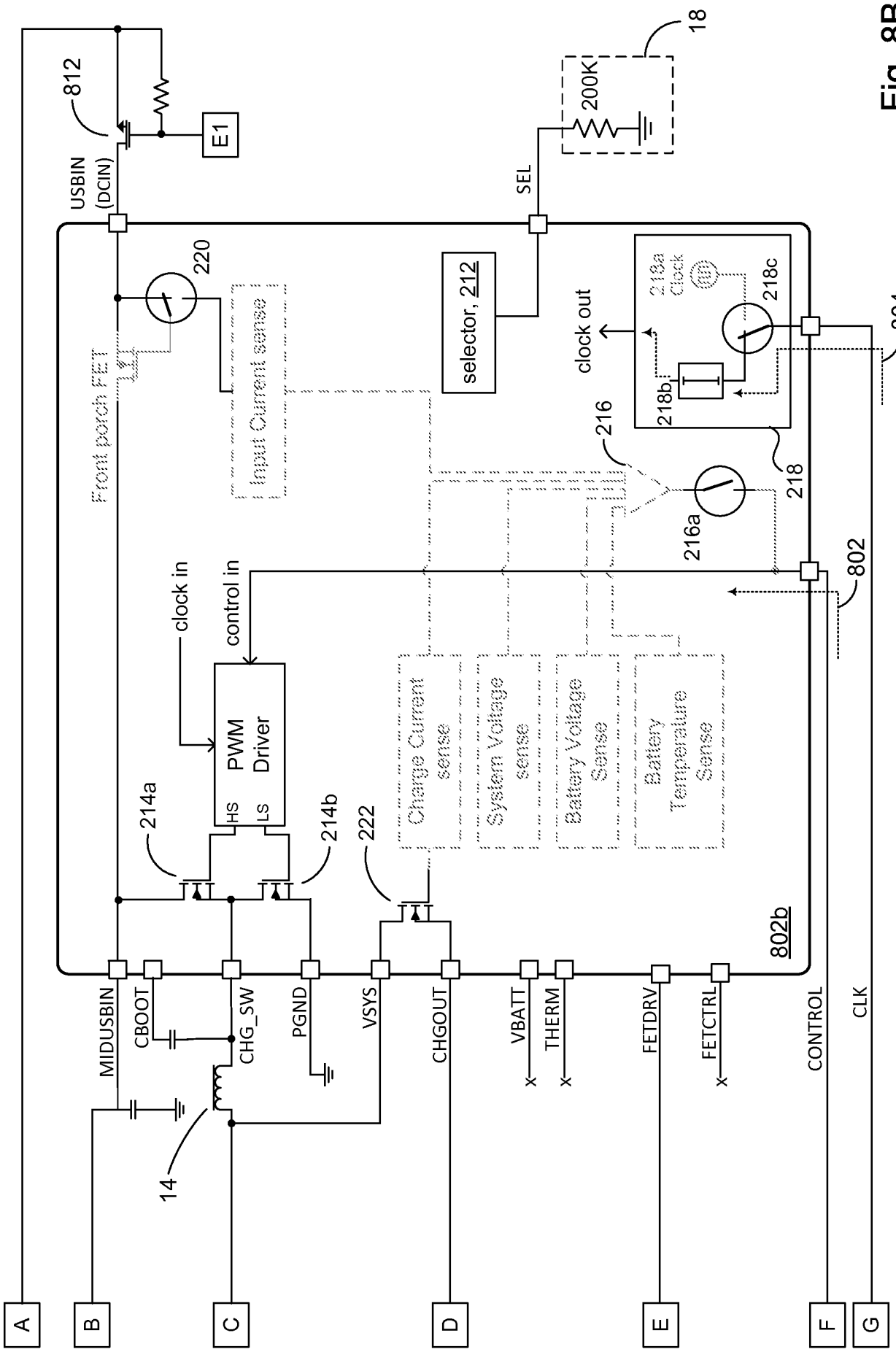
Fig. 8A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216
218
216a
802
clock in
control in
PWM Driver
HS
LS
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214b
222
Charge Current sense
System Voltage sense
Battery Voltage Sense
Battery Temperature Sense
802b
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CHG_SW
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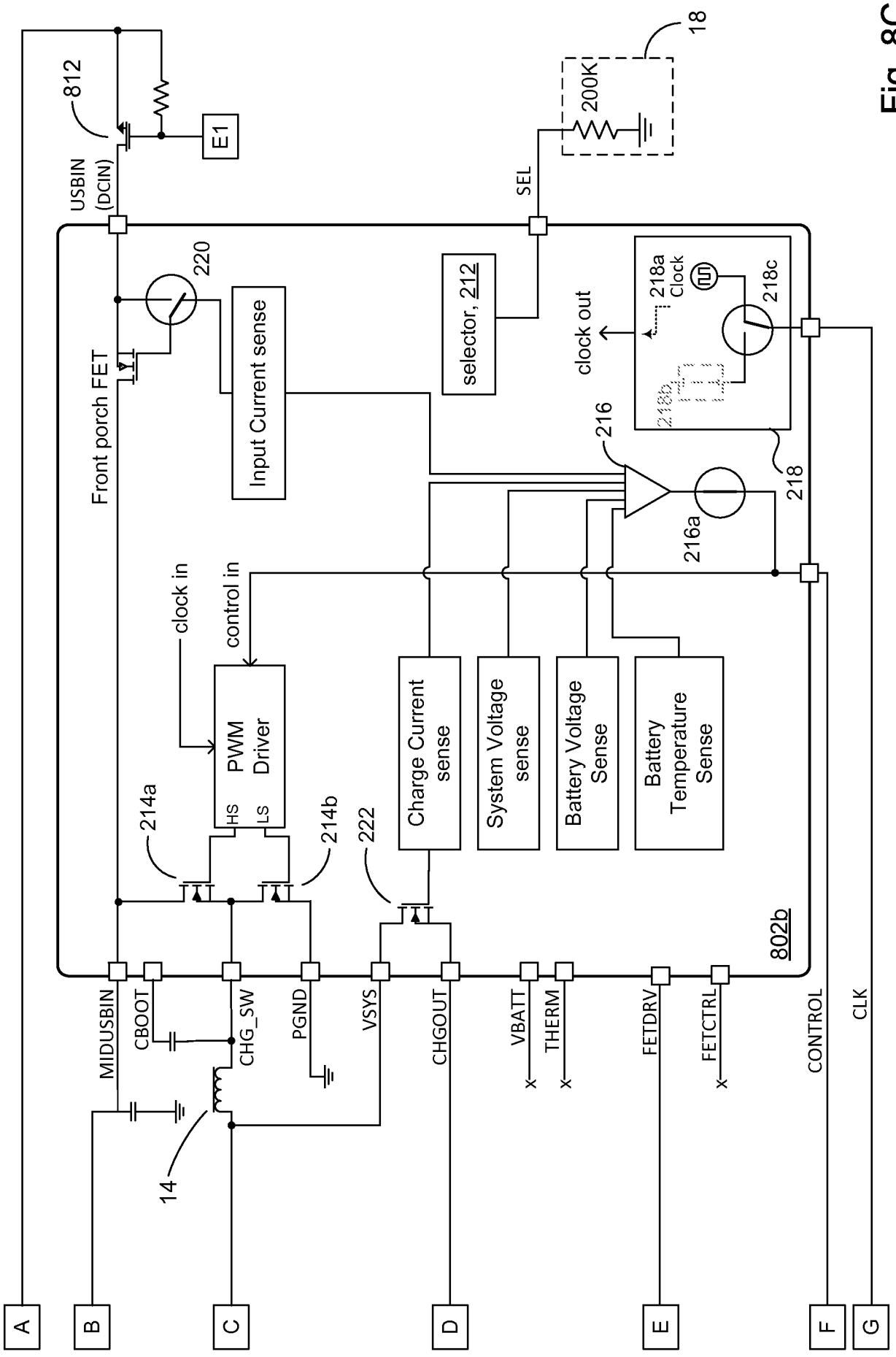
Fig. 8B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clock in
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System Voltage sense
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Battery Temperature Sense
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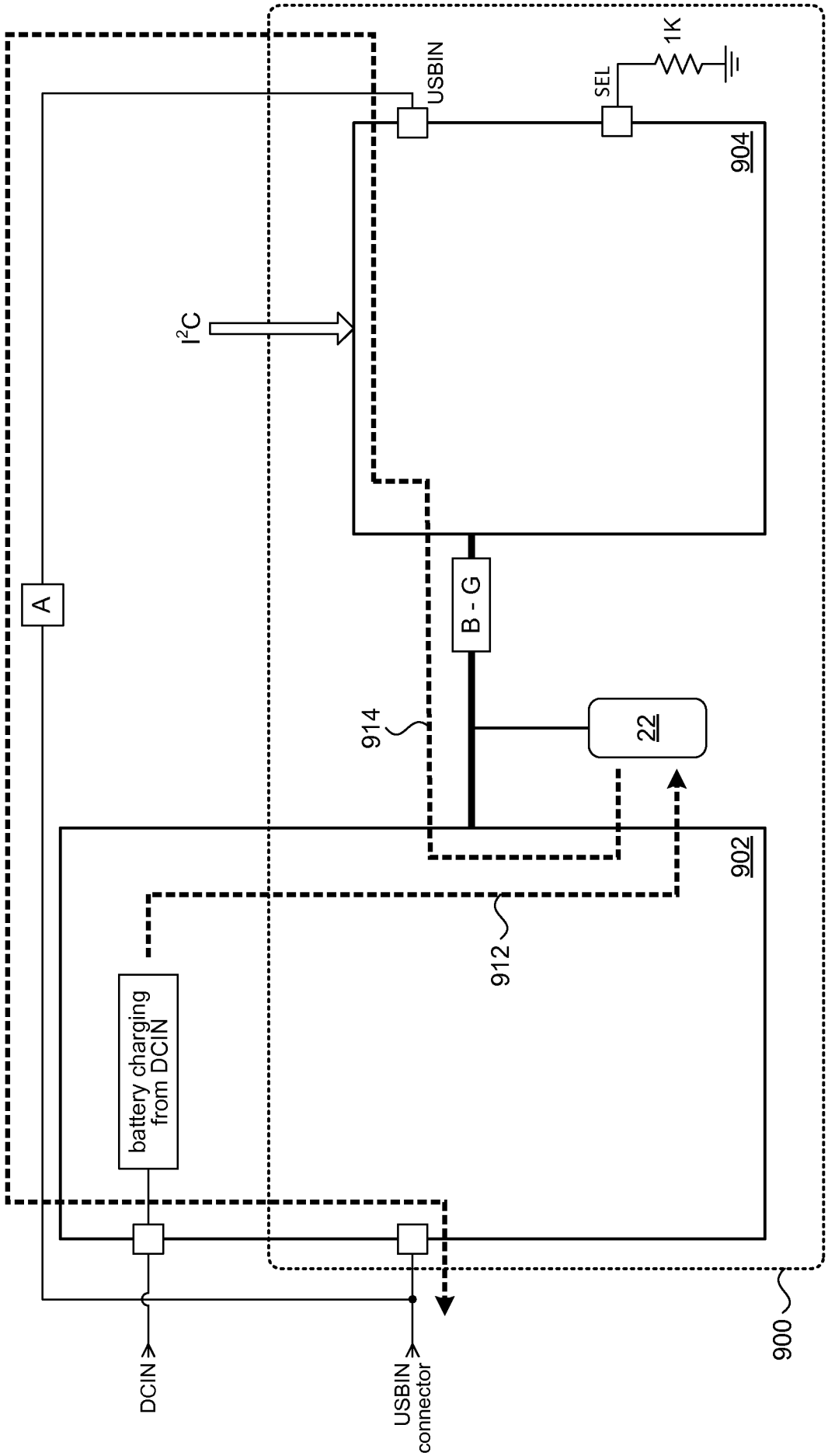
Fig. 8C


USBIN
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912
battery charging from DCIN
DCIN
USBIN connector
900

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/039380

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02J1/10 H02M3/158 H02J7/00 H02J7/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02J H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/169471 A1 (NAGASAWA TOSHIO [JP]) 14 July 2011 (2011-07-14) paragraph [0051] - paragraph [0089]; figure 2	1-20
X	US 2007/076453 A1 (SCHULTZ AARON M [US] ET AL) 5 April 2007 (2007-04-05) paragraphs [0007], [0023] - [0046], [0053] - [0058], [0065] - [0067]	1,13,18
X	US 2011/110130 A1 (WANG HSUEH-CHENG [TW] ET AL) 12 May 2011 (2011-05-12) paragraphs [0009] - [0011], [0022] - [0033]; claims 6-8	1,13,18
A	US 2012/181983 A1 (KHAN AFTAB ALI [US] ET AL) 19 July 2012 (2012-07-19) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 September 2014	23/09/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Gatzert, C

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/039380

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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