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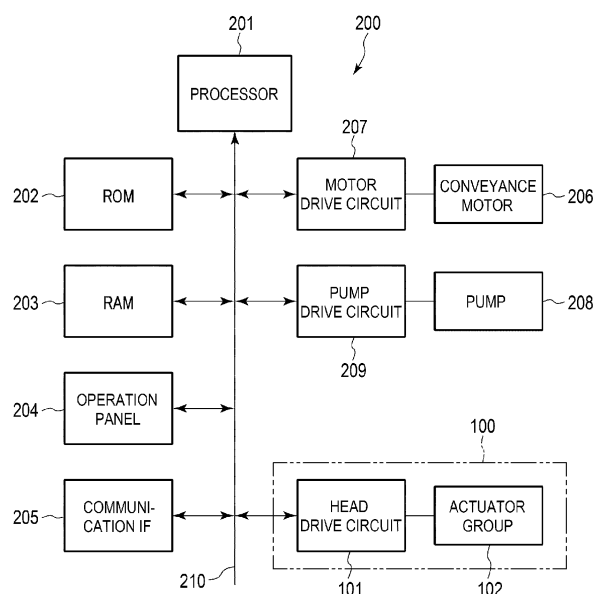
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(54) **INK JET HEAD DRIVE CIRCUIT**

(57) Provided is an ink jet head drive circuit that prevents unintentional invalidation of a protection function. The ink jet head drive circuit according to an embodiment includes a drive unit configured to drive an actuator, a protection circuit configured to execute a protection function of the inkjet head drive circuit, and a setting data register configured to store setting data including multi-bit designation data designating validation or invalidation of the protection function and to output the multi-

bit designation data to the protection circuit. The protection circuit invalidates the protection function only when bit values of the multi-bit designation data match bit values of multi-bit invalidation designation data designating the invalidation of the protection function. The protection circuit validates the protection function when the bit values of the multi-bit designation data do not match the bit values of the multi-bit invalidation designation data.

FIG. 1



Description

FIELD

[0001] Embodiments described herein relate generally to an ink jet head drive circuit.

BACKGROUND

[0002] Generally, an inkjet head includes a pressure chamber that accommodates ink, an actuator that expands and contracts the pressure chamber, and an ink jet head drive circuit that drives the actuator. The ink jet head drive circuit ejects ink from a nozzle communicating with the pressure chamber by expanding and contracting the pressure chamber by the actuator.

[0003] Generally, an ink jet head drive circuit has protection functions such as a thermal shutdown function for preventing abnormal heat generation and a short-circuit prevention function for preventing a short-circuit due to switch elements having different power supply levels being simultaneously turned on.

[0004] However, it may be desired to invalidate the protection function. For example, there are cases where it is desired to perform an operation test in a high temperature environment or at a high temperature at the time of overload, and where it is desired to drive the switch elements by simultaneously turning on the switch elements with different power supply levels set to the same potential.

[0005] The protection function is invalidated by setting data. However, the protection function may be unintentionally invalidated due to erroneous setting or a bit error. It is desirable to prevent unintentional invalidation of the protection function as much as possible.

DISCLOSURE OF INVENTION

[0006] To this end, there is provided an inkjet head drive circuit according to claim 1. Preferred embodiments are set out in the dependent claims. There is also provided an ink jet head according to claim 15.

DESCRIPTION OF THE DRAWINGS

[0007]

FIG. 1 is a block diagram showing a configuration example of an inkjet printer including an inkjet head drive circuit according to an embodiment;

FIG. 2 is a block diagram showing a configuration example of an ink jet head drive circuit according to a related-art example;

FIG. 3 is a diagram showing an example of a register map of setting data related to validation and invalidation of a protection function;

FIG. 4 is a diagram showing specific register values indicating the validation and invalidation;

FIG. 5 is a block diagram showing a configuration example of the inkjet head drive circuit according to the embodiment;

FIG. 6 is a diagram showing an example of a register map of setting data related to validation and invalidation of a protection function;

FIG. 7 is a diagram showing specific register values indicating the validation and invalidation;

FIG. 8 is a diagram showing a truth table of a logic circuit based on combinations of multiple bits;

FIG. 9 is a block diagram showing a configuration example of a gate driver;

FIG. 10 is a block diagram showing a configuration example of a waveform pattern generation unit; and FIG. 11 is a diagram showing an example of an ON switch that is enabled by invalidating a short-circuit prevention function.

DETAILED DESCRIPTION

[0008] In general, according to one embodiment, an ink jet head drive circuit that prevents unintentional invalidation of a protection function is provided.

[0009] According to one embodiment, an ink jet head drive circuit includes a drive unit configured to drive an actuator that expands and contracts a pressure chamber accommodating ink to eject the ink from a nozzle, a protection circuit configured to execute a protection function of the inkjet head drive circuit, and a setting data register configured to store setting data including multi-bit designation data designating validation or invalidation of the protection function and to output the multi-bit designation data to the protection circuit. The protection circuit invalidates the protection function only when bit values of the multi-bit designation data match bit values of multi-bit invalidation designation data designating the invalidation of the protection function. The protection circuit validates the protection function when the bit values of the multi-bit designation data do not match the bit values of the multi-bit invalidation designation data.

Ink Jet Printer

[0010] First, an inkjet printer 200 having an inkjet head 100 including an inkjet head drive circuit 101 according to an embodiment will be described with reference to FIG. 1. FIG. 1 is a block diagram showing a configuration example of the ink jet printer 200. In the following description, the inkjet printer 200 is abbreviated as a printer 200, the ink jet head 100 is abbreviated as a head 100, and the ink jet head drive circuit 101 is abbreviated as a head drive circuit 101.

[0011] The printer 200 includes the head 100. The head 100 includes the head drive circuit 101 and an actuator group 102. The actuator group 102 includes a plurality of actuators. Each actuator is a drive element for expanding and contracting a pressure chamber that accommodates ink and ejecting ink droplets from a nozzle

communicating with the pressure chamber. For example, the actuator is a piezoelectric drive element made of lead zirconate titanate (PZT). The head drive circuit 101 generates a drive signal for the actuator group 102. The actuator in the actuator group 102 operates according to the drive signal supplied from the head drive circuit 101, expands and contracts the pressure chamber, and ejects the ink droplets from the nozzle.

[0012] The printer 200 includes, in addition to the head 100, a processor 201, a read only memory (ROM) 202, a random access memory (RAM) 203, an operation panel 204, a communication interface 205, a conveyance motor 206, a motor drive circuit 207, a pump 208, and a pump drive circuit 209. In the drawings, the interface is abbreviated as "IF".

[0013] The printer 200 also includes a bus line 210 such as an address bus or a data bus. The processor 201, the ROM 202, the RAM 203, the operation panel 204, the communication interface 205, the motor drive circuit 207, the pump drive circuit 209, and the head drive circuit 101 are connected to the bus line 210 directly or via an input and output circuit, and can transmit data to and receive data from each other.

[0014] The processor 201 corresponds to a central part of a computer. The processor 201 controls the units to implement various functions of the printer 200 according to an operating system and application programs. The processor 201 is, for example, a central processing unit (CPU).

[0015] The ROM 202 corresponds to a read-only main storage portion of the computer. The ROM 202 stores the operating system and the application programs. The ROM 202 may store data necessary for the processor 201 to execute processing for controlling the units.

[0016] The RAM 203 corresponds to a rewritable main storage portion of the computer. The RAM 203 stores data necessary for the processor 201 to execute processing. The RAM 203 is also used as a work area where information is appropriately rewritten by the processor 201. The work area includes an image memory in which print data is loaded.

[0017] The operation panel 204 includes an operation unit and a display unit. The operation unit includes function keys such as a power key, a paper feed key, and an error release key arranged thereon. The display unit can display various states of the printer 200.

[0018] The communication interface 205 receives print data from a client terminal connected via a network such as a local area network (LAN). For example, when an error occurs in the printer 200, the communication interface 205 transmits a signal notifying the client terminal of the error.

[0019] The motor drive circuit 207 controls driving of the conveyance motor 206. The conveyance motor 206 functions as a drive source of a conveyance mechanism that conveys a recording medium such as printing paper. When the conveyance motor 206 is started, the conveyance mechanism starts conveying the recording med-

ium. The conveyance mechanism conveys the recording medium to a printing position of the head 100. The conveyance mechanism discharges the printed recording medium from a discharge port (not shown) to the outside of the printer 200.

[0020] The pump drive circuit 209 controls driving of the pump 208. When the pump 208 is driven, ink in an ink tank (not shown) is supplied to the head 100.

[0021] The head drive circuit 101 drives the actuator group 102 of the head 100 based on the print data. The actuator group 102 expands and contracts the pressure chamber that accommodates the ink, and ejects the ink droplets from the nozzle communicating with the pressure chamber. Accordingly, the head 100 ejects the ink onto the recording medium conveyed by the conveyance mechanism, and prints an image or the like on the recording medium.

Head Drive Circuit according to Related-art Example

[0022] Next, the head drive circuit 101 according to a related-art example will be described with reference to FIG. 2. FIG. 2 is a block diagram showing a configuration example of the head drive circuit 101 according to the related-art example.

[0023] The head drive circuit 101 includes an I/O unit 110, a logic unit 120, and an analog unit 130. The I/O unit 110, the logic unit 120, and the analog unit 130 are drive units that drive the actuator group 102.

[0024] The I/O unit 110 includes a comparator 111 and a serial-parallel conversion unit 112. In the drawings, the "serial-parallel conversion unit" is abbreviated as a "conversion unit".

[0025] The comparator 111 receives a clock signal CLK of low voltage differential signaling (LVDS) and a data signal DI. The data signal DI includes print data, setting data, and the like. The comparator 111 outputs data of the clock signal CLK and data of the data signal DI to the serial-parallel conversion unit 112.

[0026] The serial-parallel conversion unit 112 converts serial format data received from the comparator 111 into parallel format data. The data of the data signal DI is acquired at a timing when the clock signal CLK rises. Specifically, at a timing when the clock signal CLK changes from 0 to 1, values (0 or 1) of setting data and the print data included in the data signal DI are acquired. The serial-parallel conversion unit 112 outputs the data of the parallel format data signal DI to the logic unit 120. The serial-parallel conversion unit 112 outputs the data of the clock signal CLK to the logic unit 120 and the analog unit.

[0027] The logic unit 120 includes a start byte recognition unit 121, a setting data register 122, a print data register 123, and a waveform pattern generation unit 124.

[0028] The start byte recognition unit 121 recognizes a start byte for the data of the parallel format data signal DI received from the serial-parallel conversion unit 112, and separates the data into setting data and print data. The start byte recognition unit 121 outputs the setting data to

the setting data register 122 and outputs the print data to the print data register 123.

[0029] The setting data register 122 stores the setting data received from the start byte recognition unit 121.

[0030] The print data register 123 stores the print data received from the start byte recognition unit 121.

[0031] The waveform pattern generation unit 124 acquires setting data from the setting data register 122, acquires print data from the print data register 123, and generates a waveform pattern based on the setting data and the print data. The waveform pattern generation unit 124 outputs the generated waveform pattern to the analog unit 130.

[0032] The analog unit 130 includes a level shifter 131, a pre-buffer 132, and a gate driver 133.

[0033] The level shifter 131 converts the waveform pattern received from the waveform pattern generation unit 124 into a high voltage. The level shifter 131 outputs the waveform pattern converted into the high voltage to the pre-buffer 132.

[0034] The pre-buffer 132 appropriately amplifies and shapes the waveform pattern received from the level shifter 131. The pre-buffer 132 outputs the appropriately amplified and shaped waveform pattern to the gate driver 133.

[0035] The gate driver 133 outputs a drive waveform for driving the actuator group 102 of the head 100 to an output electrode OUT connected to the actuator group 102 by controlling on and off of a plurality of switch elements of the gate driver 133 based on the waveform pattern received from the pre-buffer 132. That is, the gate driver 133 is a drive waveform output unit that outputs the drive waveform based on the waveform pattern. For example, the switch element is a MOSFET, and the gate driver 133 controls on and off of the MOSFET by applying a control signal (gate voltage) to a gate of the MOSFET.

PROTECTION FUNCTION

[0036] The head drive circuit 101 also has a thermal shutdown function and a short-circuit prevention function as protection functions. The thermal shutdown function is a function for preventing abnormal heat generation of the head drive circuit 101. The short-circuit prevention function is a function for preventing occurrence of a short-circuit in the gate driver 133 due to a plurality of switch elements having different power supply levels being simultaneously turned on.

[0037] It may be desired to invalidate the thermal shutdown function and the short-circuit prevention function. For example, there are cases where it is desired to perform an operation test in a high temperature environment or at a high temperature at the time of overload, and where it is desired to drive the switch elements by simultaneously turning on the switch elements with different power supply levels set to the same potential.

[0038] Validation and invalidation of the thermal shutdown function and the short-circuit prevention function

can be switched by the setting data stored in the setting data register 122. In other words, the setting data stored in the setting data register 122 includes designation data designating the validation and invalidation of the thermal shutdown function and the short-circuit prevention function.

Thermal Shutdown Function

[0039] The head drive circuit 101 includes a temperature sensor unit 140 as a protection circuit for executing the thermal shutdown function. The temperature sensor unit 140 includes a temperature sensor 141, a reference power supply 142, and a comparator 143. The temperature sensor 141 detects a temperature of the head drive circuit 101 and outputs a voltage signal indicating the temperature. The reference power supply 142 provides a reference voltage as a threshold for determining abnormal heat generation. The comparator 143 compares the voltage signal output from the temperature sensor 141 with the reference voltage.

[0040] The comparator 143 outputs binary data TS indicating whether the head drive circuit 101 is in an abnormal heat generation state depending on a comparison result. For example, when the temperature is equal to or higher than the threshold, the comparator 143 outputs the binary data TS "1" indicating that the head drive circuit 101 is in the abnormal heat generation state. The binary data TS "1" is control data instructing execution of the thermal shutdown function. On the other hand, when the temperature is lower than the threshold, the binary data TS "0" indicating that the head drive circuit 101 is not in the abnormal heat generation state is output. The binary data TS "0" is control data not instructing execution of the thermal shutdown function.

[0041] Validation and invalidation of the thermal shutdown function can be set by the designation data in the setting data stored in the setting data register 122. The setting data register 122 outputs designation data DTS designating the validation or invalidation of the thermal shutdown function.

[0042] FIG. 3 shows an example of a register map of the designation data designating the validation and invalidation of the thermal shutdown function and the short-circuit prevention function. In FIG. 3, thermal shutdown is abbreviated as shutdown. The same applies to FIGS. 4, 7, and 8. The setting data register 122 stores, at a predetermined address, name information indicating the thermal shutdown function and the designation data DTS associated with the name information and designating the validation or invalidation of the thermal shutdown function. The setting data register 122 stores the setting data as 8-bit (D0 to D7) data. The setting data register 122 stores the designation data DTS designating the validation or invalidation of the thermal shutdown function as lowest 1-bit (D0) data.

[0043] FIG. 4 is a diagram showing specific register values indicating the validation and invalidation of the

thermal shutdown function and the short-circuit prevention function in the register map of the designation data shown in FIG. 3. The register value indicating the validation of the thermal shutdown function is "00000001". The register value indicating the invalidation of the thermal shutdown function is "00000000".

[0044] In the setting for validating the thermal shutdown function, the setting data register 122 outputs lowest 1-bit (D0) binary data, that is, "1". On the other hand, in the setting for invalidating the thermal shutdown function, the setting data register 122 outputs lowest 1-bit (D0) binary data, that is, "0".

[0045] Referring again to FIG. 2, the head drive circuit 101 will be described. The head drive circuit 101 also includes an AND circuit 145 that receives output of the temperature sensor unit 140 and output of the setting data register 122. The AND circuit 145 receives, from the setting data register 122, binary data "1" or "0" indicating that the thermal shutdown function is to be validated or invalidated.

[0046] The AND circuit 145 outputs "0" when both the received data from the temperature sensor unit 140 and the received data from the setting data register 122 are not "1". That is, the AND circuit 145 outputs "0" when the head drive circuit 101 is not in the abnormal heat generation state or the thermal shutdown function is set to be invalidated even though the head drive circuit 101 is in an abnormal heat generation state. The output data "0" from the AND circuit 145 is data instructing continuation of driving of the logic unit 120 and the analog unit 130 of the head drive circuit 101.

[0047] On the other hand, the AND circuit 145 outputs "1" when both the received data from the temperature sensor unit 140 and the received data from the setting data register 122 are "1". That is, the AND circuit 145 outputs "1" only when the head drive circuit 101 is in the abnormal heat generation state and the thermal shutdown function is set to be validated. The output data "1" from the AND circuit 145 is data instructing stop of driving of the logic unit 120 and the analog unit 130 of the head drive circuit 101.

[0048] The head drive circuit 101 can receive a reset signal for forcibly stopping the logic unit 120 and the analog unit 130. The reset signal is input to the logic unit 120 and the analog unit 130. The logic unit 120 and the analog unit 130 stop when receiving the reset signal. For example, the reset signal is binary data "1". The driving of the logic unit 120 and the analog unit 130 may be stopped by any method such as stopping reception processing of the print data and stopping output of the gate driver.

[0049] The head drive circuit 101 also includes an OR circuit 146 that receives the reset signal and output of the AND circuit 145. The OR circuit 146 outputs "1" when one of the output of the AND circuit 145 and the reset signal is "1". That is, the output data "1" from the OR circuit 146 is data instructing stop of driving of the logic unit 120 and the analog unit 130 of the head drive circuit 101.

Short-circuit Prevention Function

[0050] The head drive circuit 101 includes a short-circuit prevention circuit 125 in the waveform pattern generation unit 124 as a protection circuit for executing the short-circuit prevention function. The short-circuit prevention circuit 125 is a circuit that prevents the waveform pattern generation unit 124 from generating a waveform pattern in which switch elements of different power supply levels of the gate driver 133 are simultaneously turned on.

[0051] Validation and invalidation of the short-circuit prevention function can be designated by the designation data stored in the setting data register 122. The setting data register 122 outputs designation data DSP designating the validation or invalidation of the short-circuit prevention function to the waveform pattern generation unit 124. The waveform pattern generation unit 124 validates or invalidates the short-circuit prevention circuit 125 according to the designation data DSP.

[0052] Next, the validation and invalidation of the short-circuit prevention function will be described with reference to FIG. 3. As described above, FIG. 3 is a diagram showing the example of the register map of the data designating the validation and invalidation of the thermal shutdown function and the short-circuit prevention function.

[0053] Similarly to the thermal shutdown function, the setting data register 122 stores, at a predetermined address, name information indicating the short-circuit prevention function and the data DSP associated with the name information and indicating the validation or invalidation of the short-circuit prevention function. The setting data register 122 stores the setting data as 8-bit (D0 to D7) data. The setting data register 122 stores the designation data DSP designating the validation or invalidation of the short-circuit prevention function as lowest 1-bit (D0) data.

[0054] As shown in FIG. 4, similarly to the thermal shutdown function, the register value indicating the validation of the short-circuit prevention function is "00000001". The register value indicating the invalidation of the short-circuit prevention function is "00000000".

[0055] In the setting for validating the short-circuit prevention function, the setting data register 122 outputs, to the waveform pattern generation unit 124, lowest 1-bit (D0) binary data, that is, "1". The output data "1" from the setting data register 122 is data validating the short-circuit prevention circuit 125. In this case, the waveform pattern generation unit 124 generates a waveform pattern to be output to the analog unit 130 using the short-circuit prevention circuit 125.

[0056] On the other hand, in the setting for invalidating the short-circuit prevention function, the setting data register 122 outputs, to the waveform pattern generation unit 124, lowest 1-bit (D0) binary data, that is, "0". The output data "0" from the setting data register 122 is data invalidating the short-circuit prevention circuit 125. In this

case, the waveform pattern generation unit 124 generates a waveform pattern to be output to the analog unit 130 without using the short-circuit prevention circuit 125.

Head Drive Circuit according to Embodiment

[0057] In the head drive circuit 101 according to the related-art example described above, designation data designating validation and invalidation of protection functions (that is, the thermal shutdown function and the short-circuit prevention function) is 1-bit data stored in the setting data register 122. When the designation data is 1-bit data, the protection function may be unintentionally invalidated due to an erroneous operation at the time of inputting setting data, a bit error during data processing, or the like. Since unintentional invalidation of the protection function causes a malfunction, it is desirable to avoid this as much as possible.

[0058] The head drive circuit 101 according to the embodiment prevents occurrence of unintentional invalidation of the protection functions related to the designation data designating the validation and invalidation of the protection functions (that is, the thermal shutdown function and the short-circuit prevention function).

[0059] Hereinafter, the head drive circuit 101 according to the embodiment will be described with reference to FIG. 5. FIG. 5 is a block diagram showing a configuration example of the head drive circuit 101 according to the embodiment. In FIG. 5, members denoted by the same reference numerals as those shown in FIG. 2 are the same members, and detailed description thereof will be omitted. Hereinafter, differences will be mainly described.

[0060] In the head drive circuit 101 according to the embodiment, the setting data register 122 stores designation data designating validation and invalidation of protection functions (that is, a thermal shutdown function and a short-circuit prevention function) as multi-bit data. That is, the setting data register 122 outputs multi-bit designation data as the designation data designating the validation and invalidation of the protection functions (that is, the thermal shutdown function and the short-circuit prevention function).

[0061] For example, the setting data register 122 outputs 8-bit designation data DTS [7, 0] as designation data designating validation or invalidation of the thermal shutdown function. The setting data register 122 outputs 8-bit designation data DSP [7, 0] as designation data designating validation or invalidation of the short-circuit prevention function.

[0062] The head drive circuit 101 according to the embodiment includes a logic circuit 148 based on a combination of multiple bits and a logic circuit 126 based on a combination of multiple bits in order to generate 1-bit designation data from multi-bit designation data. Hereinafter, the logic circuit based on the combination of multiple bits is abbreviated as a combinational circuit.

[0063] The combinational circuit 148 generates 1-bit

designation data to be input to the AND circuit 145 from the 8-bit designation data DTS [7, 0] designating the validation or invalidation of the thermal shutdown function output from the setting data register 122. The combinational circuit 148 constitutes a part of a protection circuit for executing the thermal shutdown function. In other words, the head drive circuit 101 according to the embodiment includes the temperature sensor unit 140 and the combinational circuit 148 as the protection circuit for executing the thermal shutdown function. The combinational circuit 148 prevents occurrence of unintentional invalidation of the thermal shutdown function.

[0064] The combinational circuit 126 generates 1-bit designation data to be input to the waveform pattern generation unit 124 from the 8-bit designation data DSP [7, 0] designating the validation or invalidation of the short-circuit prevention function output from the setting data register 122. The combinational circuit 126 constitutes a part of a protection circuit for executing the short-circuit prevention function. The head drive circuit 101 according to the embodiment includes the short-circuit prevention circuit 125 and the combinational circuit 126 as the protection circuit for executing the short-circuit prevention function. The combinational circuit 126 prevents occurrence of unintentional invalidation of the short-circuit prevention function.

[0065] FIG. 6 shows an example of a register map of data designating the validation and invalidation of the thermal shutdown function and the short-circuit prevention function stored in the setting data register 122, in the head drive circuit 101 according to the embodiment.

[0066] The setting data register 122 stores, at a predetermined address, name information indicating the thermal shutdown function and the 8-bit designation data DTS [7, 0] associated with the name information and designating the validation or invalidation of the thermal shutdown function. Similarly, the setting data register 122 stores, at a predetermined address, name information indicating the short-circuit prevention function and the 8-bit designation data DSP [7, 0] associated with the name information and designating the validation or invalidation of the short-circuit prevention function. As described above, the setting data register 122 stores setting data as 8-bit (D0 to D7) data.

[0067] In the head drive circuit 101 according to the related-art example, the lowest 1 bit (D0) in the 8-bit (D0 to D7) setting data stored in the setting data register 122 is allocated to the designation data DTS designating the validation or invalidation of the thermal shutdown function. The same applies to the designation data DSP designating the validation or invalidation of the short-circuit prevention function.

[0068] In contrast, in the head drive circuit 101 according to the embodiment, all bits in the 8-bit (D0 to D7) setting data stored in the setting data register 122 are allocated to the designation data DTS [7, 0] designating the validation or invalidation of the thermal shutdown function. The same applies to the designation data

DSP [7, 0] designating the validation or invalidation of the short-circuit prevention function.

[0069] FIG. 7 is a diagram showing specific register values indicating the validation and invalidation of the thermal shutdown function and the short-circuit prevention function in the register map of the designation data shown in FIG. 6. The register value indicating the invalidation of the thermal shutdown function is "11101010". The register value "XXXXXXXX" indicating the validation of the thermal shutdown function is a value different from "11101010". The register value indicating the invalidation of the short-circuit prevention function is "11011010". The register value "XXXXXXXX" indicating the validation of the short-circuit prevention function is a value different from "11011010".

[0070] Next, a truth table of the combinational circuit 148 will be described with reference to FIG. 8. FIG. 8 is a diagram showing the truth table of the combinational circuit 148 that is a logic circuit based on a combination of multiple bits. In FIG. 8, D0 to D7 respectively represent bit values of 8-bit designation data. D0 represents the lowest bit value, and D7 represents the highest bit value. OUT represents a bit value output from the combinational circuit 148. Each bit value is represented by 0 or 1. "X" indicates that the bit value may be 0 or 1.

[0071] As shown in FIG. 7, the register value indicating the invalidation of the thermal shutdown function is "11101010". In FIG. 8, a second row indicates that the bit values of the 8-bit designation data respectively match bit values of the register value "11101010", and in this case, the combinational circuit 148 outputs 1-bit designation data "0" indicating the invalidation of the thermal shutdown function.

[0072] In FIG. 8, third and subsequent rows indicate that any of the bit values of the 8-bit designation data does not match bit values of the register value "11101010", and in this case, the combinational circuit 148 outputs 1-bit designation data "1" indicating the validation of the thermal shutdown function.

[0073] That is, the combinational circuit 148 outputs the 1-bit designation data "0" indicating the invalidation of the thermal shutdown function only when the bit values of the 8-bit designation data DTS [7, 0] designating the validation or invalidation of the thermal shutdown function output from the setting data register 122 completely match the bit values of the register value "11101010" designating the invalidation of the thermal shutdown function, and otherwise outputs the 1-bit designation data "1" indicating the validation of the thermal shutdown function.

[0074] The combinational circuit 148 outputs the 1-bit designation data "0" or "1" to the AND circuit 145. The AND circuit 145 that receives output of the combinational circuit 148 has the same function as the AND circuit 145 in the head drive circuit 101 according to the related-art example.

[0075] That is, the AND circuit 145 outputs "0" when both the received data from the temperature sensor unit

140 and the received data from the combinational circuit 148 are not "1". That is, the AND circuit 145 outputs "0" when the head drive circuit 101 is not in the abnormal heat generation state or the thermal shutdown function is set to be invalidated even though the head drive circuit 101 is in an abnormal heat generation state. The output data "0" from the AND circuit 145 is data instructing continuation of driving of the logic unit 120 and the analog unit 130 of the head drive circuit 101.

[0076] On the other hand, the AND circuit 145 outputs "1" when both the received data from the temperature sensor unit 140 and the received data from the combinational circuit 148 are "1". That is, the AND circuit 145 outputs "1" only when the head drive circuit 101 is in the abnormal heat generation state and the thermal shutdown function is set to be validated. The output data "1" from the AND circuit 145 is data instructing stop of driving of the logic unit 120 and the analog unit 130 of the head drive circuit 101.

[0077] The OR circuit 146 that receives output of the AND circuit 145 also has the same function as the OR circuit 146 in the head drive circuit 101 according to the related-art example.

[0078] The combinational circuit 126 has the same function as the combinational circuit 148. That is, the combinational circuit 126 outputs the 1-bit designation data "0" indicating the invalidation of the short-circuit prevention function only when the bit values of the 8-bit designation data DTS [7, 0] designating the validation or invalidation of the short-circuit prevention function output from the setting data register 122 completely match the bit values of the register value "11011010" designating the invalidation of the short-circuit prevention function, and otherwise outputs the 1-bit designation data "1" indicating the validation of the short-circuit prevention function.

Effects

[0079] As described above, in the head drive circuit 101 according to the embodiment, all bits in the 8-bit setting data stored in the setting data register 122 are allocated to the designation data designating the validation or invalidation of the protection function. For this reason, even when an erroneous operation at the time of inputting setting data, a bit error during data processing, or the like occurs, it is unlikely that all the bit values of the designation data completely match the register value designating the invalidation of the protection function. It can be considered that such a situation does not occur at all. Therefore, in the head drive circuit 101 according to the embodiment, it is considered that occurrence of unintentional invalidation of the protection function is prevented.

Short-circuit Prevention Function

[0080] Hereinafter, the short-circuit prevention func-

tion will be described with reference to FIGS. 9 to 11. Hereinafter, first, a configuration example of the gate driver 133 provided in the analog unit 130 of the head drive circuit 101 will be described, then a configuration example of the waveform pattern generation unit 124 provided in the logic unit 120 of the head drive circuit 101 will be described, and then an operation example of the gate driver 133 and the waveform pattern generation unit 124 in which the short-circuit prevention function is validated and invalidated will be described.

Gate Driver

[0081] First, the gate driver 133 will be described with reference to FIG. 9. FIG. 9 is a block diagram showing a configuration example of the gate driver 133. The gate driver 133 shown in FIG. 9 corresponds to one actuator PZT in the actuator group 102.

[0082] The gate driver 133 includes a plurality of switch elements QS, QA, QB, QC, and QD. The switch elements QS, QA, QB, QC, and QD are provided with appropriate power supply levels by a drive power supply PS.

[0083] For example, the drive power supply PS includes a plurality of power supplies PSA, PSB, PSC, and PSD. The power supply PSA provides the switch element QA with a power supply level VA with respect to a reference potential VSS. The power supply PSB provides the switch element QB with a power supply level VB with respect to the reference potential VSS. The power supply PSC provides the switch element QC with a power supply level VC with respect to the reference potential VSS. The power supply PSD provides the switch element QD with a power supply level VD with respect to the reference potential VSS. For example, the reference potential VSS is a negative potential, and the power supply levels VA, VB, VC, and VD are positive potentials.

[0084] The switch element QS connects a pair of electrodes of the actuator PZT. The switch elements QA, QB, QC, and QD connect the actuator PZT and the power supplies PSA, PSB, PSC, and PSD, respectively. Specifically, the switch element QA connects the other electrode of the actuator PZT and the other power supply terminal of the power supply PSA. The switch element QB connects the other electrode of the actuator PZT and the other power supply terminal of the power supply PSB. The switch element QC connects the other electrode of the actuator PZT and the other power supply terminal of the power supply PSC. The switch element QD connects the other electrode of the actuator PZT and the other power supply terminal of the power supply PSD.

[0085] For example, the switch elements QS and QA to QD are MOSFETs. The switch element QS is turned on by a gate voltage NSg, and an output level at that time is VSS. The switch element QA is turned on by a gate voltage PAg, and an output level at that time is VA. The switch element QB is turned on by a gate voltage PBg, and an output level at that time is VB. The switch element QC is turned on by a gate voltage PCg, and an output

level at that time is VC. The switch element QD is turned on by a gate voltage PDg, and an output level at that time is VD.

5 Waveform Pattern Generation Unit

[0086] Next, the waveform pattern generation unit 124 will be described with reference to FIG. 10. FIG. 10 is a block diagram showing a configuration example of the waveform pattern generation unit 124.

[0087] The waveform pattern generation unit 124 includes a waveform timer 171, a decoder state machine 172, a waveform level selector 173, and a waveform level selector 174.

[0088] The waveform timer 171 is a timer circuit that generates a pulse signal for forming ink drops in a multi-drop method. Fire1, Fire2, ..., and Fire14 respectively correspond to the ink drops (gradations). Timer [7:0] indicates that the pulse signal is 8-bit data.

[0089] The decoder state machine 172 outputs data designating a waveform output level to the waveform level selector 173 and the waveform level selector 174 based on the pulse signal generated by the waveform timer 171. FW [4:0] indicates 5-bit data corresponding to the power supply levels VSS, VA, VB, VC, and VD shown in FIG. 9.

[0090] The waveform level selectors 173 and 174 are selectively used according to the ink drops (gradations). The waveform level selectors 173 and 174 have the same basic functions. The waveform level selectors 173 and 174 output, to the gate driver 133, signals (gate voltages) NSg, PAg, PBg, PCg, and PDg for turning on the switch elements QS, QA, QB, QC, and QD based on the print data.

[0091] The waveform pattern generation unit 124 controls on and off of the switch elements QS, QA, QB, QC and QD in the gate driver 133 based on the print data and the setting data. Accordingly, the gate driver 133 outputs a drive waveform for driving the one actuator PZT in the actuator group 102 of the head 100.

Operation Example

[0092] In the gate driver 133 shown in FIG. 9, it is not permitted to simultaneously turn on a plurality of switch elements connected in series, specifically, the switch element QS and any of the switch elements QA, QB, QC, QD.

[0093] The power supply levels VA, VB, VC, and VD of the switch elements QA, QB, QC, and QD are generally different. In this case, it is not permitted to simultaneously turn on two or more of the switch elements QA, QB, QC, QD connected in parallel.

[0094] However, it is permitted to simultaneously turn on the switch elements QA, QB, QC, QD of the same power supply levels VA, VB, VC, VD.

[0095] FIG. 11 is a diagram showing a list of a waveform output level of a drive waveform output from the gate

driver 133, an ON switch, and an ON resistance. The ON switch means a switch element that is turned on to obtain a desired waveform output level, and the ON resistance means a resistance while the switch element is turned on.

[0096] As shown in FIG. 11, the ON resistance of each of the switch elements QS, QA, QB, QC, and QD is 200 Ω . If the power supply levels VB, VC, and VD are the same, it is permitted to simultaneously turn on the switch elements QB, QC, and QD. In this case, the combined ON resistance (parallel resistance) of the switch elements QB, QC, and QD is 66.7 Ω .

[0097] A magnitude of the ON resistance (parallel resistance) is related to a speed at which the drive waveform for driving the actuator PZT rises and falls. The drive waveform rises and falls faster when the ON resistance (parallel resistance) is low than when the ON resistance (parallel resistance) is high.

[0098] Therefore, for the plurality of switch elements connected in parallel and having the same power supply level, by invalidating the short-circuit prevention function and simultaneously turning on the switch elements, it is also possible to perform control such as speeding up rising and falling of the drive waveform of the actuator PZT.

[0099] Therefore, the decoder state machine 172 (see FIG. 10) determines whether to allow simultaneous turning-on of the plurality of switch elements connected in parallel based on power supply level data in the setting data and the designation data DSP designating the validation or invalidation of the short-circuit prevention function, and then determines the waveform pattern to be output from the waveform level selectors 173 and 174. That is, the decoder state machine 172 includes the short-circuit prevention circuit 125 (see FIG. 2), and validates or invalidates the short-circuit prevention function.

Others

[0100] The program according to the present embodiment may be transferred while being stored in an electronic device, or may be transferred without being stored in an electronic device. In the latter case, the program may be transferred via a network or may be transferred while being stored in a storage medium. The storage medium is a non-transitory tangible medium. The storage medium is a computer-readable medium. The storage medium may be of any type as long as the storage medium can store a program and is readable by a computer, such as a CD-ROM or a memory card.

[0101] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the exemplary embodiments. The novel embodiments can be implemented in various other forms, and various omissions, substitutions, and changes can be made in a scope not departing from the exemplary embodiments. The embodiments and the modifications

thereof are included in the scope of the exemplary embodiments, and are included in a scope of the exemplary embodiments disclosed in the claims.

Claims

1. An ink jet head drive circuit (101) that drives an ink jet head, the ink jet head including a pressure chamber configured to accommodate ink, a nozzle configured to communicate with the pressure chamber, and an actuator configured to expand and contract the pressure chamber to eject the ink from the nozzle, the circuit comprising:

a drive unit configured to drive the actuator;
a protection circuit configured to execute a protection function of the ink jet head drive circuit; and

a setting data register (122) configured to store setting data including multi-bit designation data designating validation or invalidation of the protection function and to output the multi-bit designation data to the protection circuit, wherein the protection circuit invalidates the protection function only when bit values of the multi-bit designation data match bit values of multi-bit invalidation designation data designating the invalidation of the protection function, and the protection circuit validates the protection function when the bit values of the multi-bit designation data do not match the bit values of the multi-bit invalidation designation data.

2. The circuit according to claim 1, wherein the protection circuit includes a logic circuit configured to generate 1-bit designation data from the multi-bit designation data.

3. The circuit according to claim 2, wherein the logic circuit receives the bit values of the multi-bit designation data, and outputs "0" when the bit values of the multi-bit designation data match the bit values of the multi-bit invalidation designation data, and outputs "1" when the bit values of the multi-bit designation data do not match the bit values of the multi-bit invalidation designation data.

4. The circuit according to any one of claims 1 to 3, wherein all bits in the setting data stored in the setting data register are allocated to the designation data designating validation or invalidation of the protection function.

5. The circuit according to any one of claims 1 to 4, wherein the protection function includes a thermal shutdown function and/or a short-circuit prevention function.

6. The circuit according to any one of claims 1 to 5, further comprising:

a temperature sensor (141) configured to detect a temperature of the inkjet head drive circuit; and a comparator (111) configured to compare the temperature detected by the temperature sensor with a threshold, wherein the protection circuit stops the drive unit when the detected temperature is equal to or higher than the threshold.

7. The circuit according to claim 6, wherein:

the protection function includes a thermal shutdown function, and the logic circuit comprises a first logic circuit (148) configured to generate 1-bit designation data from the multi-bit designation data designating the validation or invalidation of the thermal shutdown function.

8. The circuit according to claim 7, further comprising an AND circuit (145) configured to receive the output of the first logic circuit.

9. The circuit according to any one of claims 1 to 8, wherein

the drive unit includes a plurality of switch elements having different power supply levels, and the protection circuit prevents the plurality of switch elements from being simultaneously turned on.

10. The circuit according to any one of claims 1 to 9, wherein

the drive unit includes a plurality of switch elements having the same power supply level, and the switch elements of the same power supply level are permitted to simultaneously turn on.

11. The circuit according to claim 9 or 10, wherein the plurality of switch elements are connected in parallel.

12. The circuit according to any one of claims 9 to 11, wherein:

the protection function includes a short-circuit prevention function, and the logic circuit comprises a second logic circuit (126) configured to generate 1-bit designation data from the multi-bit designation data designating the validation or invalidation of the short-circuit prevention function.

13. The circuit according to claim 12, further comprising

a waveform pattern generation unit configured to receive the output of the second logic circuit.

14. The circuit according to claim 13, wherein the waveform pattern generation unit is configured to determine whether to allow simultaneous turning-on of the plurality of switch elements based on power supply level data in the setting data and the designation data, and to determine the waveform pattern to be output.

15. An inkjet head (100) comprising:

a pressure chamber configured to accommodate ink, a nozzle configured to communicate with the pressure chamber, an actuator configured to expand and contract the pressure chamber to eject the ink from the nozzle, and the inkjet head drive circuit according to any one of claims 1 to 14.

FIG. 1

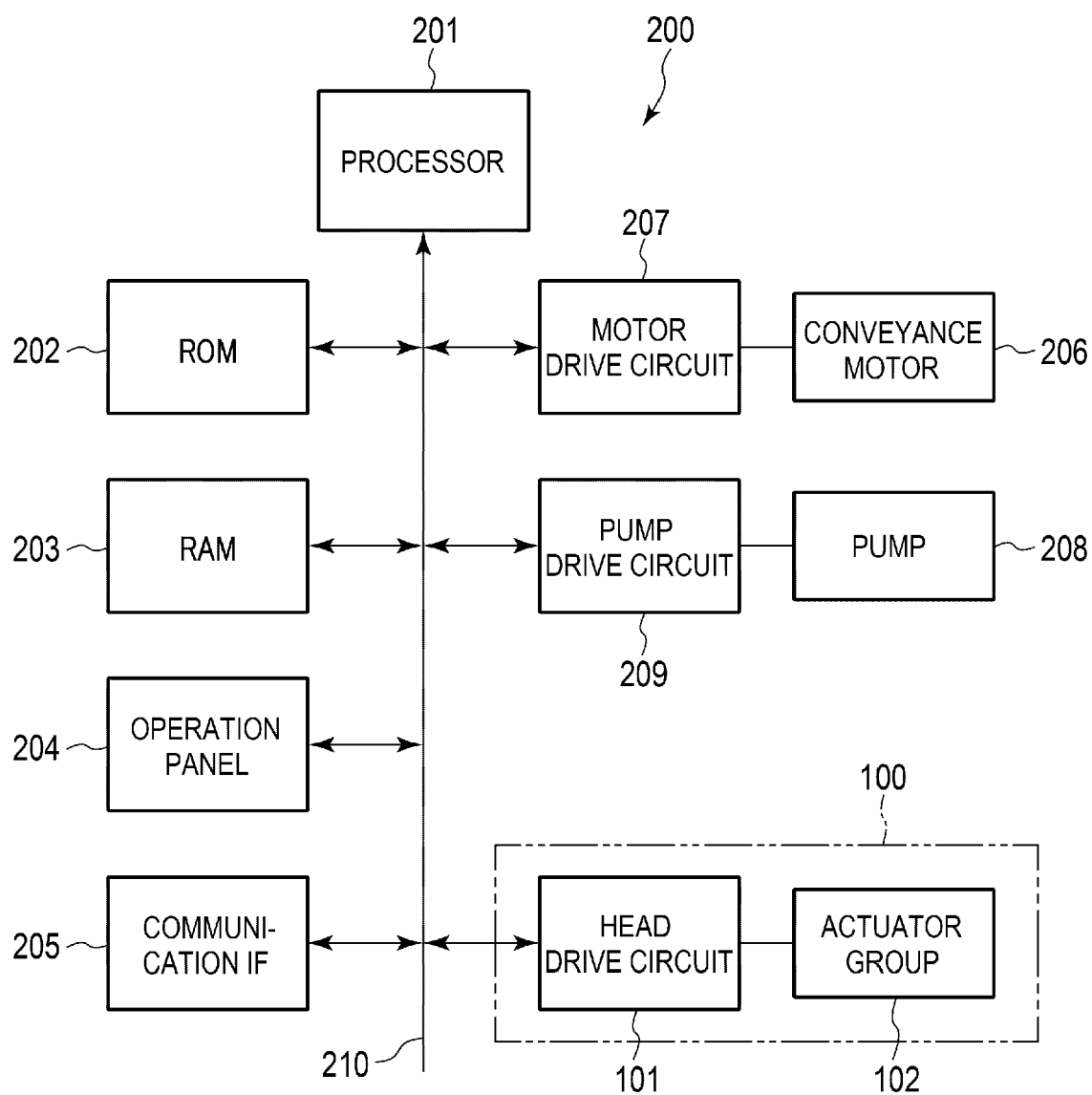


FIG. 2

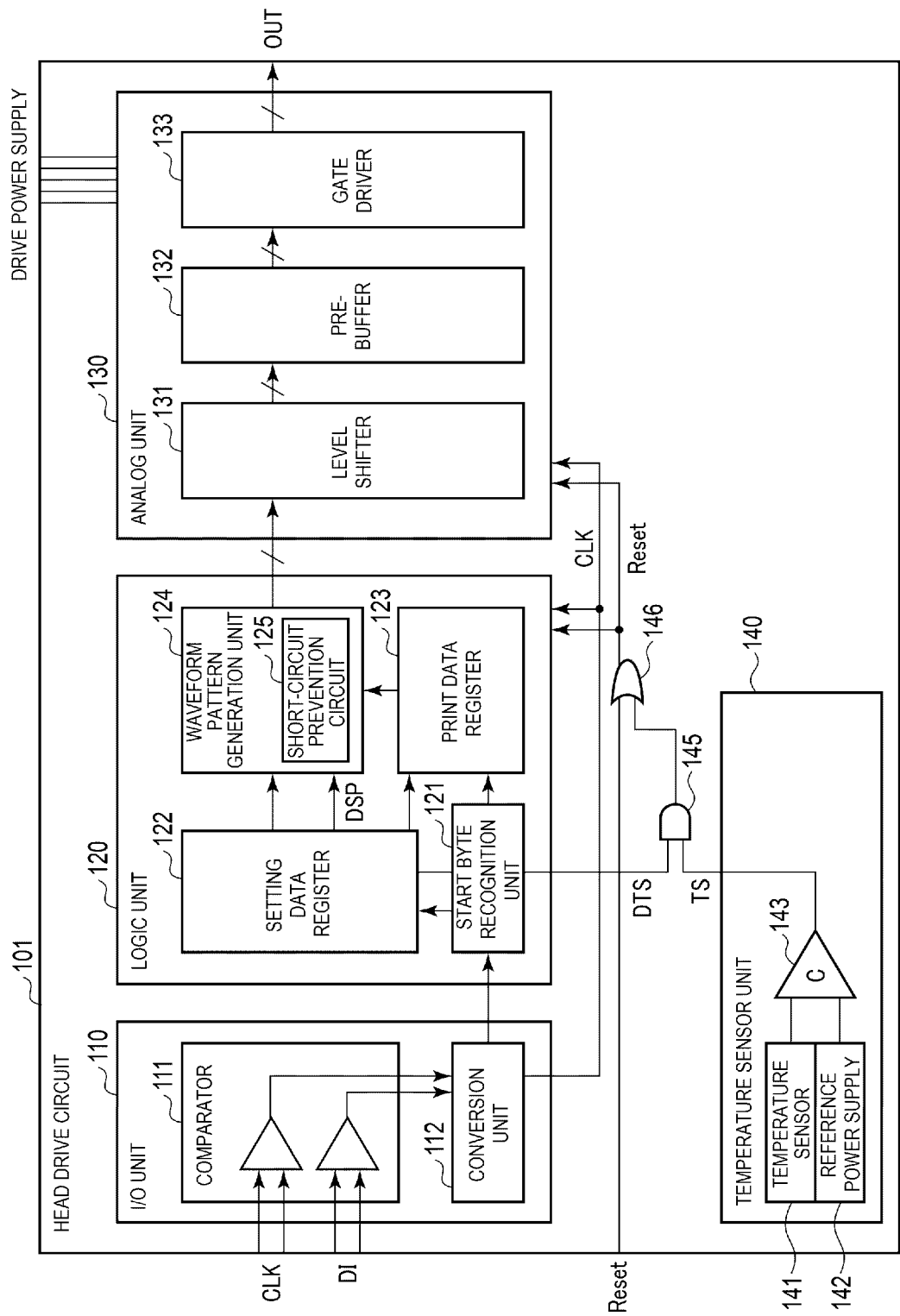


FIG. 3

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	SHUTDOWN	0	0	0	0	0	0	0	DTS
0x01	SHORT-CIRCUIT PREVENTION	0	0	0	0	0	0	0	DSP
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 4

		REGISTER VALUE	
Address	Name	VALIDATE	INVALIDATE
0x00	SHUTDOWN	00000001	00000000
0x01	SHORT-CIRCUIT PREVENTION	00000001	00000000
⋮	⋮	⋮	⋮

FIG. 5

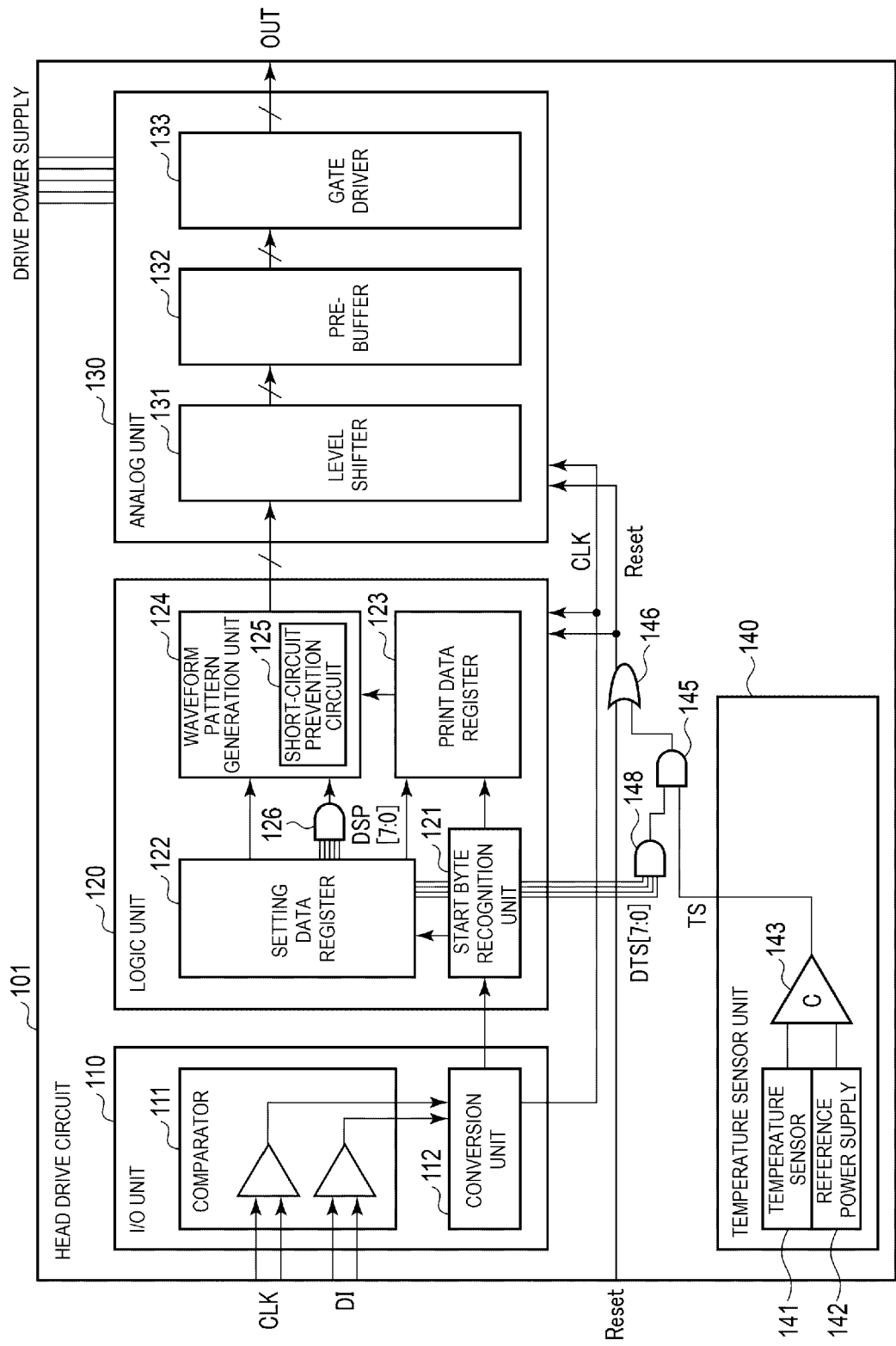


FIG. 6

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	SHUTDOWN	DTS[7:0]							
0x01	SHORT-CIRCUIT PREVENTION	DSP[7:0]							
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 7

		REGISTER VALUE	
Address	Name	VALIDATE	INVALIDATE
0x00	SHUTDOWN	XXXXXXXX	11101010
0x01	SHORT-CIRCUIT PREVENTION	XXXXXXXX	11011010
⋮	⋮	⋮	⋮

FIG. 8

D7	D6	D5	D4	D3	D2	D1	D0	OUT
1	1	1	0	1	0	1	0	0
0	X	X	X	X	X	X	X	1
X	0	X	X	X	X	X	X	1
X	X	0	X	X	X	X	X	1
X	X	X	1	X	X	X	X	1
X	X	X	X	0	X	X	X	1
X	X	X	X	X	1	X	X	1
X	X	X	X	X	X	0	X	1
X	X	X	X	X	X	X	1	1

FIG. 9

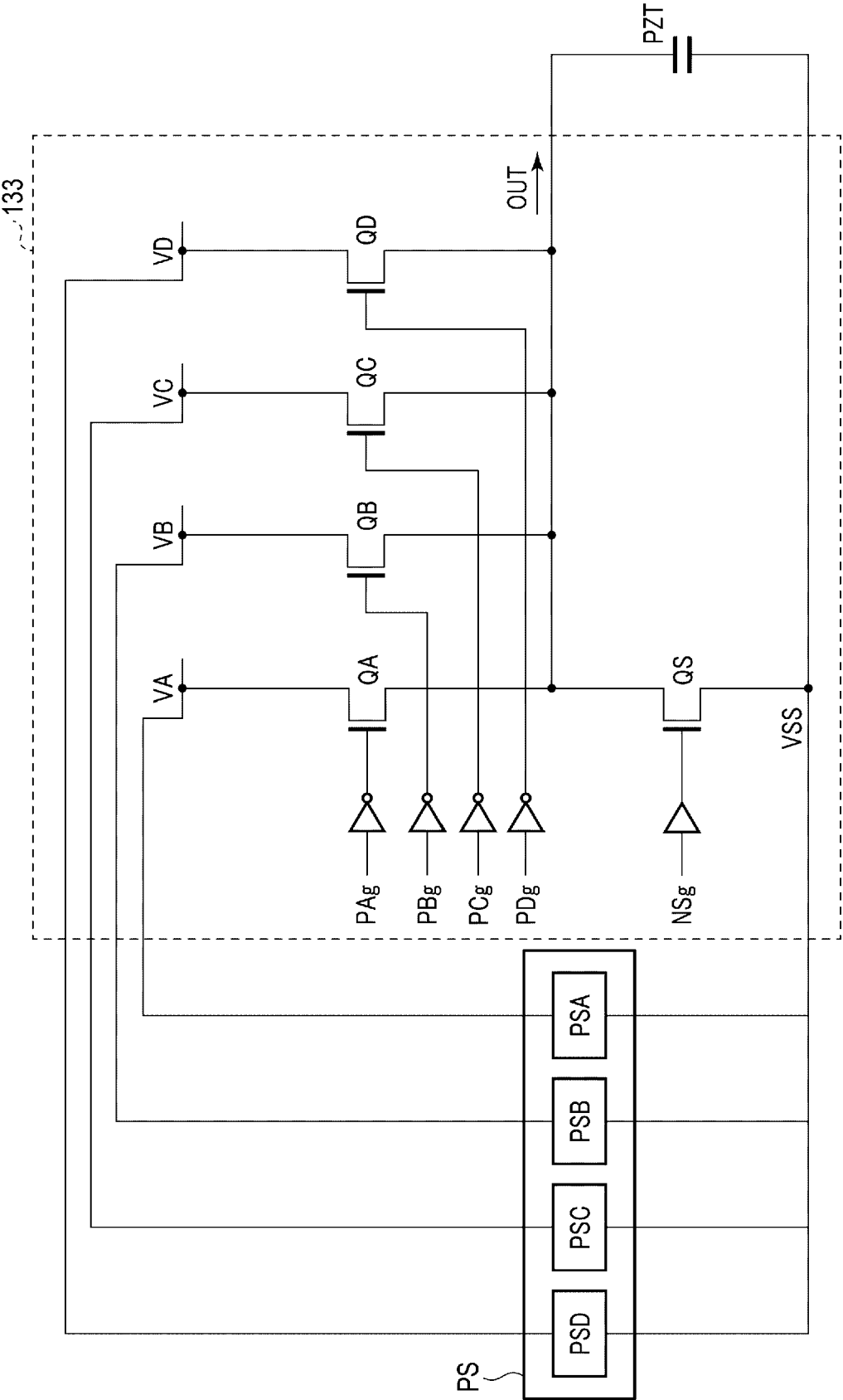


FIG. 10

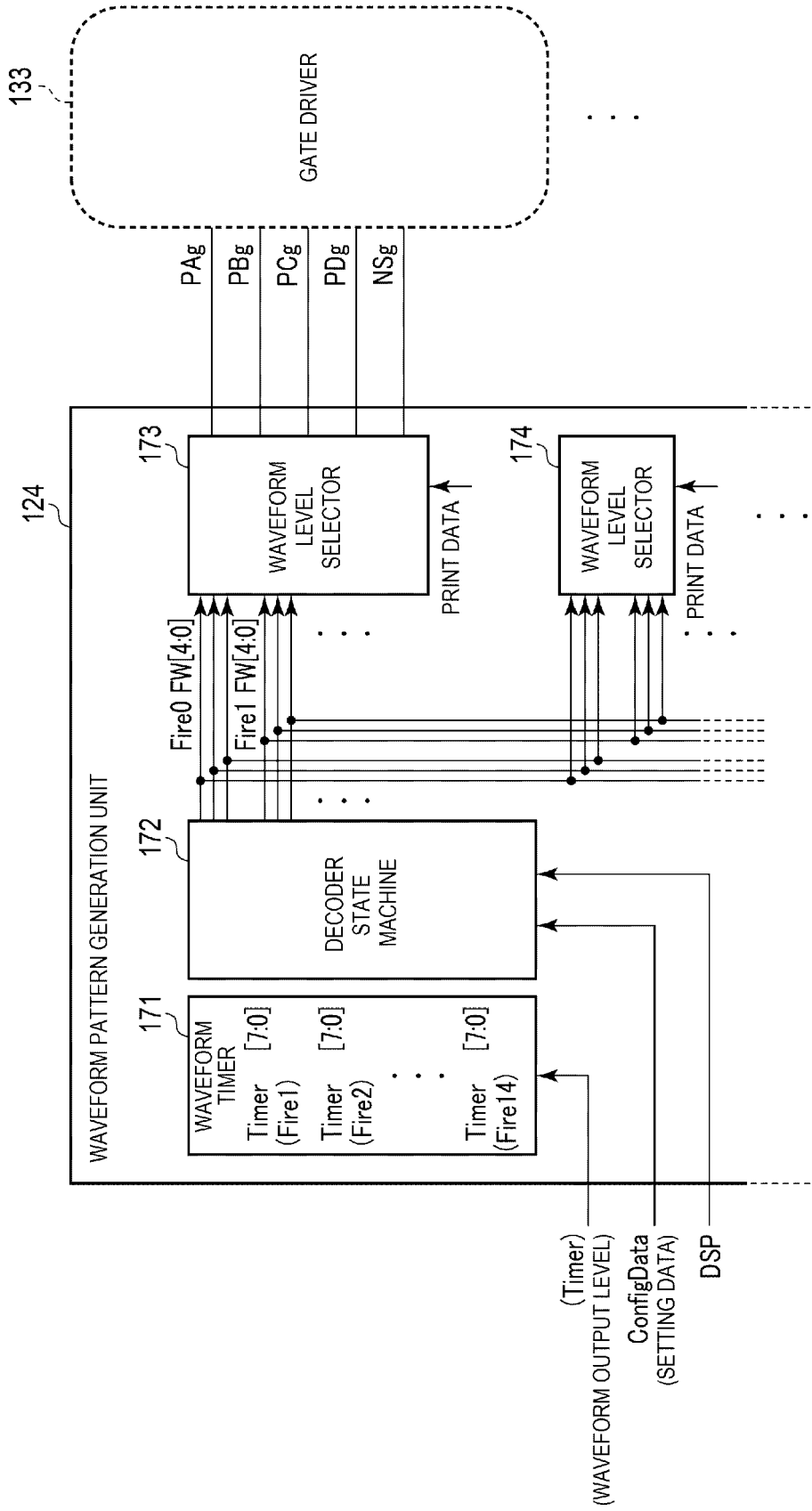


FIG. 11

WAVEFORM OUTPUT LEVEL	ON SWITCH	ON RESISTANCE
VSS	QS	200 Ω
VA	QA	200 Ω
VB	QB	200 Ω
VC	QC	200 Ω
VD	QD	200 Ω
VB=VC=VD	QB QC QD	66.7 Ω



EUROPEAN SEARCH REPORT

Application Number

EP 24 17 4998

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A	WO 2022/066166 A1 (HEWLETT PACKARD DEVELOPMENT CO [US]) 31 March 2022 (2022-03-31) * paragraph [0031] * -----	1-15	
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			B41J
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
The Hague		27 September 2024	Bardet, Maude
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