The present invention provides a strained-Si structure, in which the nFET regions of the structure are strained in tension and the pFET regions of the structure are strained in compression. Broadly the strained-Si structure comprises a substrate, a first layered stack atop the substrate, the first layered stack comprising a first Si-containing portion of the substrate, a compressive layer atop the Si-containing portion of the substrate, and a semiconducting silicon layer atop the compressive layer; and a second layered stack atop the substrate, the second layered stack comprising a second-silicon containing layer portion of the substrate, a tensile layer atop the second Si-containing portion of the substrate, and a second semiconducting silicon-layer atop the tensile layer.
FIG. 2
FIG. 3
FIG. 4a

FIG. 4b
FIG. 5a

FIG. 5b
STRAIN SI ON MULTIPLE MATERIALS FOR BULK OR SOI SUBSTRATES

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor materials having enhanced electron and hole mobilities, and more particularly, to semiconductor materials that include a silicon (Si)-containing layer having enhanced electron and hole mobilities. The present invention also provides methods for forming such semiconductor materials.

BACKGROUND OF THE INVENTION

[0002] For more than three decades, the continued miniaturization of silicon metal oxide semiconductor field effect transistors (MOSFETs) has driven the worldwide semiconductor industry. Various showstoppers to continued scaling have been predicted for decades, but a history of innovation has sustained Moore’s Law in spite of many challenges. However, there are growing signs today that MOSFETs are beginning to reach their traditional scaling limits. A concise summary of near-term and long-term challenges to continued CMOS scaling can be found in the “Grand Challenges” section of the 2002 Update of the International Technology Roadmap for Semiconductors (ITRS). A very thorough review of the device, material, circuit, and systems can be found in Proc. IEEE, Vol. 89, No. 3, March 2001, a special issue dedicated to the limits of semiconductor technology.

[0003] Since it has become increasingly difficult to improve MOSFETs and therefore complementary metal oxide semiconductor (CMOS) performance through continued scaling, methods for improving performance without scaling have become critical. One approach for doing this is to increase carrier (electron and/or hole) mobilities. One method for increasing carrier mobility is to introduce an appropriate strain into the Si lattice.

[0004] The application of stresses or strains changes the lattice dimensions of the Si-containing. By changing the lattice dimensions, the energy gap of the material is changed as well. The change may only be slight in intrinsic semiconductors resulting in only a small change in resistance, but when the semiconducting material is doped, i.e., n-type, and partially ionized, a very small change in the energy bands can cause a large percentage change in the energy difference between the impurity levels and the band edge. Thus, the change in resistance of the material with stress is large.

[0005] Prior attempts to provide strain-based improvements of semiconductor substrates have utilized etch stop liners or embedded SiGe structures. N-type channel field effect transistors (nFETs) need tension on the channel for strain-based device improvements, while p-type channel field effect transistors (pFETs) need a compressive force on the channel for strain-based device improvements. Further scaling of semiconducting devices requires that the strain levels produced within the substrate be controlled and that new methods be developed to increase the strain that can be produced.

[0006] In view of the state of the art mentioned above, there is a continued need for providing strained-Si substrates in bulk-Si or SOI substrates in which the substrate can be appropriately strained for both nFET and pFET devices.

SUMMARY

[0007] The present invention provides a strained-Si substrate, in which the nFET regions of the substrate are strained in tension and the pFET regions of the substrate are strained in compression. The present invention also provides a strained-Si substrate incorporating either bulk-Si or SOI substrate configurations.

[0008] The foregoing is achieved in the present invention by positioning a compressive SiGe layer or tensile Si:C layer underlying a semiconducting layer. The term “compressive SiGe layer” denotes that a SiGe layer is under an internal compressive strain (also referred to as an intrinsic compressive strain), in which the compressive strain is produced by a lattice mismatch between the larger lattice dimension of the compressive SiGe layer and the smaller lattice dimension of the layer on which the compressive SiGe layer is epitaxially grown. The term “tensile Si:C layer” denotes that a Si:C layer is under an internal tensile strain (also referred to as an intrinsic tensile strain), in which the tensile strain is produced by a lattice mismatch between the smaller lattice dimension of the tensile Si:C layer and the larger lattice dimension of the layer on which the tensile Si:C layer is epitaxially grown.

[0009] The compressive SiGe layer elastically transfers tensile stresses to the overlying semiconducting layer. Therefore, the compressive SiGe layer provides strain based device improvements for n-type field effect transistors (nFETs). The tensile Si:C layer elastically transfers compressive stresses to the overlying semiconducting layer. Therefore, the tensile Si:C layer provides strain based device improvements for p-type field effect transistors (pFETs).

[0010] a substrate;

[0011] a first layered stack atop the substrate, the first layered stack comprising a first Si-containing portion of the substrate, a compressive layer atop the first Si-containing portion of the substrate, and a first semiconductor layer atop the compressive layer;

[0012] a second layered stack atop the substrate, the second layered stack comprising a second-Si-containing layer portion of the substrate, a tensile layer atop the second Si-containing portion of the substrate, and a second semiconductor layer atop the tensile layer; and

[0013] The compressive layer elastically transfers tensile strain to the overlying first semiconducting layer. Therefore, the first semiconducting layer is strained to provide strained-Si device improvements for nFET devices, in which the tensile strain transferred from the compressive layer to the overlying first semiconducting layer increases the carrier mobility for n-type channels.

[0014] The tensile layer incorporated into the second stack has lattice dimensions that are less than the underlying Si-containing portion of the substrate. The tensile layer may comprise SiGe. The first semiconducting layer may be a Si-containing material that has lattice dimensions greater than the tensile layer.
The tensile layer elastically transfers compressive strain to the second semiconducting layer. Therefore, the second semiconducting layer is strained to provide strained-Si device improvements for pFET devices, in which the compressive stress transferred from the tensile layer to the overlying second semiconducting layer increases the carrier mobility for p-type channels. The substrate, on which the first layered stack and second layered stack is formed, can be an SOI substrate or a bulk-Si substrate.

Another aspect of the present invention is a method for forming the above described strained-Si substrate. Broadly, the inventive method for forming a strained-Si substrate comprises:

- providing a Si-containing substrate;
- forming a first pad stack atop a first portion of the Si-containing substrate, the first pad stack comprising a compressive layer positioned atop the first portion of the Si-containing substrate, a first semiconducting layer atop the compressive layer and a first etch barrier atop the first semiconducting layer;
- forming a second pad stack atop a second portion of the Si-containing substrate, the second pad stack comprising a tensile layer positioned atop the second portion of the Si-containing layer, a second semiconducting layer atop the tensile layer, and a second etch barrier atop the second semiconducting layer;
- etching the Si-containing substrate selective to the first etch stop barrier and the second etch stop barrier, wherein the compressive layer elastically transfers a tensile strain to the first semiconducting layer and the tensile layer elastically transfers a compressive strain to second semiconducting layer;
- removing the first etch stop barrier and the second etch stop barrier; and
- forming an isolation region between the first pad stack and the second pad stack.

The compressive layer can be formed by epitaxially growing SiGe atop the Si-containing substrate, wherein the SiGe is grown to a thickness that is less than the critical thickness of SiGe. If the thickness of the SiGe is greater than the critical thickness, the layer can relax due to the formation of defects. The tensile layer can be formed by epitaxially growing Si, which is in-situ doped with carbon. The Si:C tensile layer may be grown to a thickness that is less than the critical thickness of Si:C. If the thickness of Si:C exceeds its critical thickness, the layer will relax due to the formation of defects. To maintain tension within the tensile layer, the Si:C should not be thicker than the critical thickness.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) illustrates (through a cross-sectional view) one embodiment of the present invention including a SOI substrate having a compressively strained semiconducting portion and a tensile strained semiconducting portion.

FIG. 1(b) illustrates (through a cross-sectional view) one embodiment of the present invention including a bulk-Si substrate having a compressively strained semiconducting portion and a tensile strained semiconducting portion.

FIG. 2 depicts (through a cross-sectional view) the compressive and tensile stresses of one embodiment of the present invention having a material stack comprising a SiGe layer.

FIG. 3 depicts (through a cross-sectional view) the compressive and tensile stresses of one embodiment of the present invention having a material stack comprising a Si:C layer.

FIGS. 4(a)-10(c) illustrate (through cross-sectional views) the process steps for producing the structure depicted in FIG. 1(a).

FIGS. 4(b)-10(b) illustrate (through cross-sectional views) the process steps for producing the structure depicted in FIG. 1(b).

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides substrates comprising both a compressively strained semiconducting portion and a tensile strained semiconducting portion, and a method of forming the same.

The present invention advantageously provides substrates having both compressively strained and tensile strained semiconducting portions by forming a first and second material stack atop a substrate, in which the first material stack comprises a compressive layer that elastically transfers a tensile strain to an overlying semiconducting portion and the second material stack comprises a tensile layer that elastically transfers a compressive strain to an overlying semiconducting portion. The present invention is now discussed in more detail referring to the drawings that accompany the present application. In the accompanying drawings, like and or corresponding elements are referred to by like reference numbers.

The present invention provides material stacks of different lattice materials for nFET and pFET devices that can be incorporated onto the same substrate. It is advantageous for nFETs to have a channel region that is strained in tension and for pFETs to have a channel that is strained in compression, where the strain applied to the channel improves the device's performance.

Referring to FIG. 1(a), in one embodiment of the present invention, an nFET stack 11 and a pFET stack 12 are positioned on a buried insulating layer 15 of a silicon-on-insulator (SOI) substrate 30, in which the nFET stack 11 and the pFET stack 12 are separated by an isolation region 13.

The nFET stack 11 comprises a first semiconducting layer 16, a compressive SiGe layer 17 and a Si-containing substrate portion 18. The Si-containing substrate portion 18 is formed from the upper Si-containing layer of the SOI substrate 30. The compressive SiGe layer 17 elastically transfers a tensile strain to the overlying first semiconductor layer 16. The first semiconductor layer 16 is under a tensile strain and is therefore well suited to be the channel region of an nFET device.

The pFET stack 12 comprises a second semiconducting layer 20, a tensile Si:C layer 21, and a Si-containing substrate portion 18. The Si-containing substrate portion 18 is formed from the upper Si-containing layer of the SOI substrate 30. The tensile Si:C layer 21 elastically transfers a
compressive strain to the overlying second semiconductor layer 20. The second semiconducting layer 20 is under a compressive strain and is therefore well suited to be the channel region of a pFET device.

[0036] FIG. 1(b) represents another embodiment of the present invention, in which an nFET stack 11 and a pFET stack 12 are formed on a bulk-silicon (bulk-Si) substrate 14. In this embodiment, the Si-containing substrate portion 18 of the nFET stack 11 and the pFET stack 12 are mesa portions of the bulk-Si substrate 14, which are produced using a timed directional etch process.

[0037] Referring to FIG. 2, the tensile strain produced in the first semiconducting layer 16 of the nFET stack 11 is produced by the appropriate combinations of different lattice materials positioned in the stacked structure. Specifically, the lattice structures of the Si-containing substrate portion 18 and the SiGe compressive layer 17 allow for the SiGe layer to be compressively strained. The compressive strain is the result of the larger lattice dimensions of SiGe being epitaxially grown atop the smaller lattice dimensions of the underlying Si-containing substrate portion 18. Silicon has a lattice dimension of approximately 5.43 Å, and Ge has a lattice structure on the order of about 5.65 Å. During epilaxial growth, SiGe is grown so that the larger lattice structure of the SiGe grows atop and is aligned to the smaller lattice structure of the underlying Si-containing substrate portion 18. Therefore, the SiGe is grown having a smaller lattice than is energetically favorable and a compressive strain is produced within the SiGe.

[0038] The first semiconducting layer 16 is epitaxially grown atop the compressive SiGe layer 17, in which the first semiconducting layer 16 comprises a Si-containing material having a smaller lattice structure than the compressive SiGe layer 17. Following epitaxial growth of the first semiconducting layer 16, the nFET stack 11 is etched so that the exposed edge of the compressive SiGe layer 17 elastically relaxes and transfers a tensile strain to the overlying first semiconducting layer 16.

[0039] Referring to FIG. 2, a simulation of one embodiment of an nFET stack 11 of the present invention is provided, where the solid lines represent stress in tension and the dotted lines represent stress in compression. In the simulation depicted, a compressive SiGe layer 17 is formed having a thickness on the order of 250 Å comprising Ge present in a concentration of approximately 25%, by atomic weight %, which were a compressive stress on the order of about 2000 MPa is produced by the above described lattice mismatch. Still referring to FIG. 2, the compressive SiGe layer 17 elastically transfers tensile stresses, on the order of 250 MPa, to the overlying first semiconducting layer 16, which comprises epitaxially grown silicon having a thickness on the order of about 250 Å.

[0040] Referring now to FIG. 3, the compressive strain produced in the second semiconducting layer 20 of the pFET stack 12 is produced by the appropriate combinations of different lattice dimension materials positioned in a stacked structure. Specifically, the lattice structures of the Si-containing substrate portion 18 and the SiC tensile layer 21 allow for the SiC layer 21 to be strained in tension. The tensile strain is the result of the smaller lattice dimension of SiC layer being epitaxially grown atop the larger lattice dimension of the underlying Si-containing substrate portion 18. The size of the carbon atoms introduced into the Si is small enough, that when incorporated into a material layer of Si it produces a field of tensile strain around the carbon atom. By incorporating carbon into a Si material layer a tensile stress may be produced within the material layer on the order of about 1000 MPa for every 2% of carbon present, by atomic weight %.

[0041] The tensile SiC tensile layer 21 is epitaxially grown so that the smaller lattice structure of the SiC grows atop and is aligned to the larger lattice structure of the underlying Si-containing layer 18. Therefore, the SiC is grown having a larger lattice than is energetically favorable and a tensile strain is produced within the SiC.

[0042] The second semiconducting layer 20 is epitaxially grown atop the SiC tensile layer 21, in which the second semiconducting layer 20 comprises a Si-containing material having a larger lattice structure than the tensile SiC layer 21. Following the epitaxial growth of the second semiconducting layer 20, the pFET stack 12 is etched so that the exposed edge of the tensile SiC layer 21 elastically relaxes and transfers a compressive strain to the overlying second semiconducting layer 20.

[0043] Referring to FIG. 3, a simulation of one embodiment of a pFET stack 12 of the present invention is provided, where the solid lines represent stress in tension and the dotted lines represent stress in compression. In the simulation depicted, a tensile SiC layer 21 is formed having a thickness on the order of 250 Å comprising C present in a concentration of approximately 4% by atomic weight %, in which the tensile stress produced by the above described lattice mismatch is on the order of about 2000 MPa. Still referring to FIG. 3, the tensile SiC layer 21 elastically transfers a compressive stress, on the order of 250 MPa, to the overlying second semiconducting layer 20, which comprises epitaxially grown silicon having a thickness on the order of about 250 Å.

[0044] As discussed above, depositing a material layer (such as the compressive SiGe layer 17 or the tensile SiC layer 21) having a different energetically favorable lattice dimension than the surface on which the material layer is grown (such as the Si-containing substrate) produces a strain, since the lattice dimension of the material layer is strained to match the lattice dimension of the surface on which the material layer is grown. This form of growth may be referred to as pseudomorphic growth.

[0045] The strain produced in the material layer is maintained so long as the material layer is not grown to a thickness greater than it’s critical thickness. If the material layer is grown to a thickness greater than it’s critical thickness, the material layer will grow having it’s energetically favorable lattice dimension that differs from the lattice dimension of the surface on which the material layer is grown. This type of growth, in which the lattice dimensions of the material layer are no longer matched to the surface on which the material layer is deposited, may be referred to as incommensurate growth. The difference in lattice dimension of the material layer and the surface, on which the material layer is grown, results in the formation of misfit dislocations.

[0046] Once the deposited layer surpasses it’s critical thickness, relaxation can occur through slip mechanisms, such as dislocation motion. Relaxation disadvantageously...
diminishes the internal strain produced in the deposited layer. The “critical thickness” is the maximum thickness at which the layer will not relax.

In order for the strain produced in the compressive SiGe layer 17, the tensile Si:C layer 21, the first semiconducting layer 16, and the second semiconducting layer 20 of the present invention to be maintained, the thickness of the layer in which the strain is produced must be below its critical thickness. Expressed in terms of dislocation density, the critical thickness of the present invention is the maximum thickness of the strained layer in which the dislocation density is less than 1.0×10⁹ cm⁻².

The method for forming a strained-Si substrate that simultaneously comprises both appropriately strained nFET and pFET regions, is now discussed in greater detail. The method for forming appropriately strained nFET and pFET regions atop a silicon-on-insulator (SOI) substrate, as depicted in FIG. 1(a), is described with reference to FIGS. 4(a)-9(a). The method for forming appropriately strained nFET and pFET regions atop a bulk-Si substrate, as depicted in FIG. 1(b), is described with reference to FIGS. 4(b)-9(b).

Referring to FIG. 4(a), a SOI substrate 30 is provided comprising bottom Si-containing layer 19, a buried insulating layer 15 present atop the bottom Si-containing layer 19, and top Si-containing layer 18 present atop the surface of the buried insulating layer 15. The term “Si-containing layer” is used herein to denote a material that includes silicon. Illustrative examples of Si-containing materials include, but are not limited to: Si, SiGe, SiGeC, SiC, polysilicon, i.e., polySi, epitaxial silicon, i.e., epit-Si, amorphous Si, i.e., a-Si, and multilayers thereof. A preferred Si-containing material for the top and bottom Si-containing layers 18 and 19 is Si.

The top Si-containing layer 18 of SOI substrate 10 typically has a vertical thickness, t₁, i.e., height, of less than about 300 nm, with a vertical thickness of about 20 nm to about 50 nm being more typical. The composition of the top Si-containing layer 18 should have a lattice dimension that is smaller than the lattice dimension of the subsequently formed compressive SiGe layer and larger than the subsequently formed tensile Si:C layer. The top Si-containing layer 18 is hereafter referred to as the Si-containing substrate portion 18.

The thickness of the buried insulating layer 15 may vary, but typically, the buried insulating layer 15 has a thickness of less than about 350 nm, with a thickness from about 70 to about 150 nm being more highly preferred. The thickness of the bottom Si-containing layer 19 is inconsequential to the present invention.

The SOI substrate 30 is fabricated using techniques that are well known to those skilled in the art. For example, the SOI substrate 30 may be fabricated using a thermal bonding process, or alternatively the SOI substrate 30 may be fabricated by an ion implantation process, which is referred to as separation by implantation of oxygen (SIMOX). When a thermal bonding process is employed in fabricating the SOI substrate 30, an optional thinning step may be utilized to thin the top Si-containing layer 18 into an ultra-thin regime, which is on the order of less than 50 nm. The substrate 30 can also be a bulk-Si substrate 14, preferably comprising single crystal-Si, as depicted in FIG. 4(b).

Referring to FIG. 5(a), a compressive SiGe layer 17 is then formed atop the entire SOI substrate 30 depicted in FIG. 4(a). The compressive SiGe layer 17 can be grown using an epitaxial growth process. The Ge content of the compressive SiGe layer 17 may range from 5% to 50%, by atomic weight %, preferably ranging from 10% to 20%, more preferably being 15%.

The compressive SiGe layer 17 is grown to a thickness that is less than it’s critical thickness. Typically, the compressive SiGe layer 17 can be grown to a thickness ranging from about 10 nm to about 100 nm. The critical thickness of the compressive SiGe layer 17 is dependent on the Ge concentration of the layer. The critical thickness is also partial to high temperature processing steps, such as activation anneal, which are on the order of about 1100°C. The temperature of the SiGe growth process may range from about 500°C to about 800°C. In one example, when the Ge content of the compressive SiGe layer 17 is on the order of about 15%, by atomic weight %, the critical thickness of the compressive SiGe layer 17 is on the order of about 100 nm. It is noted that high temperature processing steps may reduce the critical thickness of the compressive SiGe layer 17 to about 20 nm. FIG. 5(b) represents this process step when the compressive SiGe layer 17 is formed atop a bulk-Si substrate 14.

Referring to FIG. 5(a), the first semiconducting layer 16 is then formed atop the compressive SiGe layer 17. The first semiconducting layer 16 comprises an epitaxially grown Si-containing material having lattice dimensions that are less than the lattice dimensions of the underlying compressive SiGe layer 17.

The first semiconducting layer 16 can be grown to a thickness that is less than it’s critical thickness. Typically, the first semiconducting layer 16 can be grown to a thickness ranging from about 10 nm to about 100 nm. The critical thickness of the first semiconducting layer 16 is on the order of 100 nm or less, depending on the properties of the underlying compressive SiGe layer 17. In one example, when the Ge content of the compressive SiGe layer 17 is on the order of about 15% by atomic weight %, the critical thickness of the first semiconducting layer 16 is on the order of about 100 nm. It is noted that high temperature processing steps may reduce the critical thickness of the first semiconducting layer 16 to about 20 nm. FIG. 5(b) represents this process step when the first semiconducting layer 16 is formed atop the compressive SiGe layer 17 positioned on the bulk-Si substrate 14.

Referring back to FIG. 5(a), a first cap layer 22 is formed deposited atop the first semiconducting layer 16. The first cap layer 22 may be any dielectric such as an oxide, nitride, or oxynitride, preferably being a nitride, such as Si₃N₄. Combinations of said dielectrics are also contemplated herein. The first cap layer 22 is deposited using deposition methods, such as chemical vapor deposition (CVD), plasma-assisted CVD, high-density chemical vapor deposition (HDCVD), and chemical solution deposition. The first cap layer 22 has a preferred thickness ranging from about 20 nm to about 30 nm. FIG. 5(b) represents this process step when utilizing a bulk-Si substrate 14.

Referring to FIG. 6(a), in a next process step the first cap layer 22 is patterned and etched to provide an etch mask that is subsequently utilized to pattern the nFET stack. Specifi
cally, a pattern is produced by applying a photoresist to the surface to be etched; exposing the photoresist to a pattern of radiation; and then developing the pattern into the photoresist utilizing a conventional resist developer. Once the patterning of the photoresist is completed, the sections of the first cap layer 22 covered by the photoresist are protected, while the exposed regions are removed using a selective etching process that removes the unprotected regions of the first cap layer 22 without substantially etching the underlying first semiconductor layer 16. The patterned first cap layer 22 is then utilized as an etch mask toetch the first semiconducting layer 16 and the compressive SiGe layer 17. Preferably a directional etch process, such as reactive ion etch, is utilized to etch the first semiconductor layer 16 and the compressive SiGe layer 17.

[0059] In a preferred embodiment, the first semiconductor layer 16 is etched with an etch chemistry that does not substantially etch the first cap layer 22 or the underlying compressive SiGe layer 17. Following first semiconductor layer 16 etch, the compressive SiGe layer 17 is then etched using an etch chemistry that does not substantially etch the Si-containing substrate portion 18. FIG. 6(b) depicts patterning and etching the first cap layer 22, the first semiconducting layer 16, and the compressive SiGe layer 17 atop a bulk-Si substrate 14.

[0060] Turning to FIG. 7(a), a tensile Si:C layer 21 is then formed atop the entire structure depicted in FIG. 6(a). The tensile Si:C layer 21 may be grown using an epitaxial growth process. The C content of the compressive Si:C layer 21 is less than about 6%, by atomic weight %, preferably ranging from 1% to 4%, more preferably being 3%. The tensile Si:C layer 17 is grown to a thickness that is less than its critical thickness. Typically, the tensile Si:C layer 17 is grown to a thickness ranging from about 10 nm to about 100 nm. The critical thickness of the tensile Si:C layer 17 is dependent on the C concentration of the layer. The temperature of the Si:C growth process may range from about 500° C. to about 800° C. In one example, when the C content of the tensile Si:C layer 21 is on the order of about 3%, by atomic weight %, the critical thickness of the tensile Si:C layer 21 is on the order of about 100 nm. It is noted that high temperature processing steps may reduce the critical thickness of the tensile Si:C layer 17 to about 20 nm.

[0061] Referring to FIG. 7(a), a second semiconducting layer 20 is then formed atop the tensile Si:C layer 21. The second semiconducting layer 20 comprises an epoxially grown Si-containing material having lattice dimensions that are greater than the lattice dimensions of the underlying tensile Si:C layer 21.

[0062] The second semiconducting layer 20 can be grown to a thickness that is less than it’s critical thickness. Typically, the second semiconducting layer 20 can be grown to a thickness ranging from about 10 nm to about 100 nm. The critical thickness of the second semiconducting layer 20 is on the order of 100 nm or less, depending on the properties of the underlying tensile Si:C layer 21. In one example, when the C content of the tensile Si:C layer 21 is on the order of about 3%, by atomic weight %, the critical thickness of the second semiconducting layer 20 is on the order of about 100 nm. It is noted that high temperature processing steps may reduce the critical thickness of the second semiconducting layer 20 to about 20 nm. FIG. 7(b) represents this process step when the second semiconducting layer 20 is formed atop the tensile Si:C layer 21 positioned on the bulk-Si substrate 14.

[0063] Referring back to FIG. 7(a), a second cap layer 23 is then formed atop the second semiconducting layer 20. The second cap layer 23 may be any dielectric such as an oxide, nitride, oxy-nitride, or a combination thereof, preferably being a nitride, such as Si₃N₄. The second cap layer 23 is deposited using deposition methods, such as chemical vapor deposition (CVD), plasma-assisted CVD, high-density chemical vapor deposition (HDCVD), and chemical solution deposition. The second cap layer 23 has a thickness ranging from about 20 nm to about 30 nm. FIG. 7(b) represents this process step when utilizing a bulk Si substrate 14.

[0064] Referring to FIG. 8(a), in a next process step the second cap layer 23 is patterned and etched to provide an etch mask that is subsequently utilized to pattern the pFET stack. Specifically, a pattern is produced by applying a photoresist to the surface to be etched; exposing the photoresist to a pattern of radiation; and then developing the pattern into the photoresist utilizing a conventional resist developer.

[0065] Once the patterning of the photoresist is completed, the sections of the second cap layer 23 covered by the photoresist are protected, while the exposed regions are removed using a selective etching process that removes the unprotected regions of the second cap layer 23 without substantially etching the underlying second semiconducting layer 20. The patterned second cap layer 23 is then utilized as an etch mask to etch the second semiconducting layer 20 and the tensile Si:C layer 21. Preferably a directional etch process, such as reactive ion etch, is utilized to etch the second semiconductor layer 20 and the compressive Si:C layer 21.

[0066] In a preferred embodiment, the second semiconductor layer 20 is etched with an etch chemistry that does not substantially etch the second cap layer 23 or the underlying tensile Si:C layer 21. Following second semiconductor layer 20 etch, the tensile Si:C layer 21 is then etched using an etch chemistry that does not substantially etch the Si-containing substrate portion 18. It is noted that the first cap layer 22 protects the underlying portions of the first semiconducting layer 16 and the compressive SiGe layer 17 during this etch step. FIG. 8(b) depicts patterning and etching the second cap layer 23, the second semiconducting layer 20, and the tensile Si:C layer 21 atop a bulk-Si substrate 14.

[0067] Referring to FIG. 9(a), in a next process step the Si-containing substrate portion 18 is then etched with a highly selective directional etch process, such as reactive ion etch, in which the first cap layer 22 and the second cap layer 23 function as an etch mask for the nFET stack 11 and the pFET stack 12. Preferably, the etch chemistry selectively etches the Si-containing substrate portion 18 without substantially etching the first cap layer 22, the second cap layer 23, and the buried insulating layer 15. The etch process may be timed or may utilize end point detection. Following Si-containing substrate portion 18 etch the first cap layer 22 and the second cap layer 23 are removed using a wet etch process.

[0068] FIG. 9(b) depicts this process step when forming strained nFET 11 and pFET 12 stacks on a bulk-Si substrate 14. In this embodiment, the upper surface of the bulk-Si
substrate 14 is etched with a highly selective directional etch process, such as reactive ion etch, in which the first cap layer 22 and the second cap layer 23 function as an etch mask for the nFET stack 11 and the pFET stack 12. In this embodiment, the etch process may be timed so that the surface of the bulk Si substrate 14 is etched to a depth ranging from about 20 nm to about 50 nm. The portion of the bulk-Si substrate 14 protected by the first and second cap layers 22, 23 during substrate etch and underlying the compressive SiGe layer 17 and the tensile SiC layer 21 is the Si-containing substrate portion 18 of the nFET and pFET stacks 11, 12.

[0069] Referring back to FIG. 9(a), an isolation region 13 is then formed separating the nFET stack 111 and the pFET stack 12. The isolation regions 13 may optionally be lined with a conventional liner material, e.g., an oxide or nitride, and then CVD or another like deposition process is used to fill the trench with insulating material. The dielectric may optionally be densified after deposition. A conventional planarization process such as chemical-mechanical polishing (CMP) may optionally be used to provide a planar structure.

[0070] FIG. 9(b) depicts forming an isolation region 13 separating the nFET stack 11 and the pFET stack 12, where the nFET stack 11 and the pFET stack 12 are positioned on a bulk-Si substrate 14. In this embodiment, region 18 denotes a mesa (i.e., non-etched) portion of the bulk substrate.

[0071] Conventional nFET and pFET forming processes may then be conducted to form at least one nFET device 35 on the nFET stack 11 and at least one pFET device 40 on the pFET stack 12, as depicted in FIGS. 10(a) and 10(b).

[0072] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made with departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

What is claimed is:

1. A semiconducting material comprising:
   a substrate;
   a first layered stack atop said substrate, said first layered stack comprising a first Si-containing portion of said substrate, a compressive layer atop said first Si-containing layer portion of said substrate, and a first semiconducting layer atop said compressive layer; and
   a second layered stack atop said substrate, second layered stack comprising a second Si-containing portion of said substrate, a tensile layer atop said second Si-containing portion of said substrate, and a second semiconducting layer atop said tensile layer.

2. The semiconducting substrate of claim 1 wherein said substrate is a silicon-on-insulating substrate or a bulk-silicon substrate.

3. The semiconducting substrate of claim 1 wherein said compressive layer comprises SiGe having Ge present in a concentration ranging from about 5% to about 30% by atomic weight percent.

4. The semiconducting substrate of claim 1 wherein said tensile layer comprises silicon doped with carbon, said carbon is present in a concentration ranging from about 1% to 6% by atomic weight percent.

5. The semiconducting substrate of claim 1 wherein said compressive layer elastically transfers tensile stresses to a first semiconducting layer.

6. The semiconducting substrate of claim 1 wherein said tensile layer elastically transfers compressive stresses to said second semiconducting layer.

7. The semiconducting substrate of claim 1 wherein said compressive layer and said tensile layer have a thickness ranging from about 10 nm to about 100 nm.

8. The semiconducting substrate of claim 1 wherein at least one nFET device is formed atop said first layered stack.

9. The semiconducting device of claim 1 wherein at least one pFET device is formed atop said second layered stack.

10. The semiconductor substrate of claim 1 wherein said first layered stack and said second layered stack are separated by an isolation region.

11. A method of forming a semiconducting substrate comprising:
   providing a Si-containing substrate;
   forming a first pad stack atop a first portion of said Si-containing substrate, said first pad stack comprising a compressive layer positioned atop said first portion of said Si-containing substrate, a first semiconducting layer atop said compressive layer and a first etch barrier atop said first semiconducting layer;
   forming a second pad stack atop a second portion of said Si-containing substrate, said second pad stack comprising a tensile layer positioned atop said second portion of said Si-containing substrate, a second semiconducting layer atop said tensile layer, and a second etch barrier atop said second semiconducting layer;
   etching said Si-containing substrate selective to said first etch barrier and said second etch barrier, wherein said compressive layer elastically transfers a tensile strain to said first semiconducting layer and said tensile layer elastically transfers a compressive strain to said second semiconducting layer;
   removing said first etch barrier and said second etch barrier; and
   forming an isolation region between said first pad stack and said second pad stack.

12. The method of claim 11, wherein said compressive layer comprises SiGe.

13. The method of claim 12, wherein SiGe comprises Ge present in a concentration ranging from about 5% to about 30% by atomic weight percent.

14. The method of claim 11, wherein said tensile layer comprises Si:C, wherein said Si:C comprises carbon present in a concentration of less than about 6% by atomic weight percent.

15. The method of claim 12 wherein forming said first pad stack further comprises:
   epitaxially growing SiGe atop said Si-containing substrate, wherein said SiGe is grown to a thickness which is less than a SiGe critical thickness;
   epitaxially growing said first semiconducting layer atop said SiGe, wherein said first semiconducting layer has a thickness which is less than a first semiconducting layer critical thickness; and
depositing said first etch barrier, where said first etch barrier comprises a dielectric.

16. The method of claim 15 wherein said SiGe critical thickness is a dimension at which said SiGe layer is in compression.

17. The method of claim 15 wherein said SiGe critical thickness and said semiconducting layer critical thickness is a maximum dimension under which defects formed within said SiGe and said first semiconducting layer are less than $1.0 \times 10^7$ cm$^{-2}$.

18. The method of claim 14 wherein forming said second pad stack further comprises:

epitaxially growing Si:C atop said Si-containing substrate, wherein said Si:C is grown to a thickness which is less than a Si:C critical thickness;

epitaxially growing said first semiconducting layer atop said Si:C, wherein said first semiconducting layer has a thickness which is less than a first semiconducting layer critical thickness; and

depositing said first etch barrier, wherein said first etch barrier comprises a dielectric.

19. The method of claim 17 wherein said Si:C critical thickness is a dimension at which said Si:C layer is in tension.

20. The method of claim 17 wherein said Si:C critical thickness and said semiconducting layer critical thickness is a maximum dimension under which defects formed within said Si:C layer and said first semiconducting layer are less than $1.0 \times 10^7$ cm$^{-2}$.

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