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(54) **SELF-REFERENCED MATCH-LINE SENSE AMPLIFIER FOR CONTENT ADDRESSABLE MEMORIES**

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G11C 15/00　　　(2006.01)
(52) **U.S. Cl.** **365/49.17**; 365/49.1; 365/189.06; 365/203; 327/51
(58) **Field of Classification Search** 365/49, 365/189.06, 203, 207, 49.1, 49.17; 327/51
See application file for complete search history.

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(57)　　　　**ABSTRACT**

A design structure for designing, manufacturing, or testing a content addressable memory (CAM) device. The CAM device includes a plurality of CAM cells, match-lines (MLs), search lines, and ML sense amplifiers. The ML sense amplifiers are capable of self-calibration to their respective thresholds to reduce effects of random device variation between adjacent sense amplifiers.
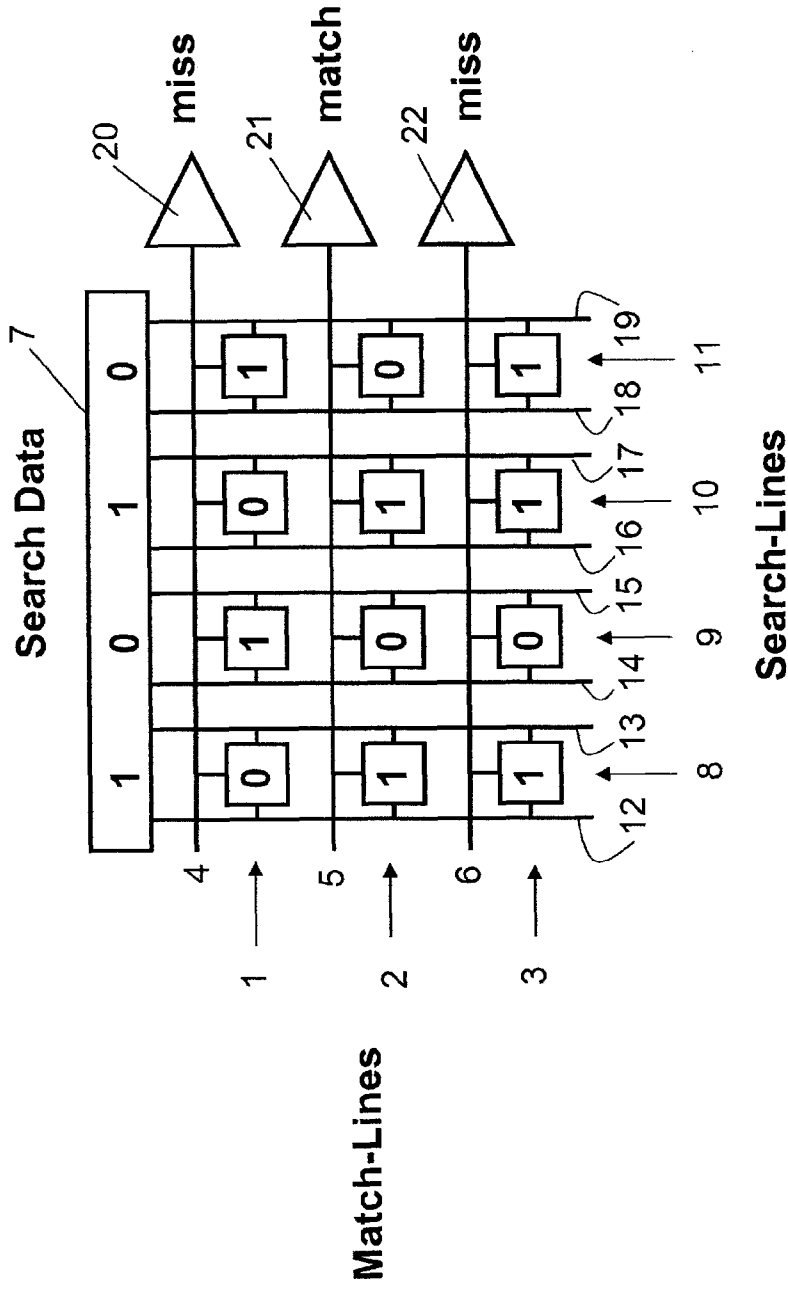
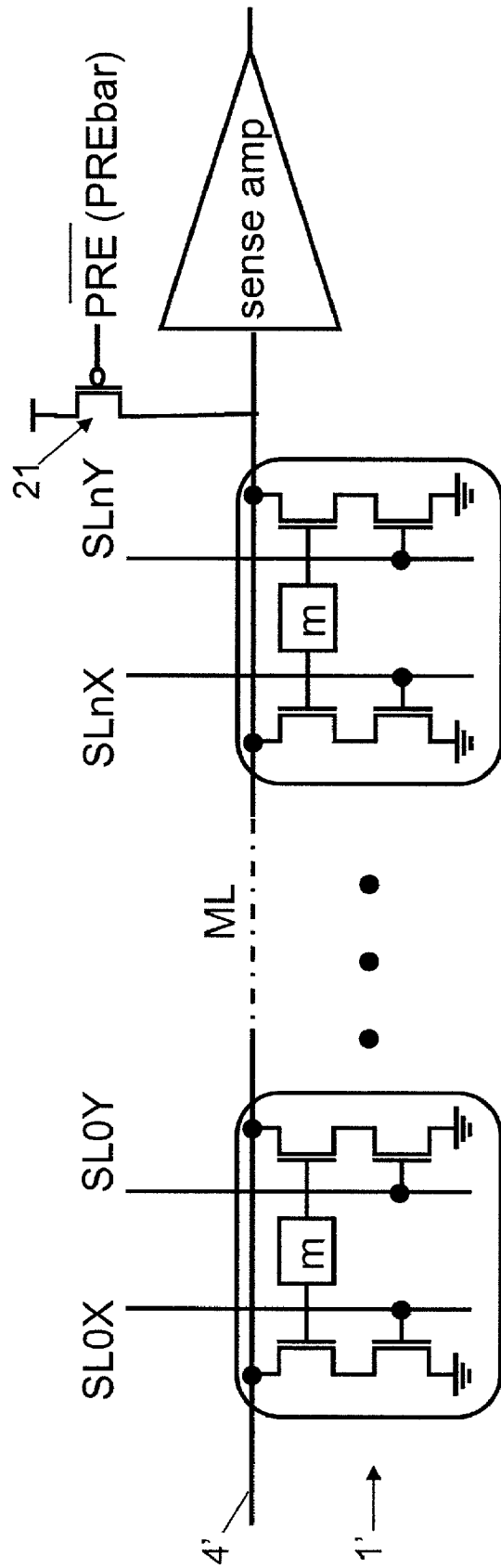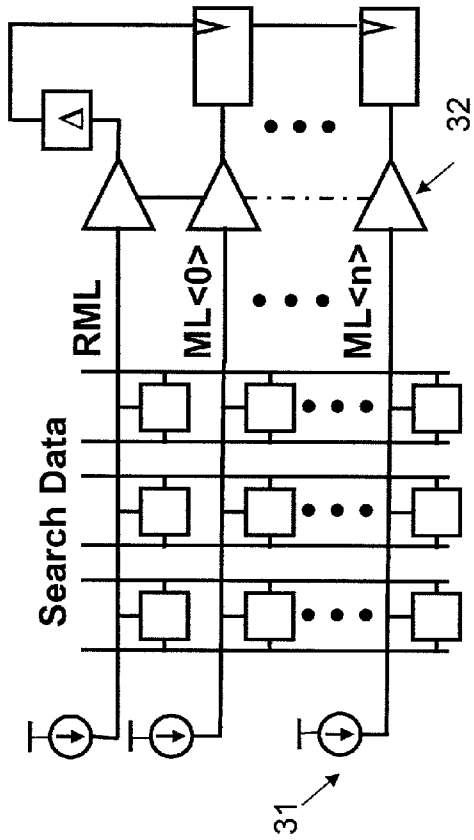**18 Claims, 7 Drawing Sheets**
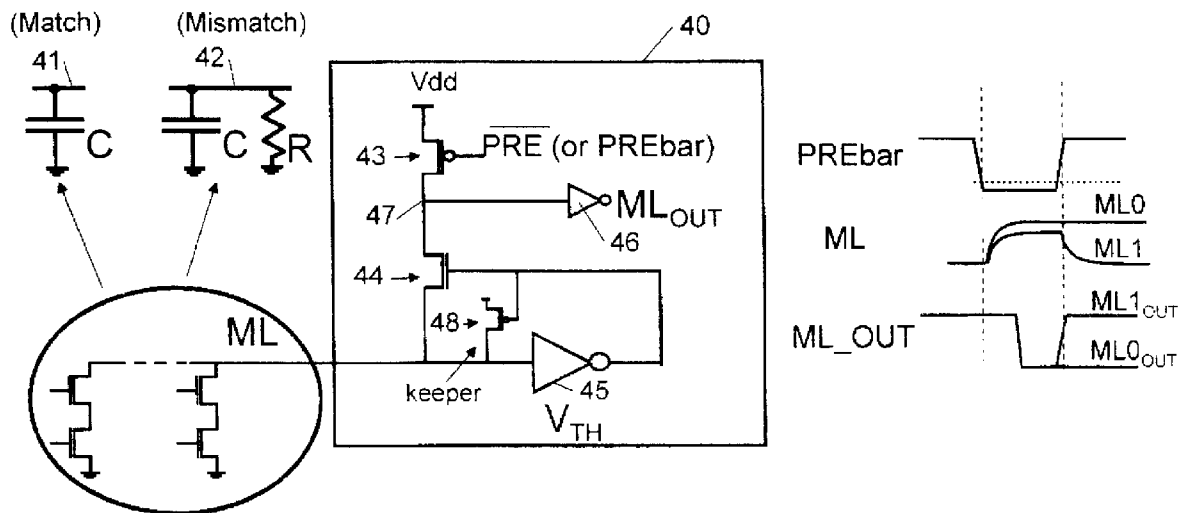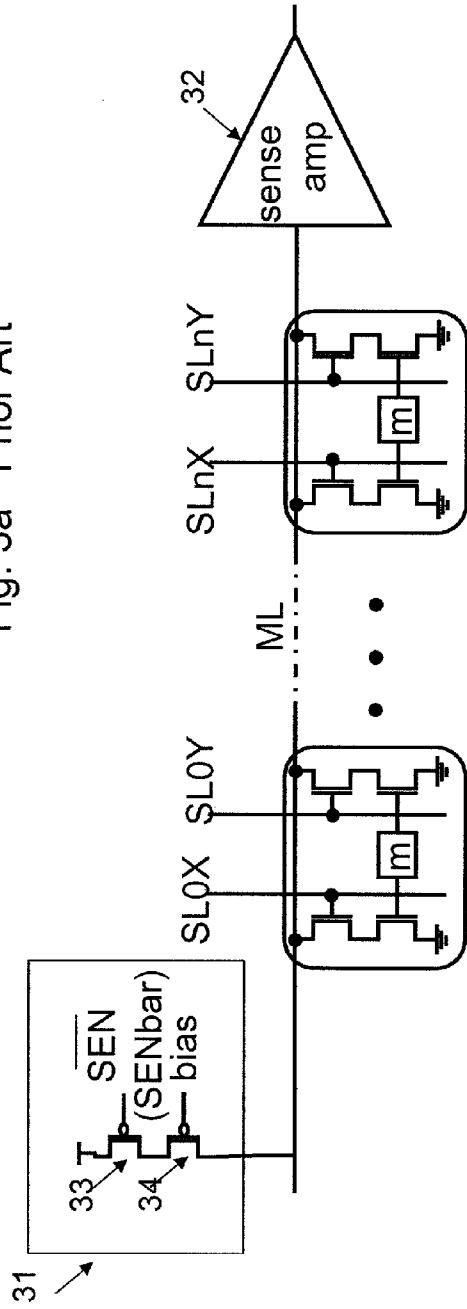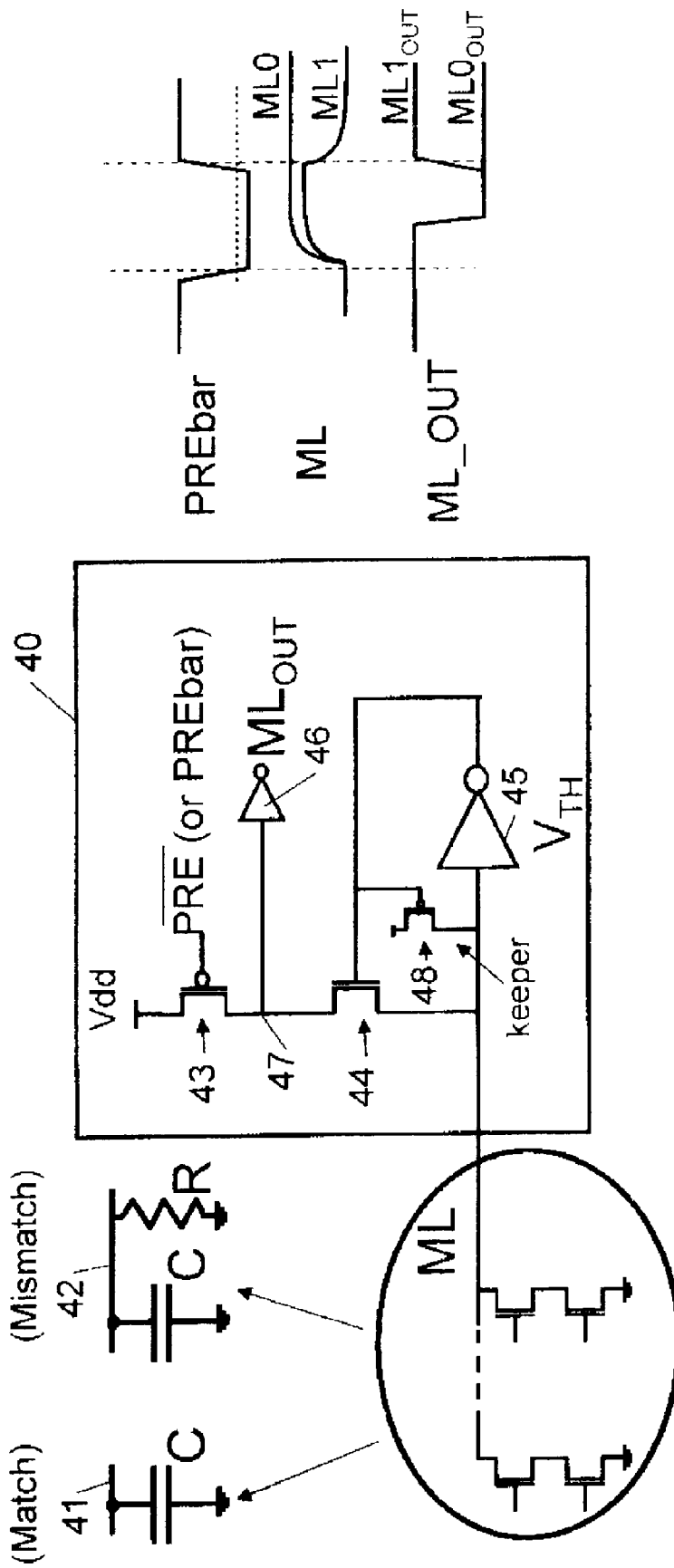
Fig. 1

Prior Art
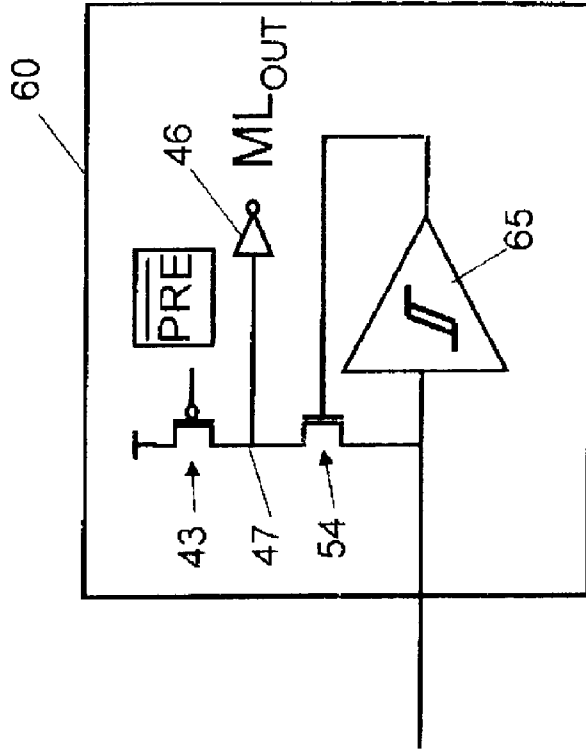
Fig. 2

Prior Art

Fig. 3a Prior Art

Fig. 3b Prior Art

Fig. 4

Fig. 6

Fig. 5

Fig. 7

Design Flow
800

Library
Elements
830

Design
Structure
820

Design
Specifications
840

Netlist
880

Design
Process
810

Characterization
Data
850

Design Rules
870

Verification
Data
860

Test Data
885

Final Design
Structure
890

895
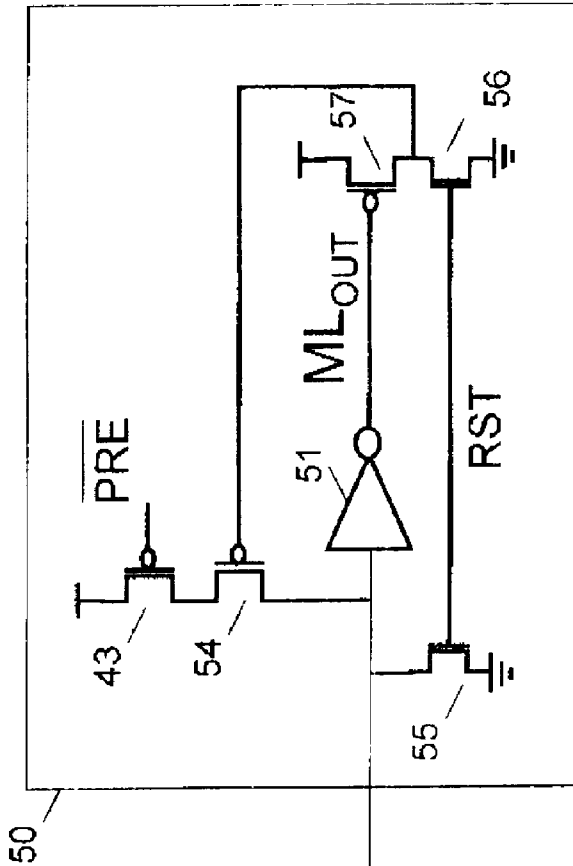
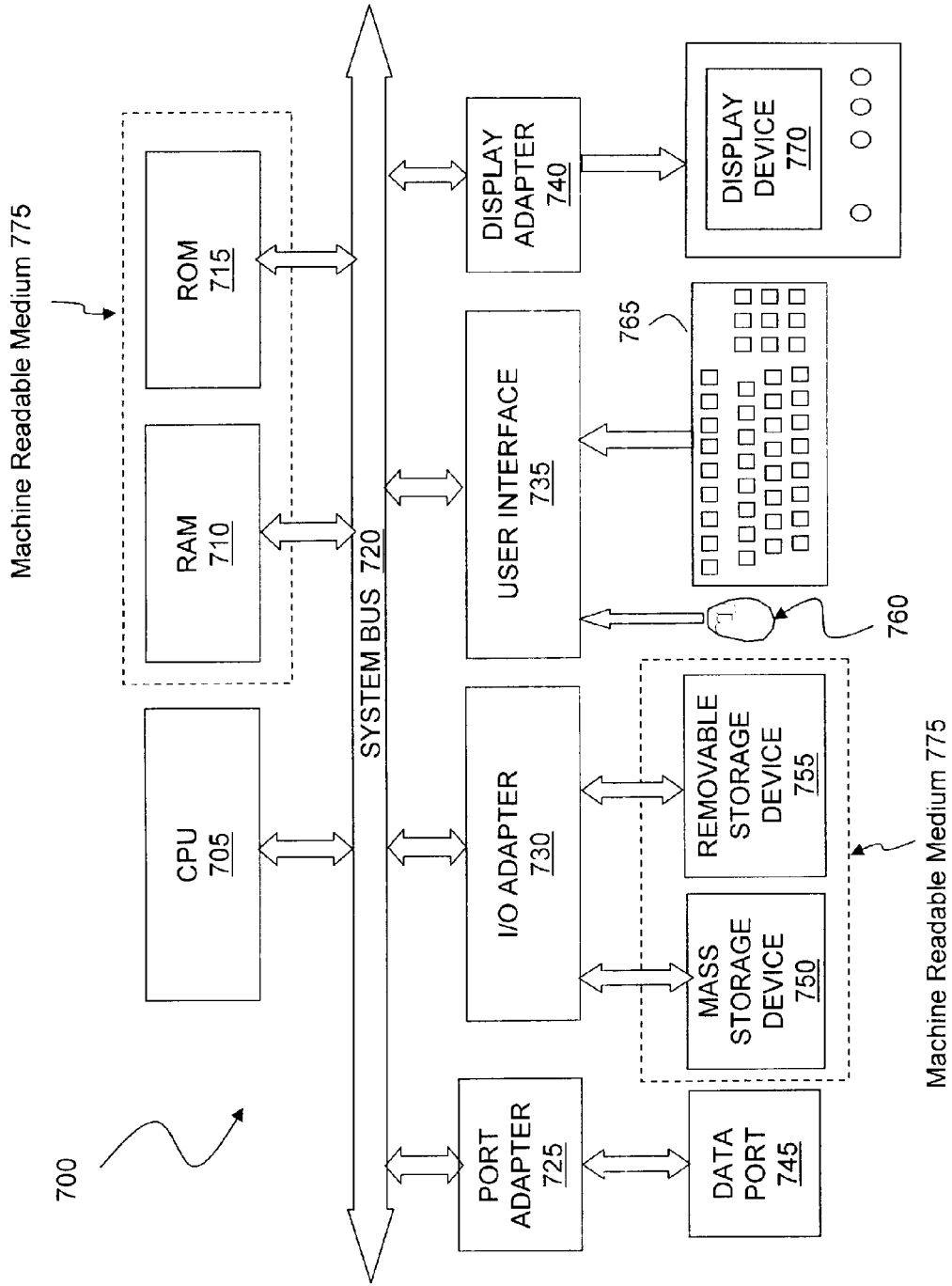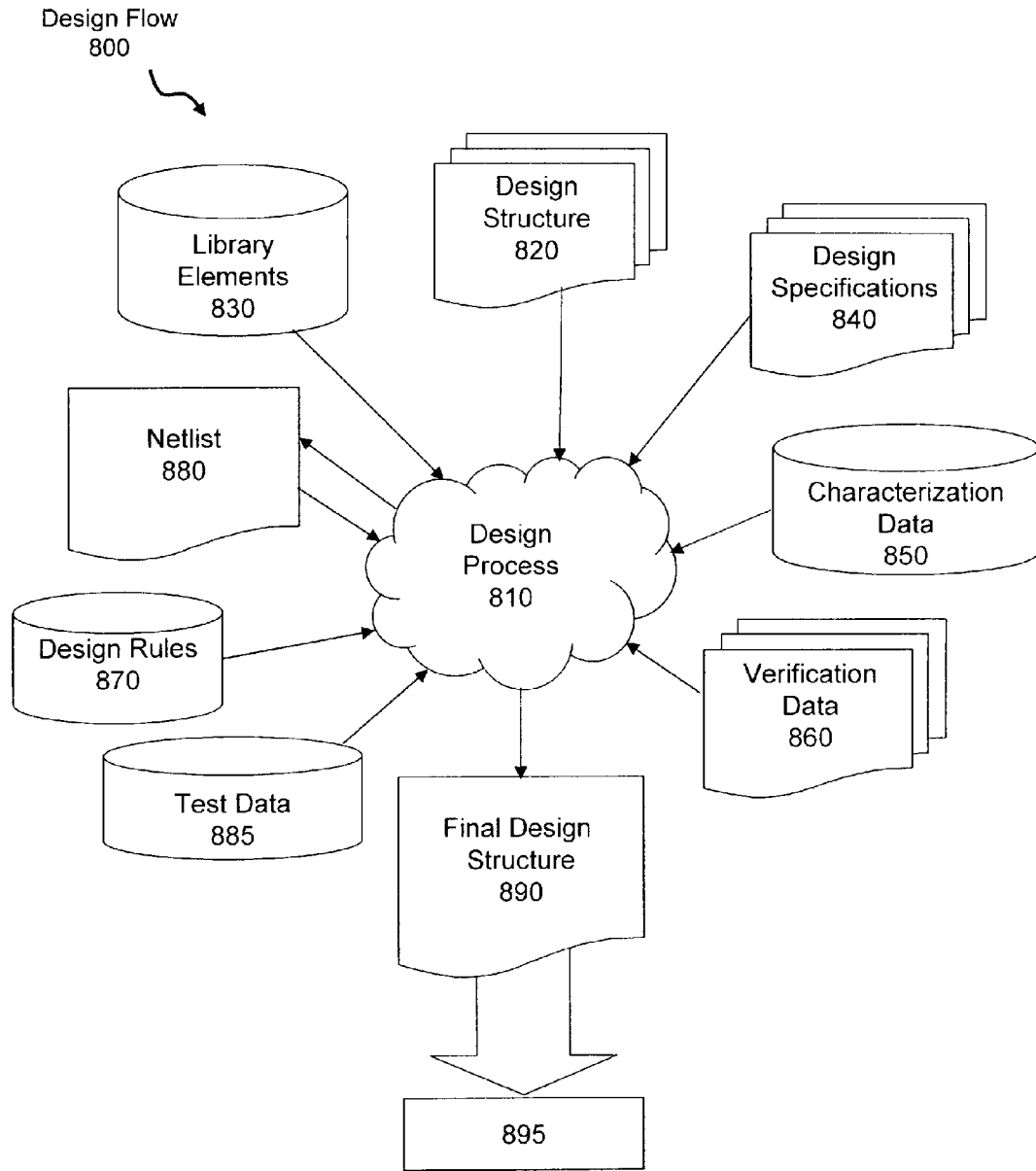*Fig. 8*

SELF-REFERENCED MATCH-LINE SENSE AMPLIFIER FOR CONTENT ADDRESSABLE MEMORIES

CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part of U.S. patent application Ser. No. 11/457,477 filed Jul. 14, 2006 and assigned to the present assignee.

FIELD OF THE INVENTION

The instant invention relates to content addressable memories (CAM), and particularly to a design structure for designing, manufacturing, and/or testing such a CAM and performing a search operations in a CAM.

BACKGROUND DESCRIPTION

An associative memory system called Content Addressable Memory (CAM) has been developed to permit its memory cells to be referenced by their contents. Thus CAM has found use in lookup table implementations such as cache memory subsystems and is now rapidly finding use in networking system applications such as network address translation, and other applications such as pattern recognition, and data compression. CAM's most valuable feature is its ability to perform a fast search operation in which search data is compared with data stored within the CAM. Typically search data is loaded onto search lines and compared with stored words in the CAM. During a search-and-compare operation, the CAM performs a fully parallel search and generates a match or mismatch signal associated with each stored word, indicating whether the search word matches a stored word or not.

To allow this fast parallel comparison between all stored words to a single search word, each CAM word contains dedicated search hardware. Each CAM cell contains additional bit-comparison transistors, in addition to a conventional storage element, which is typically implemented as a Static Random Access Memory (SRAM) cell or a Dynamic Random Access Memory (DRAM) cell. This added circuitry is combined across the word with a match-line (ML) to produce a match or mismatch signal for each CAM word.

Moreover, this search hardware allows the entire contents of the CAM memory to be searched in a single memory cycle.

Thus, in contrast to standard memory (SRAM or DRAM) which would typically require 1 K clock cycles to complete a search of a 1 K words memory, a CAM has the ability to search all entries simultaneously in a single clock cycle.

Unfortunately, as technology scales to submicron geometries, random device variation (RDV) is becoming more prominent. RDV of parameters such as transistor length, transistor width and transistor threshold voltage could be significant even in identically designed neighboring devices. The effects of RDV are especially evident in the design of semiconductor memories. Because most memories rely on sense amplifiers to detect small voltage signals on largely capacitive array lines, RDV in the memory cells as well as sense-amplifier devices can produce incorrect results. To improve reliability, memory designers tune their sensing circuits conservatively, thereby trading off performance in order to maintain a large sensing margin for reliable operation.

In advanced technologies (i.e. 100 nm and smaller gate geometry) RDV is becoming a major bottleneck for improving performance. As device variation increases, timing uncertainty for signal arrival and data capture increases, requiring larger data capture margins, and therefore limiting performance.

Due to its single-ended nature, the ML sensing performed during the CAM search operation is even more sensitive to RDV than the differential sensing used in the SRAM read circuitry. Thus, to maintain reliable operation, most ML sensing schemes employ full-swing sensing which is both slow and power-inefficient.

SUMMARY OF THE INVENTION

An aspect of the invention is a design structure for designing, manufacturing, and/or testing a CAM device that includes a plurality of CAM cells, match-lines, search lines, and match-line sense amplifiers. The match-line sense amplifiers are capable of self-calibration to their respective thresholds to reduce effects of random device variation between adjacent sense amplifiers.

Another aspect of the invention is a process for searching a CAM device having match-lines and sense amplifiers. The process includes precharging the match-lines to thresholds of their respective sense amplifiers.

Another aspect of the invention is a design structure for designing, manufacturing, and/or testing a CAM device that includes elements coupled to ends of match-lines, in which each element has a respective threshold voltage value. Further, the design structure comprising a CAM device includes a device for charging the match-lines to the respective threshold voltage values.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a general architecture for a conventional CAM arrangement;

FIG. 2 illustrates a conventional CAM entry illustrating a ML architecture that can be used to sense a ML that is initially pre-charged high;

FIGS. 3a and 3b illustrate an alternative CAM array architecture and ML arrangement which can be used to sense a ML which is initially precharged low;

FIG. 4 illustrates a self-referenced sense amplifier in accordance with the invention;

FIG. 5 illustrates an alternative arrangement of the self-referenced sense amplifier depicted in FIG. 4;

FIG. 6 illustrates an alternative arrangement of the self-referenced sense amplifier depicted in FIG. 5.

FIG. 7 illustrates a block diagram of a general-purpose computer system which can be used to implement the CAM array architecture and circuit design structure described herein; and

FIG. 8 shows a block diagram of an example design flow used in designing the CAM of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS OF THE INVENTION

The present invention is directed to a design structure for designing, manufacturing, and/or testing a self-referenced matched line sense amplifier, such that the ML sense amplifier benefits from conventional low power ML sensing schemes with significantly reduced susceptibility to RDV. Thus, the invention is directed to a design structure comprising a novel RDV-insensitive self-referenced ML sense amplifier, which provides reliable operation and achieves sub-nanosecond match-times while dissipating less power than a number of currently used methods.

The sense amplifier performs a self-calibration to reduce the timing uncertainty caused by device variation in both the sensed circuitry and the sense amplifier itself. After this calibration, the sense amplifier simply determines whether a Match-Line is matched or mismatched to complete the search.

In a conventional CAM sensing scheme, as shown in FIG. 1, CAM core cells are arranged in horizontal rows, 1, 2, and 3, composed of, e.g., four cells, and each CAM core cell of a respective horizontal row is coupled to MLs 4, 5, and 6. As the number of cells in a row corresponds to the length of the word to be searched, any number of cells can be utilized by those ordinarily skilled in the art without departing from the spirit of the invention. Further, for the sake of easy explanation, only three MLs 4-6 are shown. Again, any number of MLs can be utilized by the ordinarily skilled artisan. Moreover, the CAM core cells are arranged in columns 8, 9, 10, and 11. While only four columns are shown, the number of columns corresponds to the number of bits in the CAM core cell word to be searched, such that any number of columns can be utilized.

Search data 7, i.e., the data word to be searched, is provided for comparison with each word formed in CAM rows 1-3. Parallel search lines 12-19 are coupled to search data 4, and each CAM core cell in a respective column is coupled to two search lines so that each cell corresponding to a data bit of the search data 7 can be searched for a match. Thus, search data 7 is applied to search lines 12-19 in parallel. Search results develop on MLs 4-6 in parallel and are applied to respective search amplifiers 20-22.

Conventional CAM searches have been performed with the MLs precharged high. As shown in FIG. 2, a conventional row 1' of CAM core cells to be searched is shown, and each cell of row 1' is coupled to a ML 4'. Moreover, each CAM core cell, which can be in binary or ternary form, includes a storage element m, e.g., an SRAM or DRAM, and a pair of stacks of nFETs coupled between ML 4' and ground. The upper nFETs of each stack is coupled to storage element m, while the lower nFETs are coupled to the pair of search lines associated with the cell column. For a search operation, search lines are initially set to ground, and the MLs are precharged high to Vdd, when a precharge bar signal (PREbar) is low to turn on pFET 21. To perform the comparison between the search to stored data the signal PREbar is raised high to stop the precharge and the search data is applied on the search lines, causing the results to appear on the MLs. If any bit in the storage elements does not match the respective searched bits of the search data, the precharged ML is pulled to ground through the mismatched nFET stacks, whereas, if all bits match the searched data, the precharged ML stays high. The signals on the MLs are applied to respective sense amplifiers, which differentiates whether the respective ML is at Vdd or ground.

In an alternative conventional CAM search arrangement shown in FIGS. 3a and 3b, the MLs are initially precharged low. The arrangement depicted in FIG. 3a additionally includes an additional row provided as a reference ML RML, which develops at a same time as a full match. As shown in the figure, the sensing amplifier associated with RML is coupled to a latch to establish a search time corresponding to the time to reach the threshold voltage of the sensing amplifier. For a search, the MLs are initially set to ground, instead of Vdd as in FIG. 2, and equal currents are applied to them through a current source shown as 31. For ease of explanation and illustration, FIG. 3b shows a single ML in which current source 31 can be formed by a stack of pFET devices 33 and 34. As illustrated, pFET 33 turns current source 31 "on" and

"off" with the SENbar signal, while pFET 34 acts as a current limiting device to ensure correct differentiation between a match and a mismatch. As the voltage on the MLs increases, matches ramp up faster than mismatches, and the current race stops when RML voltage reaches the threshold voltage of its sense amplifier. At this point, the RML search amplifier generates the LATCH signal to capture all search results and complete the search operation, in which the voltage on all matched MLs would have crossed the threshold of their respective sense amplifiers, while the voltage on the mismatched MLs would have stayed below the threshold of their respective sense-amplifiers. Since the voltage swing on all MLs is reduced from Vdd to about ½ Vdd, and the precharge to ground statistically reduces search line switching activity by 50%, this search scheme significantly reduces power. Moreover, in contrast to the ML configuration depicted in FIG. 2, in the precharge-low ML sensing scheme of FIG. 3b the nFET stacks within the CAM cells are reversed. In particular, the upper nFETs in the CAM cells are coupled to the pair of search lines associated with the cell column, while the lower nFETs are coupled to storage element m.

The sense amplifiers for the above-noted conventional arrangements are very sensitive to variations in PMOS/NMOS skews and RDV which cause large sensing-circuit trip-point variation, which in turn demands large delay for reliable data capture timing and increased sense times. Therefore, in contrast to the noted conventional arrangements, the present invention employs self-referenced ML sense amplifiers to quickly precharge the MLs to the threshold of their respective sense amplifiers, to release-the-precharge, to develop-ML-signal, and finally to sense the developed signal. By precharging each ML to the threshold voltage of its unique sense-amplifier, the invention significantly reduces the timing uncertainty caused by the above-noted skews and large RDV. Moreover, because threshold voltages can vary largely even for neighboring sense-amplifiers, each sense amplifier can be advantageously self-referencing.

As shown in FIG. 4, a self-referenced sense amplifier 40 is coupled to the ML of a CAM to determine the state of the ML. The self-referenced sense amplifier 40 includes a pFET transistor 43 coupled in series to an nFET transistor 44 to connect ML to a voltage source at Vdd. An inverter 45 is coupled to the end of ML, and the output of inverter 45 is fed back to the gate of nFET 44, while the gate of pFET 43 is coupled to PREbar. Moreover, an inverter 46 is coupled to a sense node 47 between pFET 43 and nFET 44 to output the ML determination. Self-referenced sense amplifier 40, pFET transistor 43, nFET transistor 44, inverters 45 and 46, and sense node 47 are represented in a design structure 820 (see FIG. 8), which may be in the form of a data file stored on a computer readable medium and used for designing, manufacturing, and/or testing the CAM device described herein.

Prior to operation, ML is set low, e.g., to ground, and precharge bar PREbar is set high, e.g., to Vdd. In operation, ML is precharged to the threshold (or trigger point) of the inverter 45, and, thereafter, ML sensing occurs. To begin precharging ML from its initial low, PREbar goes low from its initial high, which turns on pFET 43. Because ML is initially set low, the gate of nFET 44 is set high by inverter 45, turning on nFET 44, whereby current flows to begin quickly charging ML to the threshold of inverter 45. When the voltage on ML crosses the threshold of inverter 45, inverter 45 will start discharging the gate of nFET 44 low until nFET 44 turns off. As a result, sense node 47, which was originally coupled to ML through nFET 44, uses the full charge provided by pFET 43 to charge node 47 to Vdd and, cause the output of inverter 46 is discharged low to GND. Precharge bar PREbar is sub-

sequently disabled by a signal from a one-bit miss reference ML (not shown). Moreover, an optional keeper 48 can be coupled between the gate of nFET 44 and ML. Keeper 48 is provided to maintain the precharged value to prevent leakage on ML from being misinterpreted as a mismatch.

According to the invention, a reference ML (RML), such as depicted in FIG. 3a, can be utilized with the embodiment depicted in FIG. 4. Moreover, as shown in the timing diagrams, when PREbar is low, e.g., for 750 psec., the MLs ML0 (match) and ML1 (one-bit miss) begin charging. Because ML1, which corresponds to reference ML (RML) depicted in FIG. 3a, charges up slower than match ML0, it ensures that the PREbar will be low for a sufficient time to precharge all matched MLs to the unique threshold of their respective sense-amplifiers. The one-bit miss reference ML will then stop or disable PREbar and allow all MLs to develop a match or mismatch signal. By precharging all MLs to the threshold of their respective sense-amplifiers, each one-bit mismatched ML will trigger its respective sense amplifier at essentially the same time as the reference ML, thereby reducing the timing uncertainty caused by RDV and improving sense-performance. The one-bit miss reference ML1 is used to generate both the precharge timing and the data capture timing to ensure sufficient time for even the worst case match charge up, as well as fast latch time that ensures reliable data capture.

When matched, ML acts like a simple capacitor (schematically shown as 41) such that both the ML as well as the sense node 47 remain precharged, and the output of inverter 46 remains low. Alternatively, when a mismatch occurs, ML acts like a capacitor in parallel with a resistor (schematically shown as 42), where the resistor models a turned-on pull-down device, to pull down ML. As a result of this pull down, ML will fall below the threshold voltage of inverter 45, such that the output of inverter 45 will flip to a high state and turn on nFET 44. Turning on nFET 44 discharges sense node 47 from its precharged Vdd-level back to the to ML voltage level, causing the output of inverter 46 to go high (see ML1 and ML1OUT timing diagram). To minimize the timing uncertainty inverter 46 is designed to have a higher trip point than inverter 45.

Thus, matches precharge above their sense threshold and remain precharged, while one-bit misses precharge above their sense threshold and then discharge. Since all but largely mismatched MLs are precharged to the thresholds of their respective sense amplifiers, the sensing is fast and all sense-amplifiers trigger at a same time reducing the timing uncertainty caused by RDV. Correspondingly, the sense nodes for matches drops to low and remains there until it is reset, whereas the sense nodes for one-bit misses and mismatches drop to low and then back to high (see timing diagram ML_OUT). Due to the self-reference nature of the sense amplifiers, even though the MLs exhibit different switching times during precharging, the sense-amplifiers trigger at the same time during sensing.

Because inverters have random variation of, e.g., 300-500 mV, at their trigger points and because all MLs are not the same due to, e.g., RDV, the self-referenced sense amplifier of the present invention reduces timing uncertainty by allowing each sense-amplifier to precharge its match line MLs to a unique voltage level relative to its threshold. By doing so, the invention improves timing uncertainty and with it sensing speed.

In an alternative embodiment of the invention as shown in FIG. 5, self-referenced sense amplifier 50 is created using only pFET transistors in its ML precharge path. This alternative embodiment includes a pFET transistor 43 coupled in series to a pFET transistor 54 to connect ML to a voltage

source at Vdd. An inverter 51 is coupled to the end of ML, and the output of inverter 51' is fed to the gate of pFET 57. The source of pFET 57 is connected to Vdd, while its drain is connected back to the gate of pFET transistor 54 and to the drain of nFET 56. The gate of nFET 56 is connected to a signal RST, which is also attached to the gate of nFET 55. The drain of nFET 55 is attached to the ML and its source is attached to Gnd. Precharge pFET 43 is coupled to PREbar. Self-referenced sense amplifier 50, pFET transistor 43, pFET transistor 54, inverter 51, pFET 57, nFET 56, and nFET 55 are represented in a design structure 820 (see FIG. 8), which may be in the form of a data file stored on a computer readable medium and used for designing, manufacturing, and/or testing the CAM device described herein.

Prior to searching in this embodiment, the ML and the gate of pFET 54 are discharged low by pulsing RST high. PREbar is then pulsed low for a period of time to allow adequate precharging of the MLs. As the MLs pass the threshold of their respective inverters, and in the illustrated embodiment, as the ML passes the threshold of inverter 51, pFET 57 is turned 'on' to begin charging the gate of pFET 54 to Vdd. This causes pFET 54 to turn off and stop the precharging of the MLs. At this point, matches will remain at the precharged voltage, while mismatches will discharge to Gnd, thereby switching ML_{OUT} back high. As a result of this configuration, ML can be charged to slightly higher than the threshold of a single inverter (sense amplifier), thereby improving noise immunity.

A self-referenced sense amplifier 60 shown in FIG. 6 depicts a further embodiment of the invention. Like the alternative embodiment depicted in FIG. 5, self-referenced sense amplifier 60 includes a pFET transistor 43 coupled in series to an nFET transistor 54 to connect ML to a voltage source at Vdd. A Schmitt-trigger 65 is coupled to the end of ML, and the output of Schmitt-trigger 65 is fed back to the gate of nFET 54, while the gate of pFET 43 is coupled to PREbar. Moreover, an inverter 46 is coupled to a sense node 47 between pFET 43 and nFET 54 to output the ML determination. As a result of this Schmitt-trigger controlled arrangement, the ML sense amplifier can have a precharge point of the ML higher than the sense node, allowing additional noise margin during sense time.

Accordingly, the self-referenced sense amplifier of the present invention improves tolerance to RDV. Even with a large process variation in critical devices in both across wafer and across chip, the self-referenced sense amplifier provides fast and reliable sensing.

As the invention senses a pull-down on a highly capacitive line, it is contemplated that, without departing from the scope and spirit of the invention, the invention can be used in Read-Only Memories (ROM) multi-port SRAM or single port SRAMs which use an eight-transistor cell as their storage unit) or other RAMs where the pull-down structure is similar to the CAM ML. In general, the invention can be used to sense small resistance on a highly capacitive line in processes with large RDV.

FIG. 7 illustrates a block diagram of a general-purpose computer system which can be used to implement the circuit and circuit design structure described herein. The design structure may be coded as a set of instructions on removable or hard media for use by general-purpose computer. FIG. 7 is a schematic block diagram of a general-purpose computer for practicing the present invention. FIG. 7 shows a computer system 700, which has at least one microprocessor or central processing unit (CPU) 705. CPU 705 is interconnected via a system bus 720 to machine readable media 775, which includes, for example, a random access memory (RAM) 710,

a read-only memory (ROM) **715**, a removable and/or program storage device **755** and a mass data and/or program storage device **750**. An input/output (I/O) adapter **730** connects mass storage device **750** and removable storage device **755** to system bus **720**. A user interface **735** connects a keyboard **765** and a mouse **760** to system bus **720**, and a port adapter **725** connects a data port **745** to system bus **720** and a display adapter **740** connect a display device **770**. ROM **715** contains the basic operating system for computer system **700**. Examples of removable data and/or program storage device **755** include magnetic media such as floppy drives, tape drives, portable flash drives, zip drives, and optical media such as CD ROM or DVD drives. Examples of mass data and/or program storage device **750** include hard disk drives and non-volatile memory such as flash memory. In addition to keyboard **765** and mouse **760**, other user input devices such as trackballs, writing tablets, pressure pads, microphones, light pens and position-sensing screen displays may be connected to user interface **735**. Examples of display device **770** include cathode-ray tubes (CRT) and liquid crystal displays (LCD).

A machine readable computer program may be created by one of skill in the art and stored in computer system **700** or a data and/or any one or more of machine readable medium **775** to simplify the practicing of this invention. In operation, information for the computer program created to run the present invention is loaded on the appropriate removable data and/or program storage device **755**, fed through data port **745** or entered using keyboard **765**. A user controls the program by manipulating functions performed by the computer program and providing other data inputs via any of the above mentioned data input means. Display device **770** provides a means for the user to accurately control the computer program and perform the desired tasks described herein.

FIG. **8** shows a block diagram of an example design flow **800**. Design flow **800** may vary depending on the type of IC being designed. For example, a design flow **800** for building an application specific IC (ASIC) will differ from a design flow **800** for designing a standard component. Design structure **820** is an input to a design process **810** and may come from an IP provider, a core developer, or other design company. Design structure **820** comprises at least one embodiment of the CAM device described herein in the form of schematics or HDL, a hardware-description language, (e.g., Verilog, VHDL, C, etc.). Design structure **820** may be on one or more of machine readable medium **775** as shown in FIG. **7**. For example, design structure **820** may be a text file or a graphical representation of the CAM device. Design process **810** synthesizes (or translates) the CAM device into a netlist **880**, where netlist **880** is, for example, a list of wires, transistors, logic gates, control circuits, I/O, models, etc. and describes the connections to other elements and circuits in an integrated circuit design and recorded on at least one of machine readable medium **775**.

Design process **810** includes using a variety of inputs; for example, inputs from library elements **830** which may house a set of commonly used elements, circuits, and devices, including models, layouts, and symbolic representations, for a given manufacturing technology (e.g. different technology nodes, 32 nm, 45 nm, 90 nm, etc.), design specifications **840**, characterization data **850**, verification data **860**, design rules **870**, and test data files **885**, which may include test patterns and other testing information. Design process **810** further includes, for example, standard circuit design processes such as timing analysis, verification tools, design rule checkers, place and route tools, etc. One of ordinary skill in the art of integrated circuit design can appreciate the extent of possible

electronic design automation tools and applications used in design process **810** without deviating from the scope and spirit of the invention.

Ultimately design process **810** translates the CAM device, along with the rest of the integrated circuit design (if applicable), into a final design structure **890** (e.g., information stored in a GDS storage medium). Final design structure **890** may comprise information such as, for example, test data files, design content files, manufacturing data, layout parameters, wires, levels of metal, vias, shapes, test data, data for routing through the manufacturing line, and any other data required by a semiconductor manufacturer to produce the CAM device described herein. Final design structure **890** may then proceed to a stage **895** of design flow **800**; where stage **895** is, for example, where final design structure **890**: proceeds to tape-out, is released to manufacturing, is sent to another design house or is sent back to the customer.

While the invention has been described in terms of a preferred embodiment, those skilled in the art will recognize that the invention can be practiced with modifications within the spirit and scope of the appended claims.

What is claimed:

1. A design structure embodied in a machine readable medium used in a design process, the design structure comprising a content addressable memory (CAM) device, the (CAM) device comprising:
   a plurality of CAM cells;
   match-lines;
   search lines; and
   match-line sense amplifiers; and
   keepers arranged within the match-line sense amplifiers to maintain a precharged value on the match-lines,
   wherein the match-line sense amplifiers are capable of self-calibration to their respective thresholds to reduce effects of random device variation between adjacent sense amplifiers.

2. The design structure in accordance with claim **1**, further comprising switch units coupled to the match-lines to precharge each match-line to a threshold of its associated match-line sense amplifiers.

3. The design structure in accordance with claim **2**, wherein the switching units comprise at least two FETs arranged in series between a supply voltage and the match-lines.

4. The design structure in accordance with claim **3**, further comprising inverters coupled to sense nodes located between the at least two FETs of the switching units, wherein outputs of the inverters are indicative of one of a match or a mismatch.

5. The design structure in accordance with claim **4**, wherein the FETs located between the sense nodes and the match-lines are turned off and on by elements coupled to an end of the match-line.

6. The design structure in accordance with claim **2**, wherein the thresholds correspond to thresholds of an element coupled to an end of the match-line.

7. The design structure in accordance with claim **6**, wherein the element comprises at least one inverter.

8. The design structure of claim **1**, wherein the design structure resides on a GDS storage medium.

9. A final design structure instantiated in a machine readable medium for designing, manufacturing, or testing a circuit, the final design structure comprising:
   at least one content addressable memory (CAM) device that includes:
   a plurality of CAM cells;
   match-lines;
   search lines;
   match-line sense amplifiers; and

keepers arranged within the match-line sense amplifiers to prevent leakage on the match-lines from being mis-interpreted as a mismatch,

    wherein the match-line sense amplifiers are capable of self-calibration to their respective thresholds to reduce effects of random device variation between adjacent sense amplifiers.

10. The final design structure in accordance with claim **9**, further comprising switch units coupled to the match-lines to precharge each match-line to a threshold of its associated match-line sense amplifiers.

11. The final design structure in accordance with claim **10**, wherein the switching units comprise at least two FETs arranged in series between a supply voltage and the match-lines.

12. The final design structure in accordance with claim **11**, further comprising inverters coupled to sense nodes located between the at least two FETs of the switching units, wherein outputs of the inverters are indicative of one of a match or a mismatch.

13. The final design structure in accordance with claim **12**, wherein the FETs located between the sense nodes and the match-lines are turned off and on by elements coupled to an end of the match-line.

14. The final design structure in accordance with claim **10**, wherein the thresholds correspond to thresholds of an element coupled to an end of the match-line.

15. The final design structure in accordance with claim **14**, wherein the element comprises at least one inverter.

16. The final design structure of claim **9**, wherein the final design structure comprises a netlist, which describes the circuit.

17. The final design structure of claim **9**, wherein the final design structure resides on a GDS storage medium.

18. The final design structure of claim **9**, wherein the final design structure includes test data files, characterization data, verification data, or design specifications.

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