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(71) Applicant: **ALLIANCE FOR SUSTAINABLE ENGERY, LLC** [US/US]; c/o National Renewable Energy Laboratory, 15013 Denver West Parkway, Golden, Colorado 80401 (US).

(72) Inventors; and
(71) Applicants : **ALBERI, Kirstin** [US/US]; c/o National Renewable Energy Laboratory, 15013 Denver West Parkway, Golden, Colorado 80401 (US). **MASCARENHAS, Angelo** [US/US]; c/o National Renewable Energy Laboratory, 15013 Denver West Parkway, Golden, Colorado 80401 (US).

(74) Agents: **OWENS, W. LaNelle** et al.; c/o National Renewable Energy Laboratory, 15013 Denver West Parkway, Golden, Colorado 80401 (US).

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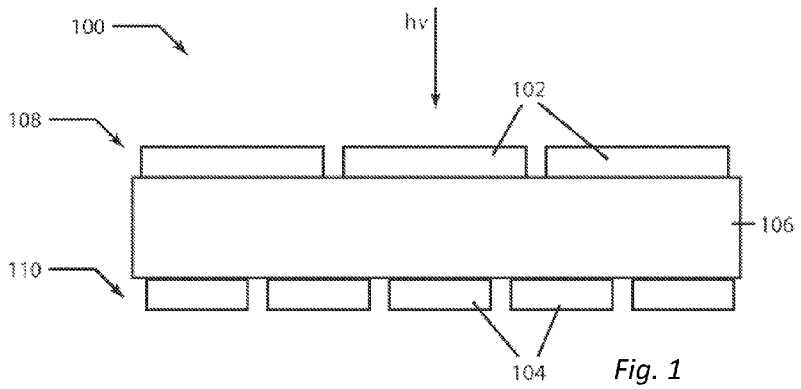

Fig. 1

(57) Abstract: Voltage-matched monolithic thin film multijunction solar cell and methods of producing cells having a first pn junction with a first band-gap energy, a second pn junction with a second band-gap energy and an insulating layer between the first and second pn junctions. The voltage-matched monolithic thin film multijunction solar cells further include a parallel connection between the first and second pn junctions to form a two-terminal photonic device.

MONOLITHIC TANDEM VOLTAGE-MATCHED MULTIJUNCTION SOLAR CELLS

CONTRACTUAL ORIGIN

[0001] The United States Government has rights in this invention under Contract No. DE-AC36-08GO28308 between the United States Department of Energy and the Alliance for Sustainable Energy, LLC, the manager and operator of the National Renewable Energy Laboratory.

BACKGROUND

[0002] In general, semiconductor-based photonic devices, such as photovoltaic cells (PV cells) include a junction formed between p-type and n-type conductivity regions in a semiconductor body. These conductivity regions generate a voltage potential and/or a current across the junction when electron-hole pairs are created in the semiconductor body in response to photons impinging upon the photovoltaic cell. When a load is connected between the p-type and n-type conductivity regions, an electric current will flow, thus producing power. PV cells therefore provide power from a renewable source, which is an attractive alternative to non-renewable energy sources.

[0003] The power conversion efficiency of a PV cell consisting of a single pn junction, referred to as a single junction solar cell, depends on the voltage that can be generated by the pn junction and the ability of the semiconductor(s) comprising the pn junction to absorb a significant portion of the solar spectrum. A semiconductor with a relatively larger bandgap energy can generate a large voltage, but photons having energies less than the bandgap energy are not absorbed by the semiconductor, and the generated current is relatively low. Likewise, a semiconductor with a relatively smaller bandgap energy can absorb a large portion of the solar spectrum and generate a high current, but photon energy in excess of the bandgap energy is lost to thermal energy, and the output voltage of the single junction solar cell is low.

[0004] Combining multiple pn junctions within a PV cell to form what is referred to as a multijunction solar cell can reduce the tradeoffs between voltage and current generation in a single junction solar cell and increase the energy conversion efficiency of the device. In a multijunction solar cell, the pn junctions are typically arranged in a vertically stacked configuration. The pn junctions may be stacked either through physical bonding or

mechanical stacking of individual pn junctions that have been grown on separate substrates, or through monolithic integration of the pn junctions on one substrate. Each pn junction is designed to absorb a portion of the photons in the solar spectrum while passing photons with energy less than the bandgap energy to the pn junction(s) situated below. The use of multiple pn junctions in a multijunction solar cell therefore reduces thermalization losses. Multijunction solar cells therefore typically have efficiencies that are higher than single junction solar cells.

[0005] The manner in which the pn junctions that make up the multijunction solar cell are electrically connected together determines the voltage and current output of the device. A single pn junction solar cell can be partitioned by subdividing it into multiple units of individual PV cells arranged laterally, referred to as sub-cells. If the sub-cells are electrically connected in series, their voltages add, and the lowest current-producing sub-cell determines the overall current output of the device. If the sub-cells are electrically connected in parallel, the currents of each of the sub-cells add, and the voltage will be limited to an intermediate voltage between the highest and lowest values produced by any of the sub-cells. Multijunction solar cells may utilize one or both of these electrical connection configurations.

[0006] Conventional multijunction solar cells are configured such that vertically-stacked pn junctions are connected in series. These devices are typically referred to as current-matched multijunction solar cells because the individual pn junctions are usually designed to have the same current output. In a monolithically integrated device, the electrical connections between adjacent pn junctions are made with a tunnel junction. The tunnel junction is an ultrathin pn junction composed of heavily doped high bandgap energy p-type conductivity and n-type conductivity regions (heavily doped being defined herein as dopant concentrations of greater than about 10^{18} cm^{-3}). From a manufacturing standpoint, tunnel junctions present a convenient way to "hard-wire" connections between vertically-stacked pn junctions, but achieving adequately high doping concentrations is difficult or impossible in many semiconductor materials. This is particularly true for many thin film semiconductors that are used in polycrystalline single junction and multijunction solar cells.

[0007] Voltage-matched multijunction solar cell designs can circumvent some of the limitations of current-matched designs. Variations in the solar spectrum throughout the day can have a large impact on the current that is output by individual pn junctions, but spectral variations will have a much smaller impact on the voltage output. Therefore, the performance of voltage-matched multijunction solar cells suffers less from diurnal spectral variations than current-matched multijunction solar cells. Moreover, tunnel junctions are not

required between vertically-stacked pn junctions in a voltage matched design. This is advantageous when designing multijunction solar cells utilizing semiconductors in which it is difficult to achieve heavily doped ultrathin layers. The primary disadvantage of voltage-matched multijunction solar cells, however, is the need for more complex intra-cell electrical connections. Sub-cells formed within the same pn-junctions are typically connected in series, forming a sub-cell string, and the strings from the different vertically stacked pn-junctions are then connected in parallel. The number of sub-cells in each of the strings need not necessarily be the same and are chosen so that the voltage outputs of all of the strings match. Isolating and connecting sub-cells in pn junctions that are buried within monolithically-integrated multijunction solar cell stacks is challenging because it usually requires physical removal of material from overlying pn junctions in order to access buried pn junctions. In these cases, fabrication requires multiple etch and growth steps, which can add to the cost of the solar cell module. It also necessarily constrains the geometry and layout of the sub-cells in each pn junction layer.

[0008] Polycrystalline or amorphous thin film solar cells, including cadmium telluride (CdTe), copper indium gallium selenide (sulfide) (CIGS), copper zinc tin sulfide (CZTS), polycrystalline or microcrystalline silicon (Si) and amorphous Si (a-Si) architectures, have many advantages over crystalline Si or III-V solar cell technologies. For example, polycrystalline or amorphous thin film designs feature relatively lower overall material usage as compared to crystalline silicon cells, and the ability to fabricate cells on large area glass substrates with atmospheric deposition techniques reduces manufacturing and module costs. One trade-off is that single junction polycrystalline and/or amorphous designs have comparatively lower conversion efficiencies than their crystalline Si or III-V counterparts.

[0009] Multijunction solar cell designs incorporating thin film materials would capitalize on inexpensive processing costs while providing an avenue to increased efficiencies over single junction polycrystalline or amorphous thin film solar cells. Thin film solar cell designs featuring monolithically integrated structures in which the individual vertically stacked pn junctions are connected in series require that the output of these individual pn junctions be substantially current matched. As noted above, this requirement necessitates that tunnel junctions are formed between the monolithically grown vertically stacked pn junctions to facilitate current flow. However, difficulty in achieving heavily doped ultrathin layers in thin film materials impedes the formation of low resistance tunnel junctions making the production of thin film current matched solar cells problematic.

Furthermore, the complexity of processing steps required by known prior-art voltage matched approaches (whether monolithic or mechanically stacked) makes known voltage matched solar cell technologies costly and thus unattractive.

[0010] The embodiments disclosed herein are intended to overcome one or more of the limitations described above. The foregoing examples of the related art and limitations related therewith are intended to be illustrative and not exclusive. Other limitations of the related art will become apparent to those of skill in the art upon a reading of the specification and a study of the drawings.

SUMMARY

[0011] The following embodiments and aspects thereof are described and illustrated in conjunction with systems, tools and methods which are meant to be exemplary and illustrative, not limiting in scope. In various embodiments, one or more of the above-described problems have been reduced or eliminated, while other embodiments are directed to other improvements.

[0012] One embodiment includes a voltage-matched multijunction solar cell having a transparent substrate, a first crystalline, polycrystalline or amorphous pn junction in contact with a first surface of the substrate and a second crystalline, polycrystalline or amorphous pn junction in contact with a second surface of the substrate opposite the first surface. In this embodiment, the first pn junction and the second pn junction are connected in parallel to form a two-terminal photonic device. The tandem voltage-matched solar cell may include front contacts and back contacts associated with each pn junction accessible from the surface of each pn junction opposite the transparent substrate. The contacts may be implemented with a transparent conducting oxide, a metal or by other means. The transparent substrate may consist of but is not limited to a glass substrate. The crystalline, polycrystalline or amorphous pn junctions may comprise at least one of; CIGS, CZTS, a-Si, polycrystalline Si, microcrystalline Si, CdTe, or CdTe alloyed with Zn, Se or S. The tandem voltage-matched thin film multijunction solar cell may also include a first string of serially connected sub-cells defined within the first crystalline, polycrystalline or amorphous pn junction voltage matched to a second string of serially connected sub-cells defined within the second crystalline, polycrystalline or amorphous pn junction.

[0013] An alternative embodiment comprises a voltage-matched thin film multijunction solar cell having a bottom pn junction formed from a doped Si, Ge or GaAs

wafer, interdigitated p-type and n-type back contacts associated with the bottom pn junction and an insulating layer in contact with the bottom cell, opposite the back contacts. The voltage-matched thin film multijunction solar cell also includes an upper pn junction, a front contact and a back contact wherein the upper pn junction is separated from the bottom pn junction by an insulating layer and wherein the bottom pn junction and the upper pn junction are connected in parallel to form a two-terminal photonic device. In this embodiment, the front and back contacts associated with the upper pn junction are accessible from the front surface of the top cell and may comprise a transparent conducting layer, for example, transparent conducting oxide layers or a metal grid layer. In selected embodiments, the upper pn junction is a crystalline, polycrystalline or amorphous thin film upper junction. The crystalline, polycrystalline or amorphous upper pn junction may comprise layers of at least one of; CIGS, CZTS, a-Si, polycrystalline Si, microcrystalline Si, CdTe, or CdTe alloyed with Zn, Se or S. The bottom pn junction may further comprise a textured surface.

[0014] Alternative embodiments include methods of fabricating the solar cells disclosed herein.

[0015] In addition to the exemplary aspects and embodiments described above, further aspects and embodiments will become apparent by reference to the drawings and by study of the following descriptions.

BRIEF DESCRIPTION OF THE DETAILED DRAWINGS

[0016] Exemplary embodiments are illustrated in referenced figures of the drawings. It is intended that the embodiments and figures disclosed herein are to be considered illustrative rather than limiting.

[0017] Fig. 1 is a simplified schematic illustration of a tandem voltage-matched solar cell as disclosed herein;

[0018] Fig. 2 is a schematic illustration of the electrical connections between the sub-cells illustrated in Fig. 1;

[0019] Fig. 3 is a schematic illustration of a tandem voltage-matched solar cell as disclosed here;

[0020] Fig. 4 is a schematic illustration of a tandem voltage-matched solar cell as disclosed herein;

DESCRIPTION

[0021] Unless otherwise indicated, all numbers expressing quantities of ingredients, dimensions, reaction conditions and so forth used in the specification and claims are to be understood as being modified in all instances by the term "about."

[0022] In this application and the claims, the use of the singular includes the plural unless specifically stated otherwise. In addition, use of "or" means "and/or" unless stated otherwise. Moreover, the use of the term "including," as well as other forms, such as "includes" and "included," is not limiting. Also, terms such as "element" or "component" encompass both elements and components comprising one unit and elements and components that comprise more than one unit unless specifically stated otherwise. A material may be described herein as being "single crystalline," "multicrystalline" or "polycrystalline." Single crystalline very specifically means an ingot, wafer or epilayer that is truly a single crystal, with no grain boundaries. "Crystalline" is a more general term for a substantially crystalline material which can have grain boundaries. "Multicrystalline" refers to a crystalline material with a small number of large crystalline grains. "Polycrystalline" refers to crystalline material comprised of a large number of small crystalline grains. The orientation of individual grains can be arbitrary and the individual grains are separated by grain boundaries. The term single crystalline does not mean absolutely defect free. Single crystalline material will have defects and/or dislocations. Certain abbreviations may be used herein with respect to the description of semiconductor alloys. These abbreviations shall not be construed as limiting the scope of the disclosure or claims. For example, the form "InGaAlN" is a common abbreviation to improve readability in technical manuscripts. Abbreviated forms such as "InGaAlN" are defined as equivalent to an expanded form, for example; "$In_xGa_yAl_{1-x-y}N$".

[0023] Known monolithically-integrated voltage-matched multijunction solar cells typically consist of a platform that includes many pn junctions vertically stacked on top of a common substrate. Access to underlying pn junctions for sub-cell isolation and contact formation therefore often occurs in a top-down approach. According to some manufacturing and deposition plans, isolation and metallization steps are designed to occur after each pn junction is deposited or added. According to other fabrication methods, all of the layers are first deposited or added, and trenches are etched through one or more upper pn junctions in order to access underlying layers and pn junctions. These approaches necessarily require a number of intricate processing steps that are costly. These approaches also can introduce

limitations in the geometrical configuration of the sub-cells in each pn junction and the way that the sub-cells are electrically connected.

[0024] As noted above, many multijunction solar cells are designed as monolithically integrated structures in which the individual pn junctions are connected in series and are current matched. This strategy requires that heavily doped tunnel junctions be formed between the pn junctions to facilitate current flow. However, difficulty in achieving heavily doped ultrathin layers in thin film materials impedes the formation of low resistance tunnel junctions if thin film pn junctions are included in a current matched vertical stack. One way to overcome this problem is to fabricate the multijunction solar cell in a voltage-matched configuration, for which parallel connections are made between the sub-cell strings that lie in different pn junctions. No tunnel junctions are needed, and the multijunction solar cells, typically fabricated with the individual pn junctions having selected bandgaps as noted herein, exhibit a greater insensitivity to spectral variations over the course of the day. In addition, the additive voltages within a subcell string enables lower current densities at a given power output. In concentrator applications, this feature is of special value as it facilitates lower sheet current densities in the contact layers and therefore lower I^2R losses.

[0025] The various embodiments more specifically disclosed herein concern the design and fabrication of monolithically integrated multijunction solar cells in which strings of serially connected sub-cells having approximately equal output voltages are fabricated from two or more vertically stacked pn junctions which are connected in parallel. Fig. 1 illustrates one possible embodiment 100 consistent with the principles disclosed herein. First and second pn junctions 102 and 104 respectively are separated by an electrically insulating transparent layer 106. The pn junctions each consist of n-type and p-type conductivity regions and the electrical junction between them. One region (p-type or n-type) is referred to as the emitter, and the other region (n-type or p-type) is referred to as the absorber. The materials for the pn junctions are chosen such that the bandgap energy of the semiconductor(s) comprising the first pn junction 102 is greater than the bandgap energy of the semiconductor(s) comprising the second pn junction 104. The pn junction 102 is operationally positioned to face the sun and is therefore alternatively referred to as the "upper," "front" or "top" junction herein. The bandgap energy of the material comprising the insulating layer 106 is also greater than that of the pn junction 104 and is equal to or greater than that of pn junction 102. Therefore, photons with energies less than the bandgap energy of the pn junction 102 pass through the pn junction 102 and insulating layer 106 to pn junction 104. In the device design of Fig. 1, one set of serially electrically connected sub-cell

strings 108 is comprised of sub-cells fabricated from pn junction 102 and the other set of serially electrically connected sub-cell strings 110 is comprised of sub-cells fabricated from pn junction 104. Because the sub-cell voltage is a function of the bandgap energy of the semiconductor(s) comprising the pn junction, the number of serially connected sub-cells in each string is chosen such that the sum of sub-cell voltages in all of the strings in each pn junction is approximately equal.

[0026] The serial electrical connections among sub-cells may be made in the following manner. All electrical connections within the sub-cell strings 108 in the top pn junction 102 are fabricated from the top side of the device. All electrical connections of the sub-cell strings 110 in the bottom pn junction 104 are fabricated from the backside of the device. The top sub-cell strings and bottom sub-cell strings are then connected in parallel to form a two terminal device. The general configuration of the electrical connections of the sub-cells depicted in Fig. 1 is illustrated schematically in Fig. 2, where the diodes 202 and 204 represent sub-cells in junctions 102 and 104 respectively. The precise sub-cell layout, electrical contact arrangement and fabrication processes will vary depending on the specific configuration and materials used in the monolithic tandem voltage-matched solar cell 100. The pn junctions may be fabricated from the substrate material, or grown on the substrate, or grown on a different substrate and subsequently transferred to the substrate used for the final monolithic tandem voltage-matched solar cell 100. Substrates may include, but are not limited to, a semiconductor wafer, glass or another optically transparent material. Processing steps may include, but are not limited to, sub-cell isolation through chemical etching, laser scribing or mechanical scribing, material removal to expose and make electrical contact to a buried contact layer and patterning electrically conducting and electrically insulating layers. The electrically conducting layers may consist of a metal, a transparent conducting oxide or other conducting material, among other choices. The insulating layers may consist of an un-doped semiconductor, oxide, nitride or other materials with high electrical resistance. High resistivity or isolating diodes can also be used for electrical isolation of the two stacked pn junctions. These insulating layers need to be transparent to light.

[0027] There are several benefits to the general monolithic tandem voltage-matched solar cell design 100 presented in Fig. 1. One advantage is that the formation or interconnection of sub-cell strings within one pn junction layer can occur independently of the formation or interconnection of sub-cell strings within the other pn junction layer. No material removal from the top pn junction 102 is needed to access the underlying pn junction layer 104 for processing. Additionally, the geometric configuration of sub-cells fabricated

within the top pn junction layer 102 is not dependent on the geometric configuration of the sub-cells fabricated within the bottom pn junction layer 104 or vice versa. Many single junction solar cells are also already fabricated such that all of the electrical contacts are made either from the front or from the back of the device. This is true of many thin film single junction solar cells grown on glass in a substrate or superstrate configuration as well as Si wafer-based single junction solar cells fabricated with all back or interdigitated back contacts. The present monolithic tandem voltage-matched solar cell design approach allows for the use of established processing routines with very little alteration.

[0028] Another embodiment of a voltage-matched monolithic solar cell is shown in Fig. 3. The Fig. 3 embodiment includes a monolithic tandem voltage-matched solar cell 300 which can be fabricated from a polycrystalline or amorphous thin film pn junction, such as CIGS, CZTS, a-Si, polycrystalline Si, microcrystalline Si, CdTe, or CdTe alloyed with Zn, Se or S, grown on or attached to a Si wafer-based pn junction. Strings of sub-cells 306 are formed in the lightly p-type (or n-type) doped Si wafer 304 using an all back or interdigitated back contact configuration, in which all contacts are made on the back side of the Si wafer 304. For example, heavily n-type doped regions (or heavily p-type doped regions) 308 are patterned onto the backside of the Si wafer to form the emitter regions. Electrical connection to the lightly p-type doped (or lightly n-type doped) Si absorber region may also be facilitated though the patterning of local regions 310 of heavy p-type (or n-type) doping on the backside of the Si wafer as well. Doping of regions 308 and 310 may be achieved through a number of approaches including, but not limited to, dopant diffusion from Si inks, pastes or liquid dopant sources, ion implantation or amorphous Si deposition. The heavily doped regions 308 and 310 are not restricted to any particular shape or configuration.

[0029] Metal contacts 312 and 314 are formed in contact with the doped regions 308 and 310, respectively. Laser scribing, among other options, may be used to carry out sub-cell isolation. Texturing one or both sides of the Si wafer may be implemented to improve light absorption in the Si sub-cells. A heavily doped layer 316 with the same conductivity type as the lightly doped Si wafer may also be included on the top side of the Si wafer in order to reduce carrier recombination at that interface. This may also be achieved by processes including, but not limited to, dopant diffusion from Si inks, pastes or liquid dopant sources, or ion implantation, or amorphous Si deposition.

[0030] Electrical isolation of the bottom Si and the upper polycrystalline or amorphous sub-cell strings is achieved by forming a transparent electrically insulating layer 318 on top of the Si wafer. This layer may be composed of an oxide or nitride material, an

un-doped semiconductor or another electrically insulating and optically transparent material. The electrical insulating layer 318 may also consist of a high resistivity layer or isolating diode. Alternatively, low index of refraction layers could also be utilized in the electrical insulating layer 318 to enhance photon recycling and/or light trapping.

[0031] The upper polycrystalline or amorphous thin film pn junction is formed on top of the electrically insulating layer 318. The disclosed embodiments can be implemented with any of the existing polycrystalline or amorphous thin film single junction solar cell architectures, and fabrication of the sub-cell strings 302 from the pn junction 322 can follow existing processing methods and routines. For example, the structure may include a back contact layer 320, which may consist of, but not be limited to, a heavily doped semiconductor or a transparent conducting oxide that is transparent to photons with energies less than the bandgap energy of the polycrystalline or amorphous thin film material that comprises the pn junction of the top sub-cells. The contact layer 320 may be isolated into back contacts for individual sub-cells via laser scribing or chemical etching. The pn junction 322 may be formed on top of the back contact layer 320. The pn junction of each sub-cell may then be isolated through laser scribing, chemical etching or other means, such that an opening to the back contact layer 320 is formed. An electrically conducting layer 324 may then be deposited on top of the pn junction 322 to form the top contact as well as the electrical connection to the back contact of the adjacent sub-cell when they are to be serially electrically connected to form sub-cell strings 302. The top contact layer 324 should be deposited or formed from a material that has a higher bandgap than the pn junction 322 so that it is transparent to light absorbed in pn junction 322. For example, this material may include, but is not limited to, transparent conducting oxides. The top contact layer 324 may then be isolated between sub-cells via laser scribing, chemical etching or other means. Metal grids may also be used in conjunction with or in place of the top contact layer 324 to facilitate current collection from the top sub-cells. Metal contacts may also be used to connect adjacent sub-cells within a string. Finally, passive layers 326 may be deposited on top of the device to protect the top sub-cells. A similar layer could also be used on the back side of the device to passivate the bottom sub-cells if needed. Such layers could also incorporate a variety of photon recycling or light trapping configurations. Post-deposition treatments may be applied at any time during the processing to passivate defects in the polycrystalline or amorphous material and improve the overall performance of the sub-cells. The device structure may also include additional layers or features that are conventionally used to facilitate the performance of silicon or thin-film solar cells but are not shown in Fig. 3.

[0032] The use of a Si wafer to fabricate the bottom sub-cells has many advantages including but not limited to the following:

[0033] • An interdigitated back contact (IBC) or other strategy which positions both the n-type contacts 312 and the p-type contacts 314 on the back side of the device (or away from the insulating layer 318) can be used to facilitate contacting and improve light absorption in the Si active layers. Implementation of an IBC can be carried out at low cost using Si ink technologies, which allow screen-printing of patterned n-type and p-type contacts in close proximity to one another. Dopant diffusion from pastes or liquid dopant sources, ion implantation or amorphous Si deposition could also be used to create regions of high doping for the IBC. In the IBC embodiment, isolation of the Si sub-cells can also occur from the back-side of the device, which will reduce the complexity of the isolation processing steps. A heavily doped layer 316 can also be incorporated into the Si sub-cells at the interface with the isolation layer 318 to reduce carrier recombination. Alternatively, transparent conducting layers and/or selective emitter technologies could be used to form the front contact of the Si active layers.

[0034] • Planar or textured geometries can be used for the Si layers. The later improves the absorption of long wavelength light via light-trapping effects. A textured surface should also not significantly affect the subsequent deposition of the upper polycrystalline or amorphous pn junction layer.

[0035] The bandgap energies of the materials comprising the pn junctions in the monolithic tandem voltage-matched solar cells of Fig. 3 can span the range of 0.25 eV to 2.5 eV. However, the ideal combination of bandgap energies for a tandem solar cell under one sun illumination is approximately 1.1 eV and 1.7 eV. The bandgap energy of Si is near the ideal 1.1 eV value for a bottom sub-cell. A wafer of Ge or any other crystalline semiconductor may also be used in the place of a Si wafer for the bottom sub-cells, but this may increase the cost of the device. A number of polycrystalline or amorphous thin film materials may be used for the top sub-cells. CdTe (1.45 eV) has a bandgap energy that is slightly lower than the ideal value but would still be viable. CdTe may also be alloyed with Zn, Se or S to increase the bandgap energy. Other possible thin film materials may include, but are not limited to, polycrystalline CIGS (0.9 – 2.5 eV), CZTS (1.4 – 15. eV), a-Si (1.7 eV), or microcrystalline Si. These materials have the advantage that they do not need to be grown on a crystalline template, and no lattice-matching is required.

Thin single crystalline or large-grained multicrystalline semiconductor layers may also be utilized as the pn junction material for the top sub-cell strings in the embodiments shown in

Fig. 3. Thin single crystalline or large-grained multicrystalline semiconductor layers may include, but are not limited to, $GaAs_xP_{1-x}$, $GaIn_xP_{1-x}$, GaAs, CdTe, CdSe, ZnTe, CIGS or CZTS. These crystalline pn junctions may be metamorphically grown directly on a crystalline electrically insulating layer 318 with the potential use of a compositionally-graded transitional buffer (CGTB) layer. A CGTB layer is designed to accommodate large differences in lattice constants between two crystalline materials that may cause defects by gradually shifting the lattice constant between the values of the electrically insulating material 318 and pn junction 322. The CGTB layer is designed to be transparent to light passing through the top pn junction 322 to the bottom pn junction. In this embodiment, the back contact layer 320 associated with the top pn junction 322 may also consist of a heavily doped single crystalline semiconductor. The CGTB layer may also be used between the top of the heavily doped layer in the bottom sub-cell wafer 316 and the electrically insulating layer 318, the electrically insulating layer 318 and the back contact layer 320, the back contact layer 320 and the pn junction 322 of the top sub-cells or any combination thereof. In embodiments featuring a single crystalline or large-grained multicrystalline pn junction 322, the single crystalline or large-grained multicrystalline junction layers may optionally be grown on a separate template substrate designed to template the desired crystalline growth. The separately grown single crystalline or large-grained multicrystalline pn junction 322 may then be removed from the template substrate and bonded to the final device structure. This allows for flexibility in choosing the materials of the electrically insulating layer 318 and back contact layer 320. Neither layer is required to be single crystalline or large-grained multicrystalline in this case. If these layers are implemented with single crystalline materials, however, they may be grown on the final device structure itself or on the same substrate that is used for the growth of the crystalline pn junction 322. A single crystalline or large-grained multicrystalline electrically insulating layer 318 or back contact layer 320 may also be grown on a different substrate entirely, in which case it also would have to be transferred and bonded to the final device structure. In addition, the pn junction 322 may consist of several pn junction layers connected in series via tunnel junctions instead of a single pn junction layer. The set of vertically stacked pn junctions that make up 322 would constitute a single sub-cell that would be serially connected to neighboring sub-cells in 322 in the same manner as outlined above for the case where the pn junction 322 consists of a single pn junction.

[0036] In another embodiment, a monolithic tandem voltage-matched solar cell can be fabricated from two polycrystalline and/or amorphous thin film pn junctions separated by an electrically insulating substrate. A schematic representation of an example device design

400 is shown in Fig. 4. The bottom sub-cell strings 402 are configured in a superstrate design approach on a transparent substrate 404, while the top sub-cell strings 406 are configured in a substrate design approach on top of the transparent substrate 404. The bottom sub-cell string 402 has an associated transparent front contact layer 408 deposited on the backside of the transparent substrate 404. The bottom pn junction 410 is deposited on the front contact layer 408 and the bottom contact layer 412 is deposited on the bottom pn junction 410. Patterning, etching, or scribing of these layers may occur in any sequence during the fabrication of the bottom sub-cells. The bottom sub-cells are connected in series to form sub-cell strings with the desired number of sub-cells to achieve a required voltage. The top sub-cell strings 406 are formed from a transparent back contact layer 414, a pn junction 416 and a transparent front contact layer 418. Patterning, etching, or scribing of these layers may occur in any sequence during the fabrication of the top sub-cells. The top sub-cells are connected in series to form sub-cell strings with the desired number of sub-cells to achieve a required voltage.

[0037] The polycrystalline or amorphous materials grown or deposited to form the top and bottom pn junctions 410 and 416, respectively, may consist of, but are not limited to, CIGS, CZTS, a-Si, polycrystalline Si, microcrystalline Si, CdTe, or CdTe alloyed with Zn, Se or S. Both the transparent back contact layer 414 of the top sub-cells and the front contact layer 408 of the bottom sub-cells should be transparent to photons with energy less than those absorbed by the top pn junction 416. These layers may be fabricated from materials including but not limited to transparent conducting oxides. The transparent substrate 404 may be glass or any other material that is transparent to photons with energy less than those absorbed by the top pn junction 416. The transparent substrate 404 may act as the electrically insulating layer, or a separate electrically insulating layer may be deposited anywhere between the front contact 408 of the bottom pn junction and the back contact 414 of the top pn junction. As noted above, layers or configurations that support photon recycling and/or light trapping could also be incorporated into top and bottom sub-cells.

[0038] One advantage provided by a monolithic tandem voltage-matched solar cell 400 is that the polycrystalline or amorphous pn junction can be grown or deposited directly on an inexpensive and readily available substrate such as glass. This design provides the efficiency boost of integrating two polycrystalline or amorphous thin film single junction solar cells into a multijunction solar cell while maintaining a one sun, flat plate configuration with a relatively low module cost. Single crystalline or large-grained multicrystalline layers can also be used for the top pn junction 416, bottom pn junction 410 or both in this design by using layer transfer techniques. The crystalline pn junction can be grown on a single or

multicrystalline template substrate. These layers can then be detached from the template substrate and bonded to the final device structure. This approach offers a greater selection of semiconductor materials in order to tune the bandgap energy or performance of the top and/or bottom sub-cells. The front and back contacts to each of the pn junctions may be made in any manner that is necessary for fabricating sub-cells out of crystalline pn junctions. This includes the sub-cell design, processing steps and material used for the top and bottom contacts. Metal grids may be used in place of or in addition to the low electrical resistivity front or back contact layers as required. All back contact or interdigitated back contact designs can also be used for the bottom sub-cells in this embodiment. Pn junction layers 416 and 410 could also comprise vertically stacked sets of pn junctions that are connected in series via tunnel junctions.

[0039] The various solar cell embodiments disclosed herein include voltage-matched multijunction solar cell designs and devices containing at least one polycrystalline or amorphous thin film pn junction layer. This enables several device design enhancements, including but not limited to:

[0040] • The ability to grow polycrystalline or amorphous thin films on non-crystalline surfaces allows for the use of non-crystalline transparent conducting contacts to be incorporated into the device stack.

[0041] • Elimination of the need for a crystalline growth template for the polycrystalline or amorphous thin film layers also allows for the incorporation of many different PV technologies and their associated efficiency-enhancing design improvements. This includes the use of inexpensive, non-crystalline substrates, such as glass, and light trapping features for embodiments that incorporate a crystalline Si pn junction. Eliminating the dependence on a crystalline growth template also obviates the need for thick CGTB layers and reduces the growth complexity and material usage in the device.

[0042] • In addition, the connection of pn junctions in parallel instead of series eliminates the need for heavily doped tunnel junctions, which is a major impediment to the development of thin film multijunction solar cells. The ability to isolate and contact the top sub-cells from the top of the device and to isolate and contact the bottom sub-cells from the back of the device also reduces device processing complexity and cost.

[0043] The description of the disclosed embodiments has been presented for purposes of illustration and description, but is not intended to be exhaustive or limiting of the claims to any particular form disclosed. The scope of the present disclosure is limited only by the scope of the following claims. Many modifications and variations will be apparent to those

of ordinary skill in the art. The embodiments described and shown in the figures were chosen and described in order to best explain the principles of the various embodiments, the practical application, and to enable others of ordinary skill in the art to understand the various embodiments with various modifications as are suited to the particular use contemplated.

[0044] While a number of exemplary aspects and embodiments have been discussed above, those of skill in the art will recognize certain modifications, permutations, additions and sub combinations thereof. It is therefore intended that the following appended claims and claims hereafter introduced are interpreted to include all such modifications, permutations, additions and sub-combinations as are within their true spirit and scope of the disclosure.

[0045] Various embodiments of the disclosure could also include permutations of the various elements recited in the claims as if each dependent claim was a multiple dependent claim incorporating the limitations of each of the preceding dependent claims as well as the independent claims. Such permutations are expressly within the scope of this disclosure.

CLAIMS

What is claimed is:

1. A voltage-matched monolithic thin film multijunction solar cell comprising:

a first pn junction having an n-type region, a p-type region and a first band-gap energy;

a second pn junction having an n-type region, a p-type region and a second band-gap energy;

a transparent electrically insulating layer between the first pn junction and the second pn junction; wherein the first and second pn junctions are connected in parallel to form a two-terminal photonic device.

2. The voltage-matched monolithic thin film multijunction solar cell of claim 1 further comprising:

a transparent first front contact and a transparent first back contact associated with the first pn junction, wherein the transparent back contact is positioned between the transparent electrically insulating layer and the first pn junction and wherein the transparent first front contact and the transparent first back contact provide for electrical connection to the first pn junction from a first side of the solar cell; and

a transparent second front contact and a second back contact associated with the second pn junction, wherein the transparent second front contact is positioned between the transparent electrically insulating layer and the second pn junction and wherein the transparent second front contact and the second back contact provide for electrical connection to the second pn junction from a second side of the solar cell.

3. The voltage-matched monolithic thin film multijunction solar cell of claim 1 further comprising:

at least one of crystalline, polycrystalline or amorphous first pn junction; and

at least one of crystalline, polycrystalline or amorphous second pn junction.

4. The voltage-matched monolithic thin film multijunction solar cell of claim 2 wherein the first pn junction and the second pn junction comprise layers of at least one of; CIGS, CZTS, a-Si, polycrystalline Si, microcrystalline Si, CdTe, or CdTe alloyed with Zn, Se or S.

5. The voltage-matched monolithic thin film multijunction solar cell of claim 1 further comprising:

a first string of serially connected sub-cells defined within the first pn junction;

a second string of serially connected sub-cells defined within the second pn junction; and

a parallel connection between the first string of serially connected sub-cells and the second string of serially connected sub-cells.

6. The voltage-matched monolithic thin film multijunction solar cell of claim 1 wherein the transparent electrically insulating region further comprises one or more low index of refraction layers providing for enhanced photon recycling or light trapping.

7. The voltage-matched monolithic thin film multijunction solar cell of claim 1 wherein at least one of the first pn junction or the second pn junction comprises a vertically stacked set of multiple pn junctions that are connected in series with tunnel junctions.

8. A voltage-matched thin film multijunction solar cell comprising:

a first pn junction comprising;

an n-type region;

a p-type region; and

a first bandgap;

a second pn junction comprising a doped Si, Ge or GaAs wafer;

a transparent electrically insulating region separating the first pn junction and second pn junction;

a transparent first front contact and a transparent first back contact associated with the first pn junction, wherein the transparent back contact is positioned between the transparent electrically insulating region and the first pn junction; and

an interdigitated p-type and n-type back contact associated with the second pn junction on the side of the wafer opposite the electrically insulating layer, wherein the first pn junction and the second pn junction are connected in parallel to form a two-terminal photonic device.

9. The voltage-matched thin film multijunction solar cell of claim 8 further comprising at least one of a crystalline, polycrystalline or amorphous first pn junction.

10. The voltage-matched thin film multijunction solar cell of claim 9 wherein the first pn junction comprises layers of at least one of; CIGS, CZTS, a-Si, polycrystalline Si, microcrystalline Si, CdTe, or CdTe alloyed with Zn, Se or S.

11. The voltage-matched thin film multijunction solar cell of claim 8 wherein the second pn junction further comprises a textured surface.

12. The voltage-matched thin film multijunction solar cell of claim 8 further comprising:

a first string of serially connected sub-cells defined within the first pn junction;

a second string of serially connected sub-cells defined within the second pn junction; and

a parallel connection between the first string of serially connected sub-cells and the second string of serially connected sub-cells.

13. The voltage-matched thin film multijunction solar cell of claim 8 wherein the transparent electrically insulating region further comprises one or more low index of refraction layers providing for enhanced photon recycling or light trapping.

14. The voltage-matched thin film multijunction solar cell of claim 8 wherein the first pn junction comprises a vertically stacked set of multiple pn junctions that are connected in series with tunnel junctions.

15. A method of fabricating a tandem voltage-matched solar cell comprising:

providing a transparent substrate;

forming a first crystalline, polycrystalline or amorphous pn junction comprising an n-type region, a p-type region and a first band-gap energy, in contact with a first surface of the substrate;

forming a second crystalline, polycrystalline or amorphous pn junction comprising an n-type region, a p-type region and a second band-gap energy in contact with a second surface of the substrate, opposite the first surface; and

connecting the first pn junction and the second pn junction in parallel to form a two-terminal photonic device.

16. The method of claim 15 further comprising:

forming first front contacts and first back contacts associated with the first pn junction, which first front contacts and first back contacts are accessible from a surface of the first pn junction opposite the transparent substrate; and

forming second front contacts and second back contacts associated with the second pn junction, which second front contacts and second back contacts are accessible from a surface of the second pn junction opposite the transparent substrate.

17. The method of claim 16 wherein the first front and first back contacts and the second front contacts are formed of a transparent conducting oxide.

18. The method of claim 16 further comprising providing a transparent glass substrate.

19. The method of claim 16 wherein the first pn junction and the second pn junction each comprise at least one of; CIGS, CZTS, a-Si, polycrystalline Si, microcrystalline Si, CdTe, or CdTe alloyed with Zn, Se or S.

20. The method of claim 16 further comprising:

forming a first string of serially connected sub-cells defined within the first pn junction;

forming a second string of serially connected sub-cells defined within the second pn junction; and

forming a parallel connection between the first string of serially connected sub-cells and the second string of serially connected sub-cells.

21. The method of claim 16 further comprising forming at least one of the first or second pn junctions as a vertically stacked set of multiple pn junctions that are connected in series with tunnel junctions.

22. A method of fabricating a voltage-matched thin film multijunction solar cell comprising:

providing a bottom pn junction comprising;

a doped Si, Ge or GaAs region; and

interdigitated p-type and n-type back contacts;

forming an insulating layer in contact with the bottom pn junction, opposite the interdigitated p-type and n-type back contacts;

forming an upper pn junction in contact with the insulating layer, wherein the upper pn junction comprises;

an n-type region,

a p-type region;

a transparent front contact; and

a transparent back contact, wherein the transparent back contact is positioned between the insulating layer and the upper pn junction; and

connecting the bottom pn junction and the upper pn junction in parallel to form a two-terminal photonic device.

23. The method of claim 22 further comprising forming a crystalline, polycrystalline or amorphous upper pn junction.

24. The method of claim 22 wherein the upper pn junction comprises at least one of; CIGS, CZTS, a-Si, polycrystalline Si, microcrystalline Si, CdTe, or CdTe alloyed with Zn, Se or S.

25. The method of claim 22 further comprising forming the transparent front contact and the transparent back contact associated with the upper pn junction from a transparent conducting oxide.

26. The method of claim 22 further comprising exposing the transparent back contact associated with the upper pn junction by scribing or chemically removing a portion of the upper pn junction and the transparent front contact associated with the upper pn junction.

27. The method of claim 22 further comprising texturing a surface of the bottom pn junction.

28. The method of claim 22 further comprising:

forming a first string of serially connected sub-cells defined within the bottom pn junction;

forming a second string of serially connected sub-cells defined within the upper pn junction; and

forming a parallel connection between the first string of serially connected sub-cells and the second string of serially connected sub-cells.

29. The method of claim 22 further comprising forming the upper pn junction as a vertically stacked set of multiple pn junctions that are connected in series with tunnel junctions.

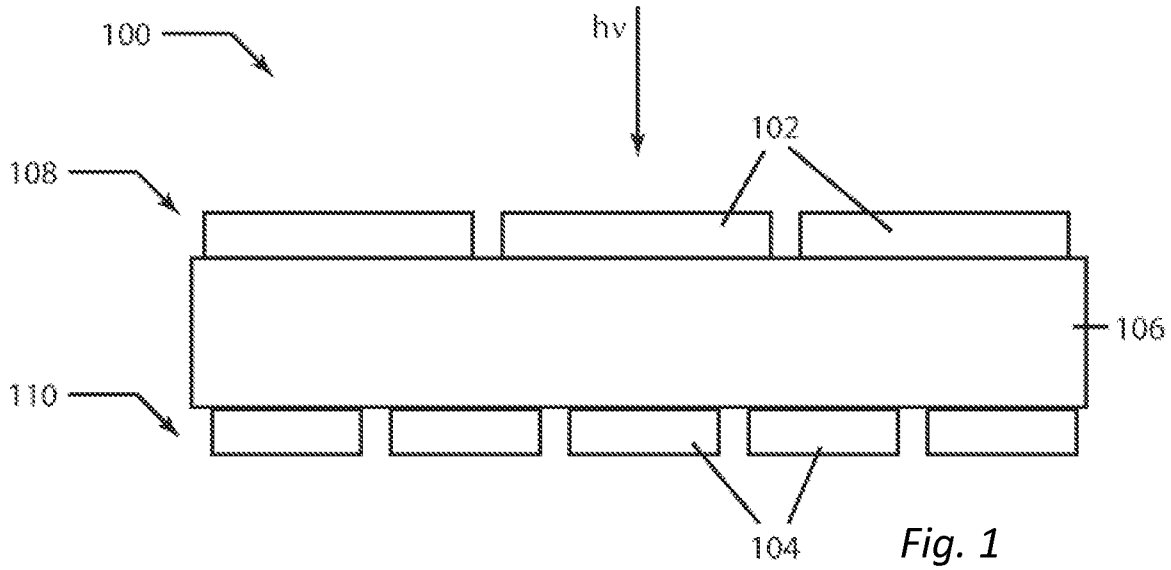

Fig. 1

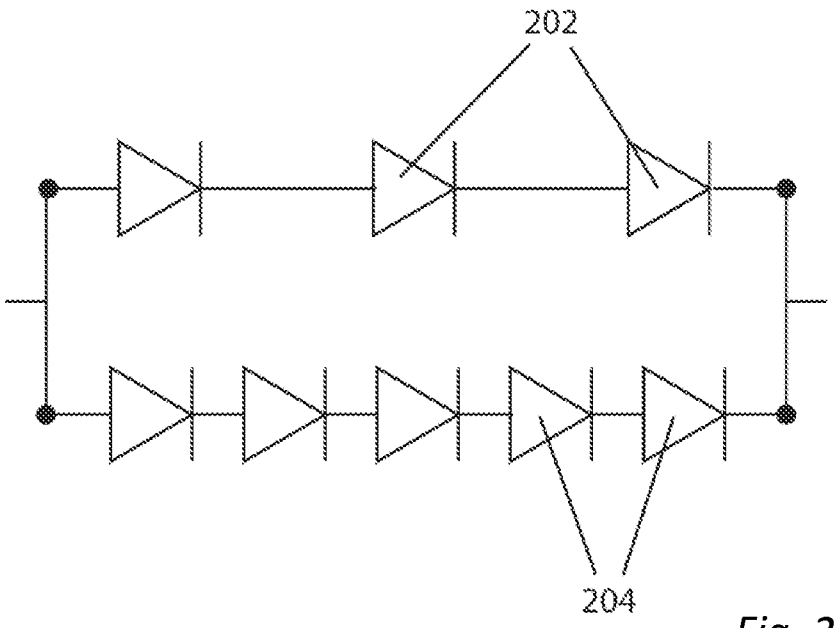

Fig. 2

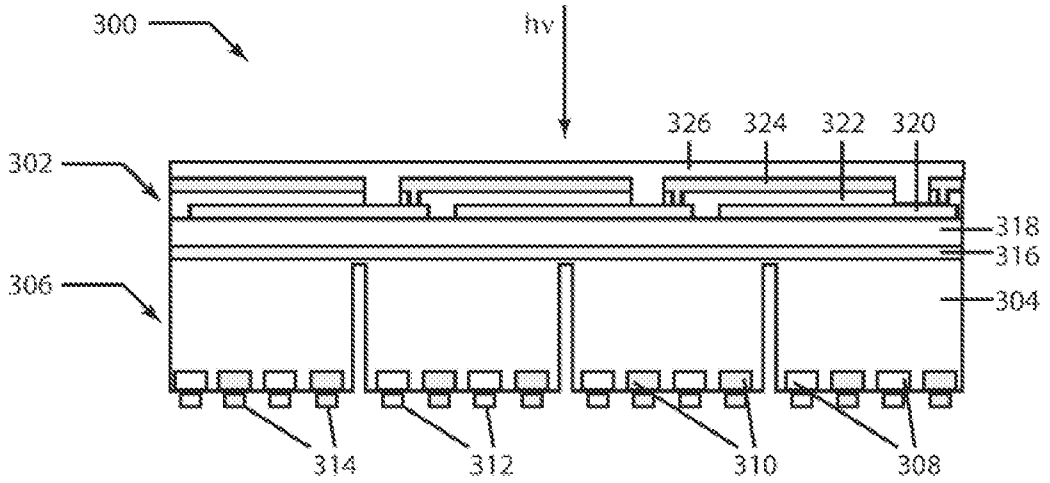
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Fig. 3

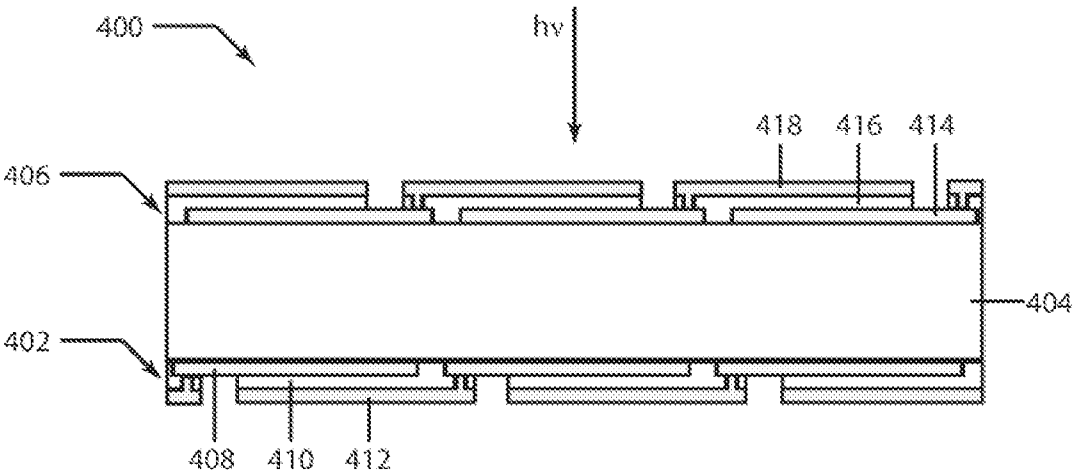
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Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/068761

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 31/06 (2013.01)
USPC - 136/249
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 31/00, 31/02, 31/04, 31/042, 31/05, 31/06, 31/038, 31/0687, 31/072, 31/0725 (2013.01)
USPC - 136/243, 249, 252, 258

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
CPC - H01L 31/042, 31/05; Y02E 10/50

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase, Google Patents, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2006/0144435 A1 (WANLASS) 06 July 06 (06.07.2006) entire document	1, 3, 5, 7, 15 --- 2, 4, 6, 8-14, 16-29
Y	US 2005/0056312 A1 (YOUNG et al) 17 March 2005 (17.03.2005) entire document	2, 4, 8-14, 16-29
Y	US 2010/0059109 A1 (NAKAYASHIKI et al) 11 March 2010 (11.03.2010) entire document	8-14, 22-29
Y	US 2011/0023958 A1 (MASSON et al) 03 February 2011 (03.02.2011) entire document	6, 13
A	US 2012/0152322 A1 (KRIBUS et al) 21 June 2012 (21.06.2012) entire document	1-29
A	US 2011/0232731 A1 (NAMKOONG et al) 29 September 2011 (29.09.2011) entire document	1-29

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 January 2013	14 FEB 2013
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774