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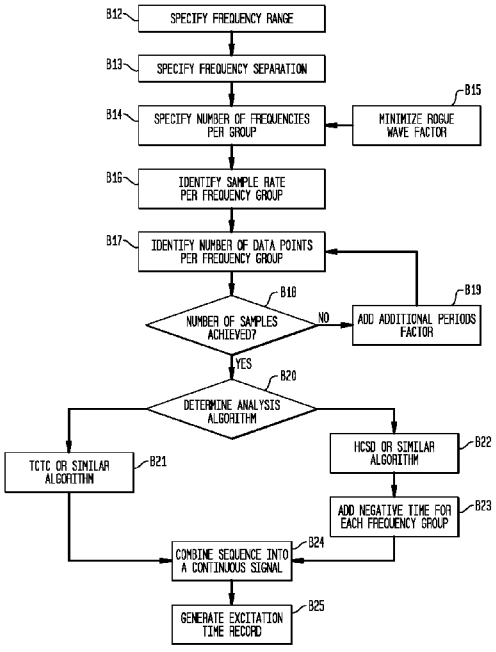
(54) Title: ENHANCED CHIRP EXCITATION SIGNAL FOR BROADBAND IMPEDANCE MEASUREMENT

(57) Abstract: Devices and methods to perform AC impedance measurement of a device which use an excitation signal including a root mean squared current or a root mean squared voltage in a sequence of one or more frequency groups, wherein each of said frequency groups includes a summation of one or more frequencies within a frequency spread.

FIG. 50



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ENHANCED CHIRP EXCITATION SIGNAL FOR BROADBAND IMPEDANCE MEASUREMENT

This International Patent Cooperation Treaty Patent Application claims the benefit of United States Provisional Patent Application No. 62/842,313, filed May 2, 2019, hereby incorporated by reference herein.

I. TECHNICAL FIELD

Devices and methods to perform AC impedance measurement of a device which use an excitation signal including a root mean squared current or a root mean squared voltage in a sequence of one or more frequency groups, wherein each of said frequency groups includes a summation of one or more frequencies within a frequency spread.

II. BACKGROUND

Electrochemical cells ("EC") transform stored chemical energy into electrical energy. Impedance measurement devices ("IMD") perform measurements that can reveal changes in the behavior of electrochemical processes in an electrochemical cell as a function of age and use which can provide insights into changes in the electrode surface and diffusion layer. The frequency range of interest of the impedance spectra of these energy storage devices generally spans a range of about 0.01 Hz to about 2 kHz. It can be difficult to obtain impedance spectrum having a steady state frequency response with very low frequencies of interest and meeting the requirement of a rapid measurement. This difficulty can be overcome by the use of an EC excitation test signal which comprises a sum of sines (SOS) with the frequencies of interest applied in parallel and restricted to harmonics that spanned the range of interest. The IMD assembles an excitation time record of an SOS current or voltage at the frequencies of interest, and implements the excitation time record to excite the EC with the SOS current or voltage (also referred to as the "excitation signal") and simultaneously captures a response time record comprising the voltage response to the current and frequencies (or a current response to the voltage and frequencies)(also referred as referred to as the "response signal") applied to the EC. A variety of impedance measurement algorithms can be used to transform the captured response time record into the frequency spectrum, including as examples, harmonic compensated synchronous detection ("HCSD"), fast summation transformation ("FST"), time cross talk compensation ("TCTC"), and harmonic orthogonal synchronous transformation ("HOST"). The excitation time record can have a duration of one period of the lowest frequency. The beginning of the excitation time record can further include a portion going backwards from time zero (also

referred to as “a negative time period), which as an example can be ten percent (10%) of the period of the lowest frequency in excitation time record. The "negative time" can be discarded from the captured response time record prior to being processed into the impedance spectrum to effectively satisfy a steady state sinusoidal assumption for the resulting impedance spectrum.

However, there remains an unresolved and long-standing problem, for that reason that the response time record can include a rogue wave artifact (also referred to as a “crest factor”) of approximately three times the root mean square (“RMS”) of the SOS. This artifact impacts resolution of the impedance measurement, pursuant to Equation 1.

$$V_P = \sqrt{\frac{2}{N}}\frac{V_{FS}}{3}$$

There would be a very substantial advantage in an IMD that applied an excitation time record to excite and EC which reduced or eliminated the rogue wave artifact.

III. DISCLOSURE OF THE INVENTION

Accordingly, a broad object of embodiments of the invention can be to provide devices to perform AC impedance measurement which reduces or eliminates the rogue wave artifact with excitation time records which excite a test device using an excitation signal including a root mean squared current or a root mean squared voltage in a sequence of one or more frequency groups, wherein each of said frequency groups includes a summation of one or more frequencies within a frequency spread and recording a response time record of a response of said device to the excitation time record and wherein an initial time period of the response time record of each of the one or more frequency groups can be discarded prior to the response time record being processed with an impedance spectrum algorithm to determine impedance of the test device.

Another broad object of embodiments of the invention can be to provide a method of determining impedance of a test device including exciting the device using an excitation time record including one or more of a root mean squared current or a root mean squared voltage in a sequence of one or more frequency groups, wherein each of said frequency groups includes a summation of one or more frequencies within a frequency spread, recording a response time record of a response of said device to said excitation time record, discarding an initial time period of said response time record of each of said one or more frequency groups, processing said response time record using an impedance spectrum algorithm, and determining impedance of said device.

Naturally, further objects of the invention are disclosed throughout other areas of the specification, drawings, photographs, and claims.

IV. BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a battery impedance plot of real impedance on the X axis versus negative imaginary impedance on the Y axis and illustrates ohmic resistance value (Ro) where the plot crosses the X axis, the charge transfer resistance (Rct) and the low-frequency tail referred to as the Warburg tail (Warburg).

Figure 2 illustrates a plurality of impedance spectrum as battery impedance plots 7a. . . .7j showing change in impedance of a battery over time.

Figure 3A depicts circuits of an illustrative impedance measurement device and battery management system disposed in a vehicle or other device.

Figure 3B is an enlargement of the processor and memory depicted in Figure 3A.

Figure 4 is an electrical schematic diagram of a model test electrical circuit and corresponding test device.

Figure 5 depicts an ideal *jw* Nyquist impedance plot of the model test circuit or test device shown in Figure 4.

Figure 6 depicts an embodiment of a simulated chirp response time record of a chirp excitation signal used to excite the model test circuit.

Figure 7 depicts a simulated chirp impedance spectrum obtained from the chirp response signal shown in Figure 6 as chirp impedance spectrum plot superimposed with the j*w* ideal spectrum plot shown in Figure 5.

Figure 8 depicts an embodiment of a simulated step chirp excitation record including a step chirp excitation signal having one period of each frequency.

Figure 9 depicts a simulated step chirp impedance spectrum plot of the embodiment of Figure 8 superimposed with the ideal *jw* impedance spectrum depicted in Figure 5.

Figure 10 depicts a simulated step chirp impedance spectrum plot superimposed with the ideal *jw* impedance spectrum depicted in Figure 5 resulting from an embodiment of a step chirp

excitation record including a step chirp excitation signal having two periods in each frequency and discarding the first period of each frequency.

Figure 11 depicts a simulated step chirp impedance spectrum plot superimposed with the plot of the ideal impedance jw spectrum plot depicted in Figure 5 resulting from an embodiment of a step chirp excitation record including a step chirp excitation signal having one period in each frequency and discarding the initial portion of each frequency for analysis by TCTC.

Figure 12 depicts an embodiment of a measured chirp response time record including the chirp response signal of the test device shown in Figure 4.

Figure 13 depicts a part of the measured magnitude of the chirp frequency response of Figure 12 evidencing increasing noise with increasing frequency.

Figure 14 depicts the plot of Figure 13 of the first 500 points of the chirp frequency response depicted in Figure 13.

Figure 15 depicts the measured chirp impedance spectrum plot of the embodiment of Figure 12 superimposed with the EIS reference spectrum plot.

Figure 16 depicts a portion of the measured magnitude of the chirp frequency response in which the frequency sweep rate is halved and the duration of the chirp excitation signal is doubled maintaining the frequency range.

Figure 17 depicts the measured chirp impedance measurement plot of the embodiment of Figure 16 superimposed with the EIS reference spectrum plot.

Figure 18 depicts an embodiment of a measured step chirp response time record of the test device shown in Figure 4.

Figure 19 depicts the resultant measured step chirp impedance spectrum plot of the embodiment of Figure 18 superimposed with the EIS reference spectrum plot.

Figure 20 depicts another embodiment of a measured step chirp response time record of the test device shown in Figure 4.

Figure 21 depicts the resultant measured step chirp impedance spectrum plot of the embodiment of Figure 20 superimposed with the EIS reference spectrum plot.

Figure 22 depicts another embodiment of a measured step chirp response time record of the test device shown in Figure 4.

Figure 23 depicts the resultant measured step chirp impedance spectrum plot of the embodiment of Figure 22 superimposed with the EIS reference spectrum plot.

Figure 24 depicts another embodiment of a measured step chirp response time record of the test device shown in Figure 4.

Figure 25 depicts the resultant measured step chirp impedance spectrum plot of the embodiment of Figure 24 superimposed with the EIS reference spectrum plot.

Figure 26 depicts the resultant measured step chirp impedance spectrum plot of the embodiment of Figure 24 superimposed with the EIS reference spectrum plot with the addition of about 0.1mOhm to the real impedance of the step chirp impedance spectrum which results in the step chirp impedance spectrum plot overlaying the EIS reference spectrum plot.

Figure 27 depicts a plot of rogue wave factor versus the number of octave harmonic sine waves in a sum of sines.

Figure 28 depicts another embodiment of a simulated step group chirp response time record of the test electrical circuit shown in Figure 4.

Figure 29 depicts the resultant simulated step group chirp impedance spectrum plot of the embodiment of Figure 28 superimposed with the ideal *jw* impedance spectrum plot.

Figure 30 depicts another embodiment of a simulated step group chirp response time record of the test electrical circuit shown in Figure 4.

Figure 31 depicts the simulated step group chirp impedance spectrum plot of the embodiment of Figure 30 superimposed with the ideal *jw* impedance spectrum plot.

Figure 32 depicts an embodiment of a step group chirp measured excitation time record applied to the test electrical circuit shown in Figure 4.

Figure 33 depicts the resultant measured step group chirp impedance spectrum plot of the embodiment of Figure 32 superimposed with the EIS reference spectrum plot.

Figure 34 depicts another embodiment of a step group chirp measured excitation time record applied to the test electrical circuit shown in Figure 4.

Figure 35 depicts the resultant measured step group chirp impedance spectrum plot of the embodiment of Figure 34 superimposed with the EIS reference spectrum plot.

Figure 36 depicts another embodiment of a step group chirp measured excitation time record applied to the test electrical circuit shown in Figure 4.

Figure 37 depicts the measured step group chirp response time record of the test electrical circuit shown in Figure 4.

Figure 38 depicts the resultant measured step group chirp spectrum plot of the impedance spectrum of the embodiment of Figure 37 superimposed with the EIS reference impedance spectrum.

Figure 39 depicts another embodiment of a measured step group chirp response time record of the test device shown in Figure 4.

Figure 40 depicts the resultant measured step group chirp spectrum plot of the impedance spectrum of the embodiment of Figure 39 superimposed with the EIS reference impedance spectrum.

Figure 41 depicts another embodiment of a measured step group chirp response time record of the test device shown in Figure 4.

Figure 42 depicts the resultant measured step group chirp spectrum plot of the impedance spectrum of the embodiment of Figure 41 superimposed with the EIS reference impedance spectrum.

Figure 43 depicts another embodiment of a simulated step group chirp response time record of the test electrical circuit shown in Figure 4.

Figure 44 depicts the resultant simulated step group chirp spectrum plot of the impedance spectrum of the embodiment of Figure 43.

Figure 45 depicts another embodiment of a simulated step group chirp response time record of the test electrical circuit shown in Figure 4.

Figure 46 depicts the resultant simulated group chirp spectrum plot of the impedance spectrum of the embodiment of Figure 45.

Figure 47 depicts another embodiment of a simulated step group chirp response time record of the test electrical circuit shown in Figure 4.

Figure 48 depicts a plot of the rogue wave for an embodiment of the step group chirp signal to reduce the rogue wave and including target frequencies of Figure 47.

Figure 49 is a block flow diagram of a method of assembling an excitation time record for embodiments of step chirp.

Figure 50 is block flow diagram of a method of assembling an excitation time record for embodiments of step group chirp.

Figure 51 is block flow diagram of a method of capturing a response time record for embodiments of step chirp and step group chirp.

Figure 52 is block flow diagram of a method of performing embodiments of high fidelity impedance measurements of a device with step group chirp.

Figure 53 is a block flow diagram of a method of performing embodiments impedance measurement of a device (3) with step group chirp including targeted frequencies.

V. MODE(S) FOR CARRYING OUT THE INVENTION

Now, with general reference to Figures 1 through 53, which provide illustrative examples of IMD (1) and methods of using IMD (1) for performing impedance measurements (2) of a device (3). A device (3) can, as illustrative examples, include electrical circuits (4), electrochemical cells (5) (whether individual cells, modules, or packs), or electrical circuits (4) including an electrochemical cell (5), or components or combinations thereof. The electrical circuit (4) including an electrochemical cell (5) can, but need not necessarily, include a load (6) consuming electrical power from the electrochemical cell (5).

Elements, circuits, modules, and functions may be shown in block diagram form. Moreover, specific implementations shown and described are illustrative only and should not be construed as the only way to implement the present disclosure unless specified otherwise herein. Additionally, block definitions and partitioning of logic between various blocks is illustrative of a specific implementation. However, the present disclosure may be practiced by numerous other partitioning solutions. For the most part, details concerning timing considerations and the like

have been omitted where such details are not necessary to obtain a complete understanding of the present disclosure by persons of ordinary skill in the relevant art.

Those of ordinary skill would appreciate that the various illustrative logical blocks, modules, circuits, and algorithm described in connection with embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and acts are described generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the embodiments described herein.

When implemented with hardware, the embodiments disclosed herein may be implemented or performed with a general purpose processor, a special purpose processor, a Digital Signal Processor (DSP), an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. When executing software for carrying out processes for embodiments described herein, a general-purpose processor should be considered a special-purpose processor configured for carrying out such processes. A processor may also be implemented as a combination of computing devices, such as, a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

In addition, it is noted that the embodiments may be described in terms of a process that is depicted as a flowchart, a flow diagram, a structure diagram, or a block diagram. Although a flowchart may describe operational acts as a sequential process, many of these acts can be performed in another sequence, in parallel, or substantially concurrently. In addition, the order of the acts may be re-arranged. A process may correspond to a method, a function, a procedure, a subroutine, a subprogram, or a step depending on the application. Furthermore, the methods disclosed herein may be implemented in hardware, software, or both. If implemented in software, the functions may be stored or transmitted as one or more instructions or code on a computer-

readable medium. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another.

It should be understood that any reference to an element herein using a designation such as "first," "second," and so forth does not limit the quantity or order of those elements, unless such limitation is explicitly stated. Rather, these designations may be used herein as a convenient method of distinguishing between two or more elements or instances of an element. Thus, a reference to first and second elements does not mean that only two elements may be employed or that the first element must precede the second element in some manner. In addition, unless stated otherwise, a set of elements may comprise one or more elements.

Electrochemical Impedance Spectroscopy. Electrical Impedance Spectroscopy (EIS) involves measuring a response signal to a stimulus signal. The stimulus signal can be either a current stimulus signal or a voltage stimulus signal with the response signal being the complement (for example, if the stimulus signal comprises a sum of sines ("SOS") root mean square ("RMS") current stimulus signal (SOS RMS current) then the response comprises a voltage response signal, if the stimulus signal comprises a voltage stimulus signal then the response signal comprises a current response signal). Data processing then calculates the complex impedance of the device at the stimulus signal frequency. This process is generally performed at each of a plurality of frequencies to create an array of the complex impedances. Conventional use of EIS produces impedance measurements, typically including a frequency range between about 100 kHz to about 10 mHz, and depending on impedance measurement parameters have duration in a range of about ten minutes to about an hour to perform.

iRIS. In-line rapid impedance spectroscopy ("iRIS") can generate impedance measurements in less time than conventional EIS IMD and depending on impedance measurement parameters, having a duration in a range of about 1 sec to about 80 sec. iRIS devices can as examples perform impedance measurements from about 1.6 kHz to about 12 mHz in about 80 sec, from about 1.6 kHz to about 0.1 Hz in about 10 sec, or from about 1.6 kHz to about 0.8 Hz in about 1.2 sec; although this is not intended to preclude certain embodiments including or using conventional EIS IMD. As illustrative examples, iRIS devices can measure electrochemical cells of 50V having impedances to about 3 mΩ with about 0.1 mΩ resolution. Measurable impedance can be lowered to about 1 mΩ with about 0.04 mΩ resolution, as the voltage threshold is reduced toward 10 V; however, these illustrative examples are not intended to preclude embodiments having measurable impedance or resolution outside of these ranges.

Impedance Plots. Now, with primary reference to Figure 1, an impedance spectrum (7) is typically displayed graphically as a plot (8) similar to a standard Nyquist plot. Following convention among electrochemical researchers, these plots differ in that a negative imaginary impedance in ohms (9)(also referred to as "imaginary impedance") is plotted on the Y axis, and only positive impedance in ohms (10) (also referred to as "real impedance"), of each of a plurality of frequencies (11) used to excite the electrochemical cell (5), is plotted on the X axis. The ohmic resistance value (Ro) is the real impedance value where the plot crosses the X axis (in the example of Figure 1, the ohmic resistance occurs at about 251.2 Hz). The mid-frequency semicircle is the charge transfer resistance (Rct) and the low-frequency tail is often referred to as the Warburg tail ("Warburg").

Now with primary reference to Figure 2, which displays a plurality of impedance spectrum (7) as battery impedance plots (7a. . . .7j) showing change in impedance of an electrochemical cell (5) over time. Plot (7a) illustrates a baseline impedance measurement (2) of the electrochemical cell (5). Plots (7b. . .7d) illustrate impedance measurements (2) of the battery (5) upon elapse of 12, 24, and 36 weeks, respectively. Plots (7e. . .7g) illustrate impedance measurements of the battery (5) upon elapse of 48, 60, and 72 weeks, respectively. Plots (7h. . .7j) illustrate impedance measurements (2) of the electrochemical cell (5) upon elapse of 84, 96, and 108 weeks, respectively. The semicircles within the plots, corresponding to Rct or the Ro, or combinations thereof, can increase as the cell ages and can thus be used to effectively estimate the battery state of health by analyzing movement of the Rct within the plots (7b. . .7j) over time.

Impedance Measurement Device. Now, with general reference to Figure 3A and 3B which depict block diagrams of an illustrative IMD (1), which can, but need not necessarily, be an iRIS device, including a processor (13) in communication with a non-transitory computer readable medium (14) containing a program code (15) which implements one or more impedance spectrum algorithms (16), a sum of sines generator ("SOSG")(17); a data acquisition system ("DAS")(18); one or more amplifiers (12), a connection safety circuit (20) and a power supply (21). Auto calibration (22) may be included in some embodiments under control of the processor (13); although in certain embodiments, calibration can be performed as described in United States Patent No. 10,436,873, hereby incorporated by reference herein. An illustrative impedance measurement device (1) suitable for use in particular embodiments can be made and used as described in United States Patent No. 10,379,168, hereby incorporate by reference herein.

Examples of impedance spectrum algorithms (16) useful to process a response time records (23) of a response signal (24) to determine impedance measurements (2) as a function of

the plurality of frequencies (11) assembled in the excitation time record (25) to generate the excitation signal (26) to excite the device (3) under test include, but are not limited to, harmonic compensated synchronous detection (HCSD), fast summation transformation (FST), generalized fast summation transformation (GFST), frequency cross talk compensation (FCTC), time cross talk compensation (TCTC), harmonic orthogonal synchronous transformation (HOST), and combinations thereof. See, for example, United States Patents Nos. 7,688,036; 7,395,163 B1; 7,675,293 B2; 8,150,643 B1; 8,352,204 B2; 8,762,109 B2; 8,868,363 B2; and 9,244,130 B2, and United States Patent Publications Nos. 2011/0270559 A1; 2014/0358462 A1; and 2017/0003354 A1 which describe the implementation of one more of the impedance spectrum algorithms (16).

The IMD (1) can, but need not necessarily, include a remote computer (27)(or the computer may be local or integral to the IMD (1)) via a Universal Serial Bus (USB) interface (28) or other suitable interface, such as, for example, hardwire serial interfaces, hardwire parallel interfaces, and wireless interfaces (as examples, WI-FI®, ZIGBEE®, BLUETOOTH®). In particular embodiments, the remote computer (27) can include all or part of the components necessary to control the IMD (1) to perform impedance measurements (2) of the device (3) under test.

The processor (13) (whether integral to the IMD (1) or included in the remote computer (27)) can synchronize and control the DAS (18), the SOSG (17) and the preamplifier (10) in accordance with control impedance measurement parameters (29) and generate impedance measurement commands (30) to operate the IMD(1) dictated by the program code (16). In particular embodiments, the processor (13) can interface with the remote computer (27) to download desired impedance measurement parameters (29) and impedance measurement commands (30) and upload various impedance measurement data (31). As non-limiting examples, the processor (13) or memory (14) can to hold the excitation time record (25) and the response time record (24) until processed using the desired impedance spectrum algorithm (16).

The processor (13) may be configured to accept downloaded impedance measurement commands (29) and impedance measurement parameters (30) and upload to the remote computer (27) archived impedance measurement data (31) under direction of the remote computer (27). Additionally, the IMD (1) may be able to be controlled via human interaction in a user interface ("GUI") (32) on the remote computer (27) or the IMD (1) for the purpose of inputting impedance measurement parameters (29) and impedance measurement commands (30) to the IMD (1).

When an impedance measurement (2) is triggered, the DAS (18) can send out a power up signal (33) to a power supply (21) to power up a DC voltage amplifier (19) and a connection safety circuit (20). In the illustrative example, the device (3) under test is an electrochemical cell (5) (a "battery") and the DC battery voltage (34) may be measured by a battery response amplifier (35) and input to the DAS (18) as the battery voltage analog signal (36) of the DC battery voltage (34). The DAS (18) or the processor (13) may digitize the battery voltage analog signal (36) of the DC battery voltage (36) and may send the digitized result to the remote computer (27).

When the excitation signal (26), and in this particular embodiment the SOS current (37), stimulates the battery (5) under test, the response signal (24), and in this embodiment the SOS voltage response (38) at its terminals includes the DC battery voltage (34) plus a SOS voltage response (24) of the SOS current (37) acting on the internal impedance of the battery (5). It is this SOS voltage response (38) that, when captured and processed, yields the impedance spectrum (7) of the response signal (24). To accurately detect the SOS voltage response (38), the DC battery voltage (34) can be subtracted out prior to measuring the SOS voltage response (38) allowing an analog to digital convertor (39) to focus on the response signal (24) which can substantially improve accuracy. This subtraction of the DC battery voltage (34) may be accomplished by measuring the DC battery voltage (34) prior to the application of the stimulus signal (26) (for example an SOS current (37)) to the battery (5) under test and then feeding back a computer generated buck voltage signal (40) to generate a buck bias voltage (41) by the battery response amplifier (35) from the total of the DC battery voltage (34) and the SOS voltage response (38) to yield only the corresponding response signal (24) (for example an SOS voltage (38)).

The remote computer (27) or the processor (13) can send a connection signal (42) to the connection safety circuit (20) to connect the battery (5) to current drivers (43) in the DC voltage amplifier (19). With the DC voltage amplifier (19) connected to the battery (5), the remote computer (27) or processor (13) sends a battery impedance measurement signal (44) to the DC voltage amplifier (19).

The impedance measurement signal (44) may be smoothed out using a smoothing filter (45), then fed into a current driver (43), which converts the signal into the excitation signal (26), such as an SOS current (37). The battery response amplifier (35) detects the DC battery voltage (34) and subtracts the buck bias voltage (41) to become the battery response signal (24) that may be digitized by the DAS (18). The captured impedance measurement time record (23) may be

processed using one or more of the spectrum algorithms (16) to generate the impedance spectrum (7) which can be converted to impedance plots (8).

As an illustrative example, the IMD (1) can process a battery impedance spectrum (7) with at least fifteen frequencies of resolution for FST and eleven frequencies for GFST (based upon triads) or HCSD, when the start frequency is 0.1 Hz. In addition, the IMD (1) can support a dither feature (46) of high spectrum resolution with dither steps anywhere between 1 and 2 for FST based upon octaves and anywhere between 1 and 3 for GFST based upon triads. For suitable results, the captured response time record (23) may be as low as one period of the lowest frequency and the IMD (1) may be able to process a response time record (23) with a start frequency (47) of as low as about 10 mHz or a stop frequency (48) as high as about 10 kHz; however, these illustrative examples are not intended to obviate embodiments which can have a lower start frequency or a higher stop frequency.

The SOSG (17) can, under control of the processor (13) or remote computer (27), generate a zero-order hold synthesis of the SOS as an input to the DC voltage amplifier (19). As a non-limiting example, a sample rate (49) for the analog to digital convertor (43) may be configured at least one-hundred times the highest excitation signal frequency (11) and compatible with the smoothing filter (45) within the DC voltage amplifier (19).

In one embodiment, the SOSG (17) under control of the processor (13) can synthesize a sample clock (50) to be used by the DAS (18). FST requires a sampling frequency that is octave harmonic with the highest frequency of the SOS excitation signal (24) and is at least 4 times higher. GFST based on triads requires a sampling frequency that is triad harmonic with the highest frequency of the SOS excitation signal (24) and is at least 9 times higher. The SOSG (17) can include a programmable signal level for the DAC output to the smoothing filter (45), which enables the processor (13) to control the level of the SOS RMS current (37) to the battery (5) under test.

The DAS (18) may be configured with 16 bits of resolution and accept an external sample clock (50) from the SOSG (17). The DAS (18) may accept an enable signal from the processor (13) to start acquiring data concurrent with the application of the excitation signal (26), such as the SOS current signal (37) to the battery (5) under test. The DAS (18) can accept the analog battery voltage signal (36) that has been conditioned by the DC voltage amplifier (19) for digitizing. The DAS (18) may include a buffer memory to hold a sample of the digitized battery

voltage signal (36) for uploading to memory (14). Each of the acquired samples (51) may become part of the response time record (23) that is input into the spectrum algorithms (16).

The impedance spectrum (7) generated during an impedance measurement (2) of a battery (5) can be passed to the processor (13) or the remote computer (27) in any suitable format (as an illustrative example: Comma Separated Values (CSV) format). Each individual impedance spectrum (7) may further include one or more of: a time stamp (52), an information header (53), the stimulus signal frequencies (11), the real impedance (10), the imaginary impedance (9) and the DC battery voltage (34) for the impedance spectrum (7), SOS RMS current (37); the magnitude and phase calibration constants (54).

In-line Rapid Impedance Spectroscopy (iRIS®). Again, with primary reference to Figure 3, particular embodiments of the IMD (1) or iRIS device can measure the impedance spectrum (7) of a device (3), electrical circuit (4), electrochemical cell (5), or other device, or component, under test in one second or less. An iRIS device (1) can be configured to measure all of the component stimulus signal frequencies (11) of an excitation signal (26), such as an SOS current (37), in parallel within one period of the lowest frequency (11). In one embodiment, the iRIS device (1) can process a battery impedance spectrum (7) with at least 15 frequencies (11) of resolution for FST and 11 frequencies (11) for GFST (based upon triads) when the start frequency (47) comprises about 0.1 Hz. In addition, the iRIS device (1) may be able to support a dither feature (46) of high spectrum resolution with dither steps occurring in a range of 1 and 2 for FST based upon octaves and occurring in a range of 1 and 3 for GFST based upon triads. The response time record (25) can, but need not necessarily, comprise one period of the lowest frequency (11) and the IMD (1) (iRIS device) can, but need not necessarily, process a response signal (24), such as an SOS voltage response (38) with a start frequency (47) of as low as about 10 mHz or a stop frequency (48) as high as about 10 kHz, as above described.

Chirp. Now with primary reference to Figures 4 through 7, in particular embodiments, an excitation time record (25) can be assembled to excite the device (3) under test with an excitation signal (26) including a single sine wave having its frequency continuously modulated as a ramp starting at a low frequency and ending with a high frequency (referred to as "a chirp (26A)"). Thus, the IMD (1) employing excitation time record (25) which generates a chirp (26A) cannot achieve a steady state sinusoidal in the excitation signal (26) or the response signal (24). When the excitation time record (25) implements a chirp (26A) with a log frequency spread, the ratio of the FFT of the chirp excitation signal (26A) to the FFT of the chirp response signal (26A) does approach a steady state system. This approach in the form of a log base 2 chirp (26A) was

evaluated via simulations and a reduction to practice operable to generate measured data. An example of a log base 2 chirp can be performed by an IMD (1) which assembles a chirp excitation time record (25A) generating a sample frequency of 40 kHz and a frequency spread starting at 2 kHz and decreasing by octaves for a total of 15 frequencies (11). The duration of the chirp (26A) being about ten seconds with the number of data points collected of about 400,000. The expression for the discrete relationship of the log base 2 chirp is given by Equation 2, where V_P is the peak of the chirp signal, f_{START} is the start frequency, α is a scale factor for the desired sweep, and Δt is the time step.

$$\mathrm{Ch(i)} = V_P \sin\left(2\pi f_{start} 2^{\alpha(i-1)\Delta t}(i-1)\Delta t\right)$$

Given log base 2 for M=15 frequencies ending at 2 kHz (f_{end}) and decreasing to the start frequency is given by:

$$f_{start} = f_{end}\left(\frac{1}{2}\right)^{(M-1)}$$

Now, with primary reference to Figure 4, which depicts a schematic diagram of the model test circuit (4) used in evaluation of the log base 2 chirp. The model test circuit (4) having an impedance substantially equivalent to the internal impedance of a lithium ion battery. As an example, the recursive model for the test circuit was realized with the following parameters:

R1, R2, R_3 = 15 mOhms; and

C1 = 9F.

Now with primary reference to Figure 5, which depicts an ideal *jw* Nyquist plot (8D) of model test circuit (4) based on the example parameter values. The spectrum is plotted over a frequency range having a high frequency of 2 kHz stepping down by 15 octaves.

Now, with primary reference to Figure 6, the IMD (1) assembled an excitation time record (25) using the chirp excitation time record (25A) including a chirp excitation signal (26A) expressed by Equation 2 with an RMS current set at 500 mA which yields: V_P=0.707. The IMD (1) excited the model test circuit (4) using the chirp excitation signal (26A) and captured a chirp response signal (24A). Figure 6 depicts a plot of the chirp response time record (23A) of the input chirp excitation signal (26A). The ratio of the FFT of the response time record (23A) to the FFT of the input chirp excitation time record (25A) comprises the impedance spectrum. Given that the chirp response signal (24A) comprises about 10 seconds, the FFT frequency resolution is about 0.1 Hz. Additionally, with the sample frequency established at about 40 kHz

the Nyquist frequency comprises about 20 kHz with the impedance spectrum of the model test circuit (4) below about 50 Hz.

Now, with primary reference to Figure 7, the chirp impedance spectrum (7A) obtained from the chirp excitation signal (26A) can be superimposed with the *jw* ideal spectrum plot (8D) shown in Figure 5 which evidences substantial agreement between the plots. However, the use of a chirp excitation signal (26A) for impedance measurements in systems having low signal to noise ratio (S/N) may not generate or may generate data which may not have sufficient precision, reproducibility, or reliability in certain applications.

Step Chirp. Now with general reference to Figures 8 through 11, in particular embodiments, the excitation time record (25) can be assembled as a step chirp excitation time record (25B) to generate a step chirp excitation signal (26B)(also referred to as a "step chirp"). A step chirp (26B) comprises a step of at least one full period of a frequency which one full period lapses before the next frequency starts and the frequencies go from low frequency, stepping to high frequency as octave harmonics. An TCTC algorithm can, but need not necessarily, be used to process the step chirp response time record (23B) based on "least squares" which mitigates noise via averaging. In the illustrative examples of step chirp (26B), the same recursive model test circuit (4) shown in Figure 4 with the same sample rate and frequency range. However, the signal *VP* was set at 1A which yields:

$$V_{RMS} = \frac{1}{\sqrt{2}}$$

Now with primary reference to Figure 8, which depicts a step chirp excitation time record (25B), the step chirp excitation signal (26B) has a longer duration than the duration of the chirp excitation signal (26A) depicted in Figure 6 (16.5 sec vs 10 sec). In a first baseline simulation each period was processed with TCTC based upon a single known frequency with the assumption that steady state sinusoidal is valid.

Now with primary reference to Figure 9, which depicts the resultant step chirp impedance spectrum plot (8B) of the first baseline simulation superimposed with the ideal *jw* impedance spectrum (8D) depicted in Figure 5. The superimposed plots evidence that the assumption of steady state may not be valid.

Now, with primary reference to Figure 10, in a second baseline simulation, step chirp (26B) included two periods of each frequency (11) and process by TCTC included only the second of the two periods. The step chirp impedance spectrum plot (8B) superimposed with the

ideal *jw* impedance spectrum (8D) depicted in Figure 5 evidences close agreement, therefore, the steady state assumption remains valid with disagreement only at higher frequencies. However, the disadvantage of using two periods of each frequency is a doubling of the duration of the step chirp response time record (23B).

In particular embodiments, the IMD (1) assembles an excitation time record (25) including an SOS excitation signal (26) having frequencies (11) which are octave harmonic over the frequency range with an excitation signal duration for analysis of one period of the lowest frequency. To enable the assumption of steady state a fraction of the response time record (23) at the beginning of the SOS excitation signal 26, includes a negative time portion (55), usually 10% of the signal duration. This "negative time" portion (55) which is not processed enables the steady state assumption. The data processing can be accomplished by HCSD. However, HCSD requires an integer number of one or more full periods of the time record for successful data processing. The impedance spectrum algorithm (16) used with stepped chirp (26B) can also be TCTC, which enables processing of less than a full period of each frequency.

Thus, with primary reference to Figure 11, in particular embodiments of step chirp (26B), the step chirp excitation time record (25B) includes a single period of each frequency (11) but processing of the step chirp response time record (23B) includes only a part of each period of each frequency (11), wherein the initial portion (56) of the period of each frequency (11) can be discarded and processing includes only end portion of each period of each frequency (11). The discarded initial portion (56) of each period of each frequency establishes the steady state assumption. In the illustrative example of Figure 11, the embodiment of stepped chirp (26A) includes only one period of each frequency (11) and initial portion (56) comprising about 30% of the period of each frequency (11) can be discarded to establish the steady state assumption. The resultant step chirp impedance spectrum plot superimposed with the plot of the ideal impedance *jw* spectrum plot (8D) depicted in Figure 5 evidences that the result is substantially identical for embodiments which utilize two periods of each frequency and discard the first of the two periods, as above described and depicted in Figure 10. Embodiments of step chirp (26B) which discard the initial portion (56) of the period of each frequency and processed using TCTC accommodate the assumption of steady state. However, this illustrative example is not intended to preclude embodiments of step chirp (26B) in which the discarded initial portion (56) of each period of each frequency (11) is lesser or greater than 30% and depending the application, the discarded initial portion (56) of each period of each frequency occur incrementally in range of about 5% to about 80%.

EXAMPLES OF IMPEDANCE MEASUREMENTS USING CHIRP AND STEP CHIRP.

Illustrative examples of impedance measurements (2) using chirp (26A) and step chirp (26B) were performed using an IMD (1) as above described. For both chirp (26A) and step chirp (26B) the RMS of the excitation current was about 500 mA, otherwise all the parameters of the excitation signals (26) were established substantially as above described. A physical test device (3) was substantially the same or equivalent to the model test circuit (4) above described and depicted in Figure 4. The reference EIS spectrum (8E) for the test device (3) used for all of the illustrative impedance measurements was obtained using a Solartron Potentiostat Galvanostat instrument. The nominal parameters for the test device (3) were: Rl=15 mOhm, R2=15 mOhm, R3=15 mOhm, C1=9F. The impedance measurements (2) were calibrated in order to account for gains and frequency response of the IMD (1) by performing measurements with a shunt (57) of known value with the identical measurement conditions as performed with the test device (3). The shunt response time record (58) from the shunt (57) was normalized to the shunt value. The response time records (23) for the test device (3) and the shunt (57) were normalized and transformed to the frequency domain and the ratio recorded as measured impedance (2) of the test device (3).

EXAMPLES OF IMPEDANCE MEASUREMENTS USING CHIRP.

Illustrative measurements using chirp (26A) included a chirp excitation time record (25A) which generated an RMS excitation current of about 500mA RMS having 15 frequencies starting at 2 kHz and decreasing in octaves for a 10 second duration. The frequency range within the chirp was about 0.1 Hz to about 2000 Hz, well within the Nyquist frequency of 20 kHz. Two measurements were taken, the first with the shunt (57) and the second with the physical test device (3). The IMD (1) captured the time records as .csv files. Both .csv files were post processed with a software tool. The shunt (57) chirp response time record (58A) was normalized to the shunt value and processed to the frequency domain with FFT. The test device (3) chirp response time record (23A) was also processed with FFT.

CHIRP EXAMPLE I.

Now, with primary reference to Figures 12 through 15, the first example of chirp depicts a plot of the chirp response time record (23A) including the chirp response signal (24A) of the test device (3) as depicted in Figure 12. The ratio between the FFT of the chirp response time record (23A) to the FFT of the shunt normalized time record was generated to obtain the measured impedance (2) of the first 20,000 points of the time record plotted as magnitude against

frequency as shown in the example of Figure 13. Figure 13 evidences that noise in the magnitude of the chirp frequency response time record (23A) increases with frequency. However, the principle part of the test device response was well below 100 Hz, thus Figure 14 depicts the same plot as in Figure 13, but with only the first 500 points of the chirp frequency response (23A). In Figure 14, the noise is reduced but still increases with frequency. Figure 15 superimposes the chirp impedance spectrum plot (8A) with the EIS reference spectrum plot (8E). The plots have close agreement at low frequency and evidence increasing noise at high frequency.

CHIRP EXAMPLE II.

Now with primary reference to Figures 16 and 17, the second example of chirp (26A) maintains the same chirp excitation time record (25A) as the first example of chirp (26A), except that the frequency sweep rate about halved and the duration of the chirp excitation signal (26A) about doubled thus holding the about the same frequency range. Figure 16 depicts the impedance magnitude chirp frequency response (23A) to about 50 Hz and Figure 17 depicts the chirp impedance measurement plot (8A) superimposed with the EIS reference spectrum plot (8E). Because the chirp response time record (25A) is 20 seconds in the frequency domain, the frequency step is 0.05 Hz, and thus, the applicable frequencies from the FFT results exclude the first data point as 0.05 Hz was not within the chirp frequency spread. As seen in Figure 17, the agreement between the chirp impedance spectrum plot (8A) and the EIS reference spectrum plot (8E) improves; however there remains increasing noise at the higher frequency.

EXAMPLES OF IMPEDANCE MEASUREMENTS USING STEP CHIRP.

Now with general reference to Figures 18 through 26, which depict illustrative measurements using step chirp (26B) included a step chirp excitation time record (25B) which generated an RMS excitation current of about 500 mA having 15 frequencies in the first step chirp example and 18 frequencies in the second step chirp example each stepping down from 2 kHz in harmonic octaves. Impedance measurements (2) using the same step chirp excitation time record (25B) were made on the above described shunt (57) and test device (3). The impedance measurements (2) were archived in .csv files for post processing. TCTC was used to process the .csv data with the steady state assumption validated by discarding the initial portion (56) of the period of each frequency, as above described. The post processed results for each of the first and second step chirp impedance spectrum plots (8B) were superimposed with the EIS reference spectrum plot (8E).

STEP CHIRP EXAMPLE I.

Now, with primary reference to Figures 18 and 19, which respectively illustrate the step chirp response time record (23B) of the test device (3), and the resultant step chirp impedance spectrum plot (8B) superimposed with the EIS reference spectrum plot (8E) of the first example of step chirp (26B). Figure 19 evidences that there is substantial agreement between the step chirp impedance spectrum plot (8B) and the EIS reference spectrum plot (8E); although noise increases at higher frequency. However, a frequency at 2000 Hz only includes twenty data points per period and step chirp (26B) includes only one period per frequency. The noise may be corrected by including sufficient data points to average out the noise at higher frequency. This can be accomplished by either increasing the sampling rate to higher than about 40 kHz or increasing the number of periods.

STEP CHIRP EXAMPLE II.

Now, with primary reference to Figures 20 and 21 which respectively illustrate the step chirp response time record (23B) of the test device (3), and the resultant step chirp impedance spectrum plot (8B) superimposed with the EIS reference spectrum plot (8E) of the second example of step chirp in which step chirp excitation time record (25B) remains the same as in the first example of step chirp except that 18 frequencies step down from 2 kHz in harmonic octaves. Figure 20 evidences that step chirp response time record (23B) is longer in this example compared to the step chirp response time record (23B) depicted in Figure 18 due to an increased number of octave frequencies. Figure 21 evidences that there is substantial agreement between the step chirp impedance spectrum plot (8B) and the EIS reference spectrum plot (8E); although the noise still increases at higher frequency. The noise may be corrected by increasing the sample rate or including additional periods at higher frequency. Adding more periods at higher frequencies to the excitation time record may not substantially increase the overall test duration.

STEP CHIRP EXAMPLE III.

Now, with primary reference to Figures 22 and 23 which respectively illustrate the step chirp response time record (23B) for the test device (3), and the resultant step chirp impedance spectrum plot (8B) superimposed with the EIS reference spectrum plot (8E) of the third example of step chirp (26B) in which step chirp excitation time record (25B) remains the same as in the first and second examples of step chirp (26B) except that 15 frequencies step down from 2 kHz in harmonic octaves and with additional periods added at higher frequencies in decreasing number 20, 10, 5, 3, 2, 1. . . stepping down to the lowest frequency. Figure 23 evidences that there is substantial agreement between the step chirp impedance spectrum plot (8B) and the EIS

reference spectrum plot (8E), and the additional periods added at higher frequency can substantially reduce the noise at higher frequencies.

STEP CHIRP EXAMPLE IV.

Now, with primary reference to Figures 24 through 25 which respectively illustrate the step chirp response time record (23B) of the test device (3), and the resultant step chirp impedance spectrum plot (8B) superimposed with the EIS reference spectrum plot (8E) of the fourth example of step chirp (26B) in which step chirp excitation time record (25B) remains the same as in the prior examples of step chirp (26B) except that 18 frequencies step down from 2 kHz in harmonic octaves and with additional periods added at higher frequencies in decreasing number 20, 10, 5, 3, 2, 1. . . stepping down to the lowest frequency. Figure 25 evidences that there is substantial agreement between the step chirp impedance spectrum plot (8B) and the EIS reference spectrum plot (8E) data, and the additional periods added at higher frequency can substantially reduce the noise at higher frequencies.

Now with primary reference to Figure 26, the remaining offset between the step chirp impedance spectrum plot (8B) and the EIS reference spectrum plot (8E) can be resolved by the addition of about 0.1mOhm to the real impedance of the step chirp impedance spectrum which results in the step chirp impedance spectrum plot (8B) overlaying the EIS reference spectrum plot (8E). The 0.1 mOhm offset may be due to differences in contact resistance between the two measurements.

STEP GROUP CHIRP

Now, with reference to Figure 27, rogue wave is defined as: signal peak/signal RMS. For a single sine wave with a unity peak amplitude ($V_P = 1$), the rogue wave is 1.414. Step chirp (26B) as above described makes a tradeoff between time record duration and a minimal rogue wave. As an illustrative example, in a step chirp (26B) with a step chirp excitation time record (25B) including 16 frequencies stepping down from 2 kHz by harmonic octaves with one period for each frequency the duration of a step chirp time record (25B) can be about 32.75 seconds and includes a rogue wave of about 1.414. When individual frequencies are added together in a sum-of-sines, the time record duration may be decreased, but the rogue wave may be increased. Figure 27 plots the rogue wave versus the number of octave harmonic sine waves in an SOS.

As evidenced by the plot in Figure 27, including four sine waves with octave harmonic separation within a SOS can be utilized in an excitation signal (26) for sequential stepping in

frequency groups (59)(also referred to as "step group" or "group chirp (26C)") rather than stepping as single sine waves since there is a local minimum in the rogue wave factor. However, the illustrative example of four sine waves within an SOS is not intended to preclude other embodiments including frequency groups (59) having less than (as examples 2 or 3) or more than four (as examples, 8, 12, 16...) sine waves within a SOS, including groups that have harmonic or non-harmonic separation. In the illustrative example using four sine waves in a frequency group (59), the rogue wave factor was 1.75. In particular embodiments, group chirp (26C) can further include additional periods at higher frequencies. For example, the highest frequency group including 2 kHz, may include 20 periods. For step SOS with frequency groups (59) of 4 with 16 frequencies stepping down from 2 Hz and the highest frequency group (59) having 20 periods with a time duration of about 17.55 sec.

Now, with general reference to Figures 28 through 35, the illustrative examples of group chirp (26C) were implemented based upon 16 frequencies (11) with each frequency group (59) having four frequencies (11). The simulated test electrical circuit (4) was used in each of the first two examples of group chirp (26C). The first example of group chirp (26C), implemented a step group chirp excitation time record (25C) which stepped up from 0.05 Hz by harmonic octaves include 16 frequencies with four frequencies within each frequency group (59). The second example of step group chirp (26C), implemented a step group chirp excitation time record (25C) which stepped down from 2 kHz by harmonic octaves to include 16 frequencies (11) with four frequencies within each frequency group (59). In both examples, the highest different frequency group included twenty periods of the lowest frequency within the group; the next highest frequency group included five periods of the lowest frequency within the group; the penultimate frequency group included three periods of the lowest frequency within the group; the lowest frequency group included 1 period of the lowest frequency within the group. In each example, TCTC was used to process the step group chirp response time record (23C) and the steady state assumption was realized by deleting the initial portion (56)(about 20%; although a greater or lesser portion can be deleted depending upon the application) of the step group chirp response time record (23C) in each frequency group (59).

STEP GROUP CHIRP EXAMPLE I. Now, with primary reference to Figures 28 and 29, in the first simulation of step group chirp (26C), Figure 28 depicts a step chirp response time record (23C) of the step group chirp response signal (24C) of the test electronic circuit (4) to the step group chirp SOS current excitation signal (26C), and Figure 29 depicts the step chirp impedance

spectrum plot (8C) for the TCTC processed step group chirp response time record (23C) of the test electronic circuit (4) superimposed with the ideal *jw* impedance spectrum plot (8D).

STEP GROUP CHIRP EXAMPLE II. Now, with primary reference to Figures 30 and 31, in the second simulation of group chirp (26C), Figure 30 depicts a step group chirp response time record (23C) of the step group chirp response signal (24C) of the test electronic circuit (4), and Figure 31 depicts the step chirp impedance spectrum plot (8C) for the TCTC processed step group chirp response time record (23C) of the test electronic circuit (4) superimposed with the ideal *jw* impedance spectrum plot (8D).

Illustrative examples of impedance measurements (2) of the test device (3) using step group chirp (26C) were performed using an IMD (1) as above described. The RMS of the excitation current was about 500 mA, otherwise all the parameters of the excitation signals (26) were established substantially as above described. The test device (3) was substantially equivalent or equivalent to the test device (3) above described and depicted in Figure 4. The EIS reference spectrum plot (8E) used for all of the illustrative impedance measurements of the test device (3) was a plot of data obtained using a Solartron Potentiostat Galvanostat instrument. The nominal parameters for the EC were: Rl=15 mOhm, R2=15 mOhm, R3=15 mOhm, C1=9F. The impedance measurements (2) were calibrated in order to account for gains and frequency response of the IMD (1) by performing measurements with a shunt (57) of known value with substantially identical measurement conditions as performed with the test device (3). The shunt response time record (58) from the shunt (57) was normalized to the shunt value. The step group response time record (23C) and the normalized shunt response time record (58) were transformed to the frequency domain and the ratio recorded as measured impedance of the test device (3).

STEP GROUP CHIRP EXAMPLE III. Now, with primary reference to Figures 32 and 33, in a third example of step group chirp, the step group excitation time record (25C) is the same as used in the first and second simulations of group chirp (26C) with the RMS excitation current of 500 mA with 16 frequencies stepping up from 0.05 Hz applied to a physical test device (3) and a 50 mOhm shunt (57). The step group chirp response time records (23C) were captured and processed with TCTC substantially as performed in the first and second simulations of group chirp (26C). Figure 32 depicts the step group excitation time record (57A) including a plot of the step group chirp excitation signal (57B), and Figure 33 depicts the group chirp impedance spectrum plot (8C) of the step group chirp response time record (23C) of the test device (3) processed using TCTC superimposed with the EIS reference impedance spectrum plot (8E). An offset of about

+0.5 mOhm can be added to group chirp SOS impedance spectrum (8C) resulting in a substantial match with the EIS impedance reference spectrum plot (8E).

STEP GROUP CHIRP EXAMPLE IV. Now, with primary reference to Figures 34 and 35, in a fourth example of step group chirp (26C), the step group chirp excitation time record (25C) was as used in the prior examples of step group chirp (26C) with the RMS excitation current of 500 mA with 16 frequencies stepping down from 2000 Hz applied to the test device (3) and a 50 mOhm shunt (57). The step group chirp response time records (23C) were captured and processed with TCTC substantially as performed in the prior examples of step group chirp (26C). Figure 34 depicts the step group chirp excitation time record (57A) including the step group chirp excitation signal (57B), and Figure 35 depicts the group chirp impedance spectrum plot (8C) of the step group chirp response time record (23C) of the test device (3) processed using TCTC superimposed with the EIS reference impedance spectrum plot (8E).

As evidenced by the above examples, step group chirp (26C) can be performed with advantageous results in both analytical simulations using the electrical test circuit (4) and physical test devices (3). In particular embodiments, the initial portion (56) of each SOS chirp group response signal (24C) can be discarded to validate the steady state assumption and the step group chirp response time record (23C) processed with TCTC. Additionally, while the examples took advantage of the local minimum including four frequencies for the rogue wave depicted in Figure 27; this is not intended to preclude the use of embodiments using other frequency spreads based on the application.

Further illustrative examples of step group chirp (26C) were implemented by the IMD (1) based upon an step group chirp excitation time record (25C) to generate a step group chirp excitation signal (26C) at an RMS excitation current of 500 mA including 18 frequencies occurring in a range of about 0.125 Hz to about 1638.4 Hz with the first four frequency groups (59) including four frequencies and the fifth frequency group including two frequencies with additional periods at higher frequencies. Figure 36 depicts a plot of the step group chirp excitation signal (57B) over time in seconds. Note that an SOS with 18 frequencies yields a rogue wave factor of 3.17 but the frequency groups with 2 or 4 frequencies within each group have a rogue wave factor of about 1.7, as depicted in Figure 21.

STEP GROUP CHIRP EXAMPLE V. Now, referring primarily to Figures 37 and 38 which respectively depict a plot of the test device voltage response (24C) over time in seconds and the Nyquist step chirp spectrum plot (8C) of the impedance spectrum (7) for the step group chirp

response time record (23C) of the test device (3) processed using TCTC superimposed with the EIS reference impedance spectrum (8E) for the test device (3) which evidences that the test device impedance measurement (2) performed using group chirp (26C) results in a substantial match with the EIS reference impedance spectrum (8E) for the test device (3). The step group chirp time response time record (23C) was processed using TCTC and the steady state assumption was achieved by deleting the initial portion (56) of step chirp response time record (23C) of each frequency group (59) (in the examples of Figures 36 through 41 the initial portion (56) comprises an initial portion of 20%).

STEP GROUP CHIRP EXAMPLE VI. Now, with general reference to Figures 39 and 40, a further illustrative example of step group chirp (26C) was implemented by the IMD (1) based upon a harmonic frequency sweep over decades structured to yield seven harmonic frequencies (11) per decade: 1, 2, 3, 4, 5, 7, 9 and assembling an step group chirp excitation time record (25C) to generate an excitation signal at an RMS excitation current of 500mA including four decades with the starting frequency in each decade: 0.1, 1, 10, 100 yielding a total of 28 frequencies. The group SOS rogue wave constant is 2.657.

The frequency distribution factor for these frequency groups is:

$$\sqrt{\frac{2}{7}}$$

Without the step group chirp separation, the full SOS excitation for 28 frequencies, would have a distribution factor of:

$$\sqrt{\frac{2}{28}}$$

The group chirp time response time record (23C) was processed using TCTC and the steady state assumption was achieved by deleting the initial portion (56) of the step group chirp response time record (23C) of each frequency group (59) (in the examples of Figures 39 and 40) the initial portion comprises the initial portion of 20%).

Figure 39 depicts a plot of the group chirp response time record (25C) of the group chirp SOS current response signal (24C), as above described, and Figure 40 depicts the Nyquist step group chirp plot (8C) of the impedance spectrum for the TCTC processed step group chirp response time record 23C) of the test device (3) superimposed with the EIS reference spectrum

plot (8E). Figure 40 evidences a substantial match with the EIS reference impedance spectrum plot (8E) for the test device (3).

STEP GROUP CHIRP EXAMPLE VII. Now, with primary reference to Figures 41 and 42, a further illustrative example of step group chirp (26C) was implemented by the IMD (1) based upon establishing frequencies separated by a factor of $\sqrt{2}$ for a total of 29 frequencies. Although this may not comprise a harmonic frequency sweep, the IMD (1) can assemble the step group chirp excitation time record (25C) to generate a step group excitation signal (26C) at an RMS excitation current of 500 mA comprised of frequency groups (59) of every other frequency to achieve octave harmonics. Thus, the sequence of frequencies assigned to each group can be reformatted to achieve the desired 29 frequency spread while keeping octave harmonic separation within each frequency group. The time step group chirp response time record (23C) was processed using TCTC and the steady state assumption was achieved by deleting the initial portion (56) of step group chirp response time record (23C) of each frequency group (59) (in the examples of Figures 41 and 42 the initial portion (56) comprises an initial portion (56) of 20%).

Now, referring to Figure 41 which depicts the step group chirp response time (23C) for the test device (3) and Figure 42 depicts the step group chirp impedance spectrum plot (8C) superimposed with EIS reference impedance spectrum plot (8E). The step group chirp response time record (23C) has a duration comparable to a 20 second HCSD SOS time record of 16 frequencies with a rogue wave of about 3 and a frequency distribution factor of $\sqrt{\frac{2}{16}}$. By comparison, this step group chirp (26C) approach yields a rogue wave factor of about 1.7 and a frequency distribution factor of about 0.7. This comprises a substantial improvement, however, this approach doubles the time record.

STEP GROUP CHIRP EXAMPLES VIII AND IX. Now, with general reference to Figures 43 through 48, in particular embodiments, a very high-fidelity impedance spectrum can also be achieved using step group chirp (26C) at the expense of greater duration in the time records. For example, the root-2 separation in the prior Example VII can be increased to a cube-root of 2 (2^⅓) for 43 frequencies, where every third frequency is an octave harmonic. Alternatively, the step group chirp excitation signal (26C) could be developed based on a user-selected number of points per decade of frequency. For example, 10 points per decade of frequencies between 0.1 and 2 kHz would result in 38 frequencies (11) in a linear scale or 39 frequencies in a logarithmic scale. The frequency groups (59) would be selected such that the rogue wave is minimized in

either case (as described above). Processing the step group chirp response time record (23C) with TCTC, may obviate the need for harmonic separation between frequencies in frequency groups.

In particular embodiments, the step group chirp excitation time record (26C) can be supplemented with offset frequency groups (60). As an illustrative example, the step group chirp excitation time record (25C) can include 18 frequencies with octave harmonic separation comprising four groups (59) each including four frequencies and a fifth frequency group (59) including two frequencies, and where additional fidelity is required (for example, at about 1 Hz), then offset frequency groups (60), offset by the square-root of 2 (0.28 Hz, 0.57 Hz, 1.13 Hz, 2.26 Hz) can be added to the step group chirp excitation time record (25C) after the second frequency group (0.2 Hz, 0.4 Hz, 0.8 Hz, and 1.6 Hz), additional offset groups (60) can also be added to ensure sufficient fidelity in a range of interest.

Again, with primary reference to Figures 43 through 48, this illustrative example of step group chirp (26C) used a recursive model electrical circuit (4) as depicted in Figure 4, the IMD (1) assembled step group chirp excitation record (25C) for Example VIII (Figures 43 and 44) including 16 frequencies comprised of 4 frequency groups, each having 4 frequencies to afford the advantage of the local minimum for crest factor. The 16 frequencies (11) comprising octave harmonics starting at 0.0125 Hz and ending at 409.2 Hz. In Example IX (Figures 45 and 46), the IMD (1) assembled a step group chirp time excitation record (25C) for high resolution group chirp including, the first 2 frequency groups (59) as octave harmonic, the third frequency group (59) included offset frequencies (60) of those frequencies in the second frequency group (59) with the frequencies (11) adjusted by a factor of 2 to the 1/3 power, the fourth frequency group (59) included those frequencies in the second frequency group but those frequencies were adjusted by a factor of 2 to the 2/3 power, and the final two frequency groups (59) were a continuation of octave harmonic for a total of 24 frequencies. The recursive model test circuit (4) step group chip response time records (23C) were obtained for each of the examples (Figures 43 and 45) and processed using TCTC. The *jw* Nyquist plot (8D) of the model test electrical circuit (4) of each example is depicted Figures 44 and 46 respectively. In this illustrative example, the only disadvantage to the use of the high resolution step group chirp (26C) may be an increase in the time record of about 15 seconds. The crest factor and the frequency distribution factor remained substantially the same.

Broader ranges of frequencies can also be considered with step chirp (26B) and step group chirp (26C). Higher frequencies may require multiple periods to ensure capture of sufficient data points for accurate impedance calculations. Lower frequencies may have reduced sampling rates

provided there are sufficient datapoints to achieve good signal-to-noise ratios in the impedance calculation. For example, a minimum frequency of 0.00125 Hz can be used (an order of magnitude lower than the 0.0125 Hz in previous examples). Assuming a cube-root of 2 separation a frequency groups of four frequencies in each frequency group), the excitation time record would yield 62 frequencies through 1651.4 Hz. The time records would have duration of 2560 seconds (42.7 minutes).

In another embodiment, a sequence of frequency groups (59) in a step group chirp excitation time record (25C) may include one or more pre-selected target frequencies (61) included within the sequence of frequency groups (59). As an example, an impedance measurement having a pre-selected target frequency (61) at 42 Hz with a starting frequency of 0.0125 Hz and an ending frequency near 2 kHz. The frequency group (59) that encompasses or is nearest to the target frequency (61) of 42 Hz can be shifted to include 42 Hz in the illustrative example. Assuming octave harmonic separation, the nearest frequency group to the target frequency (61) of 42 Hz would include frequencies 51.2 Hz, 102.4 Hz, 204.8 Hz, and 409.6 Hz. This frequency group could be shifted by a scaling factor of 0.82 to formulate a new frequency group including 42 Hz, 84 Hz, 168 Hz, and 336 Hz. Further, in cases where the targeted frequency (61) tends to shift as a function of age and use of the device (3) as depicted in Figure 2, an impedance spectrum can be generated periodically over time and the impedance spectrum can be analyzed by direct observations of the calculated impedance data or equivalent circuit modeling to identify the shift and adjust the targeted frequency (61) to mitigate accumulating error due to drift.

STEP GROUP CHIRP EXAMPLE XI. Now, with primary reference to Figures 47 and 48 , in particular embodiments, the maximum number of frequencies (11) to be included within an impedance measurement (2) (for example, 30 frequencies) can be pre-selected, the excitation time record (25) can be assembled using a logarithmic scale to calculate the total number of frequencies required to reach the example target frequency (61) of 42 Hz (16 frequencies in this case) which can used to determine the spacing between frequencies. The resulting excitation time record (25) produces 42 Hz at the sixteenth frequency and includes a total of 23 frequencies with a maximum of 1857.3 Hz. As depicted in Figure 48, the rogue wave (Peak/RMS) for the twenty third frequency equals 3.8273 with the local minimum at the seventh frequency equals 2.03. Thus, this approach can be used with step group chirp, where each frequency group includes seven frequencies, and processed using TCTC. Further, in cases where the targeted frequency (61) tends to shift as a function of age and use of the device (3) as depicted in Figure 2, an

impedance spectrum can be generated periodically over time and the impedance spectrum can be analyzed by direct observations of the calculated impedance data or equivalent circuit modeling to identify the shift and adjust the targeted frequency (61) to mitigate accumulating error due to drift.

MIXED STEP CHIRP AND STEP GROUP CHIRP. In particular embodiments, it may be useful to include one or more specific target frequencies (61) in a sequence by combining the step chirp (26B) and step group chirp (26C) sequences. In this approach, a step chirp-group chirp excitation time record (25) can be assembled based on the required upper and lower frequency limits. The resulting excitation time record (25) would include step group chirp (26C) frequency groups (59) interspersed with step chirp (26B) single frequencies. Although this approach may require time records of greater duration, it may be useful for a pre-selected set of frequencies of interest for diagnostic purposes. In this case, multiple periods at the targeted frequencies could be conducted for improved measurement accuracy at critical points. Further, in cases where the targeted frequency tends to shift as a function of age and use as depicted in Figure 2, the full-spectrum algorithm analysis could be used to identify the shift and adjust the targeted frequency to mitigate accumulating error due to drift and adjust the excitation signal accordingly.

Now, with primary reference to Figure 49, embodiments include a method of assembling an excitation time record for step chirp including one or more of specifying a frequency range (B1), specifying the separation between frequencies in the frequency range (B2), specifying the number periods for each frequency (B3), identifying the sample rate for each frequency (B4), identifying the number of data points collected for each frequency (B5), determining the response time record analysis algorithm (B6), selecting TCTC (B7) or selecting HCSD (B8), and if HCSD, then adding a negative time period to each frequency (B9), combining the sequence of frequencies into a continuous excitation time record (B10), and generating a excitation time record (B11) for step chirp impedance measurement of a test device (3), for example, an electrochemical cell.

Now, with primary reference to Figure 50, embodiments include a method of assembling an excitation time record for step group chirp including one or more of specifying a frequency range (B12), specifying the separation between frequencies in the frequency range (B13), specifying the number frequencies per frequency group (B14), wherein specifying the number of frequencies per group can further include selecting the frequencies per group to minimize the rogue wave (B15); identifying the sample rate for each frequency group (B16), identifying the number of data points collected for each frequency group (B17), determining if a sufficient

number of samples have been collected in each frequency group (B18), and if no, adding additional periods to frequency groups having an insufficient number samples collected (B19); determining the response time record analysis algorithm (B20), selecting TCTC (B21) or selecting HCSD (B22), and if HCSD, then adding a negative time period to each frequency group (B23), combining the sequence of frequencies into a continuous excitation time record (B24), and generating a excitation time record (B25) for group chirp impedance measurement of a test device (3), for example, an electrochemical cell.

Now, with primary reference to Figure 51, embodiments include a method of capturing a response time record including one or more of identifying a sample rate of said response signal of the device under test (26), identifying the number of samples collected in the response signal (B27), capturing a response time record of the EC under test (B28), determining whether impedance measurement complete (B29), if yes, then stop data capture of response time record (B30), and if no, determine whether sample rate should be changed (B31), and if no, capturing response time record (B28), and if yes, identifying sample rate (B26).

Now with primary reference to Figure 52, embodiments include a method of performing impedance measurement of a device with step group chirp comprising one or more of: assembling frequency groups (B32) including specifying a frequency range, specifying the separation between frequencies in the frequency range, and specifying the number frequencies per frequency group, wherein specifying the number of frequencies per group can further include selecting the frequencies per group to minimize the rogue wave (B33), supplementing the frequency groups with frequency group shifts (B34), determining measurement parameters for frequency group shifts and location of the frequency group shifts to acquire sufficient fidelity in frequencies of interest (B35) including one or more of: identifying the sample rate for each frequency group, identifying the number of data points collected for each frequency group, determining if a sufficient number of samples have been collected in each frequency group, and if no, adding additional periods to frequency groups having an insufficient number samples collected, selecting an impedance spectrum algorithm, for example TCTC or HCSD, and if HCSD, then adding a negative time period to each frequency group, combining the sequence of frequencies into a continuous excitation time record, and generating a excitation time record for high-fidelity group chirp impedance measurement of the test device, for example an electrochemical cell (B36), exciting the test device using the excitation time record including a root mean squared current or a root mean squared voltage in a sequence of one or more frequency groups, wherein each of said frequency groups includes a summation of one or more frequencies within a frequency spread

(B37), recording a response time record of a response of the test device (3) to the excitation time record (B38), discarding an initial time period of said response time record of each of said one or more frequency groups (B39), and processing the response time record using the impedance spectrum algorithm to determine impedance of the test device (3) (B40).

Now with primary reference to Figure 53, embodiments include a method of performing high-fidelity impedance measurement of a device (3) with step group chirp comprising one or more of: assembling frequency groups (B41) including specifying a frequency range, specifying the separation between frequencies in the frequency range, and specifying the number frequencies per frequency group, wherein specifying the number of frequencies per group can further include selecting the frequencies per group to minimize the rogue wave (B42), identifying one or more target frequencies (B43), identifying frequency groups closest to or encompassing the target frequencies (B44); shifting frequency groups closest to target frequencies to include target frequency or supplementing the frequency groups closest to target frequencies to include target frequencies (B45), identifying additional target frequency (B46), if yes, repeat procedures (B44) and (B45), if no, generating a excitation time record for group chirp impedance measurement of the test device (3) (B47), exciting the test device (3) using the excitation time record including a root mean squared current or a root mean squared voltage in a sequence of one or more frequency groups, wherein one or more frequency groups include the target frequencies, wherein each of said frequency groups includes a summation of one or more frequencies within a frequency spread (B48), recording a response time record of a response of the test device (3) to said excitation time record (B49), discarding an initial time period of said response time record of each of said one or more frequency groups (B50), and processing the response time record using the impedance spectrum algorithm to determine impedance of the test device (3) (B51), assessing shift in target frequency (B52), if yes, adjust target frequencies in the excitation time record (B53) for the next measurement sequence.

As can be easily understood from the foregoing, the basic concepts of the present invention may be embodied in a variety of ways. The invention involves numerous and varied embodiments of an IMD configured to perform impedance spectroscopy to provide rapid, broadband impedance measurements of electrochemical cells, such as: battery packs, modules or cells or combinations or components thereof using chirp, step chirp, or group chirp excitation signals, or combinations thereof, including the best mode.

As such, the particular embodiments or elements of the invention disclosed by the description or shown in the figures or tables accompanying this application are not intended to

be limiting, but rather illustrative of the numerous and varied embodiments generically encompassed by the invention or equivalents encompassed with respect to any particular element thereof. In addition, the specific description of a single embodiment or element of the invention may not explicitly describe all embodiments or elements possible; many alternatives are implicitly disclosed by the description and figures.

It should be understood that each element of an apparatus or each step of a method may be described by an apparatus term or method term. Such terms can be substituted where desired to make explicit the implicitly broad coverage to which this invention is entitled. As but one example, it should be understood that all steps of a method may be disclosed as an action, a means for taking that action, or as an element which causes that action. Similarly, each element of an apparatus may be disclosed as the physical element or the action which that physical element facilitates. As but one example, the disclosure of a "impedance measurement" should be understood to encompass disclosure of the act of "impedance measuring" -- whether explicitly discussed or not -- and, conversely, were there effectively disclosure of the act of "impedance measuring", such a disclosure should be understood to encompass disclosure of a "impedance measurement" and even a "means for impedance measuring." Such alternative terms for each element or step are to be understood to be explicitly included in the description.

In addition, as to each term used it should be understood that unless its utilization in this application is inconsistent with such interpretation, common dictionary definitions should be understood to be included in the description for each term as contained in Merriam-Webster's Collegiate Dictionary, each definition hereby incorporated by reference.

All numeric values herein are assumed to be modified by the term "about", whether or not explicitly indicated. For the purposes of the present invention, ranges may be expressed as from "about" one particular value to "about" another particular value. When such a range is expressed, another embodiment includes from the one particular value to the other particular value. The recitation of numerical ranges by endpoints includes all the numeric values subsumed within that range. A numerical range of one to five includes for example the numeric values 1, 1.5, 2, 2.75, 3, 3.80, 4, 5, and so forth. It will be further understood that the endpoints of each of the ranges are significant both in relation to the other endpoint, and independently of the other endpoint. When a value is expressed as an approximation by use of the antecedent "about," it will be understood that the particular value forms another embodiment. The term "about" generally refers to a range of numeric values that one of skill in the art would consider equivalent to the recited numeric value or having the same function or result. Similarly, the antecedent

"substantially" means largely, but not wholly, the same form, manner or degree and the particular element will have a range of configurations as a person of ordinary skill in the art would consider as having the same function or result. When a particular element is expressed as an approximation by use of the antecedent "substantially," it will be understood that the particular element forms another embodiment.

Moreover, for the purposes of the present invention, the term "a" or "an" entity refers to one or more of that entity unless otherwise limited. As such, the terms "a" or "an", "one or more" and "at least one" can be used interchangeably herein.

Thus, the applicant(s) should be understood to claim at least: i) each IMD, ii) the related methods of exciting an IMD disclosed and described, iii) similar, equivalent, and even implicit variations of each of these devices and methods, iv) those alternative embodiments which accomplish each of the functions shown, disclosed, or described, v) those alternative designs and methods which accomplish each of the functions shown as are implicit to accomplish that which is disclosed and described, vi) each feature, component, and step shown as separate and independent inventions, vii) the applications enhanced by the various systems or components disclosed, viii) the resulting products produced by such systems or components, ix) methods and apparatuses substantially as described hereinbefore and with reference to any of the accompanying examples, x) the various combinations and permutations of each of the previous elements disclosed.

The background section of this patent application provides a statement of the field of endeavor to which the invention pertains. This section may also incorporate or contain paraphrasing of certain United States patents, patent applications, publications, or subject matter of the claimed invention useful in relating information, problems, or concerns about the state of technology to which the invention is drawn toward. It is not intended that any United States patent, patent application, publication, statement or other information cited or incorporated herein be interpreted, construed or deemed to be admitted as prior art with respect to the invention.

The claims set forth in this specification, if any, are hereby incorporated by reference as part of this description of the invention, and the applicant expressly reserves the right to use all of or a portion of such incorporated content of such claims as additional description to support any of or all of the claims or any element or component thereof, and the applicant further expressly reserves the right to move any portion of or all of the incorporated content of such claims or any element or component thereof from the description into the claims or vice-versa as

necessary to define the matter for which protection is sought by this application or by any subsequent application or continuation, division, or continuation-in-part application thereof, or to obtain any benefit of, reduction in fees pursuant to, or to comply with the patent laws, rules, or regulations of any country or treaty, and such content incorporated by reference shall survive during the entire pendency of this application including any subsequent continuation, division, or continuation-in-part application thereof or any reissue or extension thereon.

Additionally, the claims set forth in this specification, if any, are further intended to describe the metes and bounds of a limited number of the preferred embodiments of the invention and are not to be construed as the broadest embodiment of the invention or a complete listing of embodiments of the invention that may be claimed. The applicant does not waive any right to develop further claims based upon the description set forth above as a part of any continuation, division, or continuation-in-part, or similar application.

VI. CLAIMS

We claim:

1. A method for determining impedance of a device, comprising:

exciting said device using an excitation time record including a root mean squared current or a root mean squared voltage in a sequence of one or more frequency groups, wherein each of said one or more frequency groups includes a summation of one or more frequencies within a frequency spread;

recording a response time record of a response of said device to said excitation time record;

discarding an initial time portion of said response time record of each of said one or more frequency groups;

processing said response time record using an impedance spectrum algorithm; and

determining impedance of said device.

2. The method of claim 1, wherein said excitation time record comprises continuous excitation of said root mean squared current or root mean squared voltage including said one or more frequency groups.

3. The method of claim 1, wherein said excitation time record of each frequency group includes a plurality of frequencies and a duration of at least one period of the lowest frequency within said plurality of frequencies within said frequency group.

4. The method of claim 1, wherein said excitation time record of each of said one or more frequency groups includes one frequency and a duration of at least one period of said frequency.

5. The method of claim 1, wherein said impedance spectrum algorithm comprises time cross talk compensation.

6. The method of claim 1, wherein said excitation time record of each of said one or more frequency groups includes:

one or more frequencies having a harmonic separation and a duration of at least one period of said frequency; and

a negative time period preceding said at least one period of said frequency.

7. The method of claim 6, wherein said impedance spectrum algorithm comprises harmonic compensated synchronous detection.

8. The method of claim 1, wherein said initial time period of said response time record discarded from each of said one or more frequency groups occurs within a range of less than fifty percent of said period of said lowest frequency in said group.

9. The method of claim 1, wherein said excitation time record includes at least one frequency group having at least one target frequency.

10. The method of claim 1, wherein said one or more frequency groups comprise:

one or more base frequency groups, wherein each of said base frequency groups includes a summation of said one or more frequencies within said frequency spread;

one or more offset frequency groups, wherein each of said offset frequency groups includes a summation of said one or more frequencies within said frequency spread, said one or more offset frequency groups shifted in relation to said one or more base frequency groups.

11. The method of claim 9, further comprising modifying said at least one target frequency based on determining an impedance spectrum shift of said device.

12. The method of claim 11, further comprising determining said impedance spectrum shift directly based on calculated impedance data.

13. The method of claim 11, further comprising determining said impedance spectrum shift directly based on equivalent circuit modeling.

14. The method of claim 11, wherein said method for determining impedance of a device repeats based on exceeding a pre-defined impedance spectrum shift threshold value.

15. The method of claim 10, wherein said excitation time record includes at least one frequency group having at least one targeted frequency.

16. The method of claim 15, further comprising adjusting said targeted frequency based on said impedance spectrum shift.

17. The method of claim 1, wherein said one or more frequency groups determined based on a minimized rogue wave.

18. The method of claim 1, wherein a sample rate of said response time record adjusted based on period of lowest frequency of said one or more frequencies within said one or more frequency groups, wherein said sample rate of said response time record reduced as said period of lowest frequency increases, wherein said sample rate of said response time record increased as said

period of lowest frequency with said frequency group decreases within each said one or more frequency groups.

19. The method of claim 1, wherein said frequency spread within each frequency group comprises an octave harmonic.

20. The method of claim 1, wherein the frequency spread within each frequency group comprises a non-octave harmonic and said an impedance spectrum algorithm comprises time cross talk compensation.

FIG. 1

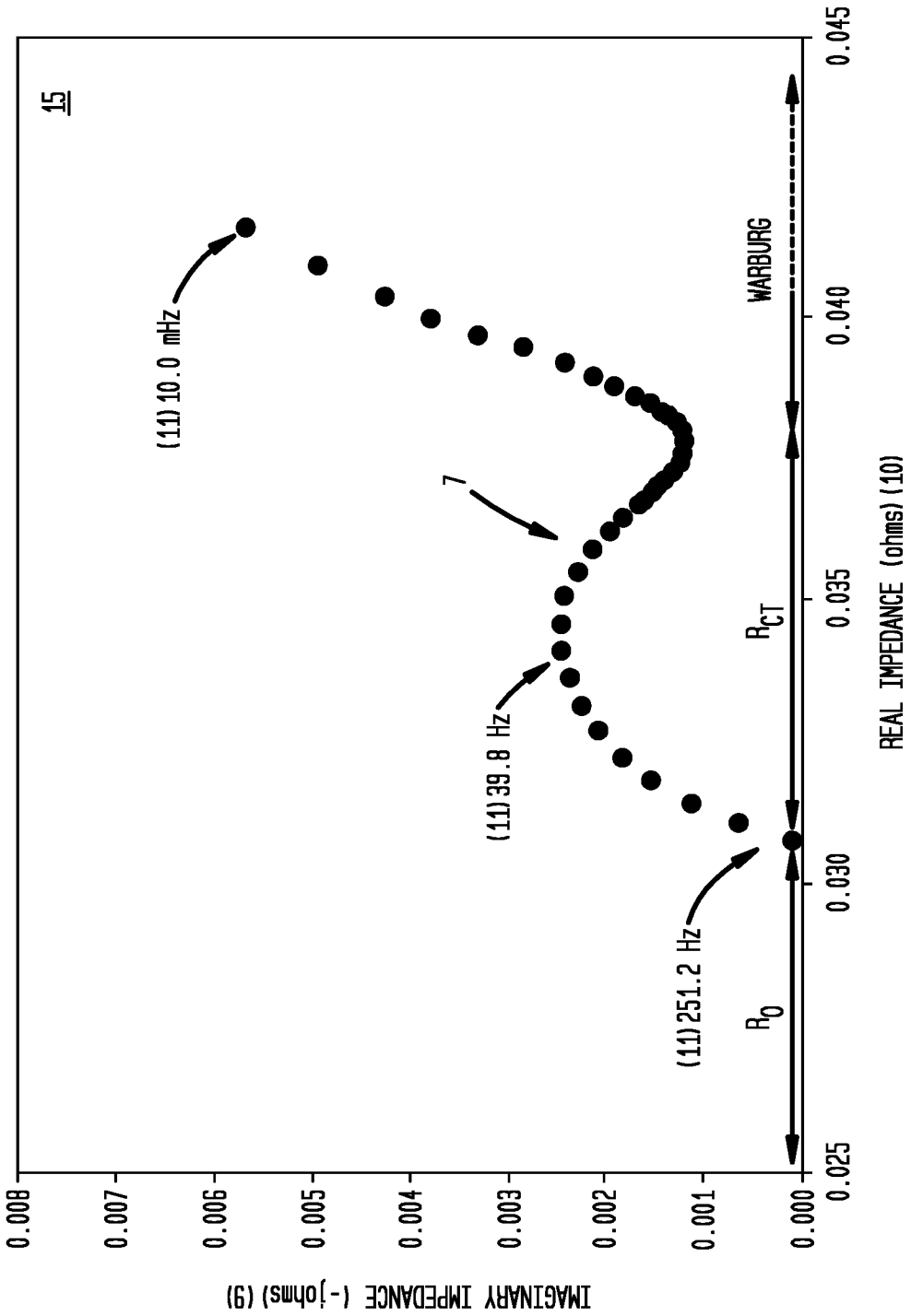

15
(11) 10.0 mHz
7
(11) 39.8 Hz
(11) 251.2 Hz
R_O
R_{CT}
WARBURG
0.000
0.001
0.002
0.003
0.004
0.005
0.006
0.007
0.008
0.025
0.030
0.035
0.040
0.045
IMAGINARY IMPEDANCE (-johms) (9)
REAL IMPEDANCE (ohms) (10)

FIG. 2

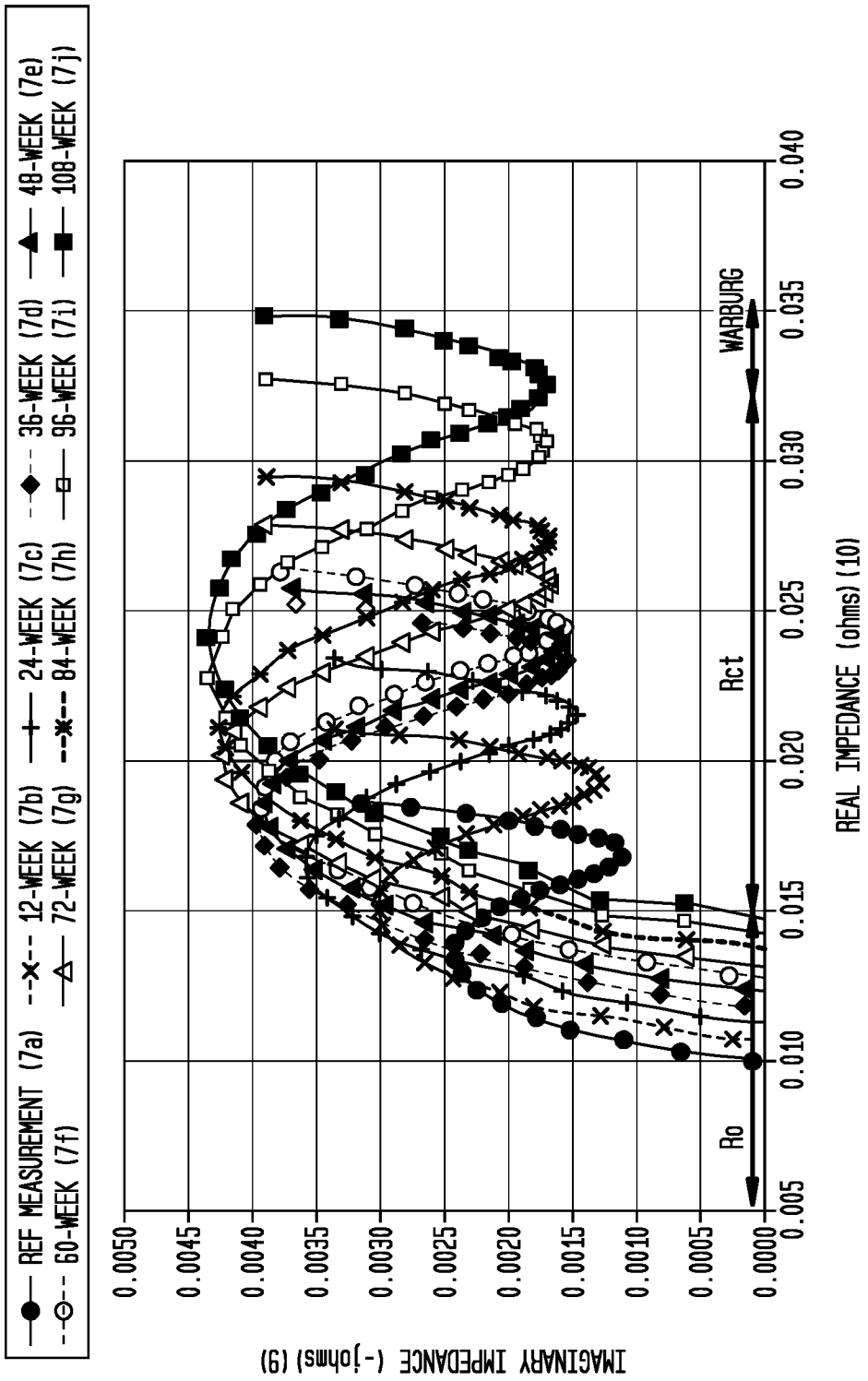

REF MEASUREMENT (7a)
12-WEEK (7b)
24-WEEK (7c)
36-WEEK (7d)
48-WEEK (7e)
60-WEEK (7f)
72-WEEK (7g)
84-WEEK (7h)
96-WEEK (7i)
108-WEEK (7j)
IMAGINARY IMPEDANCE (-johms)(9)
REAL IMPEDANCE (ohms)(10)
0.0050
0.0045
0.0040
0.0035
0.0030
0.0025
0.0020
0.0015
0.0010
0.0005
0.0000
0.005
0.010
0.015
0.020
0.025
0.030
0.035
0.040
Ro
Rct
WARBURG

FIG. 3A

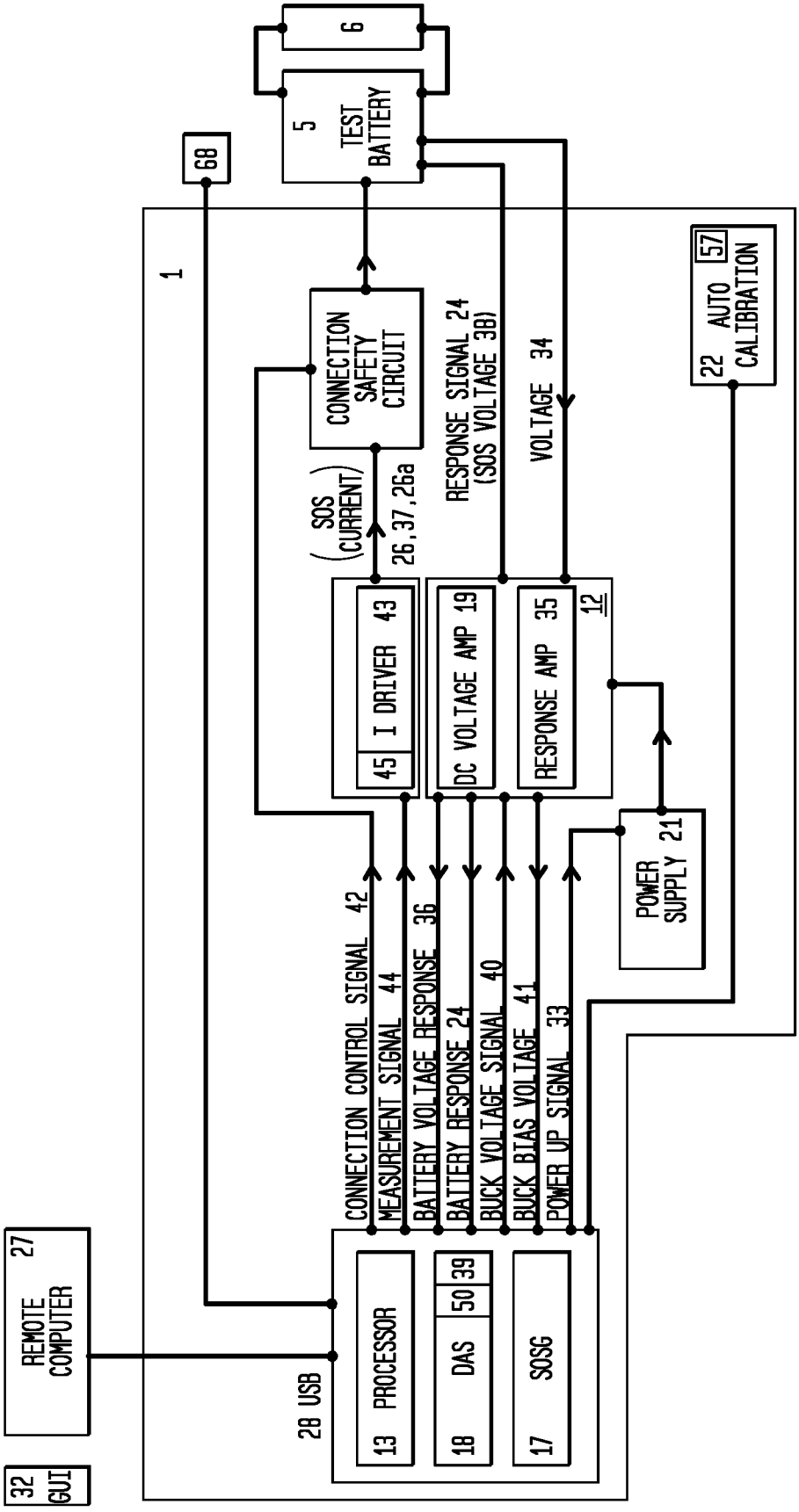

1
68
6
5 TEST BATTERY
CONNECTION SAFETY CIRCUIT
SOS (CURRENT) 26,37,26a
RESPONSE SIGNAL 24 (SOS VOLTAGE 38)
VOLTAGE 34
22 AUTO CALIBRATION 57
45 I DRIVER 43
DC VOLTAGE AMP 19
RESPONSE AMP 35
12
POWER SUPPLY 21
CONNECTION CONTROL SIGNAL 42
MEASUREMENT SIGNAL 44
BATTERY VOLTAGE RESPONSE 36
BATTERY RESPONSE 24
BUCK VOLTAGE SIGNAL 40
BUCK BIAS VOLTAGE 41
POWER UP SIGNAL 33
13 PROCESSOR
18 DAS 50 39
17 SOSG
28 USB
REMOTE COMPUTER 27
32 GUI

FIG. 3B

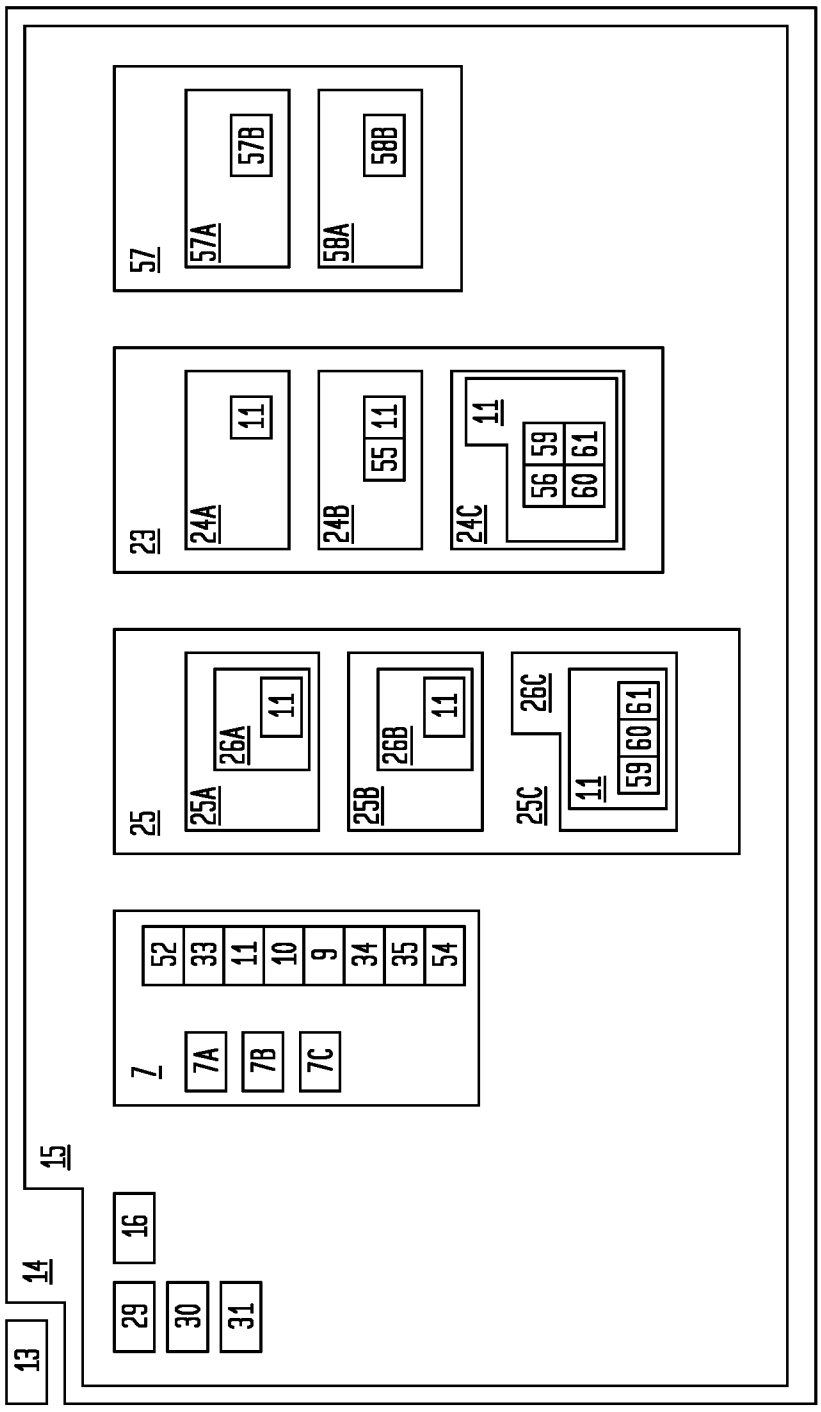

13
14
15
16
29
30
31
7
7A
7B
7C
52
33
11
10
9
34
35
54
25
25A
26A
11
25B
26B
11
25C
26C
11
59
60
61
23
24A
11
24B
55
11
24C
11
56
59
60
61
57
57A
57B
58A
58B

FIG. 4

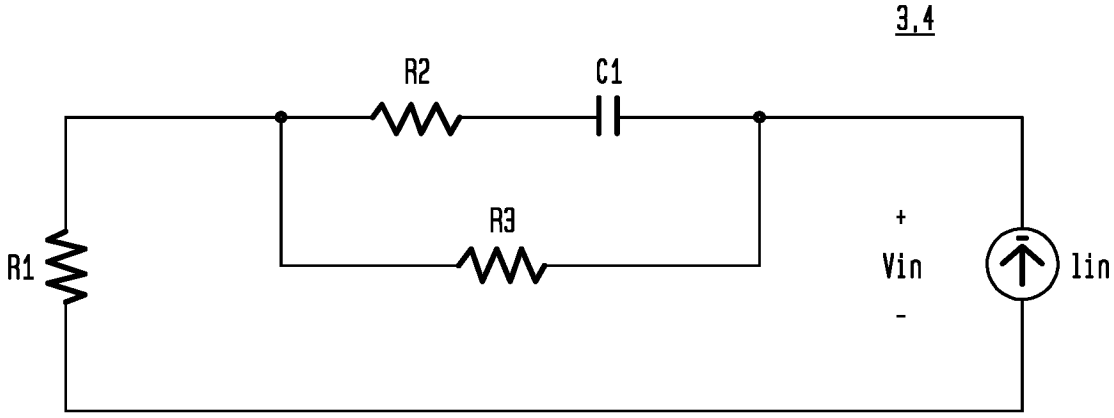


FIG. 5

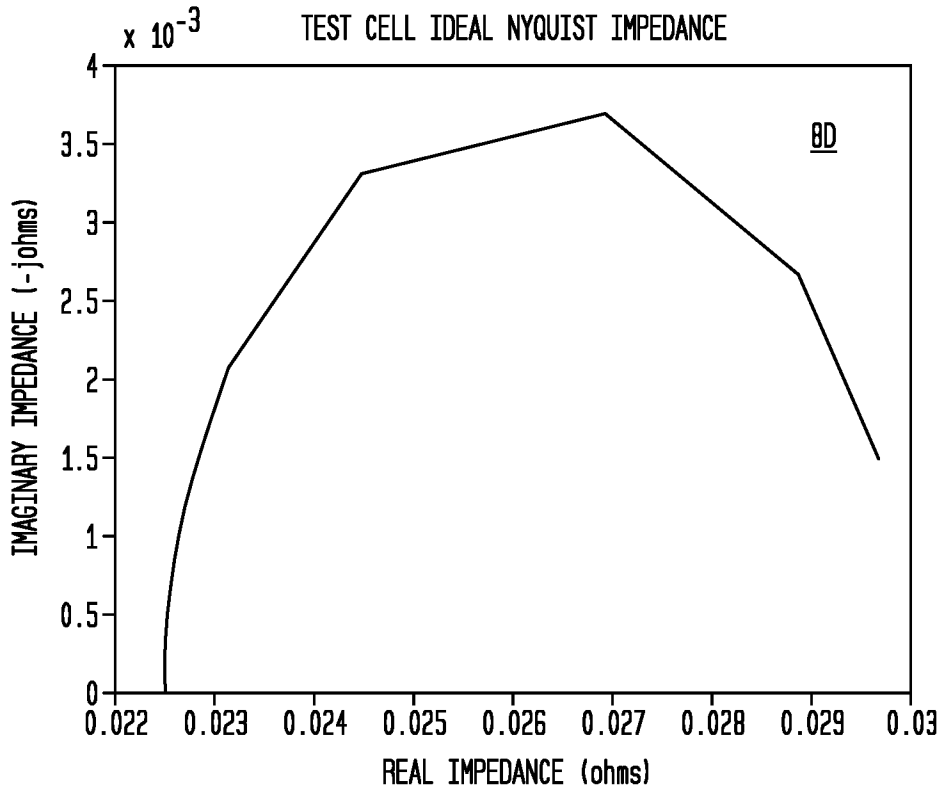

x 10^-3
TEST CELL IDEAL NYQUIST IMPEDANCE
8D
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
0
0.5
1
1.5
2
2.5
3
3.5
4
0.022
0.023
0.024
0.025
0.026
0.027
0.028
0.029
0.03

FIG. 6

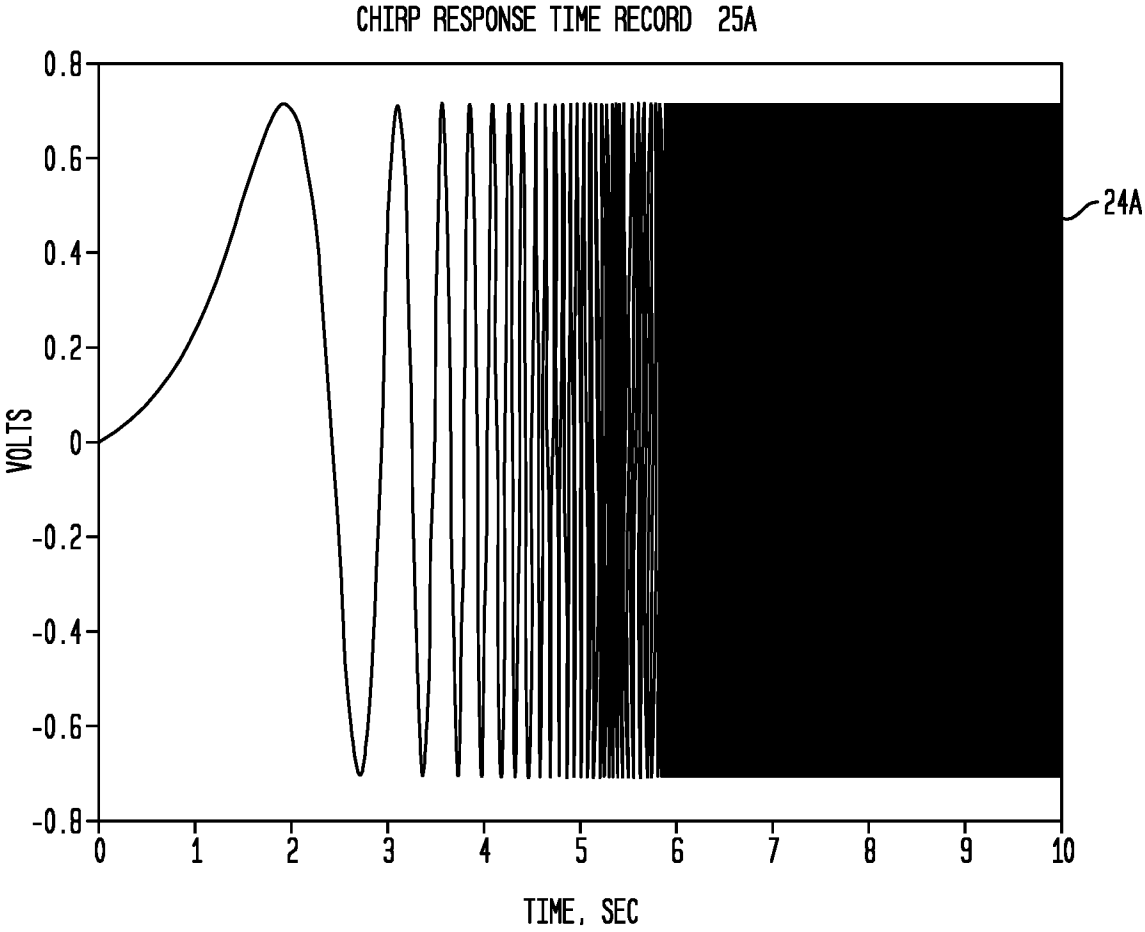

CHIRP RESPONSE TIME RECORD 25A
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
VOLTS
0
1
2
3
4
5
6
7
8
9
10
TIME, SEC
24A

FIG. 7

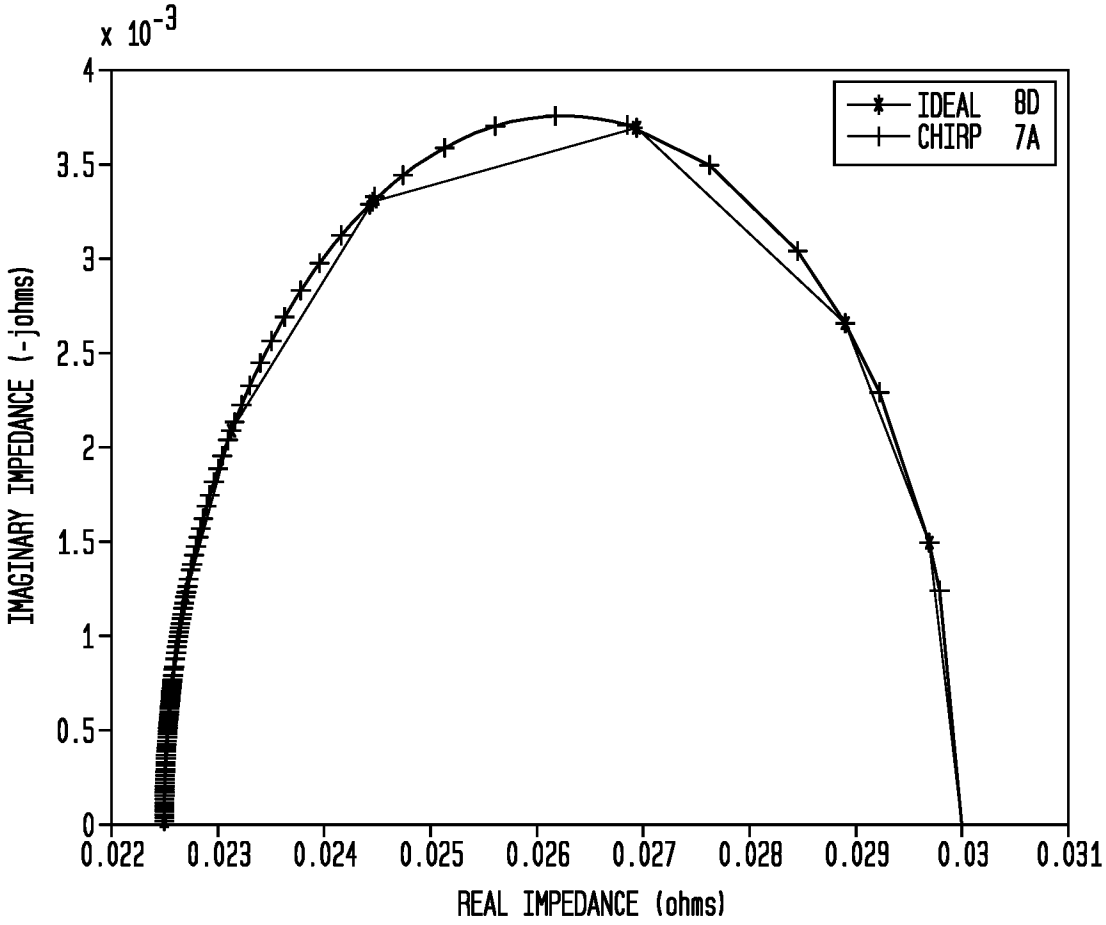

x 10-3
4
3.5
3
2.5
2
1.5
1
0.5
0
IMAGINARY IMPEDANCE (-johms)
IDEAL 8D
CHIRP 7A
0.022
0.023
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031
REAL IMPEDANCE (ohms)

FIG. 8

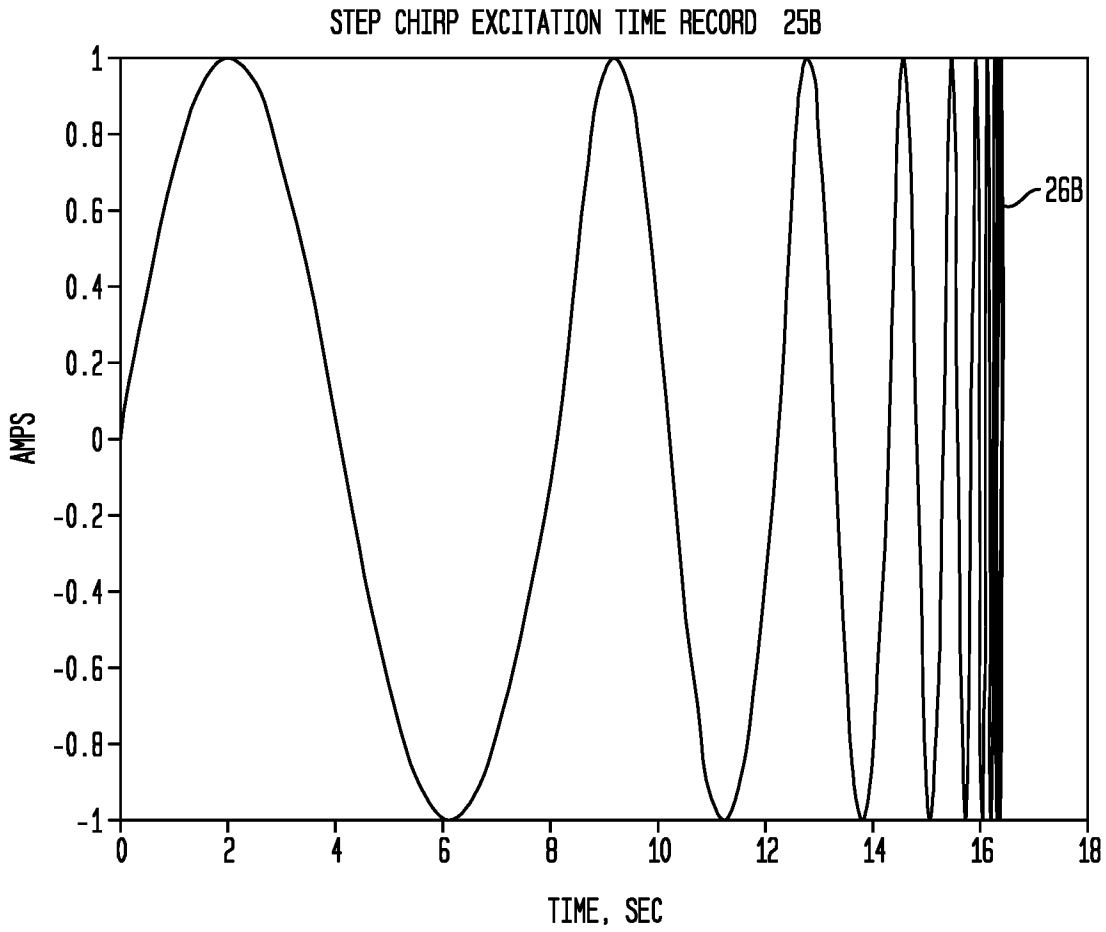

STEP CHIRP EXCITATION TIME RECORD 25B
AMPS
TIME, SEC
26B
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
2
4
6
8
10
12
14
16
18

FIG. 9

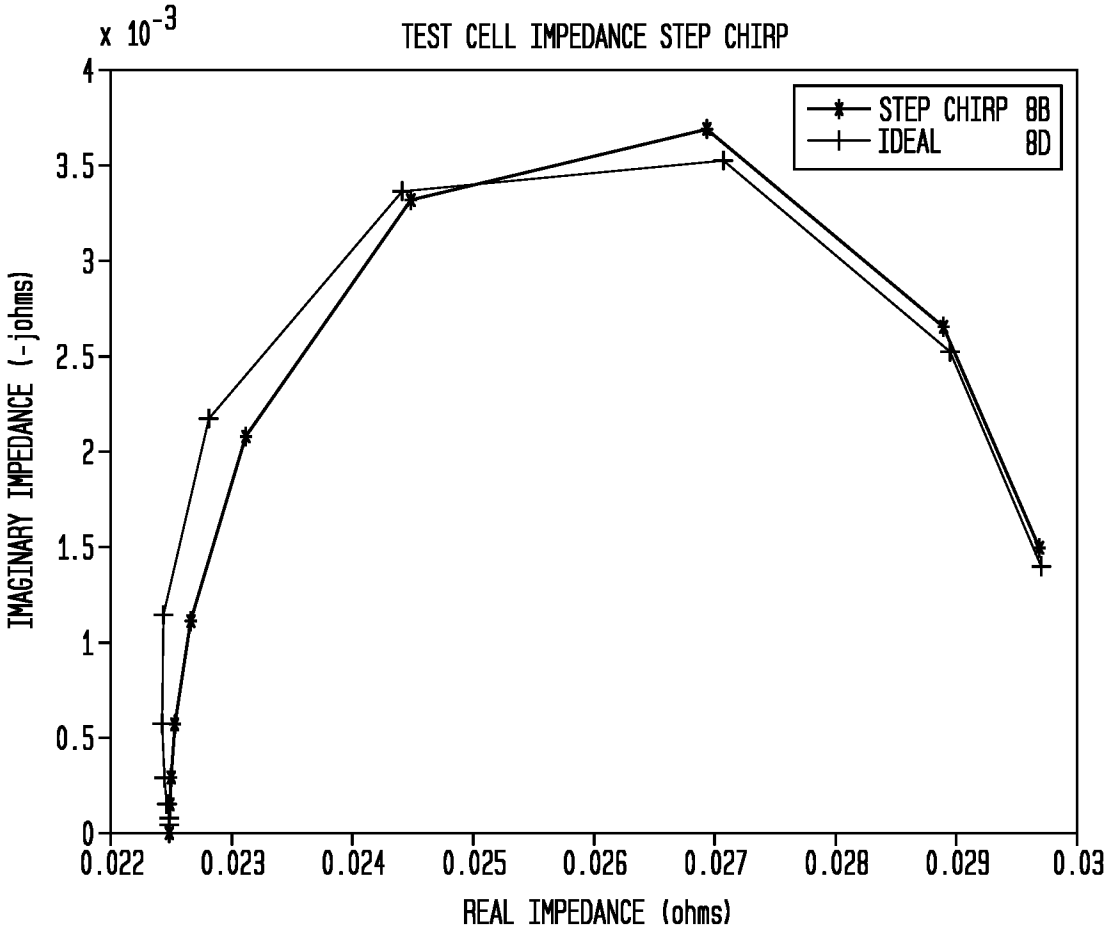

x 10^-3
TEST CELL IMPEDANCE STEP CHIRP
STEP CHIRP 8B
IDEAL 8D
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
4
3.5
3
2.5
2
1.5
1
0.5
0
0.022
0.023
0.024
0.025
0.026
0.027
0.028
0.029
0.03

FIG. 10

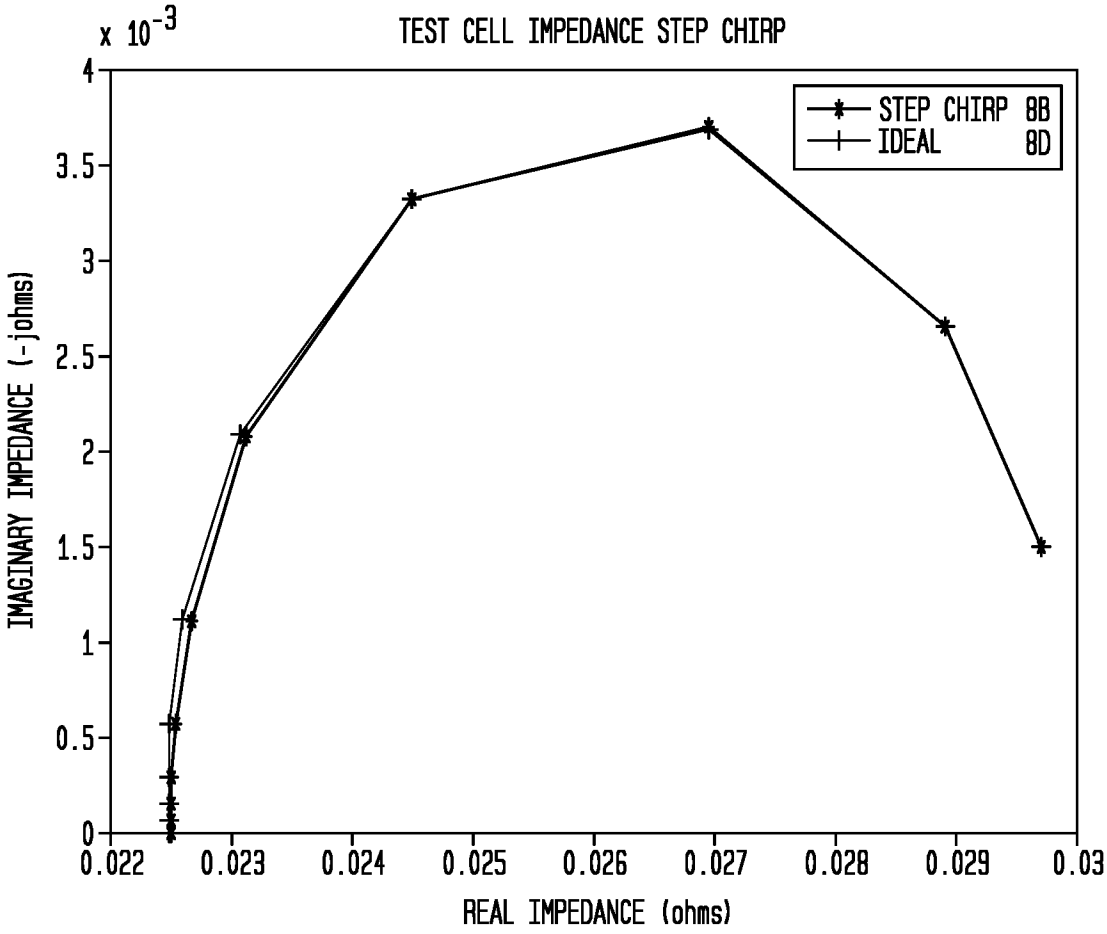

TEST CELL IMPEDANCE STEP CHIRP
x 10^-3
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
STEP CHIRP 8B
IDEAL 8D
0
0.5
1
1.5
2
2.5
3
3.5
4
0.022
0.023
0.024
0.025
0.026
0.027
0.028
0.029
0.03

FIG. 11

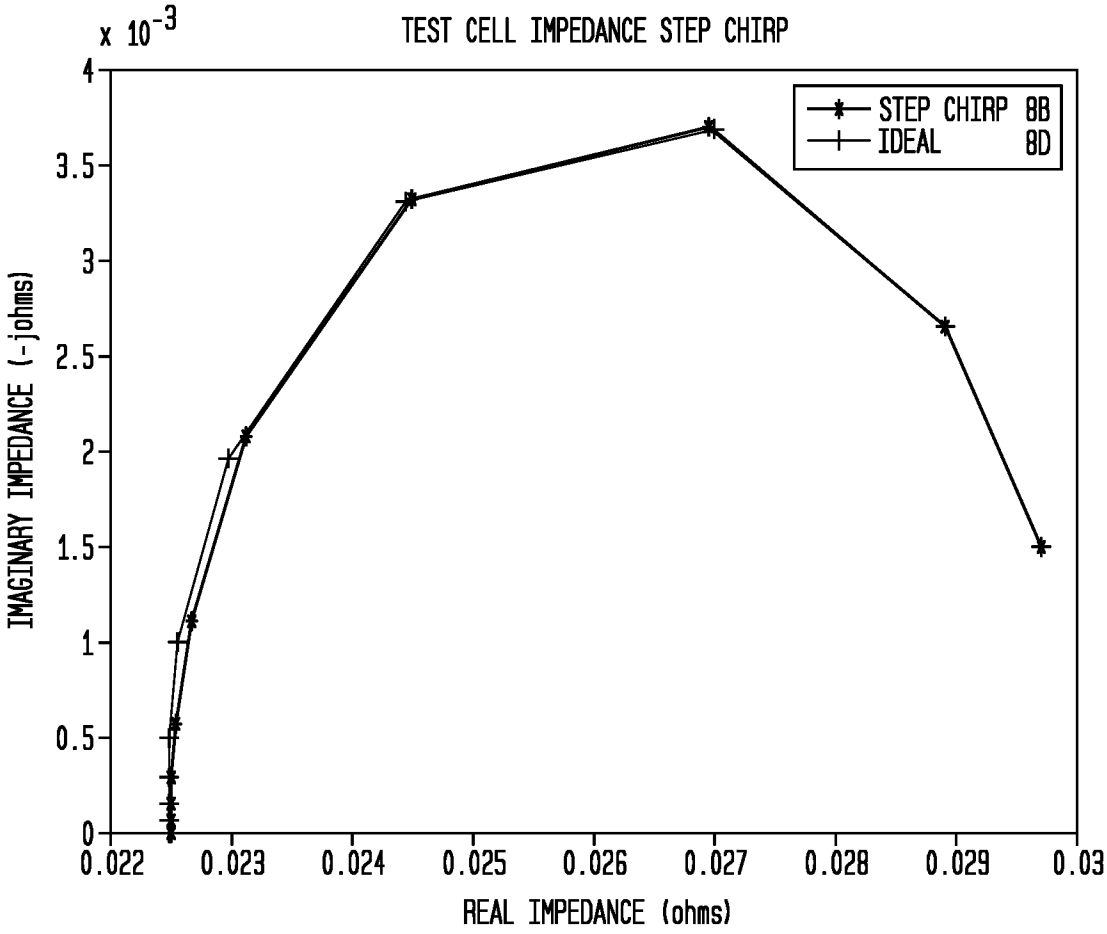

TEST CELL IMPEDANCE STEP CHIRP
x 10^-3
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
STEP CHIRP 8B
IDEAL 8D
0
0.5
1
1.5
2
2.5
3
3.5
4
0.022
0.023
0.024
0.025
0.026
0.027
0.028
0.029
0.03

FIG. 12

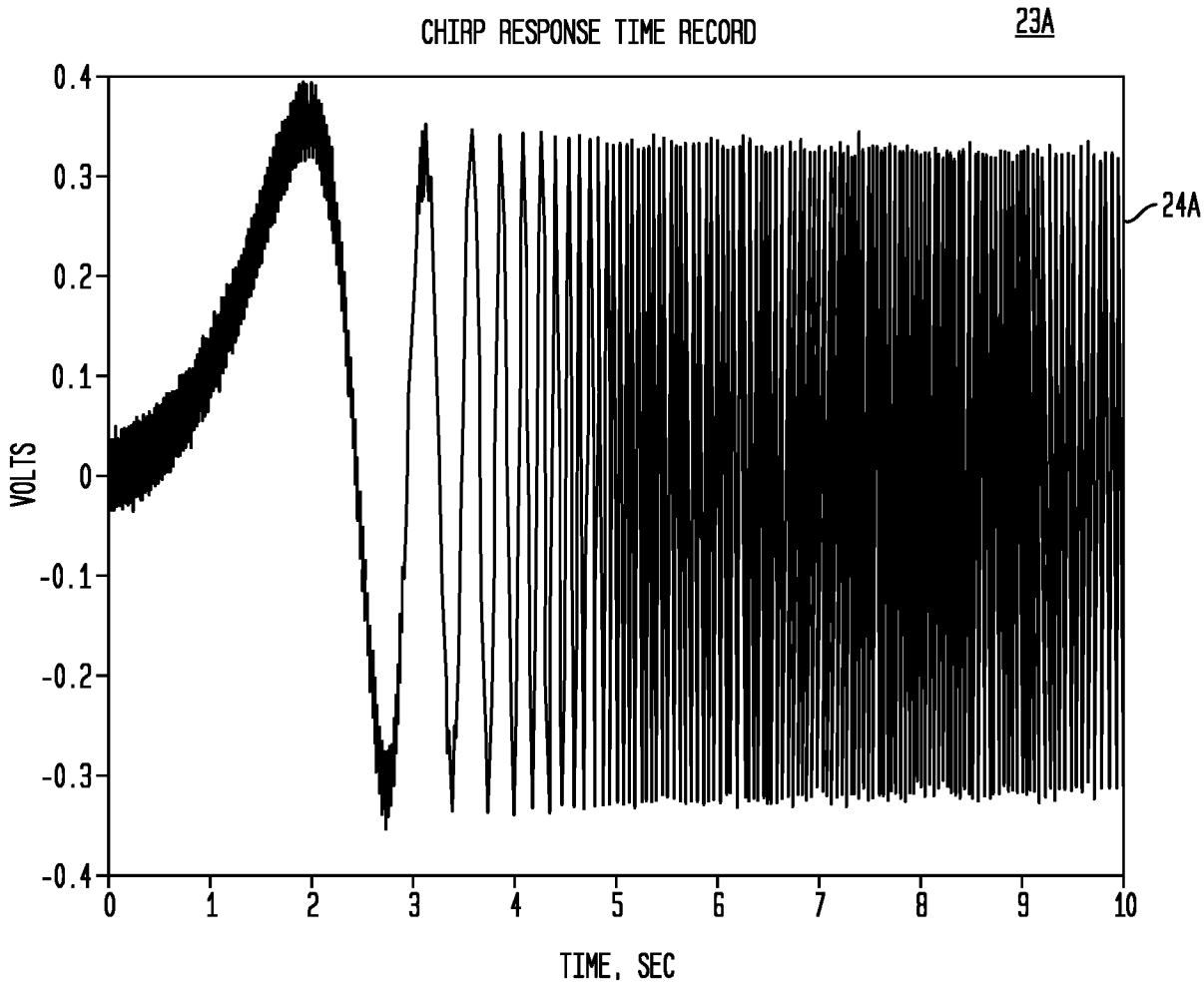

CHIRP RESPONSE TIME RECORD
23A
24A
VOLTS
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
0
1
2
3
4
5
6
7
8
9
10
TIME, SEC

FIG. 13

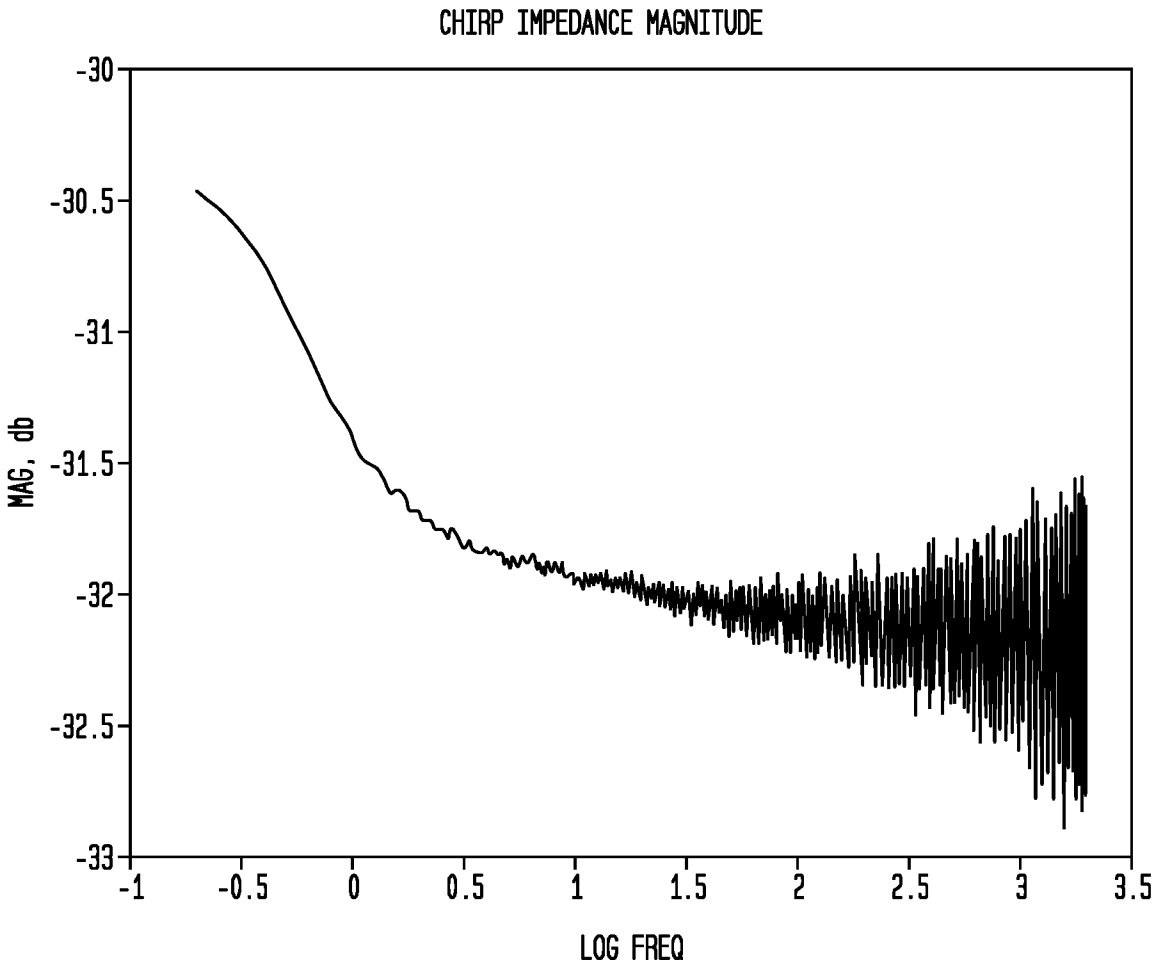

CHIRP IMPEDANCE MAGNITUDE
MAG, db
-30
-30.5
-31
-31.5
-32
-32.5
-33
-1
-0.5
0
0.5
1
1.5
2
2.5
3
3.5
LOG FREQ

FIG. 14

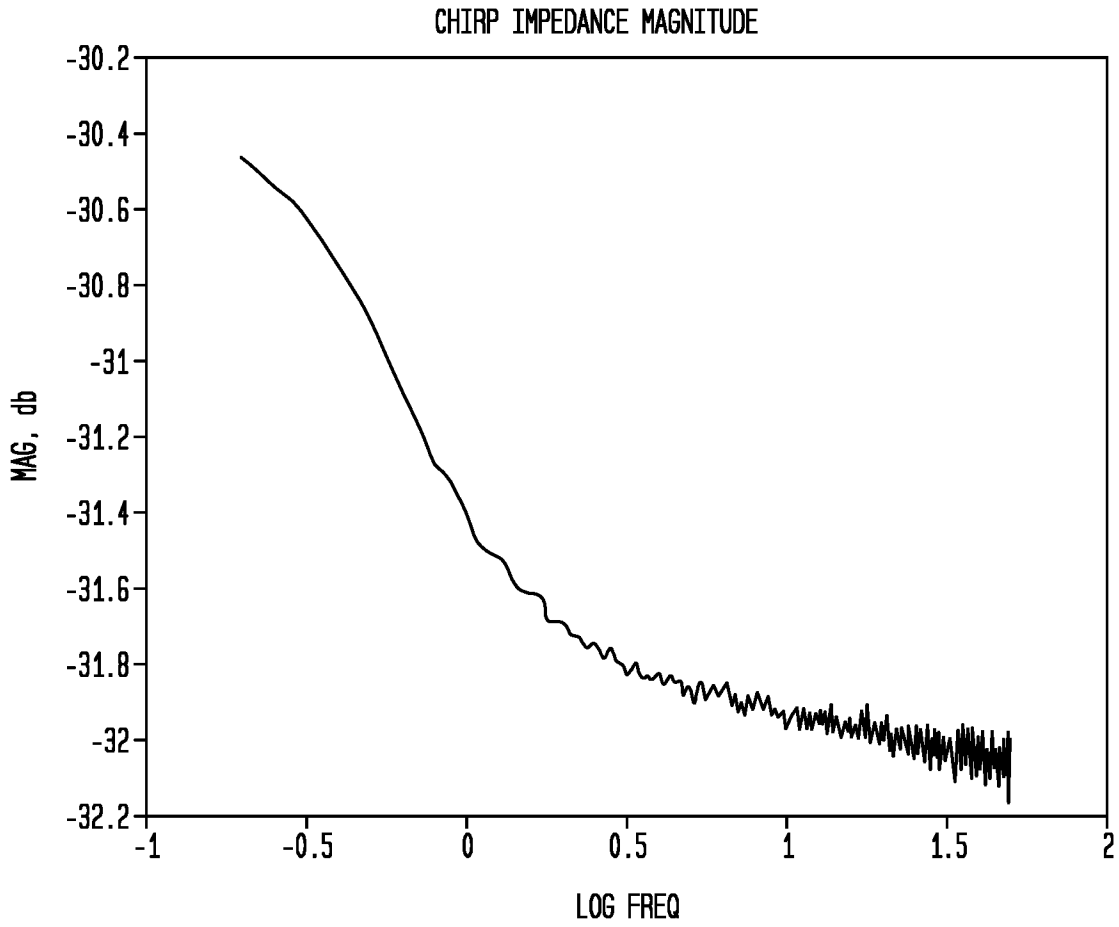

CHIRP IMPEDANCE MAGNITUDE
-30.2
-30.4
-30.6
-30.8
-31
-31.2
-31.4
-31.6
-31.8
-32
-32.2
MAG, db
-1
-0.5
0
0.5
1
1.5
2
LOG FREQ

FIG. 15

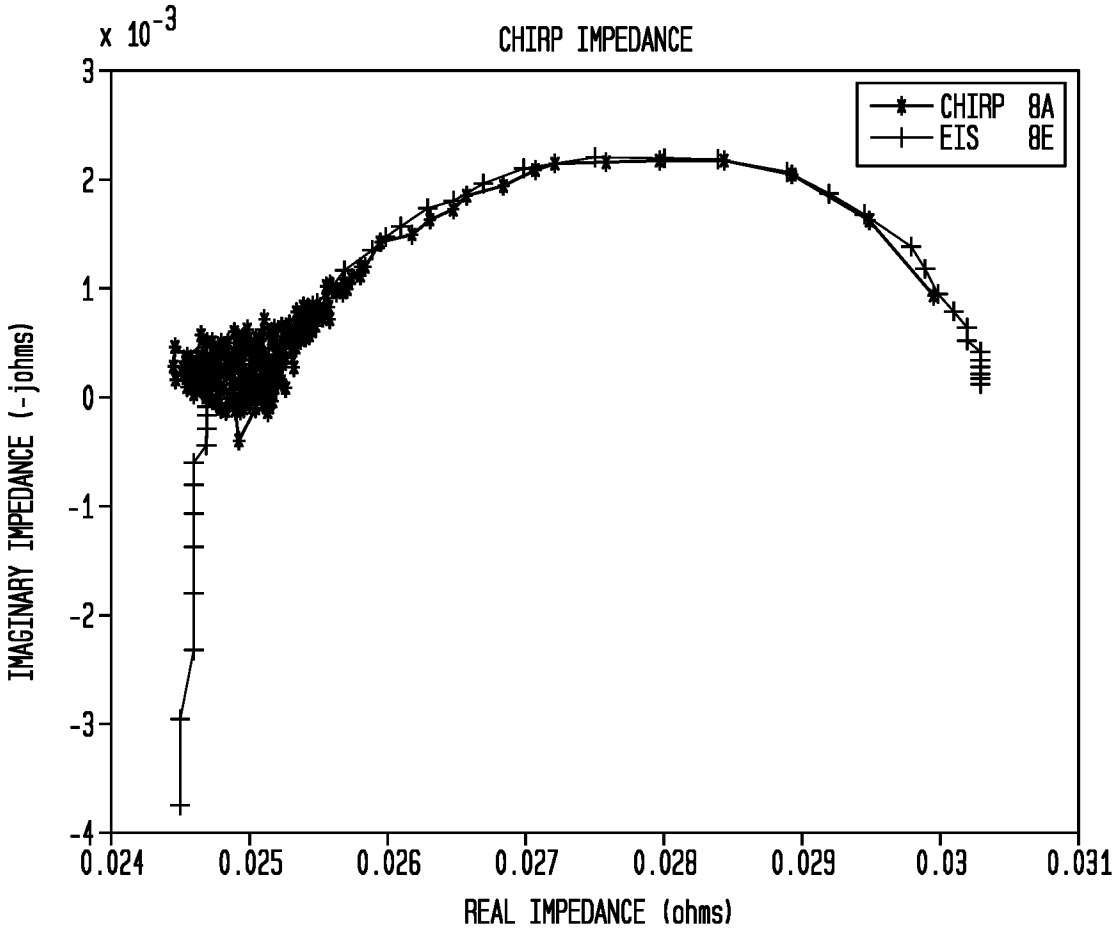

x 10^-3
CHIRP IMPEDANCE
CHIRP 8A
EIS 8E
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 16

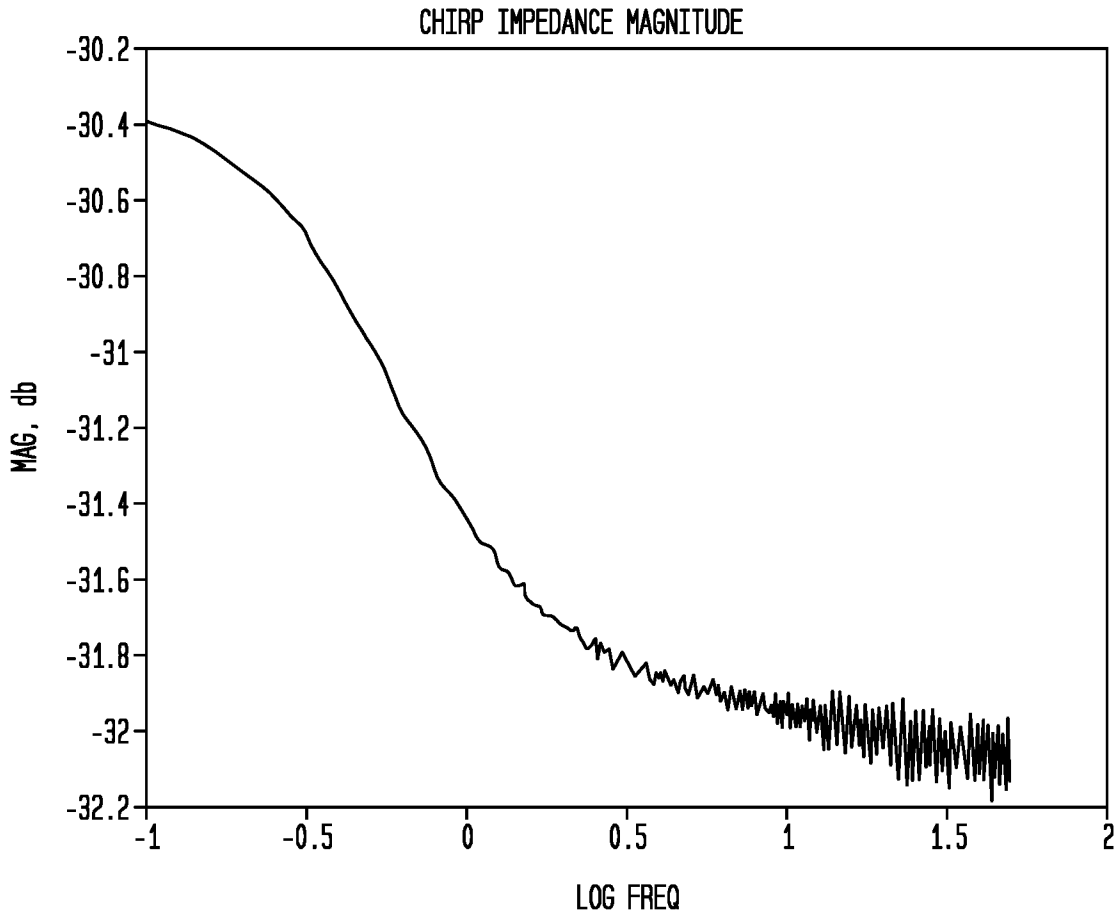

CHIRP IMPEDANCE MAGNITUDE
MAG, db
-30.2
-30.4
-30.6
-30.8
-31
-31.2
-31.4
-31.6
-31.8
-32
-32.2
-1
-0.5
0
0.5
1
1.5
2
LOG FREQ

FIG. 17

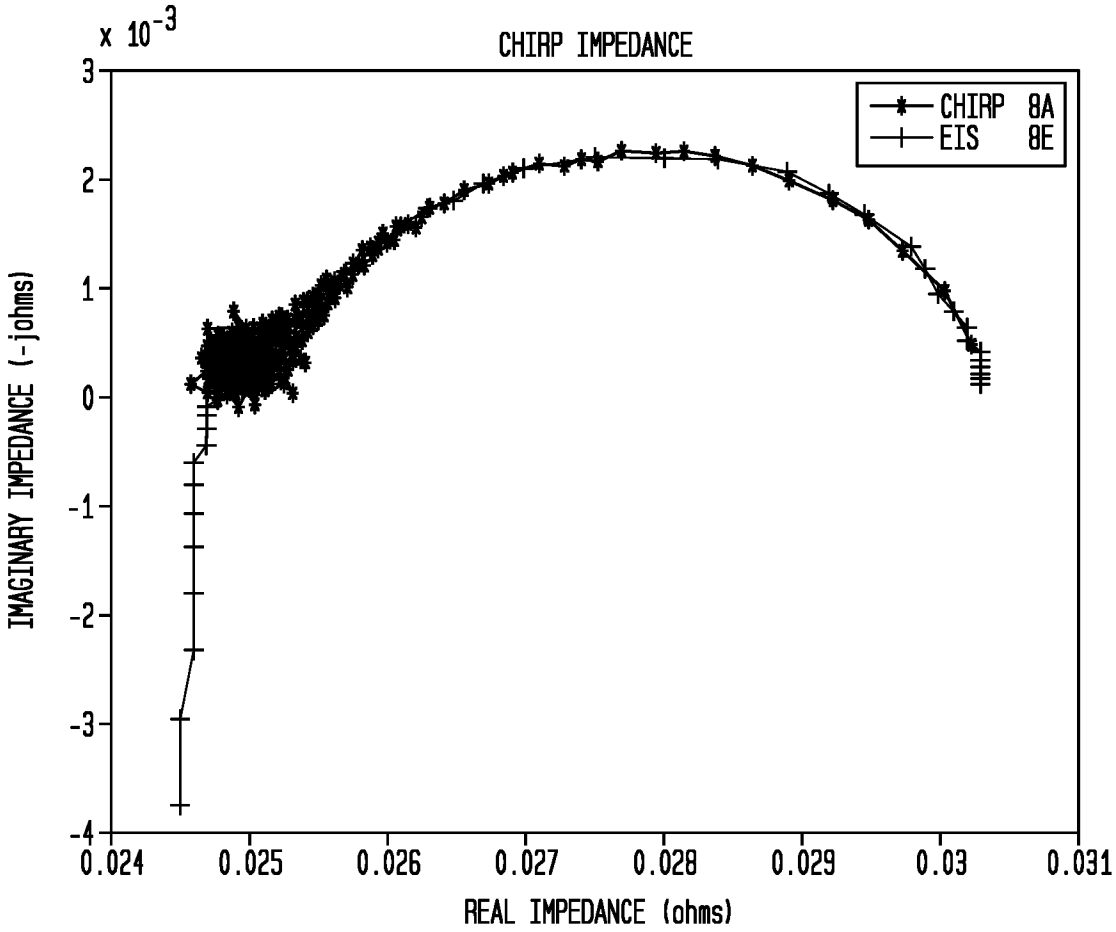

x 10^-3
CHIRP IMPEDANCE
CHIRP 8A
EIS 8E
IMAGINARY IMPEDANCE (-johms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031
REAL IMPEDANCE (ohms)

FIG. 18

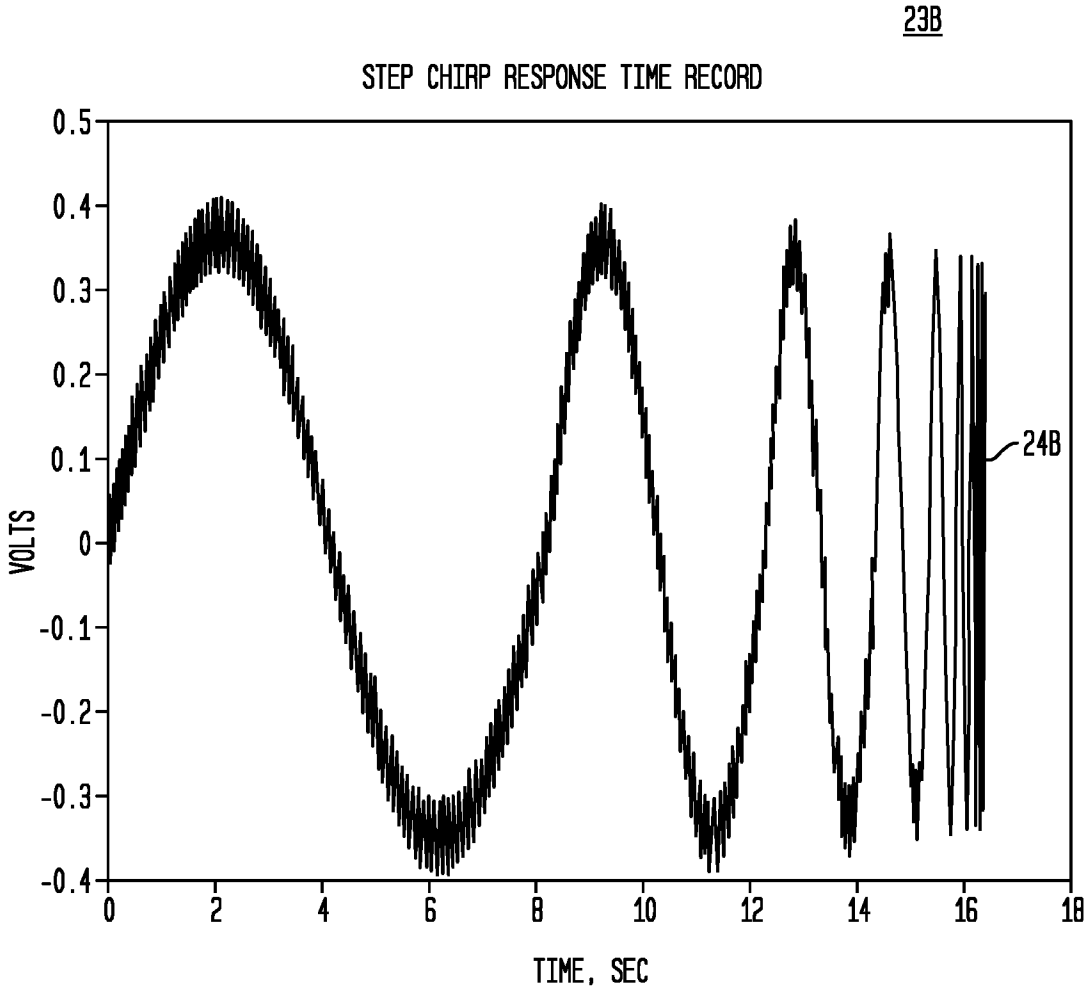

23B
STEP CHIRP RESPONSE TIME RECORD
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
VOLTS
24B
0
2
4
6
8
10
12
14
16
18
TIME, SEC

FIG. 19

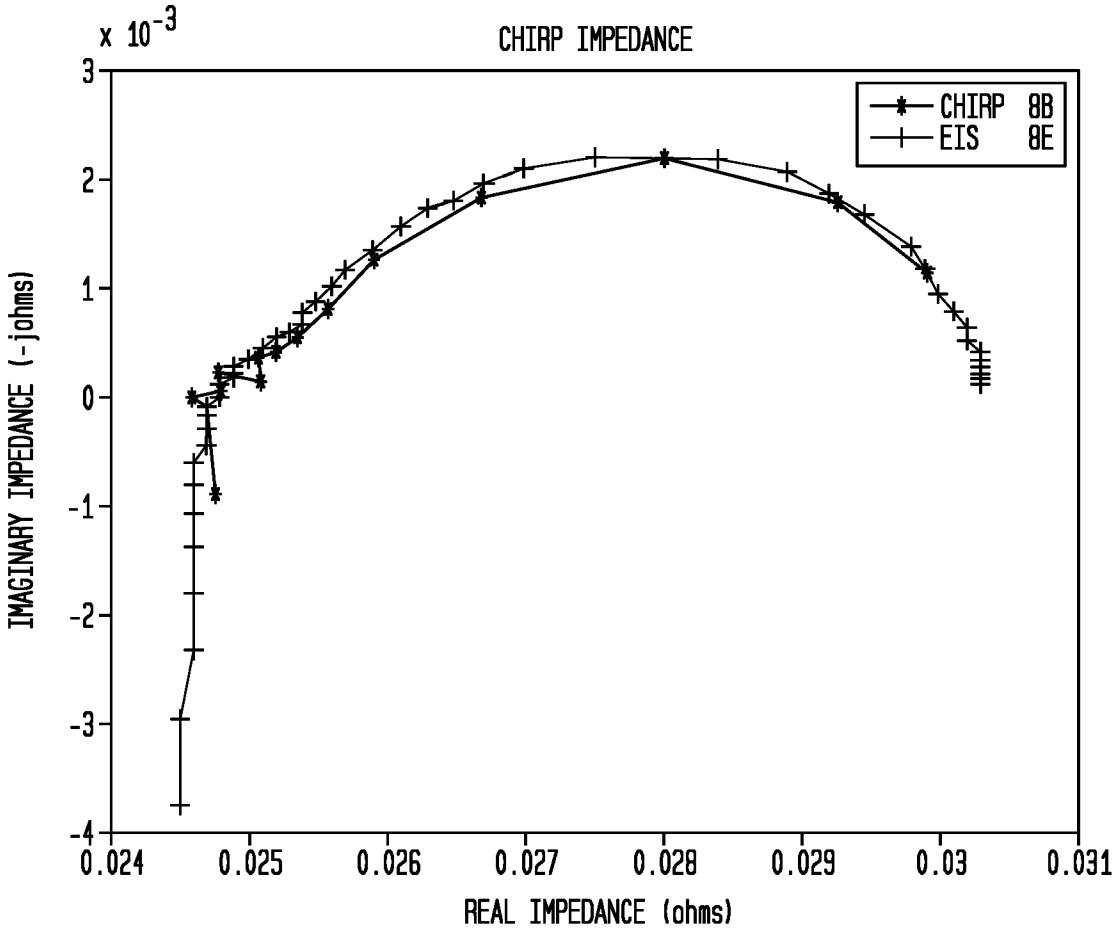

x 10-3
CHIRP IMPEDANCE
CHIRP 8B
EIS 8E
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 20

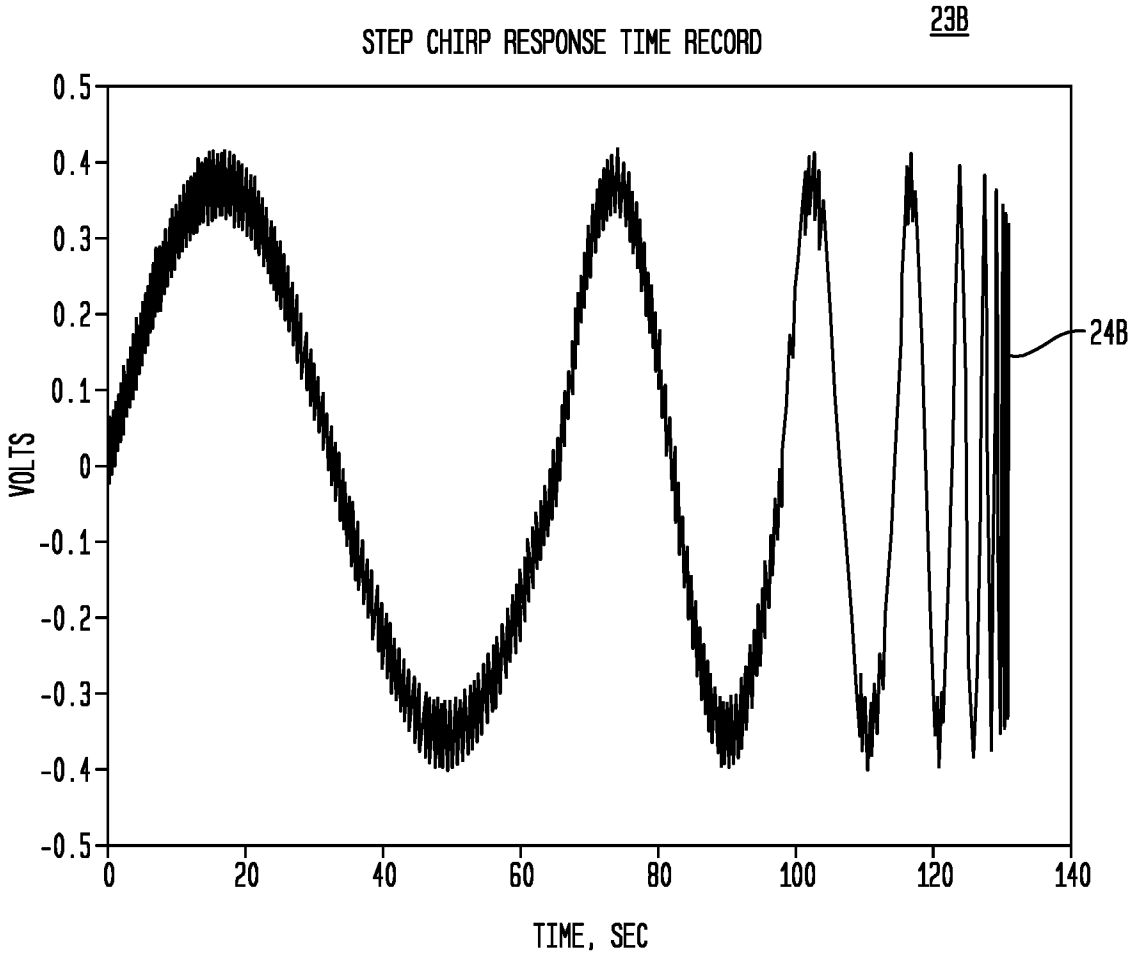

23B
STEP CHIRP RESPONSE TIME RECORD
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
-0.5
VOLTS
0
20
40
60
80
100
120
140
TIME, SEC
24B

FIG. 21

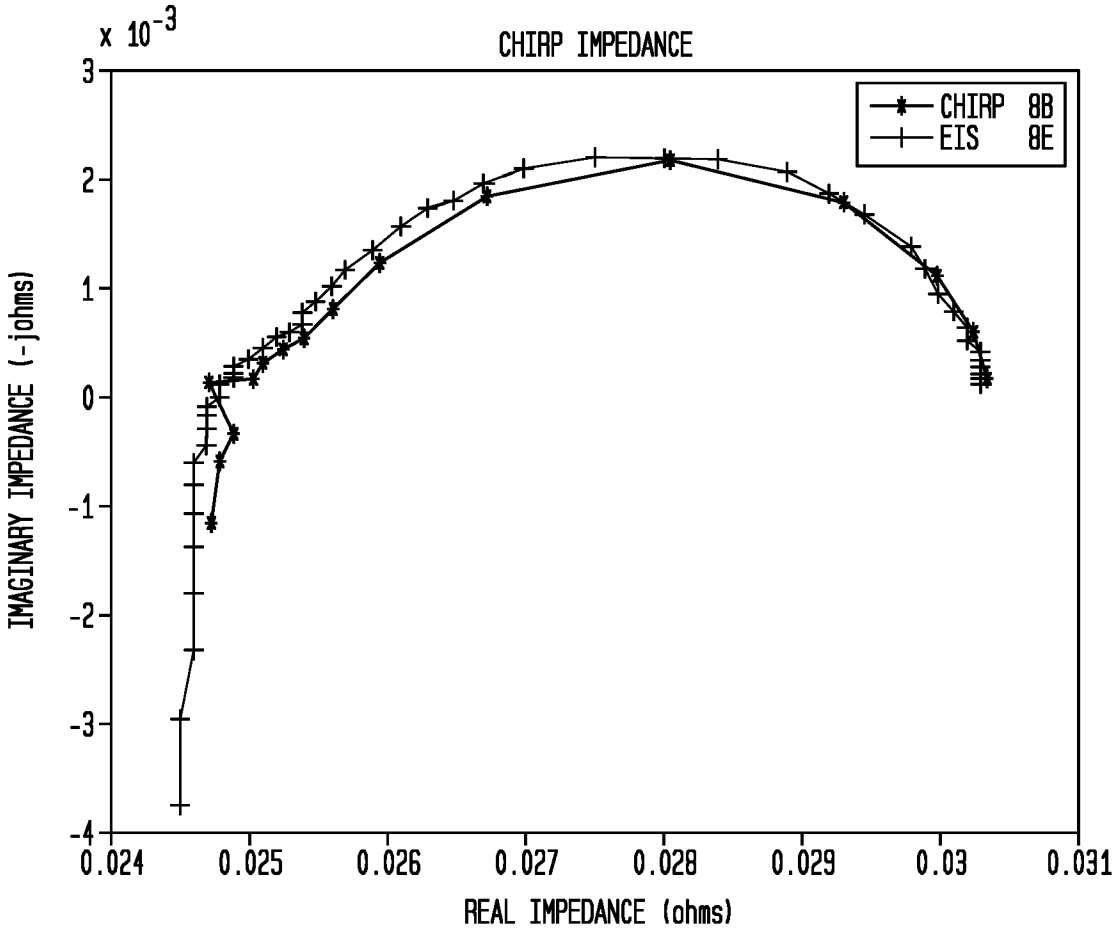

x 10^-3
CHIRP IMPEDANCE
CHIRP 8B
EIS 8E
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 22

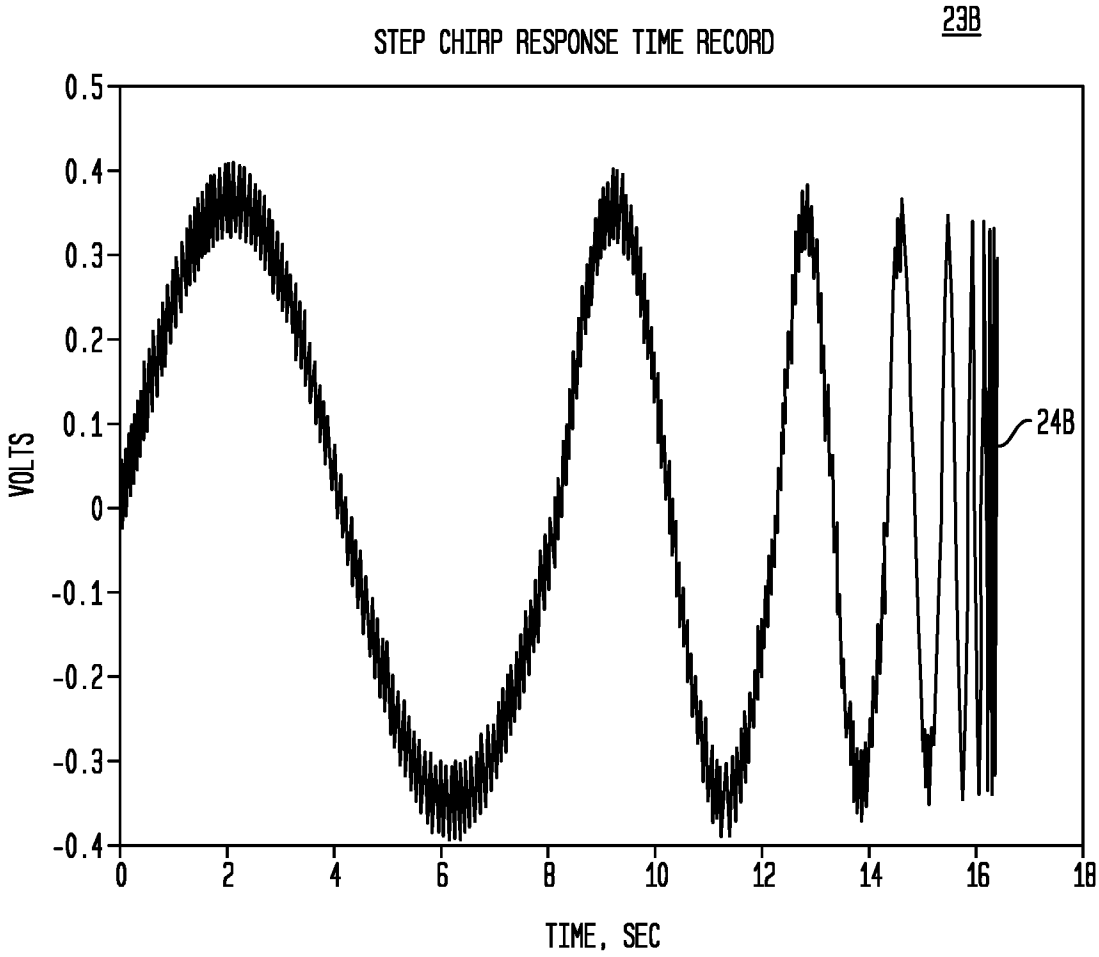

23B
STEP CHIRP RESPONSE TIME RECORD
VOLTS
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
0
2
4
6
8
10
12
14
16
18
TIME, SEC
24B

FIG. 23

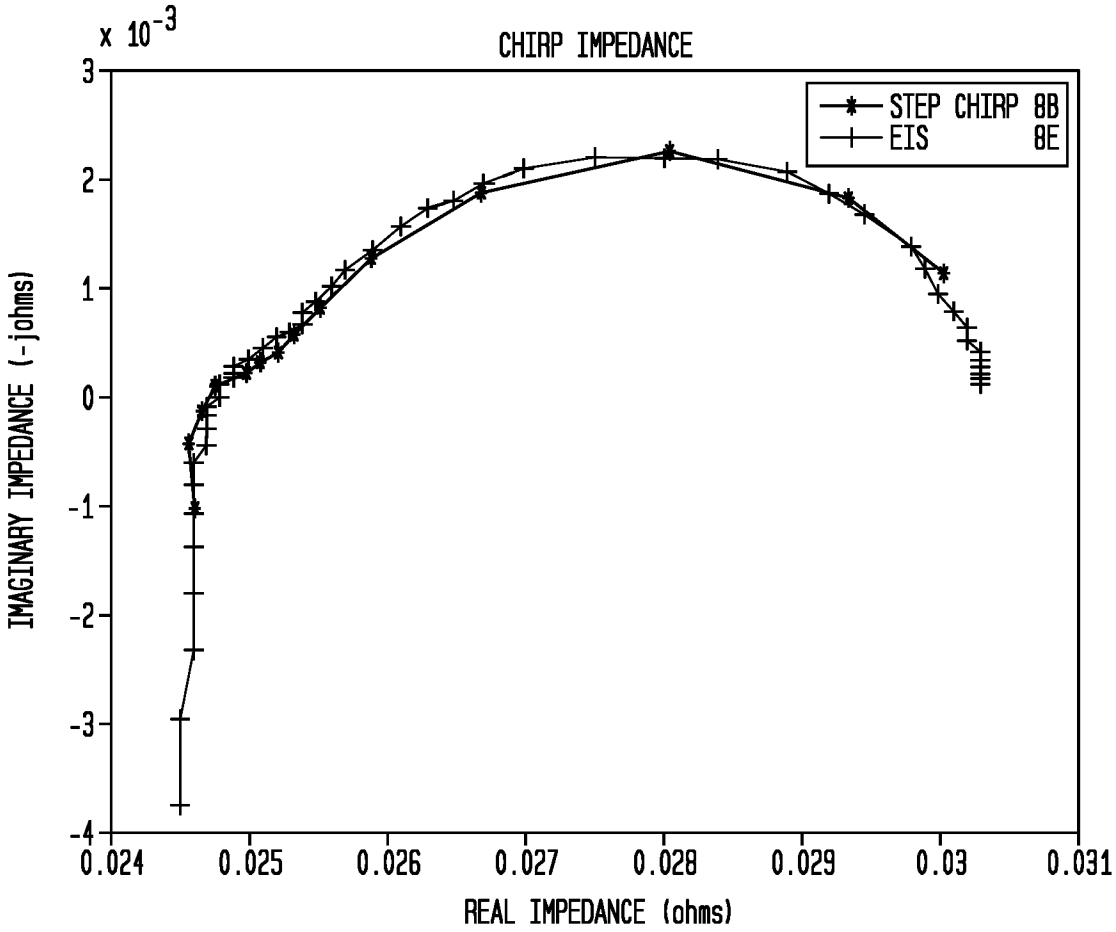

x 10^-3
CHIRP IMPEDANCE
STEP CHIRP 8B
EIS 8E
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 24

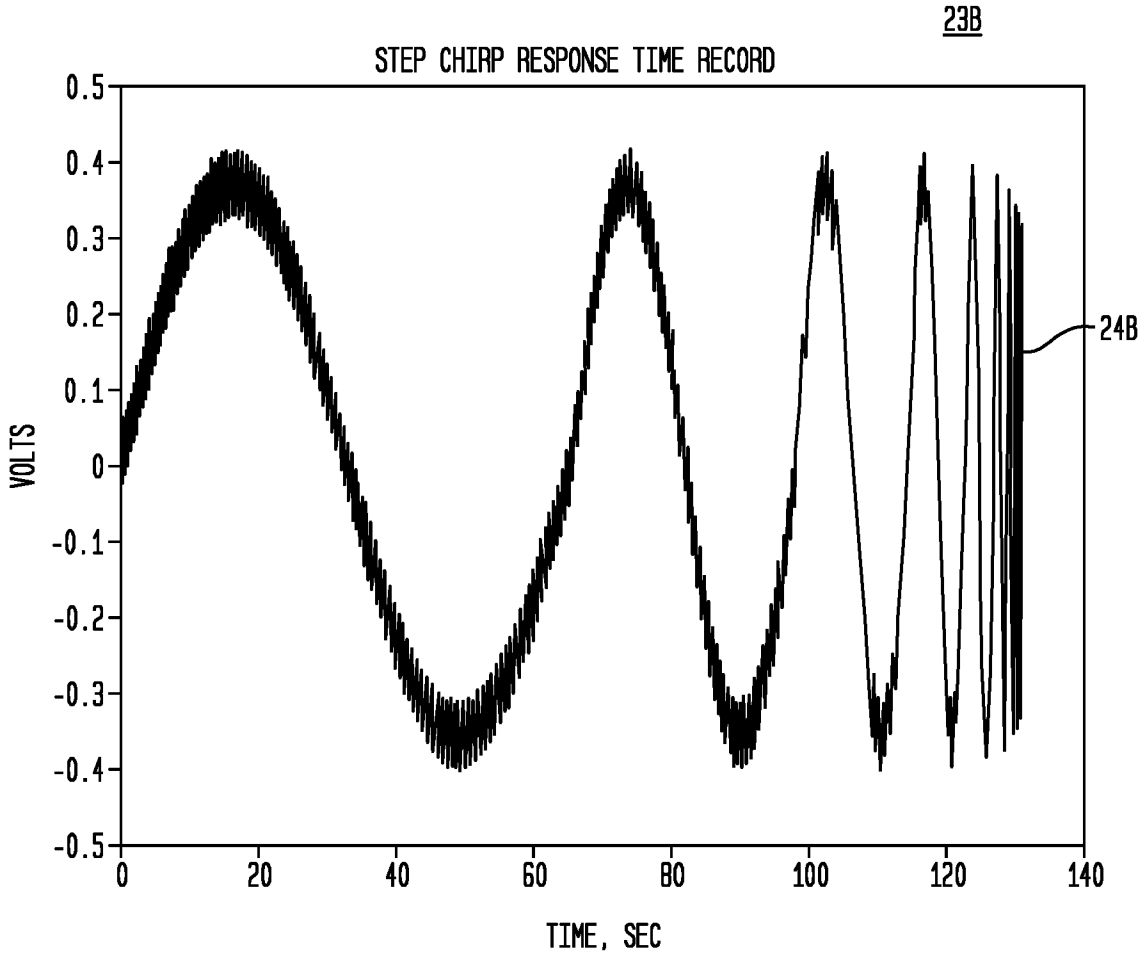

23B
STEP CHIRP RESPONSE TIME RECORD
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
-0.5
VOLTS
0
20
40
60
80
100
120
140
TIME, SEC
24B

FIG. 25

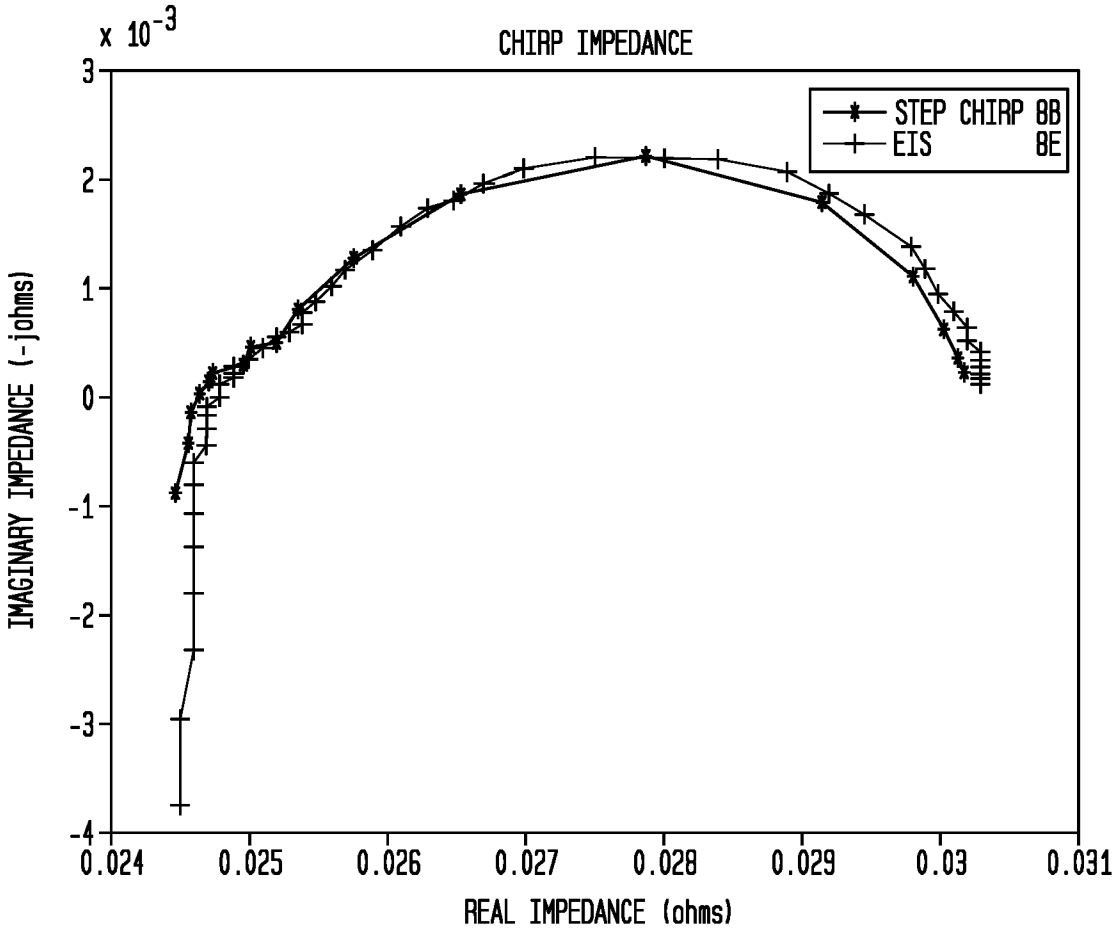

x 10^-3
CHIRP IMPEDANCE
STEP CHIRP 8B
EIS 8E
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 26

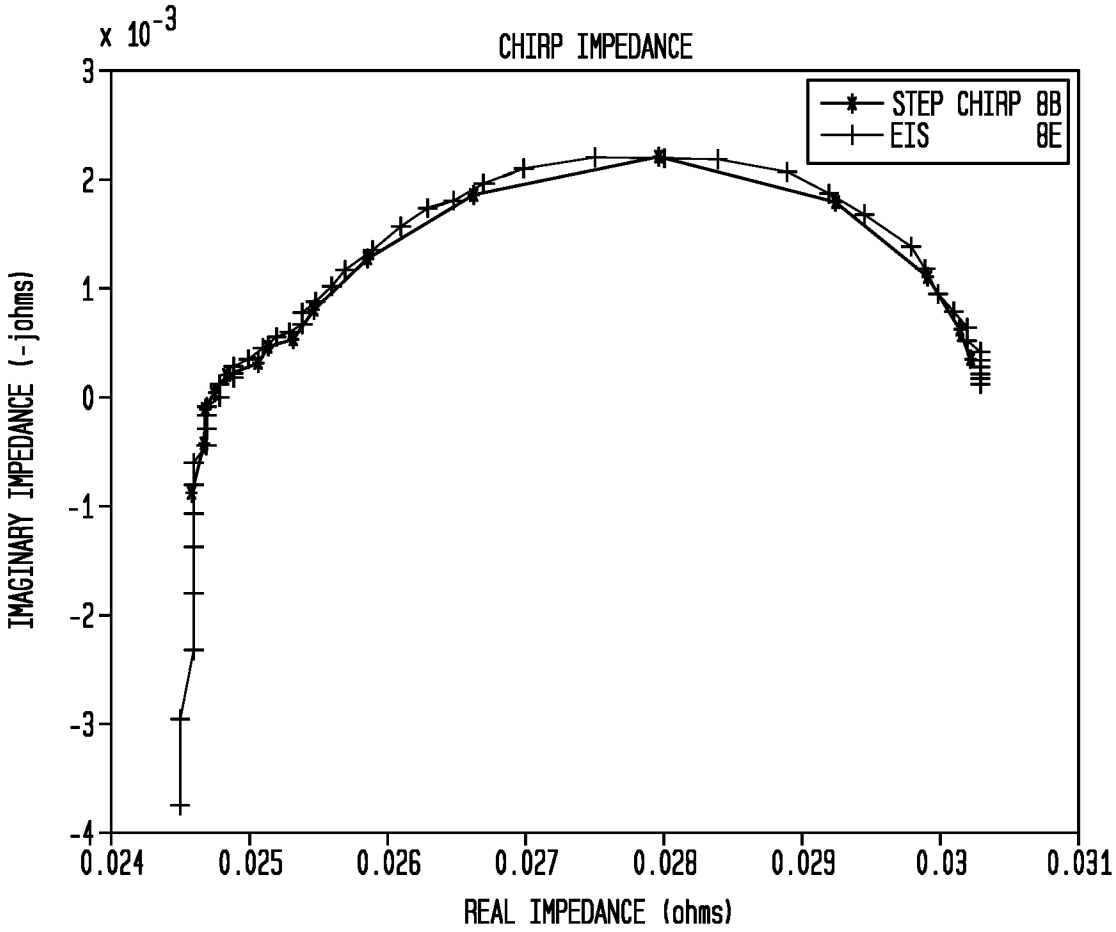

x 10^-3
CHIRP IMPEDANCE
STEP CHIRP 8B
EIS 8E
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 27

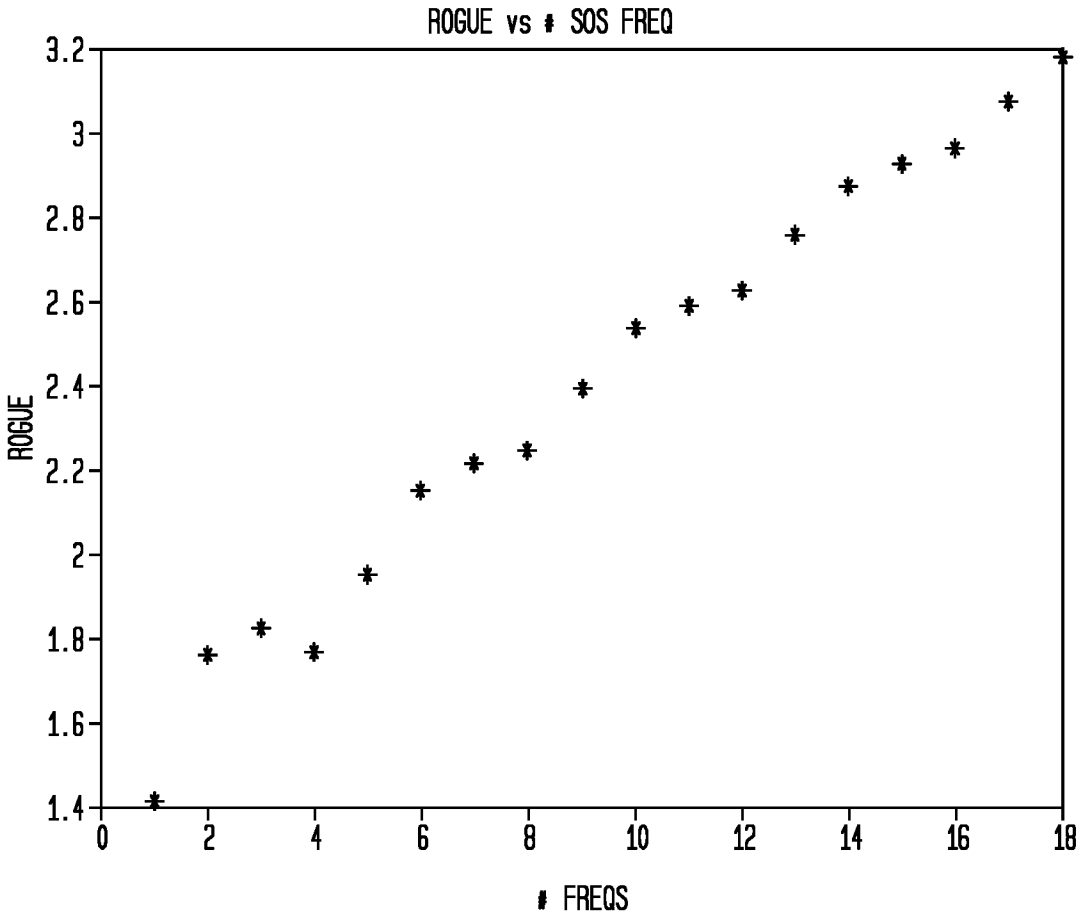

ROGUE vs # SOS FREQ
ROGUE
FREQS
3.2
3
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
0
2
4
6
8
10
12
14
16
18

FIG. 28

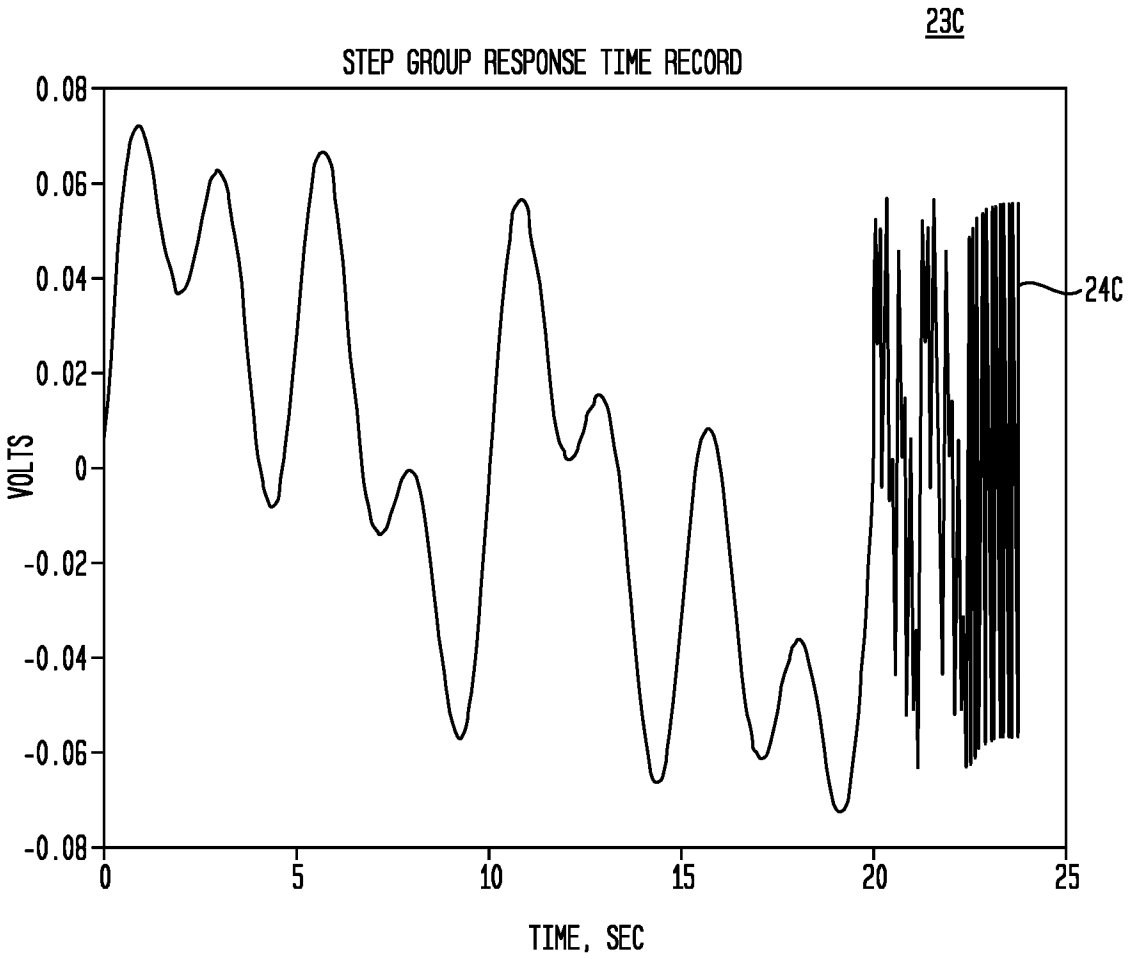

23C
STEP GROUP RESPONSE TIME RECORD
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
VOLTS
0
5
10
15
20
25
TIME, SEC
24C

FIG. 29

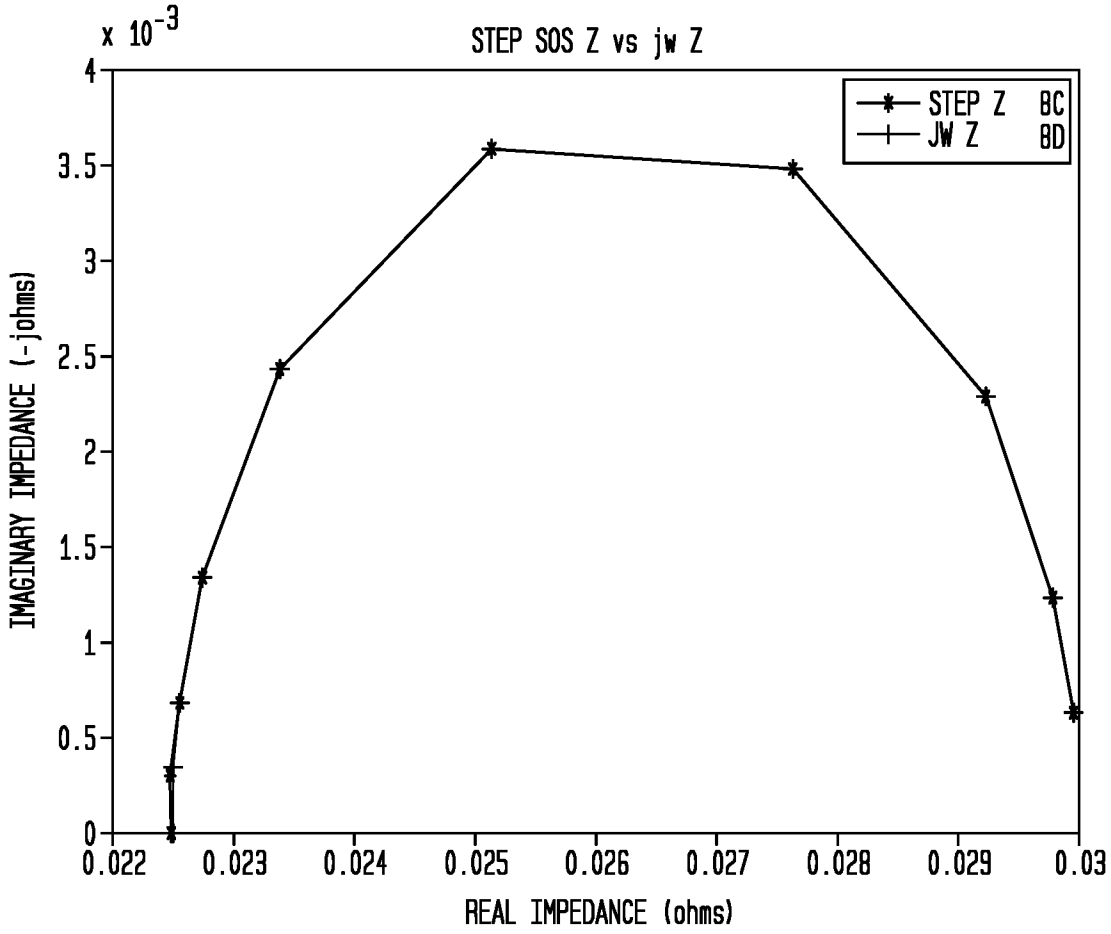

x 10^-3
STEP SOS Z vs jw Z
STEP Z 8C
JW Z 8D
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
4
3.5
3
2.5
2
1.5
1
0.5
0
0.022
0.023
0.024
0.025
0.026
0.027
0.028
0.029
0.03

FIG. 30

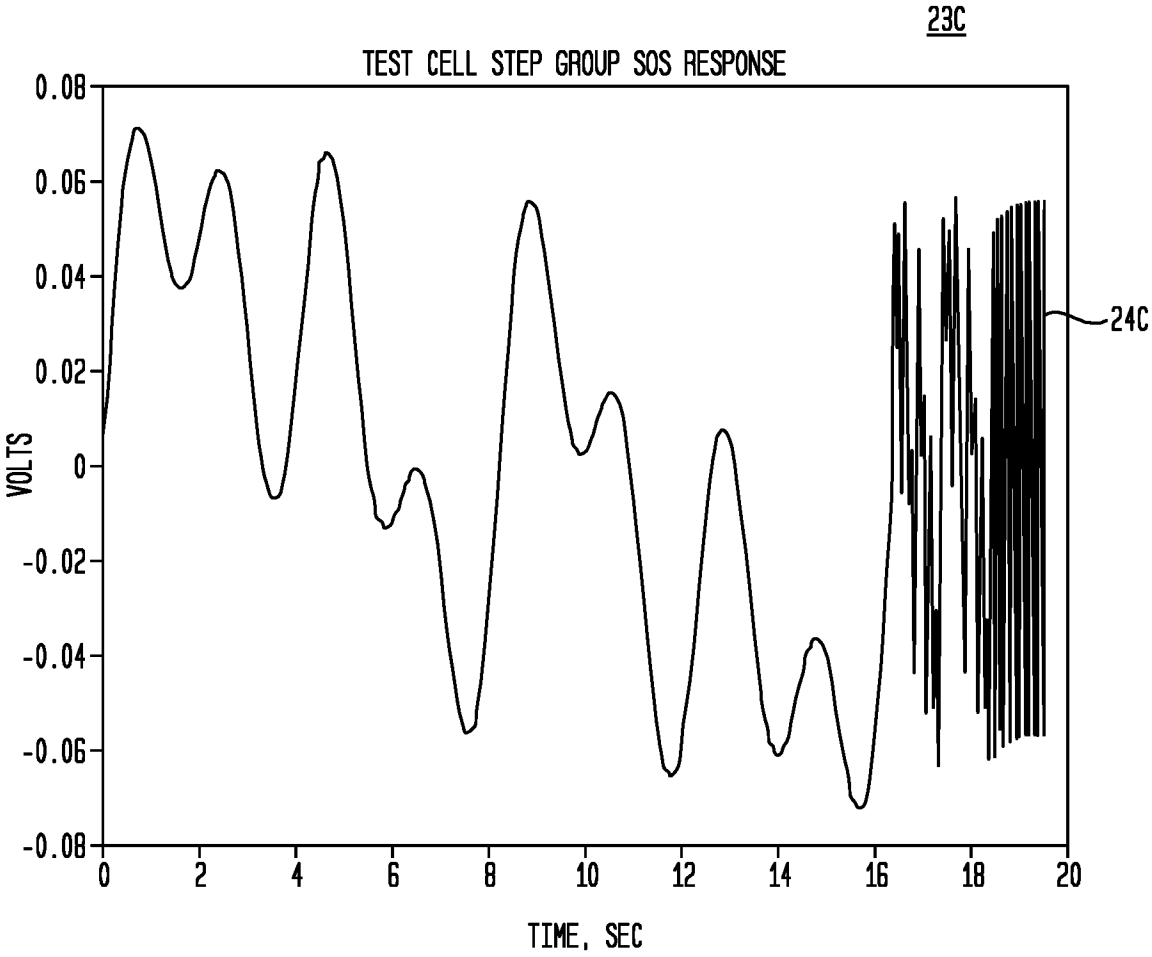

23C
TEST CELL STEP GROUP SOS RESPONSE
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
VOLTS
0
2
4
6
8
10
12
14
16
18
20
TIME, SEC
24C

FIG. 31

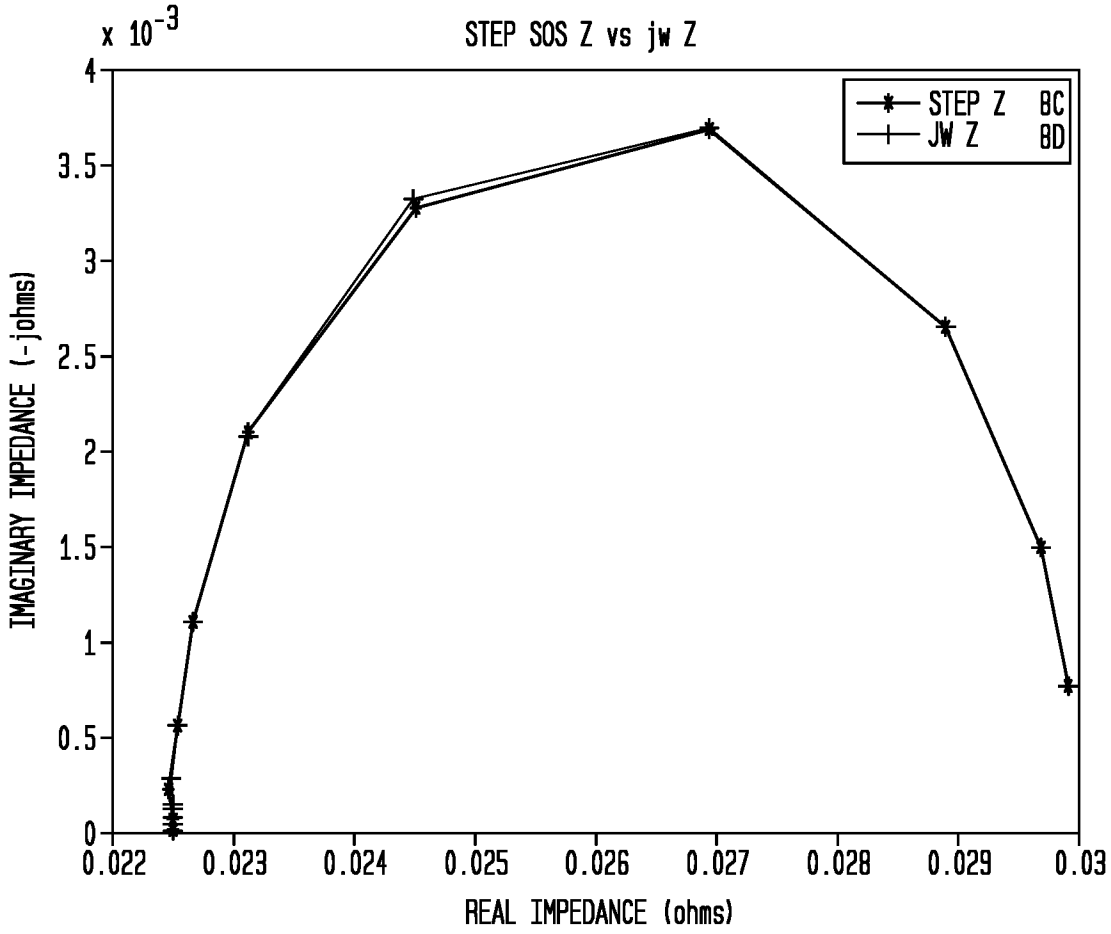

x 10^-3
STEP SOS Z vs jw Z
STEP Z 8C
JW Z 8D
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
4
3.5
3
2.5
2
1.5
1
0.5
0
0.022
0.023
0.024
0.025
0.026
0.027
0.028
0.029
0.03

FIG. 32

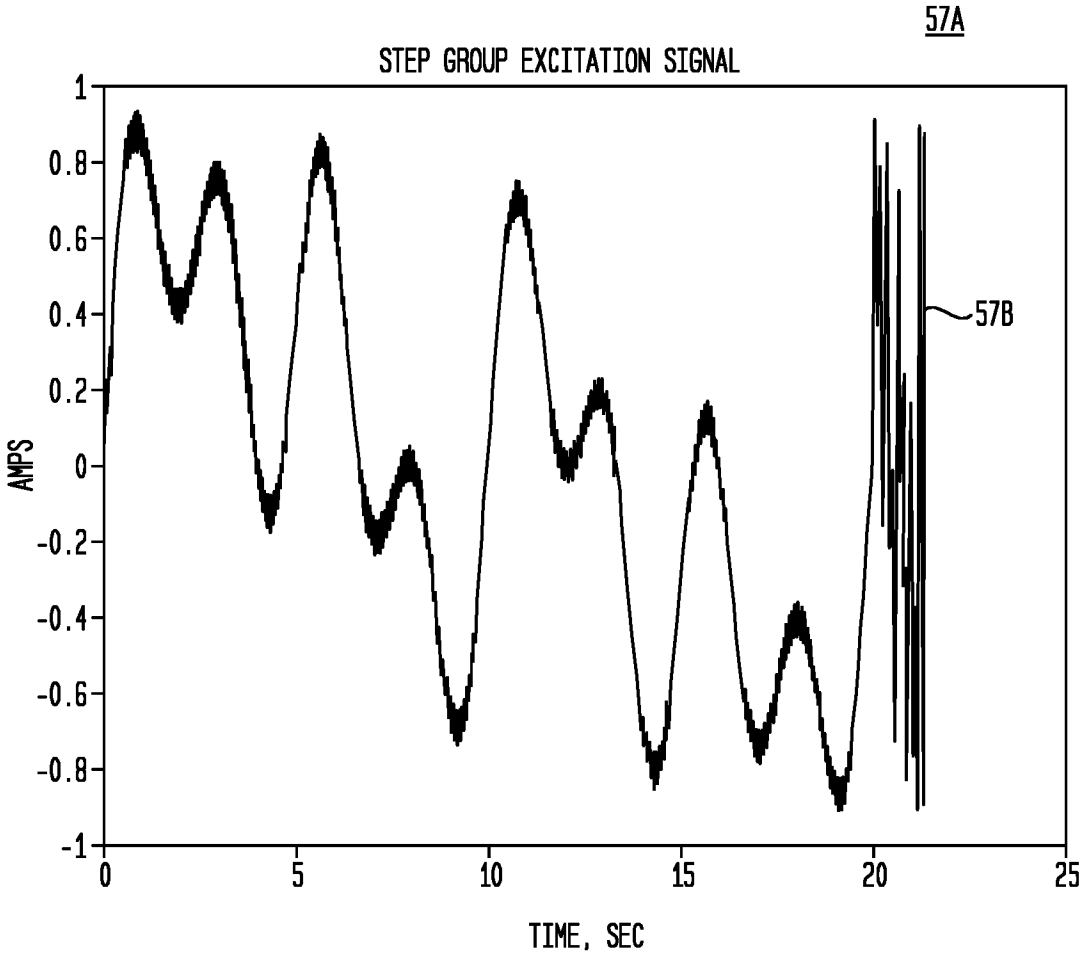

57A
STEP GROUP EXCITATION SIGNAL
AMPS
TIME, SEC
57B
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
5
10
15
20
25

FIG. 33

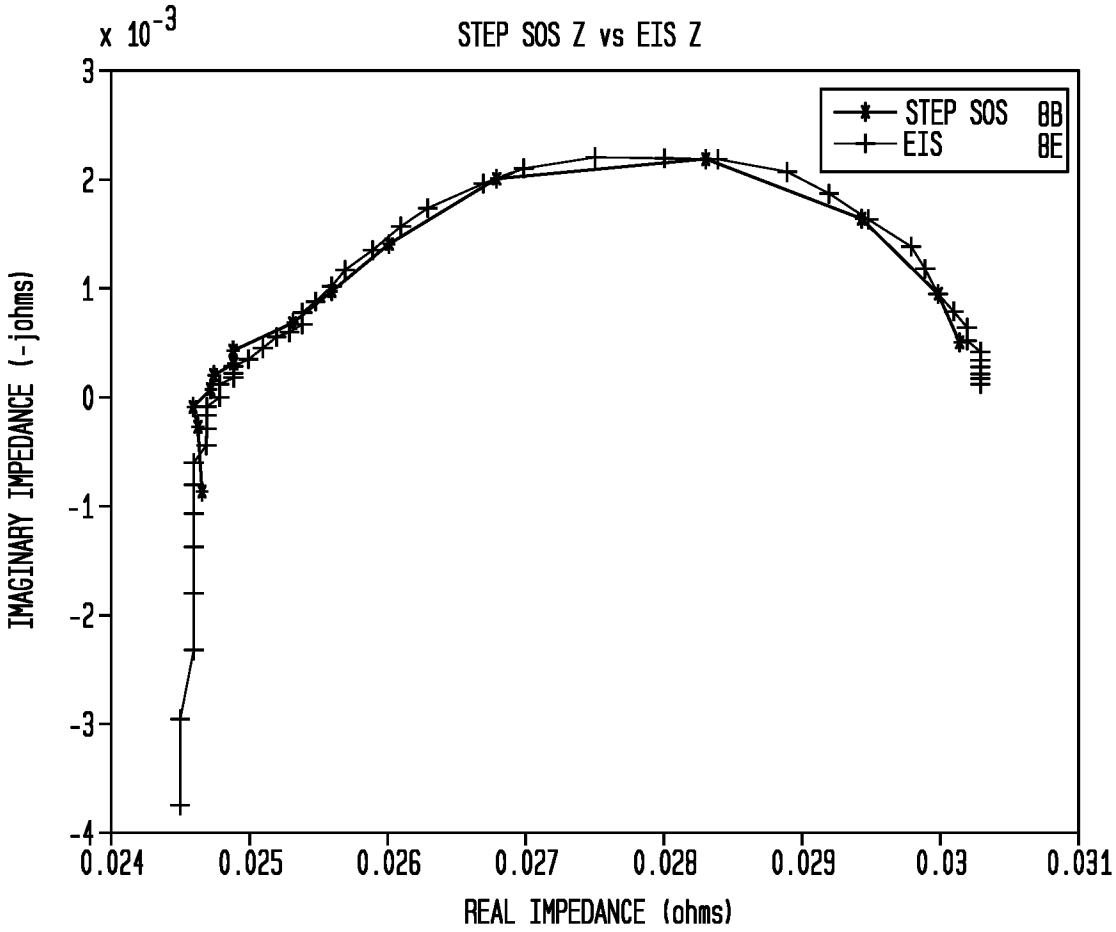

x 10^-3
STEP SOS Z vs EIS Z
STEP SOS BB
EIS BE
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 34

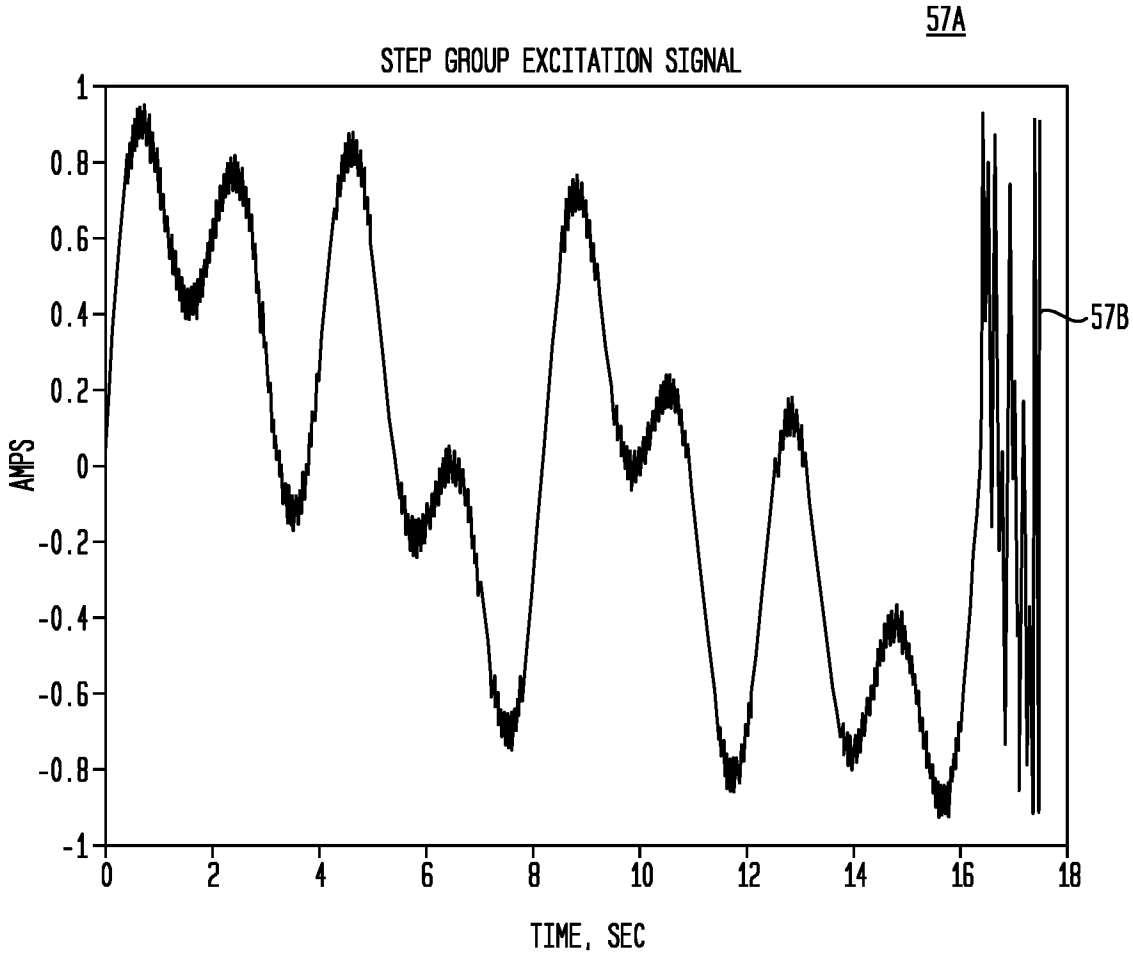

57A
STEP GROUP EXCITATION SIGNAL
AMPS
TIME, SEC
57B
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
2
4
6
8
10
12
14
16
18

FIG. 35

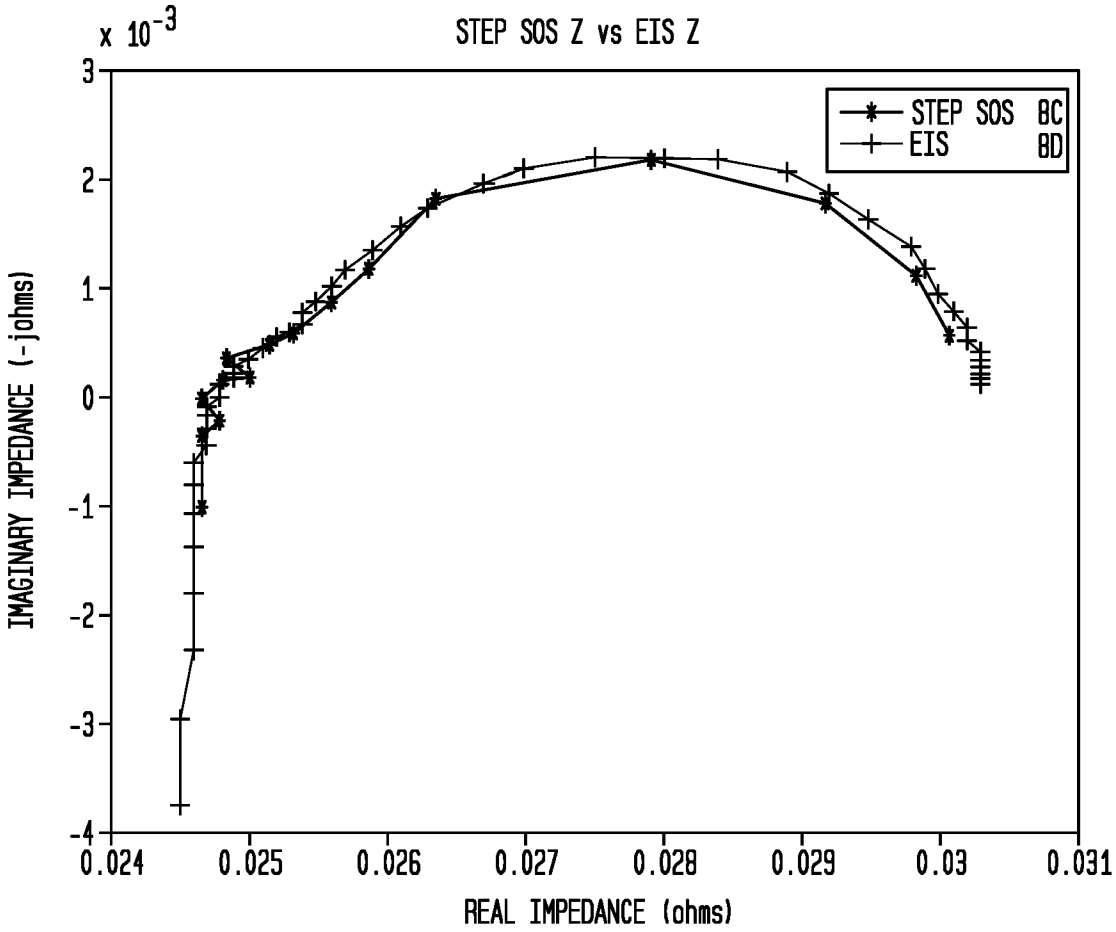

x 10^-3
STEP SOS Z vs EIS Z
STEP SOS 8C
EIS 8D
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 36

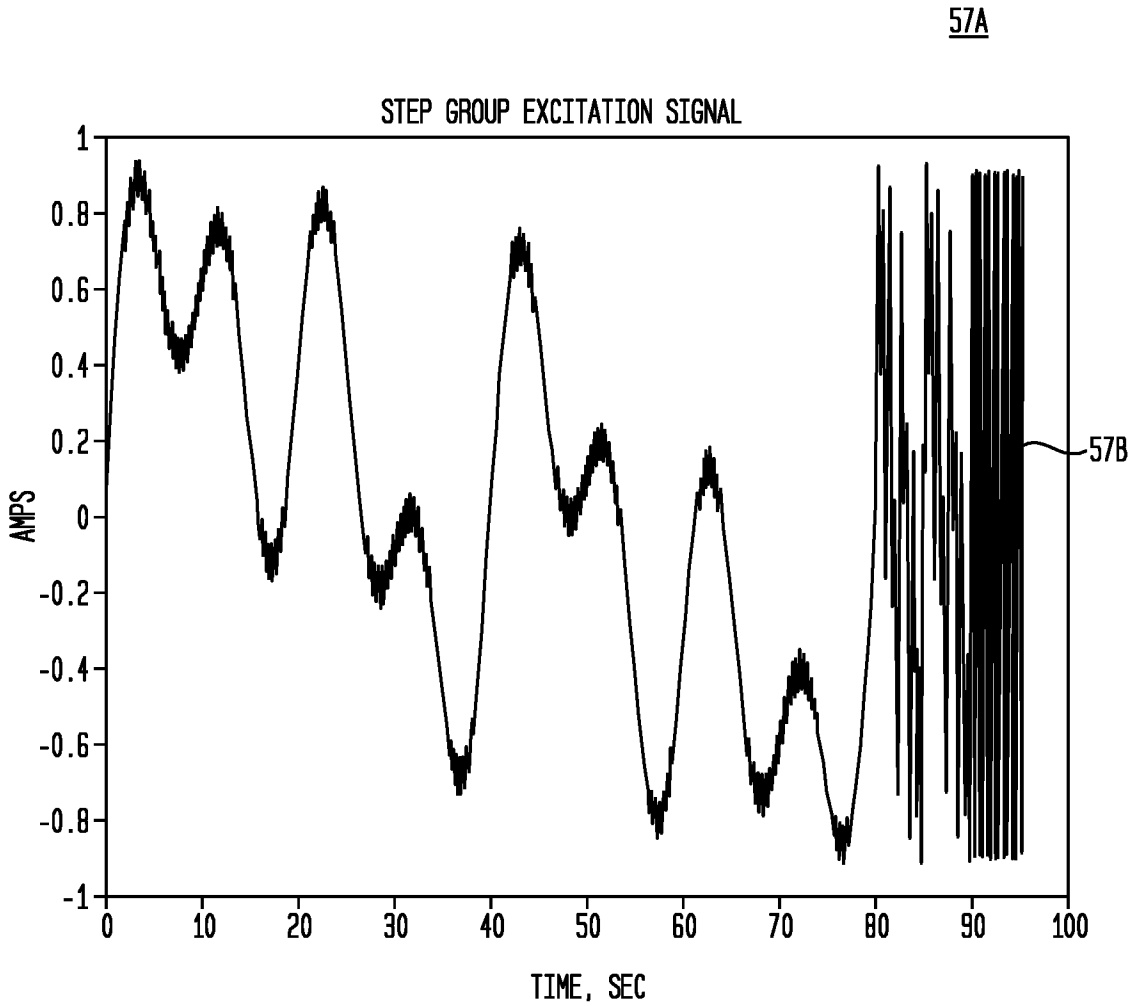

57A
STEP GROUP EXCITATION SIGNAL
AMPS
TIME, SEC
57B
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
10
20
30
40
50
60
70
80
90
100

FIG. 37

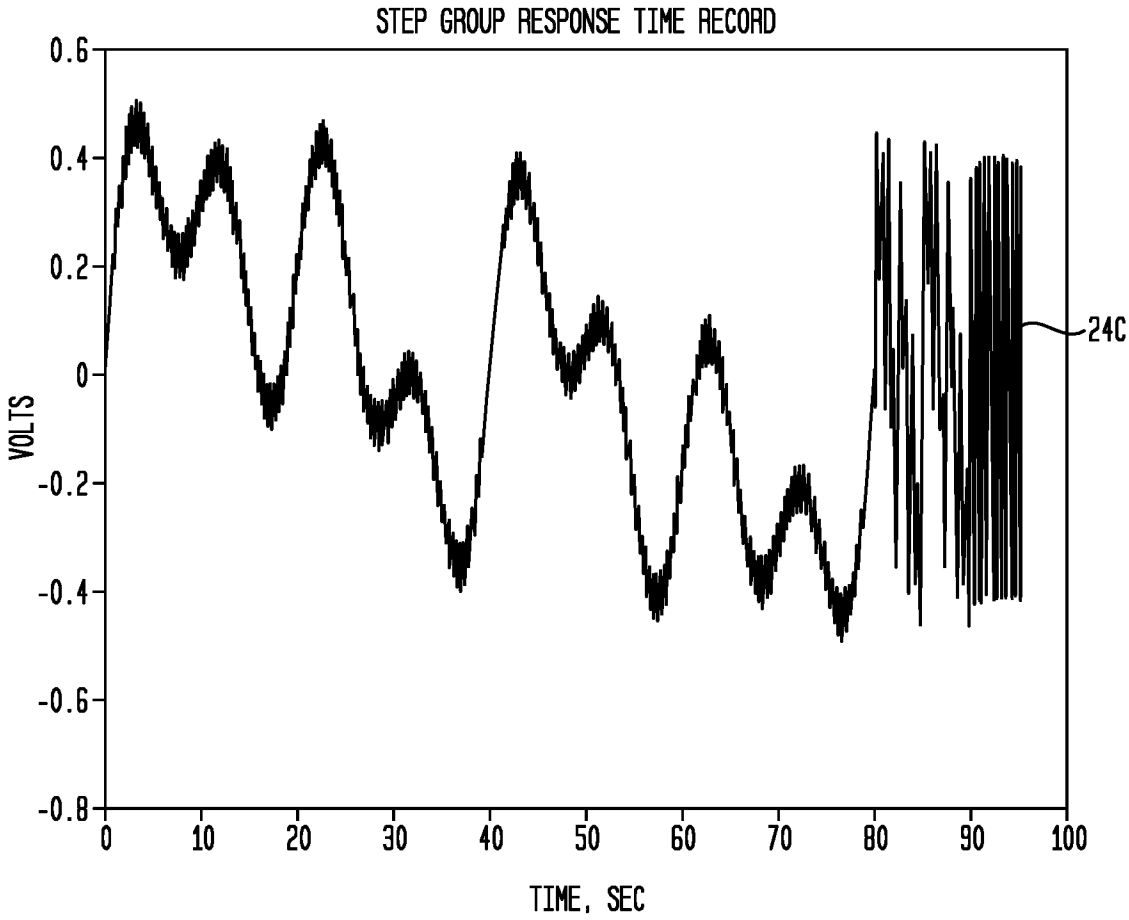

STEP GROUP RESPONSE TIME RECORD
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
VOLTS
0
10
20
30
40
50
60
70
80
90
100
TIME, SEC
24C

FIG. 38

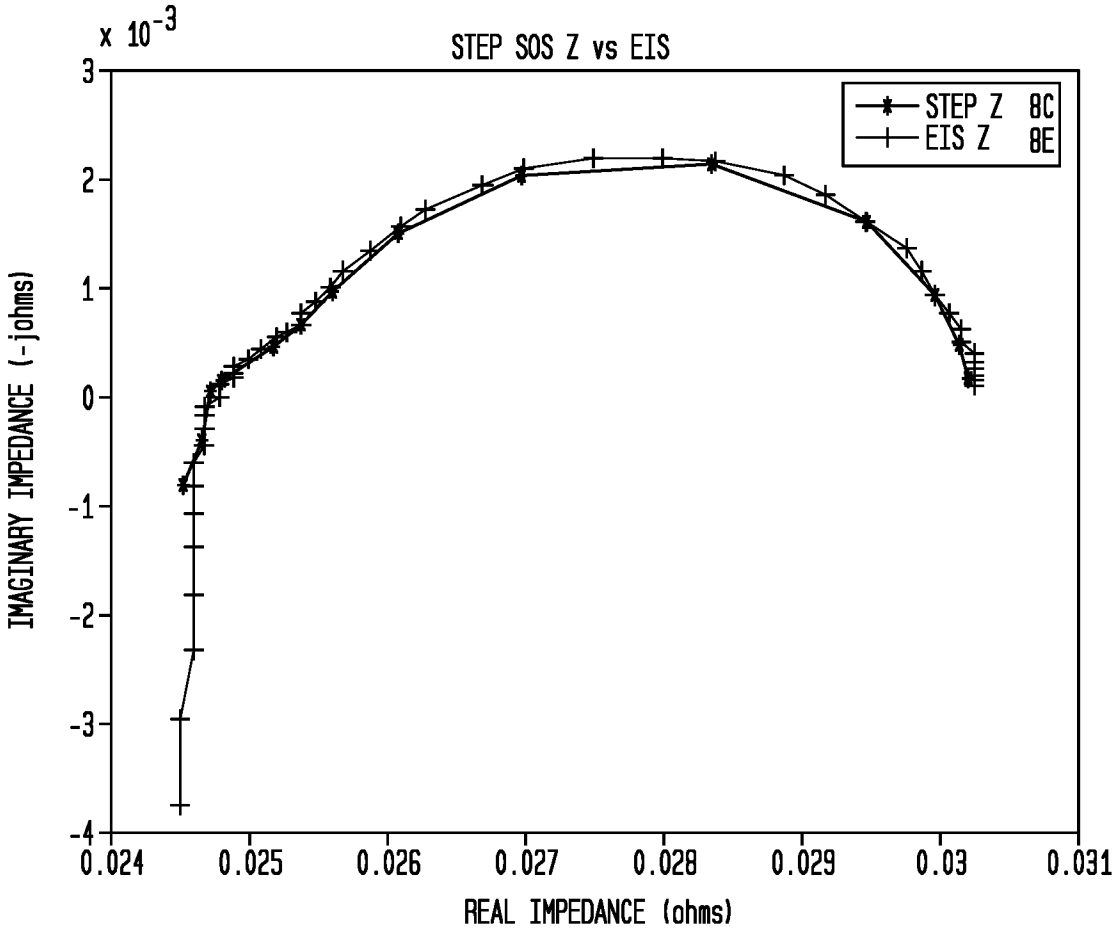

x 10^-3
STEP SOS Z vs EIS
STEP Z 8C
EIS Z 8E
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 39

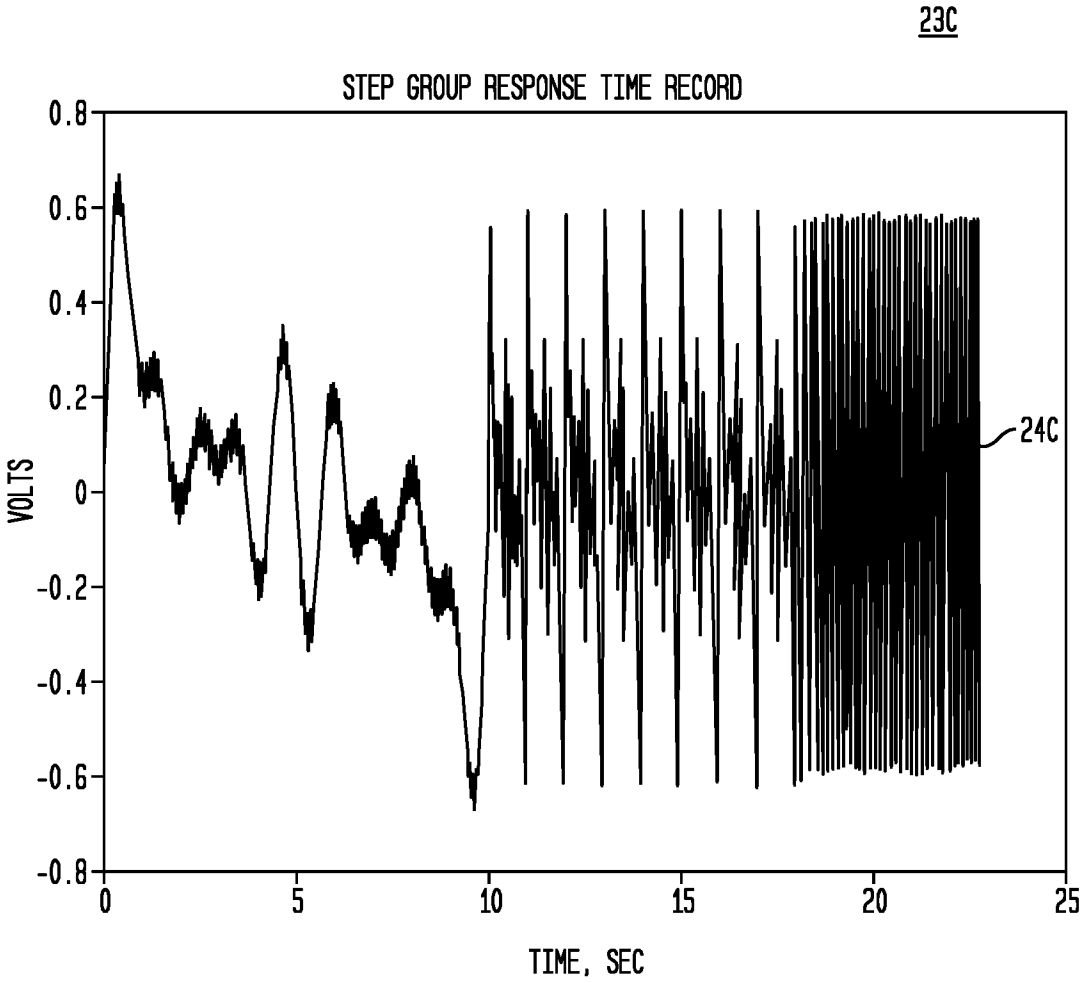

23C
STEP GROUP RESPONSE TIME RECORD
VOLTS
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
0
5
10
15
20
25
TIME, SEC
24C

FIG. 40

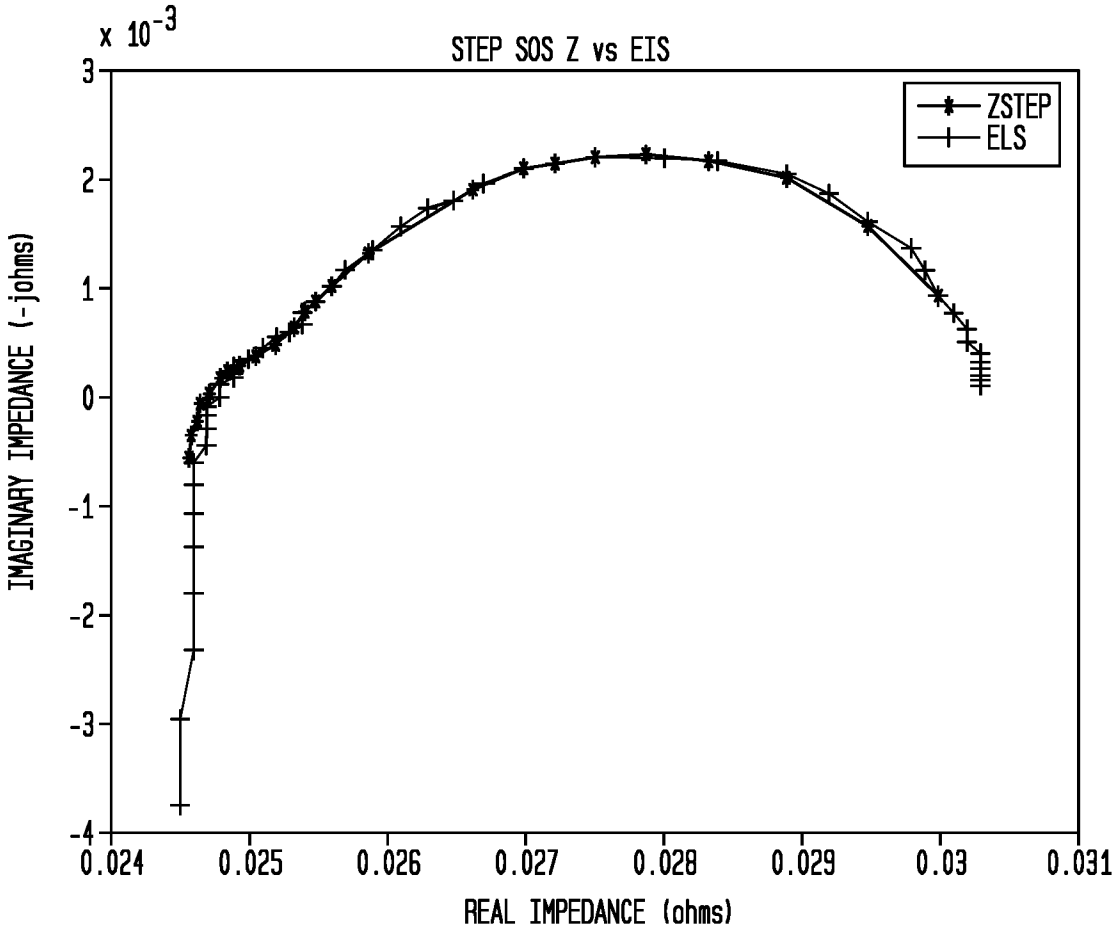

x 10-3
STEP SOS Z vs EIS
ZSTEP
ELS
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 41

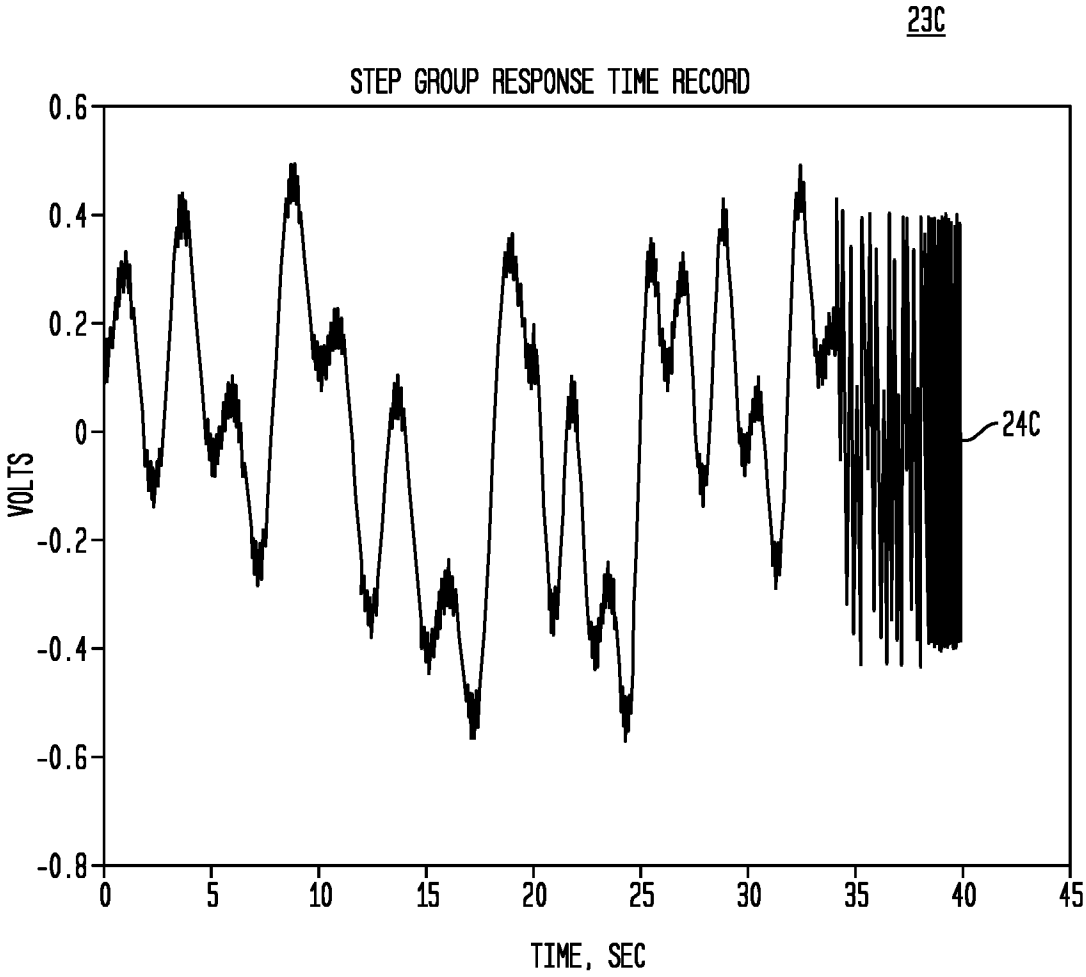

23C
STEP GROUP RESPONSE TIME RECORD
VOLTS
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
0
5
10
15
20
25
30
35
40
45
TIME, SEC
24C

FIG. 42

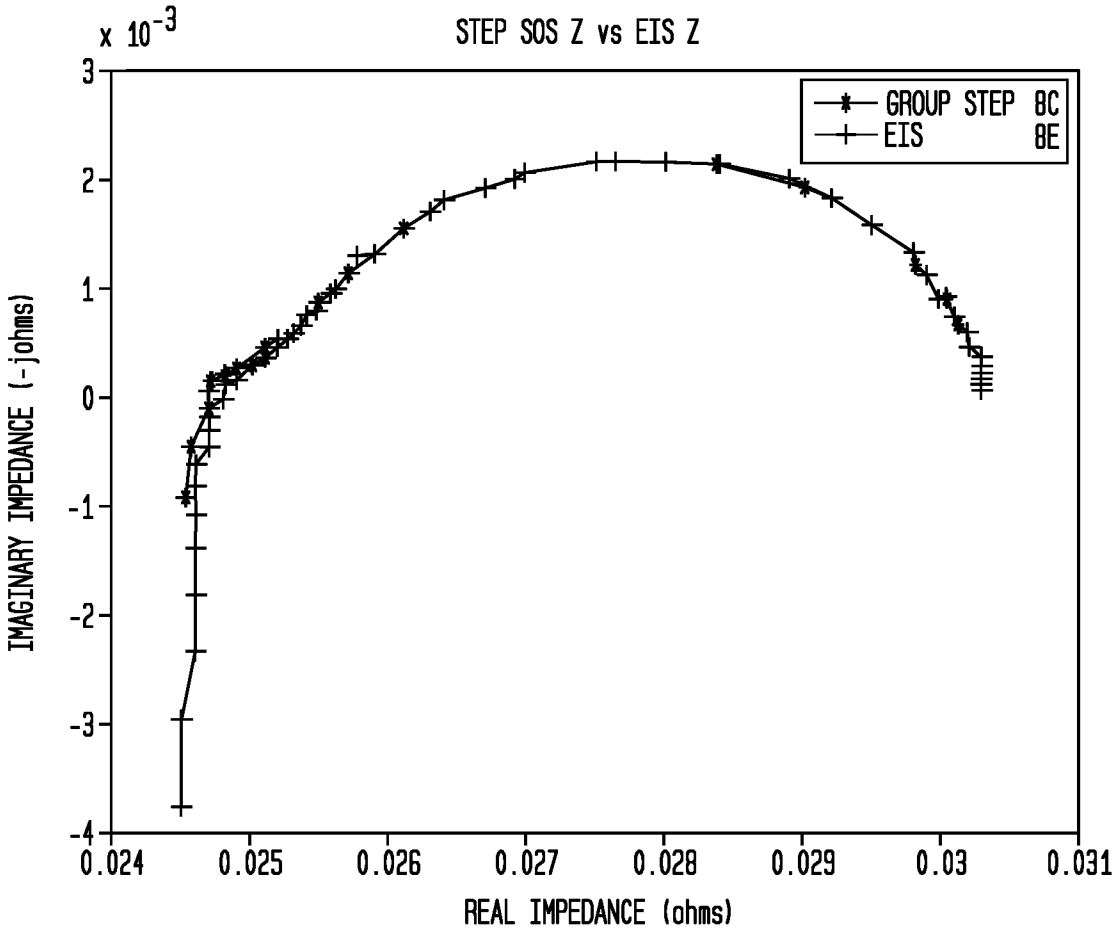

x 10^-3
STEP SOS Z vs EIS Z
GROUP STEP 8C
EIS 8E
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
3
2
1
0
-1
-2
-3
-4
0.024
0.025
0.026
0.027
0.028
0.029
0.03
0.031

FIG. 43

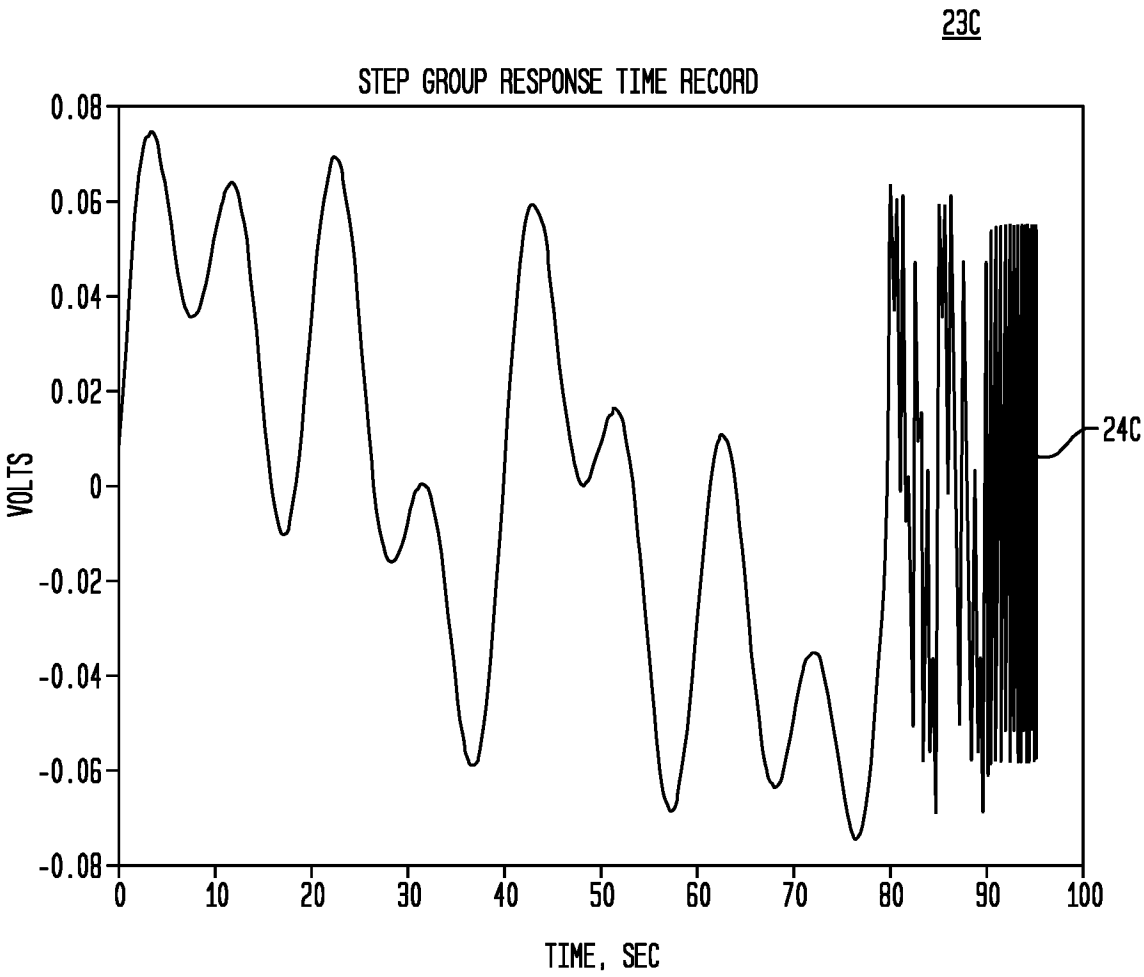

23C
STEP GROUP RESPONSE TIME RECORD
VOLTS
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
0
10
20
30
40
50
60
70
80
90
100
TIME, SEC
24C

FIG. 44

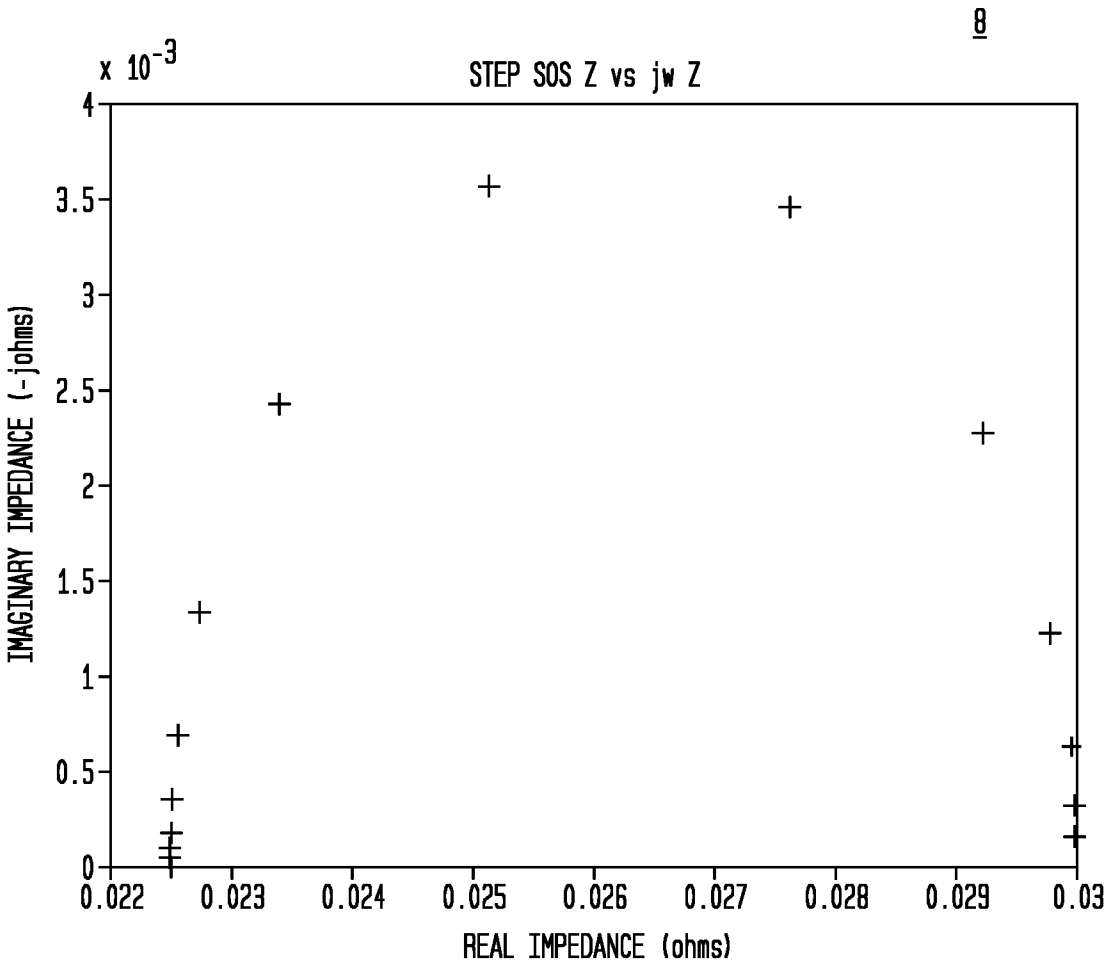

8
x 10^-3
STEP SOS Z vs jw Z
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
4
3.5
3
2.5
2
1.5
1
0.5
0
0.022
0.023
0.024
0.025
0.026
0.027
0.028
0.029
0.03

FIG. 45

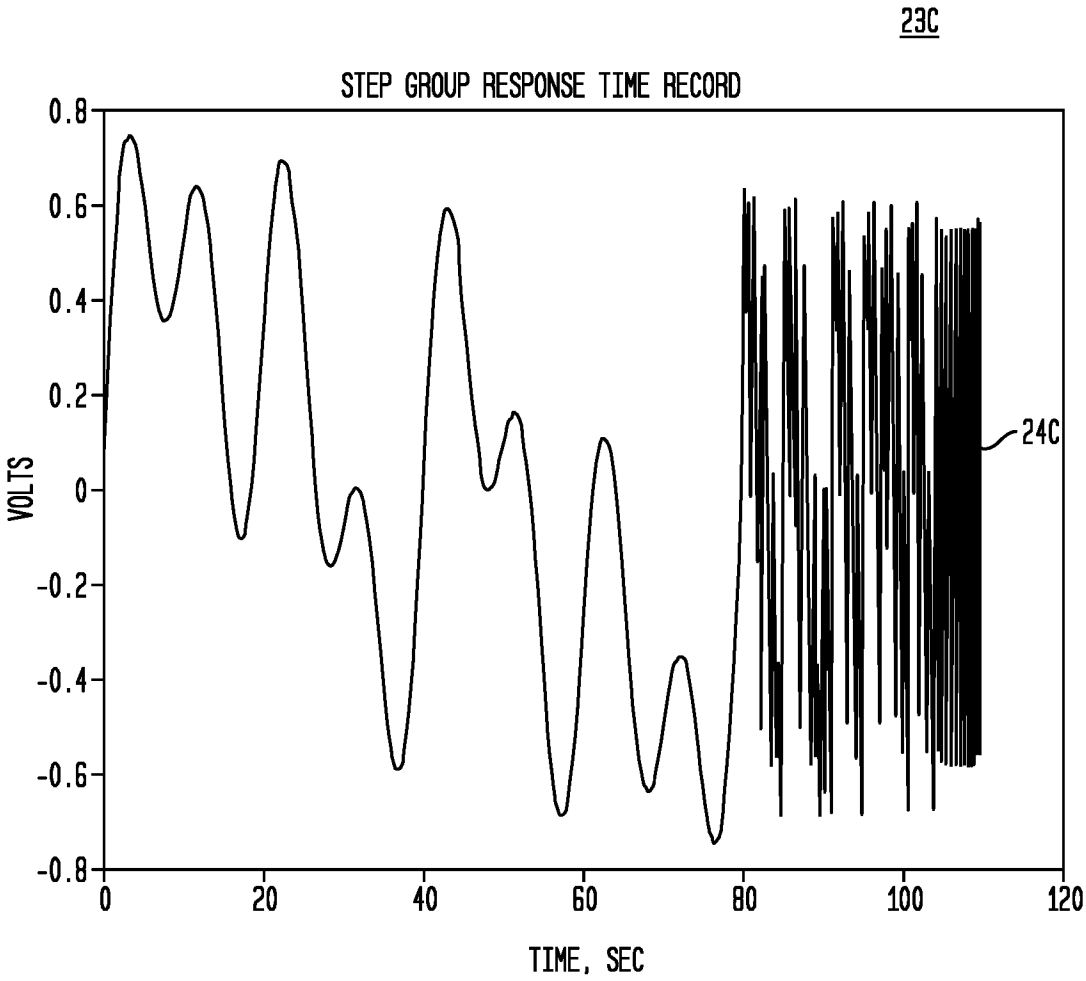

23C
STEP GROUP RESPONSE TIME RECORD
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
VOLTS
24C
0
20
40
60
80
100
120
TIME, SEC

FIG. 46

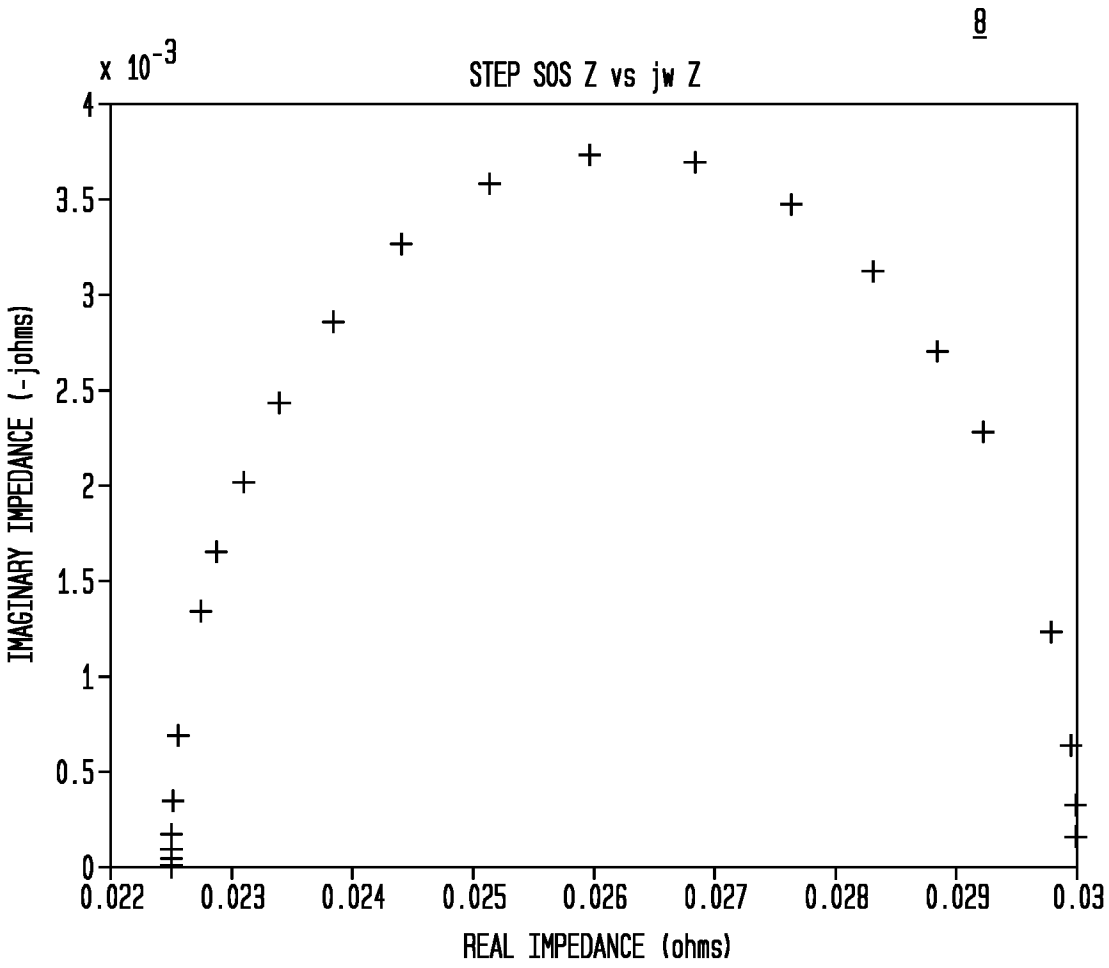

8
x 10^-3
STEP SOS Z vs jw Z
IMAGINARY IMPEDANCE (-johms)
REAL IMPEDANCE (ohms)
4
3.5
3
2.5
2
1.5
1
0.5
0
0.022
0.023
0.024
0.025
0.026
0.027
0.028
0.029
0.03

FIG. 47

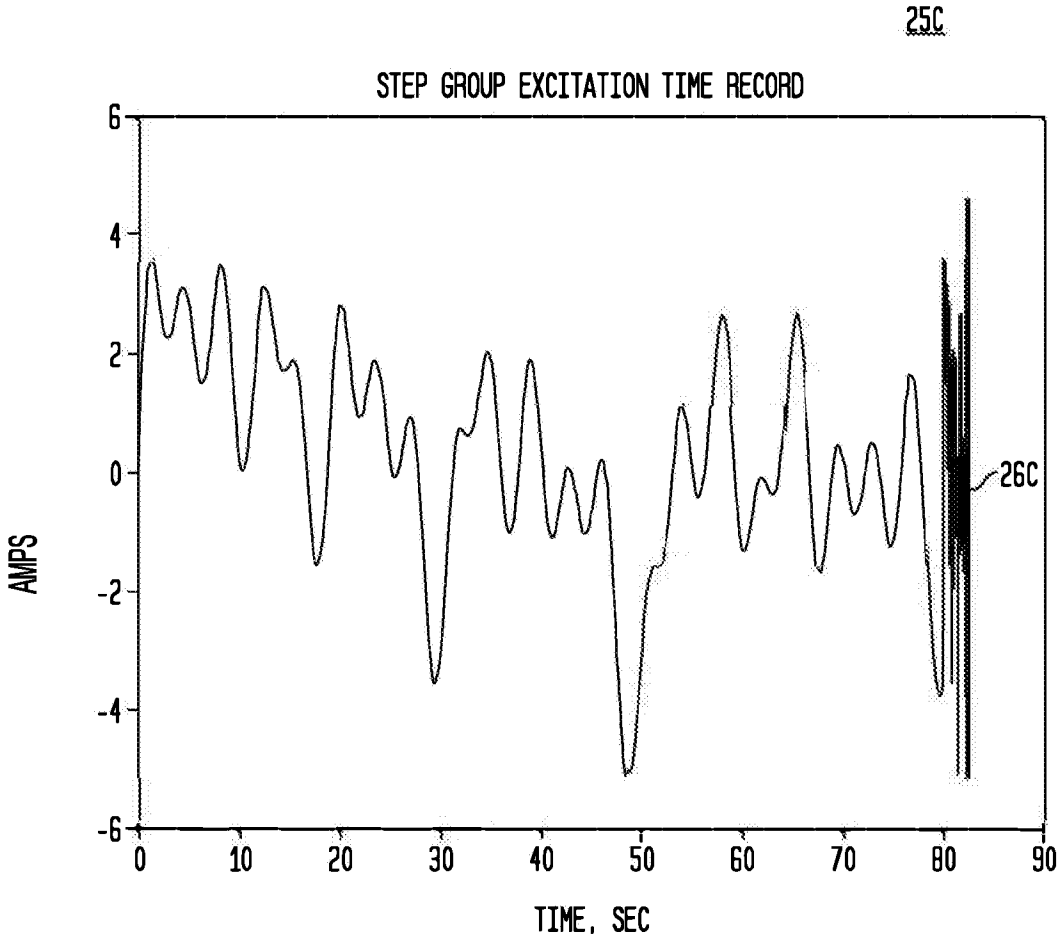

25C
STEP GROUP EXCITATION TIME RECORD
AMPS
6
4
2
0
-2
-4
-6
0
10
20
30
40
50
60
70
80
90
TIME, SEC
26C

FIG. 48

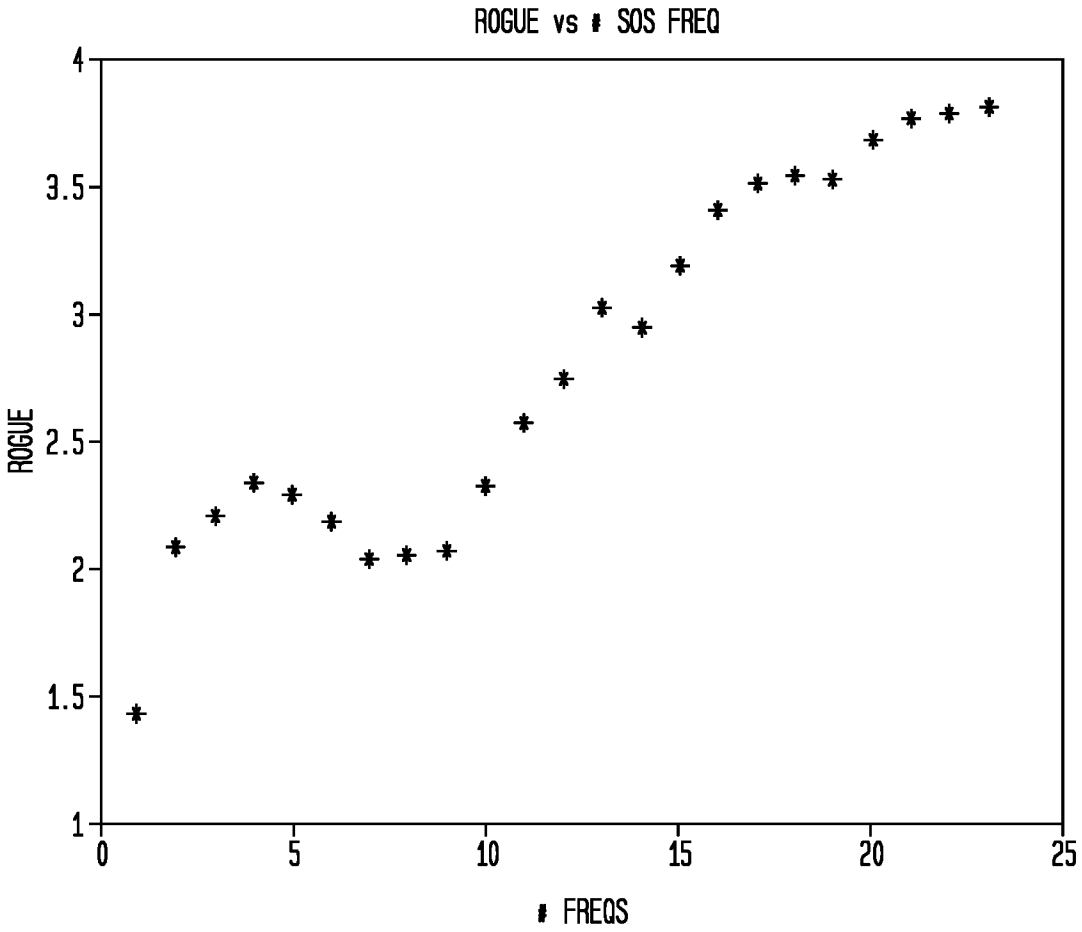


FIG. 49

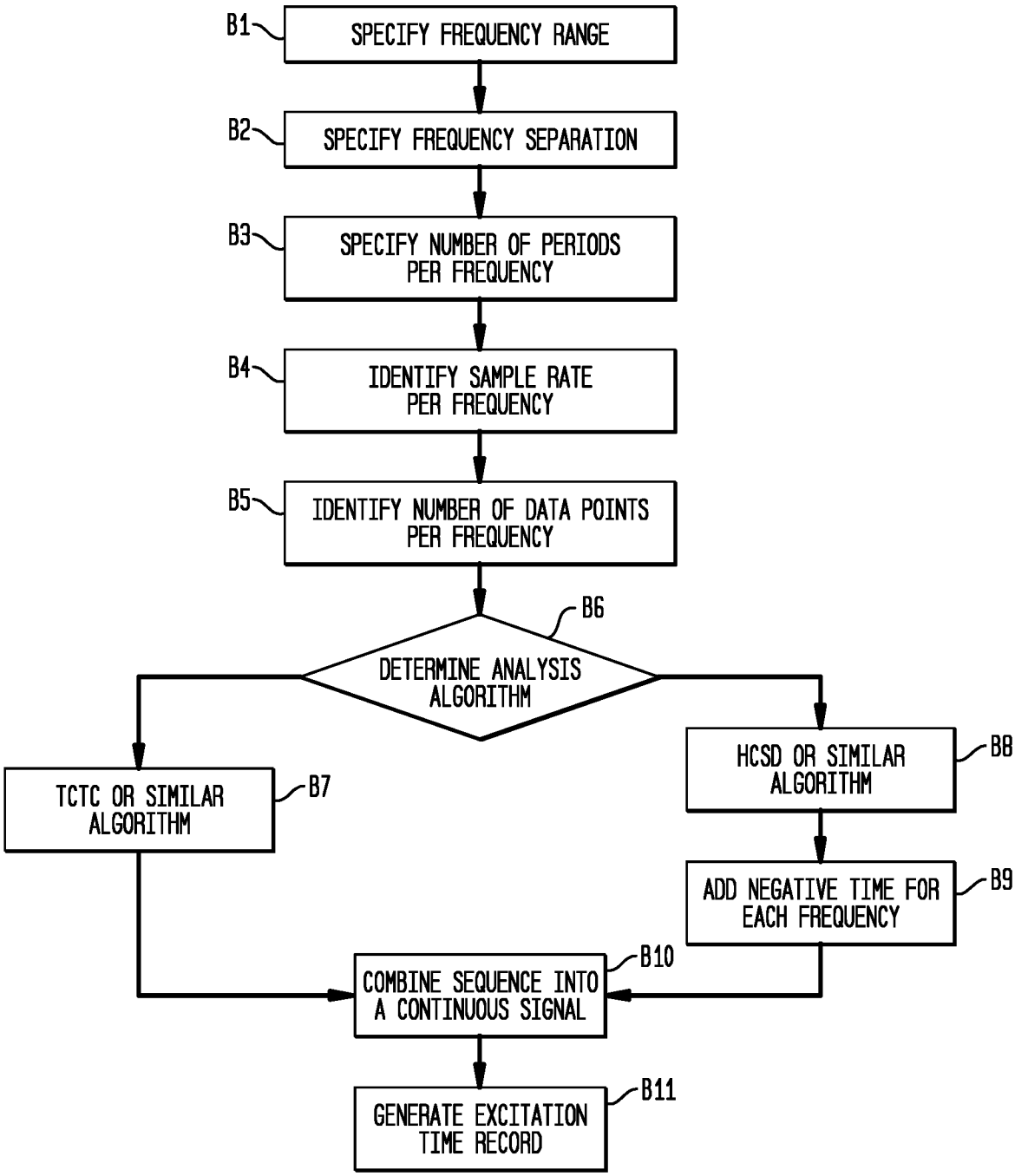

B1
SPECIFY FREQUENCY RANGE
B2
SPECIFY FREQUENCY SEPARATION
B3
SPECIFY NUMBER OF PERIODS PER FREQUENCY
B4
IDENTIFY SAMPLE RATE PER FREQUENCY
B5
IDENTIFY NUMBER OF DATA POINTS PER FREQUENCY
B6
DETERMINE ANALYSIS ALGORITHM
TCTC OR SIMILAR ALGORITHM
B7
HCSD OR SIMILAR ALGORITHM
B8
ADD NEGATIVE TIME FOR EACH FREQUENCY
B9
COMBINE SEQUENCE INTO A CONTINUOUS SIGNAL
B10
GENERATE EXCITATION TIME RECORD
B11

FIG. 50

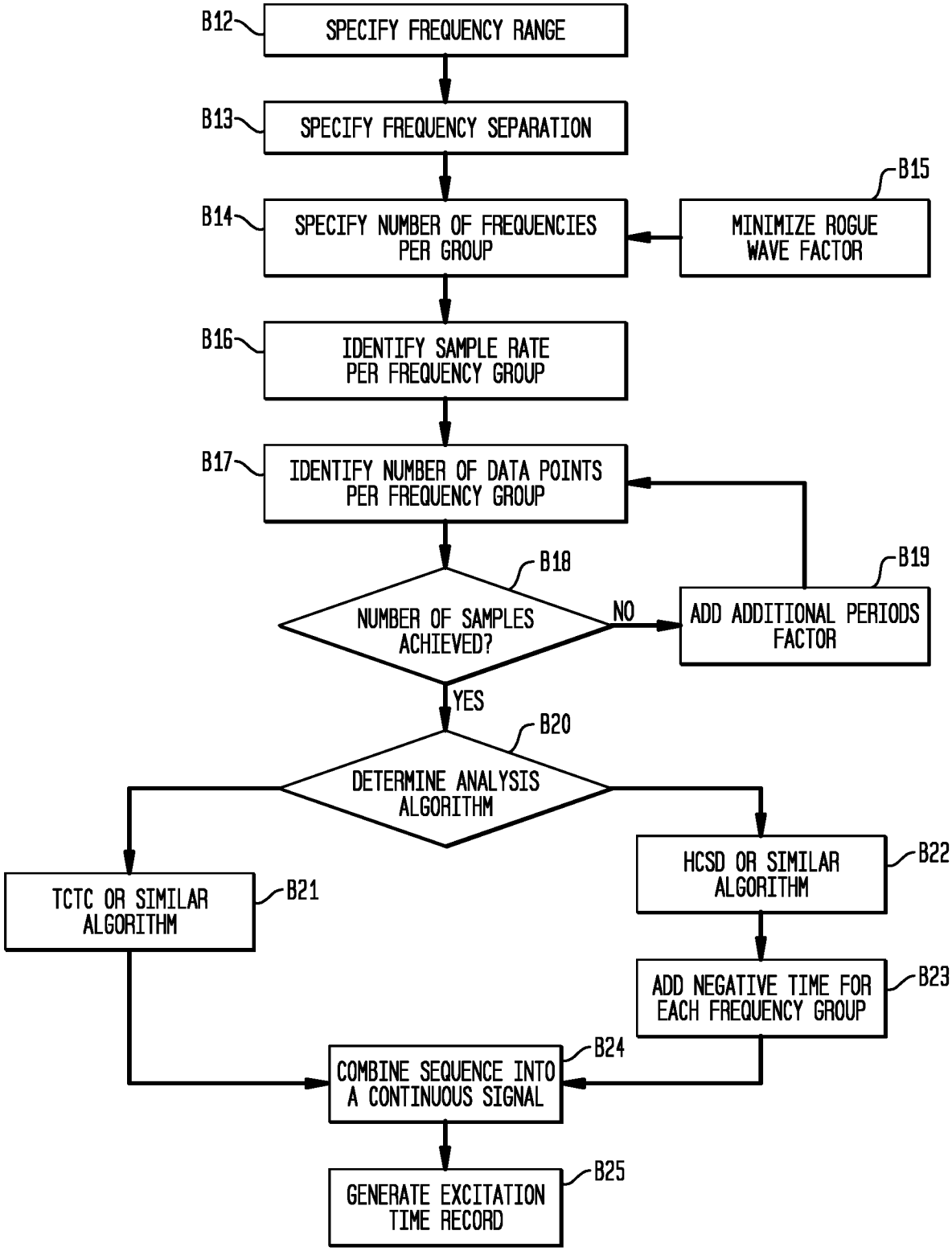

B12
SPECIFY FREQUENCY RANGE
B13
SPECIFY FREQUENCY SEPARATION
B14
SPECIFY NUMBER OF FREQUENCIES PER GROUP
B15
MINIMIZE ROGUE WAVE FACTOR
B16
IDENTIFY SAMPLE RATE PER FREQUENCY GROUP
B17
IDENTIFY NUMBER OF DATA POINTS PER FREQUENCY GROUP
B18
NUMBER OF SAMPLES ACHIEVED?
NO
B19
ADD ADDITIONAL PERIODS FACTOR
YES
B20
DETERMINE ANALYSIS ALGORITHM
TCTC OR SIMILAR ALGORITHM
B21
HCSD OR SIMILAR ALGORITHM
B22
ADD NEGATIVE TIME FOR EACH FREQUENCY GROUP
B23
COMBINE SEQUENCE INTO A CONTINUOUS SIGNAL
B24
GENERATE EXCITATION TIME RECORD
B25

FIG. 51

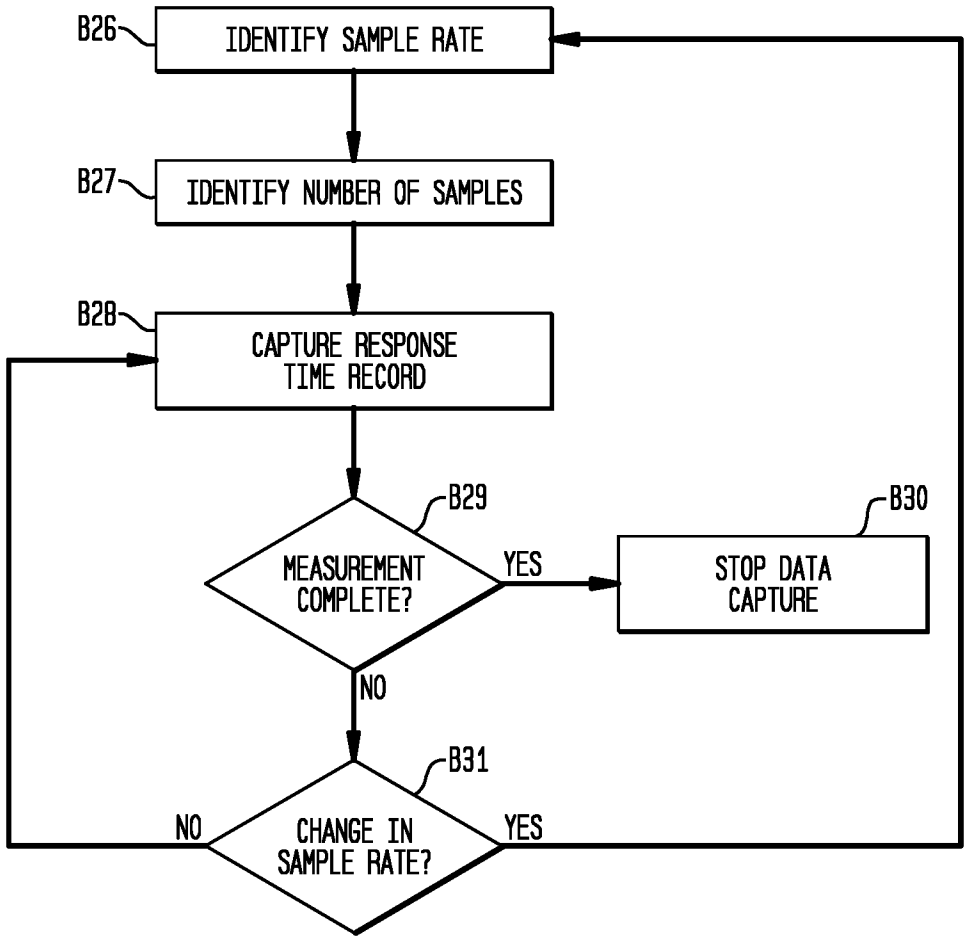

B26
IDENTIFY SAMPLE RATE
B27
IDENTIFY NUMBER OF SAMPLES
B28
CAPTURE RESPONSE TIME RECORD
B29
MEASUREMENT COMPLETE?
YES
B30
STOP DATA CAPTURE
NO
B31
CHANGE IN SAMPLE RATE?
NO
YES

FIG. 52

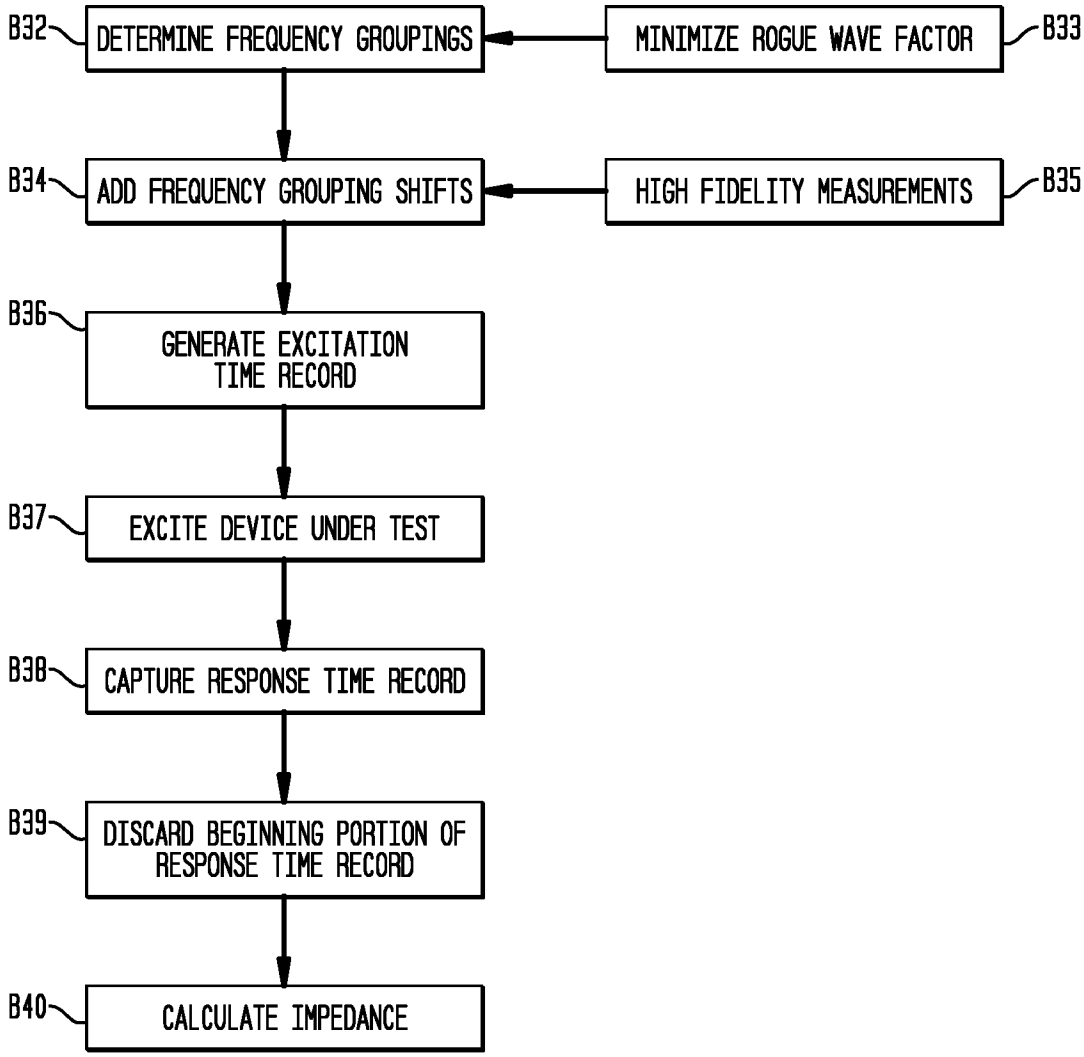
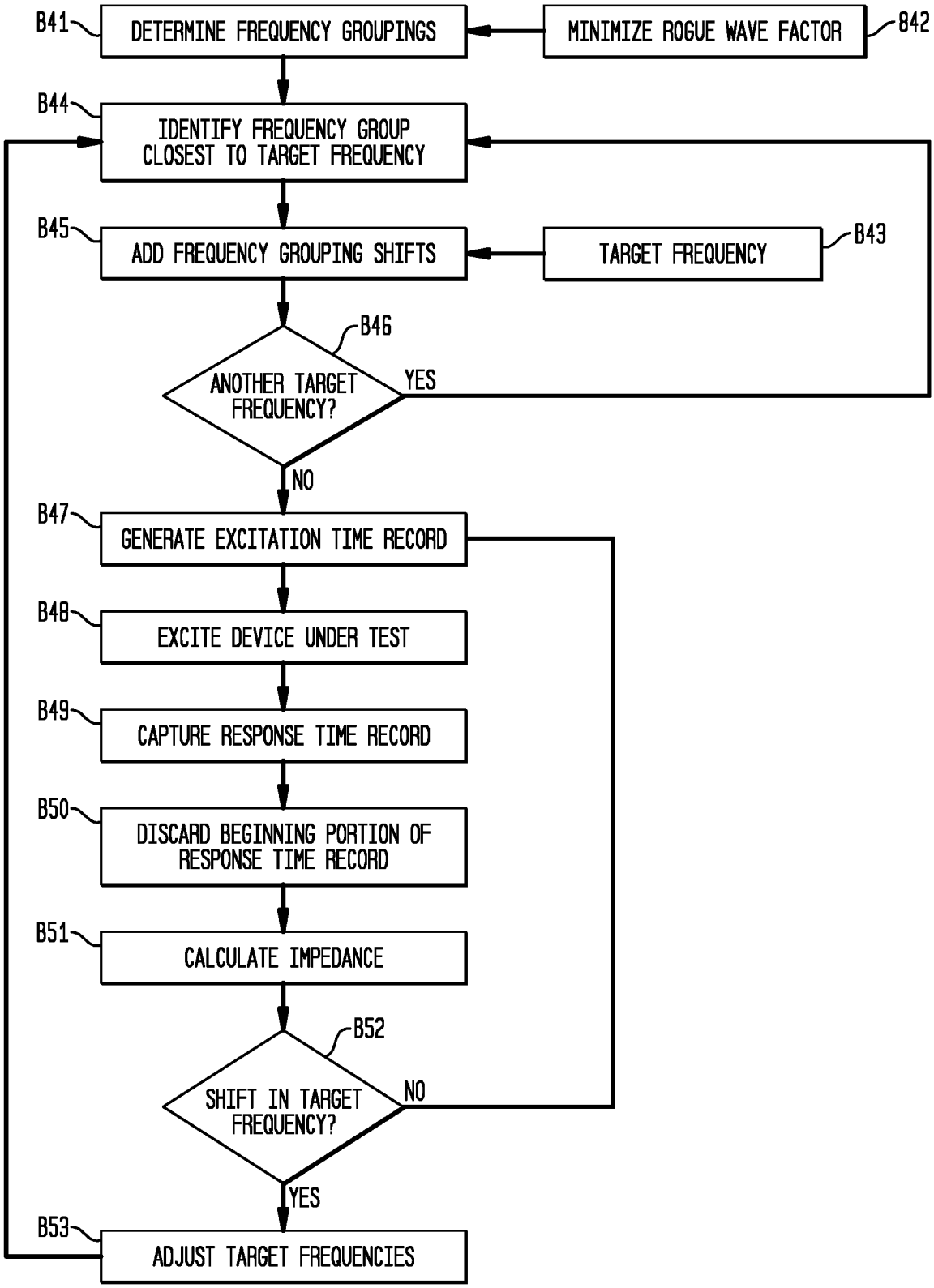

B32
DETERMINE FREQUENCY GROUPINGS
MINIMIZE ROGUE WAVE FACTOR
B33
B34
ADD FREQUENCY GROUPING SHIFTS
HIGH FIDELITY MEASUREMENTS
B35
B36
GENERATE EXCITATION TIME RECORD
B37
EXCITE DEVICE UNDER TEST
B38
CAPTURE RESPONSE TIME RECORD
B39
DISCARD BEGINNING PORTION OF RESPONSE TIME RECORD
B40
CALCULATE IMPEDANCE

FIG. 53


B41
DETERMINE FREQUENCY GROUPINGS
MINIMIZE ROGUE WAVE FACTOR
842
B44
IDENTIFY FREQUENCY GROUP CLOSEST TO TARGET FREQUENCY
B45
ADD FREQUENCY GROUPING SHIFTS
TARGET FREQUENCY
B43
B46
ANOTHER TARGET FREQUENCY?
YES
NO
B47
GENERATE EXCITATION TIME RECORD
B48
EXCITE DEVICE UNDER TEST
B49
CAPTURE RESPONSE TIME RECORD
B50
DISCARD BEGINNING PORTION OF RESPONSE TIME RECORD
B51
CALCULATE IMPEDANCE
B52
SHIFT IN TARGET FREQUENCY?
NO
YES
B53
ADJUST TARGET FREQUENCIES

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 20/31021

A. CLASSIFICATION OF SUBJECT MATTER

IPC - G01R 27/02, G01R 29/26 (2020.01)

CPC - G01R 27/02, G01R 27/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2012/0262186 A1 (Morrison et al.) 18 October 2012 (18.10.2012), para [0051]-[0054], [0056], [0060], 0089], [0096], [0126]-[0127], [0168]	1-5, 8, 10, 17, 19-20 --- 6-7, 9, 11-16, 18
Y	US 2014/0358462 A1 (Battelle Energy Alliance, LLC) 04 December 2014 (04.12.2014), para [0061], [0084], [0124]	6-7, 9, 11-16
Y	US 2010/0274510 A1 (Morrison et al.) 28 October 2010 (28.10.2010), para [0010]	18
A	US 2017/0254859 A1 (BATTELLE ENERGY ALLIANCE, LLC) 07 September 2017 (07.09.2017), entire document	1-20
A	US 6,556,001 B1 (Wiegand et al.) 29 April 2003 (29.04.2003); entire document	1-20
A	US 2017/0003354 A1 (BATTELLE ENERGY ALLIANCE, LLC) 05 January 2017 (05.01.2017), entire document	1-20
A	US 6,885,960 B2 (Wagner et al.) 26 April 2005 (26.04.2005), entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance
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"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 July 2020	06 AUG 2020
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Lee Young Telephone No. PCT Helpdesk: 571-272-4300