Title: DIRECT BUILD-UP LAYER ON AN ENCAPSULATED DIE PACKAGE

Abstract: A microelectronic package including a microelectronic die having an active surface and at least one side. An encapsulation material is disposed adjacent the microelectronic die side(s), wherein the encapsulation material includes at least one surface substantially planar to the microelectronic die active surface. A first dielectric material layer may be disposed on at least a portion of the microelectronic die active surface and the encapsulation material surface. At least one conductive trace is then disposed on the first dielectric material layer. The conductive trace(s) is in electrical contact with the microelectronic die active surface. At least one conductive trace extends adjacent the microelectronic die active surface and adjacent the encapsulation material surface.
### INTERNATIONAL SEARCH REPORT

**Intern/val Application No**  
PCT/US 01/25060

## A. CLASSIFICATION OF SUBJECT MATTER

**IPC 7**  
HO1L23/31

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

**Minimum documentation searched (classification system followed by classification symbols)**

**IPC 7**  
HO1L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

**Electronic data base consulted during the international search (name of data base and, where practical, search terms used)**

EPO-Internal, WPI Data, PAJ

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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| **X**    | EP 0 611 129 A (GEN ELECTRIC)  
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abstract; figures 1A,1E,4A,5B,8D  
column 1, line 55 -column 2, line 51  
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Further documents are listed in the continuation of box C.

### Date of the actual completion of the international search

29 April 2003

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Favre, P

### Date of mailing of the international search report

28/05/2003

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**Information on patent family members**

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