(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 April 2013 (18.04.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/055700 A1

(51) International Patent Classification:
H01L 23/60 (2006.01) *H05K 9/00* (2006.01)

(21) International Application Number:
PCT/US2012/059387

(22) International Filing Date:
9 October 2012 (09.10.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/546,862 13 October 2011 (13.10.2011) US

(71) Applicant: **FLIPCHIP INTERNATIONAL, LLC** [US/US]; 3701 E. University Drive, Phoenix, AZ 85034 (US).

(72) Inventors: **CLARK, David**; 43 Valley Road, Ipswich Suffolk IPI4EE (GB). **TESSIER, Theodore G.**; 268 W. Kingbird Drive, Chandler, AZ 85248 (US).

(74) Agents: **NEEL, Bruce T.** et al.; Greenberg Traurig, LLP (LA), Intellectual Property Department, 77 West Wacker Drive, Suite 3100, Chicago, IL 60601 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: WAFER LEVEL APPLIED RF SHIELDS

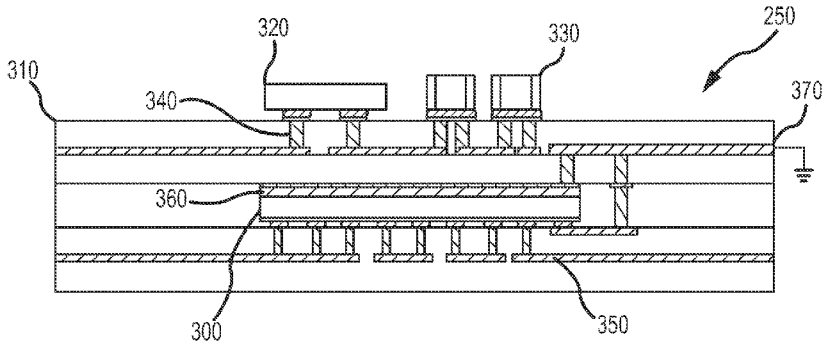

FIG.3

(57) Abstract: An embodiment of a method of forming an on-chip RF shield on an integrated circuit chip in accordance with the present disclosure includes providing a wafer level integrated circuit component wafer having a front side and a back side before singulation; applying a resin metal layer on a back side of the wafer; and then separating the wafer into discrete RF shielded components. It is this resin metal layer on the back side that acts effectively as the RF shield, after singulation, i.e. separation of the wafer, into discrete RF shielded components.

WO 2013/055700 A1

WAFER LEVEL APPLIED RF SHIELDS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of priority of United States Provisional Patent Application No. 61/546,862, filed October 13, 2011, entitled Wafer Level Applied RF Shields, the disclosure of which is incorporated by reference herein in its entirety.

FIELD

[0002] The present disclosure generally relates to formation of semiconductor chips and more particularly to a structure and method for the creation of on-chip RF shielding for active, passive or discrete components for embedded die packages.

BACKGROUND

[0003] In certain electronic packaging applications, it is imperative to protect the device and system circuitry from sources of Electro-Magnetic Interference (EMI). It is also important to ensure that said device or system circuitry does not transmit EMI radiation to systems external to it. Hereby, ensuring the ability of such systems to operate as intended within a specific electromagnetic environment.

[0004] Spurious sources of EMI can lead to overall system or integrated circuit performance degradation, for example, through noise, cross talk and reduced signal-to-noise ratios. EMI is particularly problematic in mixed signal circuits.

[0005] EMI issues are typically solved by Radio Frequency (RF) shielding, whereby, the circuitry in question is capped by a dedicated metallic RF shield. A conductive and grounded shield (also known as a Faraday shield) between the EMI signal source and the system circuitry will eliminate this noise, by routing the EMI induced displacement currents directly to ground.

[0006] Such RF shields are normally mounted onto the system printed wiring board (PWB) by Surface Mount Technology (SMT) and may enclose a single or multiple components such as active, passive or discrete devices.

[0007] In embedded die packaging applications, RF shielding is particularly challenging. Use of traditional surface mounted RF shields may impose PWB routing design limitations and may impose keep out zones above or near EMI sensitive components.

[0008] In embedded die applications, it would be highly preferable if the PWB external surface area directly above the embedded component(s) was available for further component population and integration. It is not desirable to consume this valuable surface area real estate with low value add RF shielding components.

[0009] In some PWB designs, an entire PWB layer may be dedicated to provide a digital or analog ground plane thus providing further EMI protection to the component. Dedicating an entire PWB layer to EMI protection can be a costly solution and such a layer further inhibits routing to be placed in the EMI protected zone.

[0010] Surface mounted PWB, or other RF shields are typically connected to the system electrical ground plane through the existing PWB circuitry.

[0011] Surface mounted RF shields typically form the highest point on the PWB surface. Therefore the RF shield can often limit the total package or product thickness.

[0012] Surface mounted RF shields completely encapsulate sensitive components with contact to the PWB made around the periphery of the shield and thus tending to increase component or system footprint. In addition, surface mount RF shields can generate warpage of the overall chip package shape.

SUMMARY OF THE DISCLOSURE

[0013] The method according to the present disclosure addresses the above noted deficiencies. One embodiment of a method of forming an on-chip RF shield on an integrated circuit chip in accordance with the present disclosure includes

providing a wafer level integrated circuit component wafer having a front side and a back side before singulation; applying a resin metal layer on a back side of the wafer; and then separating the wafer into discrete RF shielded components. It is this resin metal layer on the back side that acts effectively as the RF shield for the components on the wafer. The resin metal layer preferably includes a metal foil and may also have a planar copper foil on an outer surface of the layer.

[0014] Another embodiment in accordance with the present disclosure is an integrated circuit chip cut from a wafer level integrated circuit component wafer having a front side and a back side and a resin metal layer formed on at least the back side of the wafer. The wafer may also have a resin metal layer over components on the front side of the wafer. The resin metal layer preferably includes a metal foil. This metal foil preferably is a copper foil on an outer surface thereof. The metal layer on the chip may be a resin copper foil (RCF) layer. In such an embodiment the RCF layer is a conductive paste applied on the back side of the wafer over at least one component on the wafer. This conductive paste may also be applied on the front side of the wafer over another component on the wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] For a more complete understanding of the present disclosure, reference is now made to the following figures in which:

[0016] FIG. **1** is a schematic cross sectional view of a typical EMI protected printed wiring board (PWB).

[0017] FIG. **2a** is a schematic cross sectional view of an embeddable electronic integrated circuit component in accordance with the present disclosure.

[0018] FIG. **2b** is a schematic cross section view of the electronic component shown in Fig. **2a** in a wafer level chip scale package format in accordance with the present disclosure.

[0019] FIG. **3** is a schematic cross sectional view through an embedded chip packaging configuration in accordance with the present disclosure.

DETAILED DESCRIPTION

[0020] This disclosure provides a low cost method for wafer level application of RF shielding for use in multiple electronic packaging formats and applications. This method is particularly useful in embedded die package applications to provide high yielding wafer level applied RF shielding.

[0021] FIG. **1** illustrates a typical EMI shielding system on a printed wiring board (PWB). Single or multiple active and/or passive components **100** together with surface mounted discrete components **110** may be used to form an electronic system. The components are mounted on a typical printed circuit or wiring board **120**. Electrical connectivity between the components is made using standard PWB through vias **130** and redistribution tracks **140**. A typical SMT board mount RF shield **150** covers the system components and is connected through the PWB circuitry to electrical ground **160**. The RF shield is typically either soldered or glued to the PWB around the periphery of the components **170**.

[0022] FIG. **2a** illustrates an embeddable electronic integrated circuit component wafer **200** after wafer level fabrication and prior to singulation, i.e. before separation into discrete components in accordance with the present disclosure. The component wafer **200** includes a plurality of integrated circuit components and also contains integrated circuitry of the front side **210** with defined pads **220** for electronic connectivity to a printed wiring board. A layer of resin **230** with copper foil **240**, called an RCF layer, is applied at wafer level thus forming an on-chip ready RF shield prior to device singulation.

[0023] The process in accordance with the present disclosure includes operations of (1) providing a wafer level component wafer prior to singulation from a wafer foundry; (2) applying a resin metal foil layer to at least the back side of the wafer thus forming a shielded wafer; (3) then separating the shielded wafer into discrete componentry. The foil layer is preferably copper. However other electrically conductive metals may alternatively be used such as gold, silver, silver alloy, or a copper alloy.

[0024] FIG. **2b** illustrates an electronic component **200** in a wafer level chip scale package format with the wafer level applied RF shield formed on the

component back side as in FIG. **2a**. In the chip scale package (CSP) format shown, a copper paste filled through via **250** provides an electrical ground connection between the RF shield layer and the bulk semiconductor substrate.

[0025] FIG. **3** illustrates an embedded die package configuration **250** incorporating the EMI shielded component **300** produced as is shown in FIG. **2**. Active, passive or discrete component(s) **300** as shown are embedded within the PWB substrate **310**. The package **250** also has surface mounted active or passive ICs **320** and accompanying discrete components **330**. Electrical connectivity between the embedded component **300** and surface mounted components **320** and **330** is made using conventional through vias **340** and redistribution lines **350**. The embedded component **300** includes a backside RCF layer **360** forming the on-chip RF shielding. The on-chip RF shield is connected via existing PWB circuitry to the system ground plane **370**.

[0026] A wafer level RF shield in accordance with the present disclosure can be used for a variety of wafer level RF shielding solutions, designs, thickness and geometries without adding significant process complexity or cost.

[0027] The EMI protective resin copper foil (RCF) layer may also be applied, in some applications, to the front side of the wafer level wafer to thus fully encapsulate the component. The RCF layer may utilize other metal alloys than copper which are also electrically conductive so as to provide RF shielding. Thus in accordance with the present disclosure, the individual component, after singulation, contains dedicated RF shielding features for use in localized EMI protection. The resin copper foil layer is used to conduct induced noise currents from EMI sources to the system electrical ground.

[0028] An RF shielded component constructed in accordance with the present disclosure is particularly applicable, but not limited to a variety of final component packaging formats, including flipchip packages, system-in-package, embedded die packages and other multi-die, multi-discrete 3D packages. This method is particularly desirable for embedded die packages.

[0029] The method described here-in improves component adhesion within embedded die packages and improves outgassing from the integrated circuit

layers within embedded die applications. The RCF EMI shield layer maybe a conformal layer or pattern layer suitable for specific RF frequency filtering requirements. The resin layer may be chosen with a high-k material property to aid with reducing capacitively coupled EMI sources.

[0030] This method offers a lower cost solution compared to state-of-art electroplated on-chip alternatives and which can also aid with thermal dissipation. In addition the on-chip RF shield in accordance with the present disclosure eliminates potential overall package warpage that may otherwise occur with use of externally applied RF shields. Furthermore, the on-chip RF shield can be used in a surface mount configuration whereby the ground signal is provided by way of backside wirebond attach. All of these alternatives and features exemplify modifications that can be made which are within the meaning and broad scope of the disclosure and exemplified in the following claims.

Claims

1. A method of forming an on-chip RF shield on an integrated circuit chip comprising:

providing a wafer level integrated circuit component wafer having a front side and a back side;

applying a resin metal layer on at least a back side of the wafer; and

separating the wafer into discrete RF shielded components.

2. The method of claim 1 wherein the resin metal layer includes a metal foil thereon.

3. The method of claim 1 wherein the resin metal layer includes a planar copper foil on an outer surface thereof.

4. The method of claim 1 wherein the resin metal layer is selected from a group consisting of copper, gold, silver, gold alloy and copper alloy.

5. The method of claim 1 wherein the resin metal layer is applied as a paste.

6. An integrated circuit chip comprising:

a wafer level integrated circuit component wafer having a front side and a back side; and

a resin metal layer formed on at least the back side of the wafer.

7. The chip of claim 6 wherein the resin metal layer includes a metal foil.

8. The chip of claim 7 wherein the metal foil has a copper foil on an outer surface thereof.

9. The chip of claim 6 wherein the metal layer is a resin copper foil (RCF) layer.

10. The chip of claim 9 wherein the RCF layer is a paste on the back side of the wafer over at least one component on the wafer.

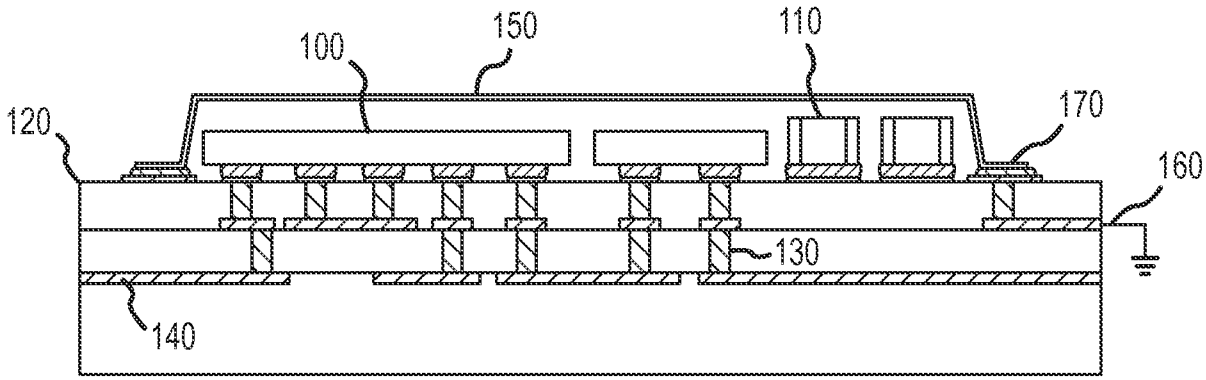

FIG.1

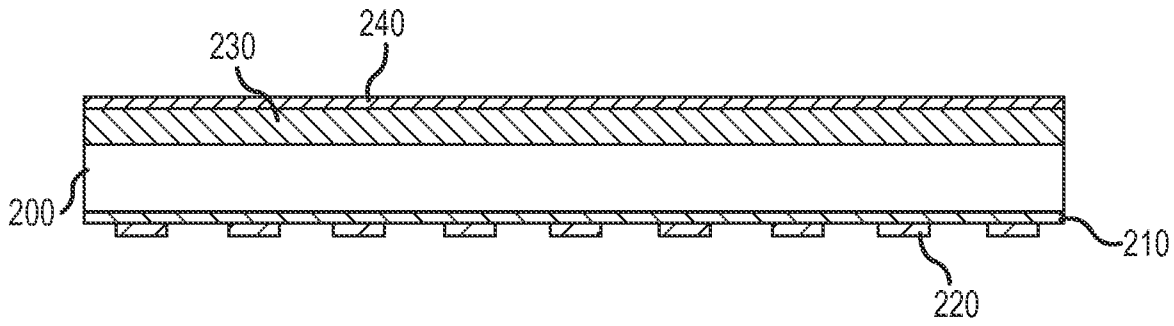

FIG.2a

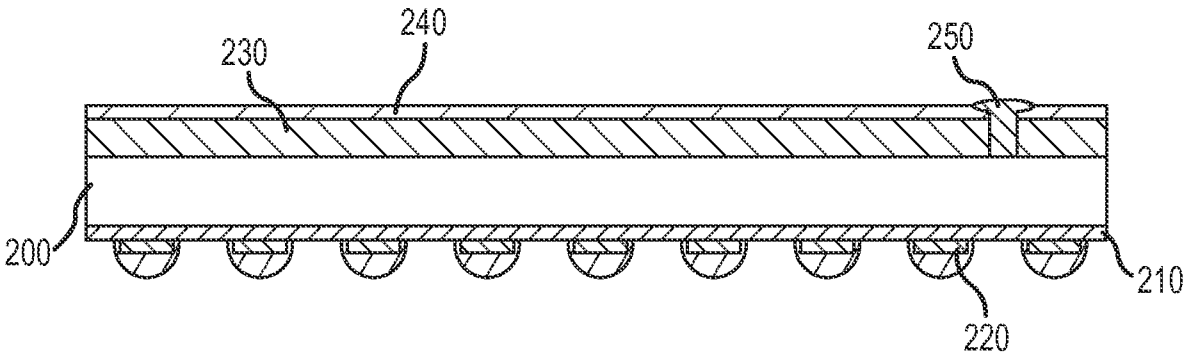

FIG.2b

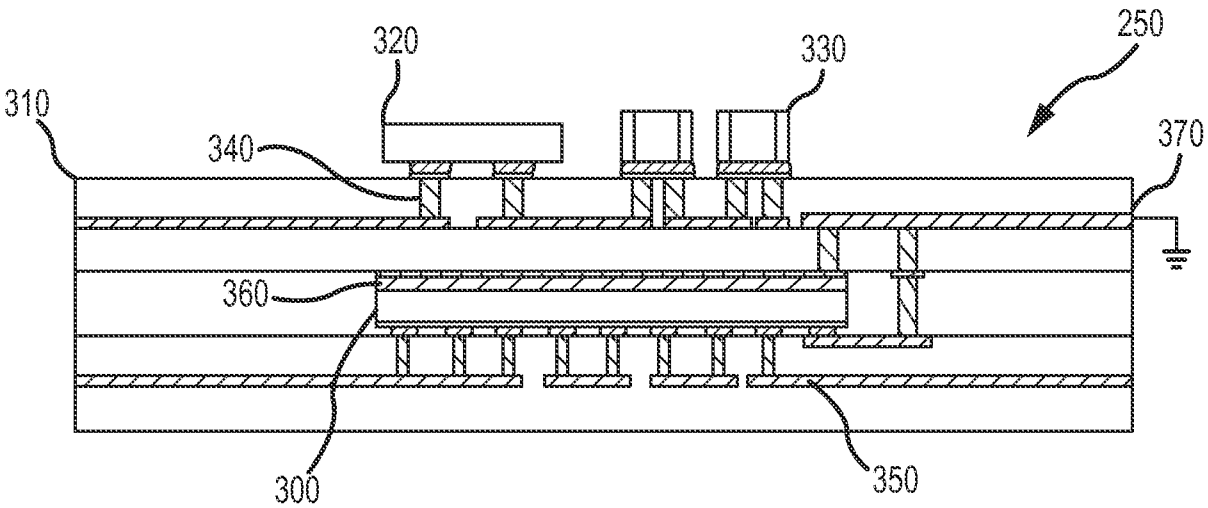

FIG.3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/059387

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/60(2006.01)i, H05K 9/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/60; H01L 23/52; H01L 21/56; H01L 25/04; H05K 9/00; H01L 23/48; H01L 21/78; H01L 23/29; H01L 23/28

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:wafer,level,resin,copper,shield,emi,electromagnetic

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006-0038245 A1 (MAKOTO TERUI) 23 February 2006 See abstract,page 2, figures 1-2.	1-10
Y	US 2009-0079041 A1 (RUI HUANG et al.) 26 March 2009 See abstract, page 2, figure 1b.	1-10
Y	US 2010-0270661 A1 (YAOJIAN LIN et al.) 28 October 2010 See abstract, pages 4-5, figure 3.	1-10
A	JP 2554040 Y2 (MITSUBA LTD) 18 July 1997 See abstract, figure 2.	1-10
A	JP 10-214923 A (FUJITSU DENSO LTD) 11 August 1998 See abstract.	1-10

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 MARCH 2013 (07.03.2013)	**08 MARCH 2013 (08.03.2013)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

LEE, Sang Don

Telephone No. 82-42-481-5665

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2012/059387

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006-0038245 A1	23.02.2006	JP 2006-059839 A	02.03.2006
		US 7687283 B2	30.03.2010
US 2009-0079041 A1	26.03.2009	KR 10-2009-0031650 A	27.03.2009
		KR20090031650A	27.03.2009
		SG151163A1	30.04.2009
		TW 200915527 A	01.04.2009
		US 7701040 B2	20.04.2010
US 2010-0270661 A1	28.10.2010	US 2009-0302439 A1	10.12.2009
		US 7772046 B2	10.08.2010
		US 8076757 B2	13.12.2011
JP 2554040 Y2	18.07.1997	JP 5041199 U	01.06.1993
		JP H0-541199 U	01.06.1993
JP 10-214923 A	11.08.1998	JP 3082905 B2	04.09.2000