



- (51) **International Patent Classification:**
H01L 21/02 (2006.01)
- (21) **International Application Number:**
PCT/GB2017/050769
- (22) **International Filing Date:**
20 March 2017 (20.03.2017)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
1604689.8 21 March 2016 (21.03.2016) GB
- (71) **Applicant:** THE UNIVERSITY OF WARWICK
[GB/GB]; University House, Coventry Warwickshire CV4
8UW (GB).
- (72) **Inventor:** BEANLAND, Richard; c/o The University of
Warwick, University House, Coventry Warwickshire CV4
8UW (GB).
- (74) **Agents:** PIOTROWICZ, Pawel et al.; Venner Shipley
LLP, Byron House, Cambridge Business Park, Cowley
Road, Cambridge Cambridgeshire CB4 0WZ (GB).
- (81) **Designated States** (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN,
KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA,
MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG,
NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS,
RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY,
TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN,
ZA, ZM, ZW.

- (84) **Designated States** (*unless otherwise indicated, for every
kind of regional protection available*): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,
TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments (Rule 48.2(h))

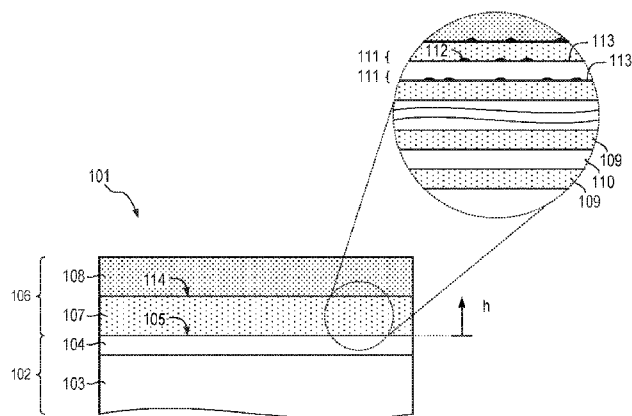
(54) **Title:** HETEROSTRUCTURE

Fig. 15

(57) **Abstract:** A method of growing a heterostructure is disclosed. The method comprises growing an epitaxial multilayer structure (106) on a base structure (102), the multilayer structure comprising a dislocation filter layer structure (107) comprising a stack of at least two dislocation filter layers (109, 110) and, optionally, a device layer structure (108) disposed on the dislocation filter layer structure comprising at least one layer. The method comprises providing at least one layer (111) in the dislocation filter layer structure for inhibiting movement of threading dislocations, wherein the threading dislocation movement inhibiting layer is interposed between two dislocation filter layers. The method comprises relaxing each layer in the dislocation filter layer structure before growing a subsequent layer such that, for each layer in the dislocation filter layer structure which is grown on a respective underlying layer (a) misfit strain-thickness product $\epsilon_0 h$ is equal to or greater than the equilibrium strain-thickness product ϵh_c when the underlying layer is relaxed and (b) strain-thickness product ϵh is equal to or less than the critical strain-thickness product $(\epsilon h)^*$ for dislocation multiplication.

Heterostructure

Field of the Invention

5 The present invention relates to a heterostructure comprising a dislocation filter layer structure.

Background

10 Growth of mismatched heteroepitaxial layers on single crystal substrates has been an active field of research for over forty years. The presence of dislocations that thread through a deposited thin film – and the resulting compromised material properties – has been a persistent problem. This has been a significant issue for the incorporation of, for example, III-V materials with silicon and III-nitride epitaxial layers on sapphire substrates.

15 US 2014/0338589 A1 describes using a semiconductor layer having a plurality of threading dislocations distributed substantially uniformly across its surface as a starting layer to subsequent growth.

20 Reference is also made to Richard Beanland: “Multiplication of misfit dislocations in epitaxial layers”, Journal of Applied Physics, volume 72, page 4031 (1992).

Summary

The present invention seeks to provide an improved heterostructure for reducing density of threading dislocation density, ρ_{TD} , particularly for materials with a high (> 4%) lattice mismatch.

5

According to a first aspect of the present invention there is provided a method of growing a heterostructure. The method comprises growing an epitaxial multilayer structure on a base structure, the multilayer structure comprising a dislocation filter layer structure comprising a stack of at least two dislocation filter layers and a device layer structure disposed on the dislocation filter structure comprising at least one layer. The method comprises providing at least one layer in the dislocation filter layer structure for inhibiting movement of threading dislocations. The threading dislocation movement inhibiting layer is interposed between two dislocation filter layers. The method comprises relaxing each layer in the dislocation filter layer structure before growing a subsequent layer such that, for each layer in the dislocation filter layer structure which is grown on a respective underlying layer (a) misfit strain-thickness product $\varepsilon_o h$ is equal to or greater than the equilibrium strain-thickness product εh_c when the underlying layer is relaxed and (b) strain-thickness product εh is equal to or less than the critical strain-thickness product $(\varepsilon h)^*$ for dislocation multiplication during growth.

10
15
20

Thus, an improved heterostructure can be grown in which the device layer structure can have a low density of threading dislocations.

The multilayer structure may further comprise a device layer structure disposed on the dislocation filter structure, the device layer comprising at least one layer, and the method may comprise relaxing each layer in the device layer structure before growing a subsequent layer such that, for each layer in the device layer structure which is grown on a respective underlying layer (a) misfit strain-thickness product $\varepsilon_o h$ is equal to or greater than the equilibrium strain-thickness product εh_c when the underlying layer is relaxed and (b) strain-thickness product εh is equal to or less than the critical strain-thickness product $(\varepsilon h)^*$ for dislocation multiplication during growth.

According to a second aspect of the present invention there is provided a method of growing a heterostructure. The method comprises growing a device layer structure comprising at least one layer on a dislocation filter layer structure comprising a stack of

25
30
35

at least two dislocation filter layers and at least one layer for inhibiting movement of threading dislocations, wherein the threading dislocation movement inhibiting layer is interposed between two dislocation filter layers. The method comprises relaxing each layer in the device layer structure before growing a subsequent layer such that, for each layer in the device layer structure which is grown on a respective underlying layer (a) misfit strain-thickness product $\epsilon_o h$ is equal to or greater than the equilibrium strain-thickness product ϵh_c when the underlying layer is relaxed and (b) strain-thickness product ϵh is equal to or less than the critical strain-thickness product $(\epsilon h)^*$ for dislocation multiplication during growth.

10

Relaxing a layer may comprise growing a layer sufficiently slowly that relaxation takes place *in-situ*. Relaxing a layer may comprise pausing growth, waiting and resuming growth of the layer. Relaxing a layer may comprise growing the layer, then waiting until the layer has relaxed. The waiting period may be chosen dependent on dislocation velocity. Relaxing a layer may comprise annealing. The anneal temperature may be chosen such that the time required to anneal the layer is less than 100 minutes, less than 50 minutes or less than 20 minutes. The waiting period may differ for different layers. The waiting period for a given layer may be less than the waiting period for a subsequently-grown layer.

20

Providing the threading dislocation movement inhibiting layer may comprise growing a layer of quantum dots. Providing the threading dislocation movement inhibiting layer may comprise introducing dopants, for example, by implanting dopants, by diffusing dopants or by growing a layer of dopants (such as a delta-doped layer). Providing the threading dislocation movement inhibiting layer may comprise implanting ions, for example, to generate small regions of damage. Providing the threading dislocation movement inhibiting layer may comprise forming a misfit dislocation array. Providing the threading dislocation movement inhibiting layer may comprise depositing or forming a non-continuous layer of material, such as dielectric material (such as an oxide or nitride) or a semiconductor material. The non-continuous layer may comprise polycrystalline regions and/or amorphous regions.

Providing the threading dislocation movement inhibiting layer may comprise forming the threading dislocation movement inhibiting layer after growing a dislocation filter layer and before growing a subsequent dislocation filter layer or a device layer. Providing the threading dislocation movement inhibiting layer may comprise forming

35

the threading dislocation movement inhibiting layer after annealing the dislocation filter layer.

5 The dislocation filter layer structure may comprise first and second dislocation filter layers comprising first and second different materials. The dislocation filter layer structure may comprise at least two pairs of dislocation filter layers comprising first and second different materials.

10 The dislocation filter layer structure may include at least a first pair of first and second dislocation filter layers relatively close to base structure which do not have a threading dislocation movement inhibiting layer interposed between the first pair of first and second dislocation filter layers and a second pair of first and second dislocation filter layers relatively far from base structure which has a threading dislocation movement inhibiting layer interposed between the second pair of first and second dislocation filter
15 layers.

The first and second dislocation filter layers may have the same crystal structure and different lattice constants. The first and second dislocation filter layers may comprise first and second semiconductor materials respectively.
20

The dislocation filter layer may include at least one third dislocation filter layer. The dislocation filter layer may include at least one fourth dislocation filter layer. Thus, the dislocation filter structure may comprise different pairs of layers, for example a pair comprising first and second materials and another pair comprising first and third or
25 third and fourth materials.

For a given layer, the critical strain-thickness product $(\epsilon h)^*$ for dislocation multiplication may be four times the equilibrium strain-thickness product ϵh_c .

30 The base structure may comprise a heterostructure comprising a substrate and an uppermost layer. The uppermost layer may have a threading dislocation density ρ_{TD} at least 10^8 cm^{-2} , for example at least 10^9 cm^{-2} , and the device layer structure may have a threading dislocation density ρ_{TD} less than or equal to 10^5 cm^{-2} .

35 According to a second aspect of the present invention there is provided a method of growing a heterostructure. The method comprises growing an epitaxial multilayer

structure directly on a base structure, the multilayer structure comprising a dislocation filter layer structure comprising a stack of at least two layers comprising first and second different materials respectively and a device layer structure disposed on the dislocation filter structure comprising at least one layer. Before growing a layer, for the subsequent layer (a) misfit strain-thickness product $\varepsilon_o h$ is equal to or greater than the equilibrium strain-thickness product εh_c when the layer (i.e. the layer underlying the subsequent layer) is relaxed (b) strain-thickness product εh does not exceed the critical strain-thickness product $(\varepsilon h)^*$ for dislocation multiplication.

According to a third aspect of the present invention there is provided a heterostructure. The heterostructure comprises a base structure and an epitaxial multilayer structure disposed on a base structure, the multilayer structure comprising a dislocation filter layer structure comprising a stack of at least two first and second dislocation filter layers and a device layer structure disposed on the dislocation filter structure comprising at least one layer. The heterostructure further comprises at least one layer in the dislocation filter layer structure for inhibiting movement of threading dislocations. The threading dislocation movement inhibiting layer is interposed between two dislocation filter layers. For each layer in the dislocation filter layer structure which is grown on a respective underlying layer (a) misfit strain-thickness product $\varepsilon_o h$ is equal to or greater than the equilibrium strain-thickness product εh_c when the underlying layer is relaxed and (b) strain-thickness product εh is equal to or less than the critical strain-thickness product $(\varepsilon h)^*$ for dislocation multiplication. For each layer in the epitaxial multilayer structure which is grown on a respective underlying layer (a) misfit strain-thickness product $\varepsilon_o h$ may be equal to or greater than the equilibrium strain-thickness product εh_c when the underlying layer is relaxed and (b) strain-thickness product εh may be equal to or less than the critical strain-thickness product $(\varepsilon h)^*$ for dislocation multiplication.

The base structure may be a heterostructure and may comprise a substrate (for example, a silicon substrate) and an uppermost layer (for example, a layer of GaAs) disposed on the substrate. The uppermost layer may be disposed directly on the substrate. The uppermost layer may have a threading dislocation density ρ_{TD} at least 10^8 cm^{-2} and the device layer structure may have a threading dislocation density ρ_{TD} no more than 10^5 cm^{-2} .

Brief Description of the Drawings

Certain embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic view of a first heterostructure;

5 Figure 2 illustrates plots of calculated strain in the first heterostructure shown in Figure 1 before and after relaxation;

Figure 3 illustrates plots of calculated strain-thickness product in the first heterostructure shown in Figure 1 before and after relaxation;

Figure 4 is a schematic view of a second heterostructure;

10 Figure 5 illustrates plots of calculated strain in the second heterostructure shown in Figure 4 before and after relaxation;

Figure 6 illustrates plots of calculated strain-thickness product in the second heterostructure shown in Figure 4 before and after relaxation;

Figure 7 is a schematic view of a third heterostructure;

15 Figure 8 illustrates plots of calculated strain in the third heterostructure shown in Figure 7 before and after relaxation;

Figure 9 illustrates plots of calculated strain-thickness product in the third heterostructure shown in Figure 1 before and after relaxation;

Figure 10 is a schematic view of a modified third heterostructure;

20 Figure 11 illustrates plots of calculated strain in the modified third heterostructure shown in Figure 10 before and after relaxation;

Figure 12 illustrates plots of calculated strain-thickness product in the modified third heterostructure shown in Figure 10 before and after relaxation;

25 Figure 13 is a schematic view of part of heterostructure in which lateral propagation of a threading dislocation is obstructed by misfit dislocations;

Figure 14 is a schematic view of part of heterostructure in which lateral propagation of a threading dislocation is obstructed by fixed, embedded obstructive regions, such as quantum dots;

Figure 15 is a schematic view of a fourth heterostructure having dislocation filters;

30 Figure 16 is detailed schematic view of the fourth heterostructure shown in Figure 15;

Figure 17 is a plot of calculated threading dislocation density as a function of thickness in the absence of kinetic constraints;

Figure 18 illustrates calculated plots of strain-thickness product in the fourth heterostructure shown in Figure 16 before and after relaxation;

Figure 19 is a plot of calculated time used to attain strain-thickness product profile shown in Figure 18 with threading dislocation velocities of $1 \mu\text{m s}^{-1}$ and of $100 \mu\text{m s}^{-1}$; and

Figure 20 is a process flow diagram of process of growing fourth heterostructure shown in Figure 15.

Detailed Description of Certain Embodiments

Single epitaxial layer

Referring to Figure 1, a first heterostructure 1 is shown.

10

The heterostructure 1 comprises a base heterostructure 2 comprising a substrate 3, which comprises a first material, and an uppermost layer 4, which may be disposed directly on the substrate 3 and which comprises a second material. The uppermost layer 4 exhibits a high density ($>10^9 \text{ cm}^{-2}$) of threading dislocations (not shown). The heterostructure 1 comprises, on an upper surface 5 of the base heterostructure 2, a heteroepitaxial layer 6 comprising a third material which has the same crystal structure as the second material, but a different parameter. In this example, the first material is silicon (i.e. the substrate is a single-crystal silicon substrate), the second material is gallium arsenide (i.e. the layer may be a layer of gallium arsenide) and the third material may be indium gallium arsenide, for example, $\text{In}_{0.2}\text{Al}_{0.8}\text{As}$.

20

The heteroepitaxial layer 6 has an internal strain ε and a thickness h . If the product of strain and thickness (herein referred to as the “strain-thickness product”) εh lies below a critical value εh_c , then it is energetically favourable for the strain in the layer to be maintained, such that the layer crystal matches the substrate crystal. In that case, the internal strain ε of the layer 6 is equal to the misfit strain $\varepsilon_0 = (a_1 - a_s)/a_s$, where a_s and a_1 are lattice parameters for the substrate 2 and epitaxial layer 4 respectively. The lattice parameter at the surface 7 of the epitaxial layer 6 is the same as that of the uppermost layer 6, i.e. $a_{\text{surface}} = a_s$. However, once the strain-thickness product exceeds the critical strain-thickness product (often referred to as a “critical thickness” for a given strain), it becomes energetically favourable for the strain in the epitaxial layer 6 to fall. This reduction in strain is caused by misfit dislocations 8 which lie at the interface 9 between the base heterostructure 2 and heteroepitaxial layer 6 and which accommodate the difference in lattice spacing.

35

In semiconductor materials, where planar growth is maintained, misfit dislocations 8 are usually formed through the lateral movement of a dislocation that threads the layer from interface 9 to surface 7 known as a “threading dislocation” (not shown). Thus, in a situation where there is a sufficiently high density ρ of threading dislocations, the
 5 internal strain in the epitaxial layer 6 relaxes by an amount ε_r , as shown in Figure 2.

Figure 2 shows the strain ε_0 in the epitaxial layer 6 without any relaxation, i.e. misfit strain, and the strain ε after relaxation by misfit dislocations. In this example, the epitaxial layer 6 is formed of $\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$ and has a thickness of 34 nm.

10

Figure 3 shows a plot 10 of strain-thickness product in the epitaxial layer 6 without any relaxation and a plot 11 of strain-thickness product after relaxation by misfit dislocations at the epitaxial layer-substrate interface 9 (Figure 1). If there are sufficient misfit dislocations, the strain-thickness product is reduced to an equilibrium value (or
 15 “critical value”) εh_c . Figure 3 also shows the equilibrium strain-thickness product εh which is found experimentally to be about 0.2 nm in GaAs and similar materials, as described in D. J. Dunstan: “Strain and strain relaxation in semiconductors”, Journal of Materials Science: Materials in Electronics, volume 8, pages 337 to 375 (1997).

20 During the course of relaxation, the lattice parameter at the surface 7 (Figure 1) of the epitaxial layer 6 changes, becoming more similar to the unstrained lattice parameter of the layer material, i.e. $a_{\text{surface}} = (1 + \varepsilon_r) a_s$. Relaxation (as illustrated by the arrow ‘a’ in Figure 3) is kinetically limited. Thus, if there are too few threading dislocations to provide a sufficient density of misfit dislocations or if insufficient time is given for the
 25 threading dislocations to move, then equilibrium strain thickness product may not be reached. In such a case, if the strain-thickness product of the epitaxial layer 6 does not exceed a second critical strain-thickness product $(\varepsilon h)^*$ for dislocation multiplication (which is about four times the equilibrium value) during growth, then the epitaxial layer 6 is stable against further relaxation. If, however, the layer strain-thickness
 30 product exceeds the second critical strain-thickness product $(\varepsilon h)^*$ during growth, then dislocation multiplication can occur, with each multiplication event producing one new misfit and two new threading dislocations. Repeated operation of dislocation multiplication results in production of several dislocations, all on the same glide plane (not shown) having the same Burgers vector. This can lead to “pile-up”. Pile-ups are
 35 detrimental to the planar growth of epitaxial layers and should be avoided.

Movement of threading dislocations that are induced by relaxation ε_r lead to encounters between pairs of threading dislocations. In certain cases, these encounters lead to a reaction between the dislocations, resulting in zero, one or two threading dislocations (dependent upon the crystal system in question). These encounters, on average, provide some reduction in the number of threading dislocations and so a strained layer can be used as a misfit dislocation filter (herein also referred to as a “dislocation filter” or even just “filter”).

A single filter can be used to remove a large fraction (e.g. up to 90%) of threading dislocations by this process. However, this is insufficient for most applications, which require reduction in threading dislocation density by several orders of magnitude. For example, a reduction in threading dislocation density from 10^9 cm^{-2} to 10^5 cm^{-2} requires elimination of 99.99% of threading dislocations. The efficacy of a single strained layer (or any other, more complex structure in which the composition profile is varied, such as a graded composition) as a dislocation filter is limited by the second critical strain-thickness product $(\varepsilon h)^*$ because, above this value, dislocation multiplication will then take place and threading dislocation density will increase once more.

Thus, to provide an efficacious dislocation filter, the value of strain-thickness product in a heterostructure should not exceed the second critical strain-thickness product $(\varepsilon h)^*$, i.e. the critical thickness for multiplication, at any place in the heterostructure during or after growth.

Double epitaxial layers

Referring to Figure 4, a second heterostructure 21 is shown.

The heterostructure 21 comprises a base heterostructure 22 comprising a substrate 22 which comprises a first material, and an uppermost layer 24, which may be disposed directly on the substrate 22 and which comprises a second material. The uppermost layer 24 exhibits a high density ($>10^9 \text{ cm}^{-2}$) of threading dislocations (not shown). The heterostructure 21 comprises, on an upper surface 25 of the base heterostructure 22, a first heteroepitaxial layer 26 comprising a third material which has the same crystal structure as the second material, but a different parameter, and, on its upper surface 27, a second heteroepitaxial layer 28 comprising the second material. The first material may be silicon, the second material may be GaAs and the third material may be indium

gallium arsenide, for example $\text{In}_{0.2}\text{Al}_{0.8}\text{As}$. Similar to the first heterostructure, misfit dislocations 30 occur at the interface 31 between the uppermost layer 24 and first layer 26.

5 Figure 5 shows the strains in the first and second epitaxial layers 26, 28 before and after relaxation. Figure 6 shows plots of strain-thickness product.

Referring to Figures 4 and 6, the first epitaxial layer 26 is grown until it reaches its nominal strain-thickness product for multiplication $(\epsilon_0 h)^*$. In this case (for $\epsilon_0 h_c$ of 0.2
10 nm), this occurs when the thickness of the first heteroepitaxial layer 26 is about 44 nm.

Growth, however, can be stopped earlier, leading to a thinner epitaxial layer, in which case relaxation $\epsilon_r(a)$ and threading dislocation reduction would be smaller. Conversely, growth can continue for longer so as to form a thicker layer (in which case $\epsilon_r(a)$ and
15 threading dislocation reduction would be larger) as long as the strain-thickness product does not exceed the critical thickness for multiplication $(\epsilon h)^*$ during growth. As explained earlier, relaxation (as illustrated by the arrow 'a' in Figure 6) allows growth without exceeding exceed the critical thickness for multiplication $(\epsilon h)^*$, but is contingent on the availability of sufficient mobile threading dislocations during growth.
20 Pausing during growth or annealing may be used to allow sufficient relaxation to take place and to ensure that strain-thickness product does not exceed the critical thickness for multiplication $(\epsilon h)^*$ during growth.

Due to decaying strain fields of threading and misfit dislocations, relaxation does not
25 take place homogeneously on a microscopic scale and there may be regions in an epitaxial layer that will have higher or lower strain than the average value. Therefore, during growth, care should be taken not to exceed the critical thickness for multiplication $(\epsilon h)^*$ in any region of the layer.

30 Referring also to Figure 5, relaxation $\epsilon_r(a)$ changes the lattice parameter of the surface 24 of the first epitaxial layer 26. Therefore, when the second epitaxial layer 28 is grown, it experiences a strain that is equal and opposite to $\epsilon_r(a)$. As shown in Figure 5, the plot of strain is shifted by $-\epsilon_r(a)$. As shown in Figure 6, as growth of the second epitaxial layer 16 continues, a negative strain-thickness product accumulates.

At a point during growth of the second epitaxial layer 28, the strain-thickness product exceeds the equilibrium strain thickness product ϵh_c and, subject to the availability of sufficient mobile threading dislocations, the second epitaxial layer 28 relaxes towards its natural lattice parameter (as illustrated by the arrow 'b' in Figure 6 and by $\epsilon_r(b)$ in Figure 5). This relaxation is produced by a second array of misfit dislocations 32 lying at the interface 33 between the first and second epitaxial layers 26, 28.

Multiple epitaxial layers can be grown such that, during formation of the heterostructure, the value of strain-thickness product in a heterostructure does not exceed the critical strain-thickness product $(\epsilon h)^*$ during growth.

Multiple epitaxial layers

Referring to Figure 7, a third heterostructure 41 is shown.

The third heterostructure 41 comprises a base heterostructure 42 comprising a substrate 44, which comprises a first material, and an uppermost layer 44, which may be disposed directly on the substrate 43 and which comprises a second material. The uppermost layer 44 exhibits a high density ($>10^9 \text{ cm}^{-2}$) of threading dislocations (not shown). The heterostructure 41 comprises, on an upper surface 45 of the base heterostructure 42, a first heteroepitaxial layer 46 comprising a third material which has the same crystal structure as the second material, but a different parameter, and, on its upper surface 47, a second heteroepitaxial layer 48 comprising the second material having an upper surface 49. The third heterostructure 41 also comprises a stack of n double layers 50, each double layer 50 comprising a first layer 51_i comprising the first material and a second layer 52_i comprising the second material, where $1 \leq i \leq n$. In this case, $n = 4$ and so there are five (i.e. $1 + 4$) double-layer dislocation units. The first material may be silicon and the second material may be GaAs. Misfit dislocations 53_j, 54_j occur at opposite layer interfaces 55_j, 56_j where $0 \leq j \leq n$.

If each double-layer dislocation unit removes 90% of existing threading dislocations, the seven units shown in Figure 7 should remove $(1-0.1^7) = 99.9999\%$ dislocations. Thus, the desired reduction in threading dislocations can be easily achieved. This reduction, however, may not be attainable in practice since relaxation relies on the existence of sufficient numbers of mobile threading dislocations, which are eliminated from the structure by the dislocation filters.

Thus, after a certain point, relaxation in epitaxial layer may not occur. Consequently, there may be little, if any, misfit dislocations at the interfaces between layers and so there might be no barrier to the movement of threading dislocations crossing several layers.

5

Referring to Figure 10, a modified third heterostructure 41' is shown. The modified third heterostructure 41' is the same as the third heterostructure 41 (Figure 7) but has a low density of threading dislocations after four double-layer dislocation units.

10 Figure 11 shows strains in the heterostructure before and after relaxation. As can be seen in Figure 11, no relaxation takes place in the fourth (and subsequent) pairs of layers 51₄, 52₄.

Referring to Figure 12, in the modified third heterostructure 41', the strain-thickness
15 product increases across the layers in the upper part of the structure: there is insufficient relaxation to maintain the strain-thickness product below the critical thickness for multiplication $(\epsilon h)^*$. As a result, dislocation multiplication takes place in the upper part of the structure and no further reduction in threading dislocation takes place.

20

This effect can also take place if the upper part of the structure comprises device layers, even if they have no nominal strain with respect to the substrate, because the surface lattice parameter upon which they are deposited is not necessarily equal to that of the substrate.

25

Therefore, not only should the value of strain-thickness product in a heterostructure not exceed the critical thickness for multiplication $(\epsilon h)^*$ for layers in the dislocation filter structure, but also for any layers, e.g. other types of buffer layer or device layer(s), grown on the dislocation filter structure.

30

One or more arrangements or structures can be used to avoid the drawbacks of the third heterostructure 41 and the modified third heterostructure 41' and, thus, help to reduce threading dislocations throughout a heterostructure.

35 First, a combination of materials may be used having positive and negative strains with respect to the substrate. In this case, by maintaining each layer (or set of layers) below

the critical thickness for multiplication (ϵh)* and maintaining a structure having zero net strain with respect to the substrate (herein referred to as a “strain-balanced” structure), dislocation filter efficacy may be maintained without dislocation multiplication taking place. As well as maintaining net strain below the critical
5 thickness for dislocation multiplication, individual layers have strain-thickness products larger than the equilibrium critical thickness in the present case, rather than below this limit.

Secondly, a structure may be employed which restricts lateral (i.e. perpendicular to the
10 axis of growth) propagation of a threading dislocation. Such a structure is preferably included at each interface 55, 56.

Referring to Figure 13, a part of heterostructure 61 is shown which illustrates how the heterostructure can be engineered to effectively decouple relaxation in adjacent layers
15 61, 62.

The heterostructure part 61 comprises first and second layers 62, 63 comprising first and second different materials (e.g. $\text{In}_x\text{Ga}_{1-x}\text{As}$ and GaAs) having the same crystal structure and having an interface 64. Misfit dislocations 65 exhibit a variety of strain
20 fields that result in attractive and repulsive forces exerted on a threading dislocation 66. These forces can be extremely strong at short distances and are large in comparison with the internal strain in the layers.

These structures appear as a natural consequence of movement of threading
25 dislocations in the lower part of the epitaxial structures 41 (Figure 7), 41' (Figure 10). The absence of misfit dislocations from interfaces in upper parts of the structures 41 (Figure 7), 41' (Figure 10), however, is responsible for loss of efficacy of threading dislocation filtering. However, other structures for preventing propagation of dislocations can be used.

30 Referring to Figure 14, a part of heterostructure 61' is shown which effectively decouples relaxation in adjacent layers.

The heterostructure part 61' comprises first and second layers 62, 63 comprising first
35 and second different materials having the same crystal structure and having an interface 64. Spaced, fixed, embedded obstructive regions 67 are disposed at the

interface 64. The obstructive regions 67 can take the form of quantum dots, precipitates, partial layers of oxides or nitrides, doping (either epitaxially grown or implanted), dislocation loops, vacancy clusters or the like.

- 5 Through the use of such structures, the condition that no part of the epitaxial structure (including layers that comprise a device structure) exceeds the critical thickness for dislocation multiplication (eh)* limit may be maintained.

Heterostructure including a dislocation filter layer structure

- 10 Referring to Figure 15, a fourth heterostructure 101 is shown.

The fourth heterostructure 101 comprises a base structure 102 comprising a substrate 103, which comprises a first material, and an optional uppermost layer 104, which may be disposed directly on the substrate 104 and which comprises a second material.

- 15 Thus, the base structure 102 may itself be a heterostructure with the uppermost layer being a heteroepitaxial layer and, optionally, the heterostructure may include one or more graded layers. Alternatively, the base structure 102 may comprise solely the substrate 102 or be a homostructure comprising a homoepitaxial layer disposed on a substrate 102. The uppermost layer 104 in a heterostructure 102 exhibits a high density
20 ($>10^9 \text{ cm}^{-2}$) of threading dislocations (not shown).

The heterostructure 101 comprises, on an upper surface 105 of the base structure 102, an epitaxial multilayer structure 106 comprising a dislocation filter layer structure 107 and a device layer structure 108.

- 25 The dislocation filter layer structure 107 is disposed on the upper surface 105 of the base structure 102 and comprises a stack of dislocation filter layers 109, 110 comprising materials having the same crystal structure and one or more thin layers 111 interposed between dislocation filter layers 109, 110 for inhibiting movement of threading
30 dislocations. The dislocation movement-inhibiting layers 111 (herein also referred to as “de-coupling layers”, “blocking layers” or “insertions”) comprise spaced-apart, fixed, embedded obstructive regions 112, for example in the form of quantum dots, at the interface 113 between adjacent layers 109, 110.

- 35 The dislocation filter layer structure 107 may comprise two types of dislocation filter layers, for example GaAs and $\text{In}_x\text{Ga}_{1-x}\text{As}$, or more than two types of layers, for example

GaAs, $\text{In}_x\text{Ga}_{1-x}\text{As}$ and InP. At least two of the materials used in the dislocation filter layer structure 107 have different lattice parameters, such as GaAs and $\text{In}_x\text{Ga}_{1-x}\text{As}$. However, the dislocation filter layer structure 107 may include layers (which may be adjacent) which have the same lattice parameter, such as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and InP. The type (i.e. composition) and thickness of the layers can change through the dislocation filter layer structure 107.

Referring also to Figure 16, the fourth heterostructure 101 is shown in more detail.

The base structure 102 takes the form of a heterostructure 104 comprising a silicon substrate and a layer 104 of (001) GaAs. The density of threading dislocations ρ_{TD} is 10^9 cm^{-2} .

Referring also to Figure 17, the dislocation filter layer structure 107 can be used to reduce the threading dislocation density ρ_{TD} by four orders of magnitude, i.e. to below 10^5 cm^{-2} . The dislocation filter layer structure 107 comprises ten layers $109_1, 110_1, \dots, 109_5, 110_5$, namely five layers $109_1, \dots, 109_5$ of $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ and five layers $110_1, \dots, 110_5$ of GaAs.

A first $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layer 109_1 has a thickness of 56 nm.

Referring also to Figure 18, the first $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layer 109_1 has a strain-thickness product of 0.8nm.

The first $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layer 109_1 is followed by a first GaAs 110_1 having a thickness of 72 nm.

Figures 19 and 20 show time needed to attain strain-thickness product profile with a threading dislocation velocity of $1 \mu\text{ms}^{-1}$ and $100 \mu\text{ms}^{-1}$ respectively.

Referring to Figure 19, if a growth temperature is chosen that gives a mobile threading dislocation velocity of about $1 \mu\text{ms}^{-1}$, then the required threading dislocation density reduction is only achieved after about 15 minutes.

Referring to Figure 20, if dislocation velocities are increased to $100 \mu\text{ms}^{-1}$, by increasing growth temperature, or annealing at high temperature during a growth pause, this relaxation can be attained quickly.

5 A second $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layer 109₂ having a thickness of 68 nm is followed by a second GaAs layer 110₂ having a thickness of 69 nm. This pair of layer is repeated another two times, except with $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ has a thickness of 69 nm. As shown in Figure 17, the threading dislocation density ρ_{TD} can be expected to approach 10^6 cm^{-2} after the second GaAs layer 110₂.

10

From this point onwards, relaxation may become limited by finite dislocation velocities and strategies to increase their velocity, such as rapid high temperature annealing is employed after growth of subsequent layers, and/or allowing relaxation to take place, for example, by using extended anneals at high temperature for 20 minutes after

15 growing the third GaAs layer 110₃ and the fourth $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layer 109₄.

In order to ensure that adjacent layers are isolated, dislocation movement-inhibiting layers 111₁,...,111₇ comprising quantum dots (e.g. InAs quantum dots) or highly-doped layers (e.g. a thin layer of silicon delta-doping) are deposited, after annealing, at the
20 interface between the second GaAs layer 110₂ and the third $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layer 109₃ and each subsequent interface. These structures are indicated by arrows in Figures 16, 17 and 18.

The dislocation filter structure 107 including the decoupling layers 111₁,...,111₇ and the
25 use of annealing can be used to reduce the threading dislocation density ρ_{TD} to below 10^5 cm^{-2} with production times of a few hours. Lower threading dislocation densities ρ_{TD} , below 10^4 cm^{-2} , can be achieved by annealing the layers for a day-and-a-half. Although such long production times may be uneconomical for many purposes, it may be practical in cases where such low threading dislocation densities ρ_{TD} are
30 unattainable by other means.

The dislocation filter structure 107 is terminated by a final decoupling layer (not shown). This allows the subsequent deposition of a device heterostructure 108 that does not exceed the critical thickness for dislocation multiplication (ϵh)*.

35

As shown in Figure 18, a device heterostructure 108 which is lattice matched may be deposited provided it does not exceed 300 nm. In this case, the device heterostructure 108 may be InGaAs quantum well laser comprising layers 114, 115 of InGaAs and GaAs and having graded buffer layers 116.

5

Generally, the thickness of the device heterostructure 108 should be less than or equal to four times this thickness of the last layer in the dislocation filter structure 107.

Growing heterostructures having dislocation filters

10 Referring to Figures 15 and 21, a method of growing a heterostructure 101 will now be described.

A base structure 102 is loaded into a reactor chamber (not shown) (step S1).

15 Optionally, one or more buffer layers (not shown) can be grown (step S2). For example, the one or more buffer layers may include a homoepitaxial layer, i.e. a layer comprising the same material as the substrate 102. The one or more buffer layers may include a compositionally-graded layer.

20 A dislocation filter layer structure 103 is then grown comprising a series of dislocation filter layers 113, 114 comprising first and second layers 109, 110 comprising different materials (steps S3 to S6).

25 First layers 109 need not all comprise the same material and the layers 109 can have different thicknesses. Likewise, second layers 110 need not all comprise the same material and the layers 110 can have different thicknesses. However, during growth of each layer 109, 110, the strain-thickness product is kept below the critical thickness for dislocation multiplication $(\epsilon h)^*$.

30 Growth pauses, annealing or other methods may be employed to ensure that this condition is maintained at all times (step S4).

As explained earlier, the dislocation filter layer structure 107 may include a strain-balanced structure and/or one or more thin layers 111 which introduce structures 112
35 for preventing propagation of dislocations (step S5).

The dislocation filter layer structure 107 preferably includes at least three pairs of first and second layers 109, 110.

Optionally, a capping first layer 133 may be grown.

5

Optionally, one or more buffer layers (not shown) can be grown. The one or more buffer layers may include a compositionally-graded layer. During growth of the one or more buffer layers, the strain-thickness product is kept below the critical thickness for dislocation multiplication (ϵh)*.

10

Finally, a device layer structure 108 is grown (step S7). The device layer structure 108 may comprise a single layer, for example, a layer used to form a transistor. However, the device layer structure 108 may comprise multiple layers and may itself comprise a heterostructure, such as a quantum well laser structure. Regardless of layer structure, during growth of the layer or layers forming the device layer structure 108, the strain-thickness product is kept below the critical thickness for dislocation multiplication (ϵh)*.

15

Materials

A substrate 103 may comprise silicon (e.g. (001) silicon), gallium arsenide (GaAs), indium phosphide (InP), gallium nitride (GaN), strontium titanate (SrTiO₃) or sapphire (Al₂O₃). Heteroepitaxial layers may comprise silicon, germanium, silicon carbide, III-V material, such as GaAs and In_xGa_{1-x}As, gallium nitride (GaN) and/or Pb(Zr_xTi_{1-x})O₃.

Examples of heterostructures include In_xGa_{1-x}As and GaAs formed on GaAs/Si base structure, In_xGa_{1-x}P and In_xGa_{1-x}As formed on InP formed on GaAs/Si base and GeSiSn on Si.

25

It will be appreciated that many modifications may be made to the embodiments hereinbefore described.

30

A layer need not be homogeneous, that is, have a constant stoichiometry or composition throughout the thickness of a layer. For example, a layer may have graded or changing compositions. The composition may vary continuously or in steps. Thus, for example, an alloy (which may be binary, tertiary or greater) may comprise a first components A and B in a ratio x and 1-x and x may vary: x may vary monotonically in

35

the layer, for example, starting with a first value of x and ending with a second, different value of x , or vary non-monotonically.

Claims

1. A method of growing a heterostructure, the method comprising:
growing an epitaxial multilayer structure (106) on a base structure (102), the
5 multilayer structure comprising:
a dislocation filter layer structure (107) comprising a stack of at least two
dislocation filter layers (109, 110),
wherein the method comprises:
providing at least one layer (111) in the dislocation filter layer structure for
10 inhibiting movement of threading dislocations, wherein the threading dislocation
movement inhibiting layer is interposed between two dislocation filter layers;
relaxing each layer in the dislocation filter layer structure before growing a
subsequent layer such that, for each layer in the dislocation filter layer structure:
misfit strain-thickness product $\varepsilon_o h$ is equal to or greater than the equilibrium
15 strain-thickness product εh_c when the underlying layer is relaxed; and
strain-thickness product εh is equal to or less than the critical strain-thickness
product $(\varepsilon h)^*$ for dislocation multiplication during growth.
2. A method according to claim 1, wherein, the multilayer structure further
20 comprises:
a device layer structure (108) disposed on the dislocation filter structure
comprising at least one layer
wherein the method comprises:
relaxing each layer in the device layer structure before growing a subsequent layer
25 such that, for each layer in the device layer structure:
misfit strain-thickness product $\varepsilon_o h$ is equal to or greater than the equilibrium
strain-thickness product εh_c when the underlying layer is relaxed; and
strain-thickness product εh is equal to or less than the critical strain-thickness
product $(\varepsilon h)^*$ for dislocation multiplication during growth.
- 30 3. A method of growing a heterostructure, the method comprising:
growing a device layer structure (108) comprising at least one layer on a
dislocation filter layer structure (107) comprising a stack of at least two dislocation
filter layers (109, 110) and at least one layer (111) for inhibiting movement of threading
35 dislocations, wherein the threading dislocation movement inhibiting layer is interposed
between two dislocation filter layers;

wherein the method comprises:

relaxing each layer in the device layer structure before growing a subsequent layer such that, for each layer in the device layer structure:

- 5 misfit strain-thickness product $\varepsilon_o h$ is equal to or greater than the equilibrium strain-thickness product εh_c when the underlying layer is relaxed; and
strain-thickness product εh is equal to or less than the critical strain-thickness product $(\varepsilon h)^*$ for dislocation multiplication during growth.

- 10 4. A method according to any preceding claim, wherein relaxing a layer comprises:
growing a layer sufficiently slowly that relaxation takes place *in-situ*.
- 15 5. A method according to any preceding claim, wherein relaxing a layer comprises:
pausing growth of the layer, waiting for a given time and resuming growth of the layer.
6. A method according to any preceding claim, wherein relaxing a layer comprises:
growing the layer, then waiting for a given time until the layer has relaxed.
- 20 7. A method according to claim 5 or 6, wherein the given time exceeds a threshold time which is dependent on dislocation velocity.
8. A method according to any preceding claim, wherein relaxing a layer comprises:
annealing the layer.
- 25 9. A method according to any preceding claim, wherein providing the threading dislocation movement inhibiting layer comprises:
growing a layer of quantum dots.
- 30 10. A method according to any preceding claim, wherein providing the threading dislocation movement inhibiting layer comprises:
introducing dopants.
- 35 11. A method according to any preceding claim, wherein providing the threading dislocation movement inhibiting layer comprises:
implanting ions.

12. A method according to any preceding claim, wherein providing the threading dislocation movement inhibiting layer comprises:
depositing a non-continuous layer of material.
- 5 13. A method according to any preceding claim, wherein providing the threading dislocation movement inhibiting layer comprises:
forming the threading dislocation movement inhibiting layer after growing a dislocation filter layer and before growing a subsequent dislocation filter layer.
- 10 14. A method according to claim 13, wherein providing the threading dislocation movement inhibiting layer comprises:
forming the threading dislocation movement inhibiting layer after annealing the dislocation filter layer.
- 15 15. A method according to any preceding claim, wherein the base structure comprises a heterostructure comprising a substrate (103) and an uppermost layer (104).
16. A method according to claim 15, wherein the uppermost layer (104) has a threading dislocation density ρ_{TD} at least 10^8 cm^{-2} and the device layer structure (108)
20 has a threading dislocation density ρ_{TD} no more than 10^5 cm^{-2} .
17. A heterostructure (101) comprising:
a base structure (102); and
an epitaxial multilayer structure (106) disposed directly on base structure, the
25 multilayer structure comprising:
a dislocation filter layer structure (107) comprising a stack of at least two layers (109, 110) comprising first and second different materials respectively,
wherein:
misfit strain-thickness product $\varepsilon_o h$ for each layer in the epitaxial multilayer
30 structure is equal to or exceeds the equilibrium strain-thickness product εh for the respective layer when the underlying layer is relaxed; and
strain-thickness product εh for each layer in the epitaxial multilayer structure does not exceed the critical strain-thickness product $(\varepsilon h)^*$ for dislocation multiplication.

18. A heterostructure according to claim 17, wherein the multilayer structure further comprises:

a device layer structure (108) disposed on the dislocation filter structure comprising at least one layer.

5

19. A heterostructure (101) comprising:

a base structure (102);

an epitaxial multilayer structure (106) disposed on a base structure (102), the multilayer structure comprising:

10 a dislocation filter layer structure (107) comprising a stack of at least two dislocation filter layers (109, 110); and

a device layer structure (108) disposed on the dislocation filter structure comprising at least one layer,

the heterostructure further comprising:

15 at least one layer in the dislocation filter layer structure for inhibiting movement of threading dislocations, wherein the threading dislocation movement inhibiting layer is interposed between two dislocation filter layers;

wherein for each layer in the epitaxial multilayer structure:

misfit strain-thickness product $\varepsilon_o h$ is equal to or greater than the equilibrium strain-thickness product εh_c when the underlying layer is relaxed; and

20 strain-thickness product εh is equal to or less than the critical strain-thickness product $(\varepsilon h)^*$ for dislocation multiplication.

20. A heterostructure according to claim 19, wherein the base structure (102) is a heterostructure comprising:

25 a substrate (103); and

an uppermost layer (104) disposed on the substrate (103).

21. A heterostructure according to claim 20, wherein the uppermost layer (104) has a threading dislocation density ρ_{TD} at least 10^8 cm^{-2} and the device layer structure (108) has a threading dislocation density ρ_{TD} no more than 10^5 cm^{-2}

30

1/13

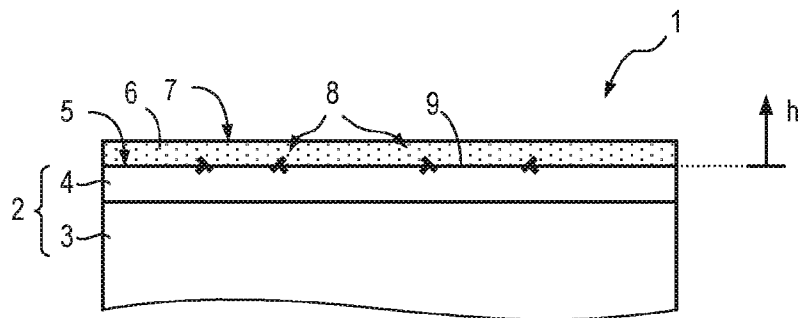


Fig. 1

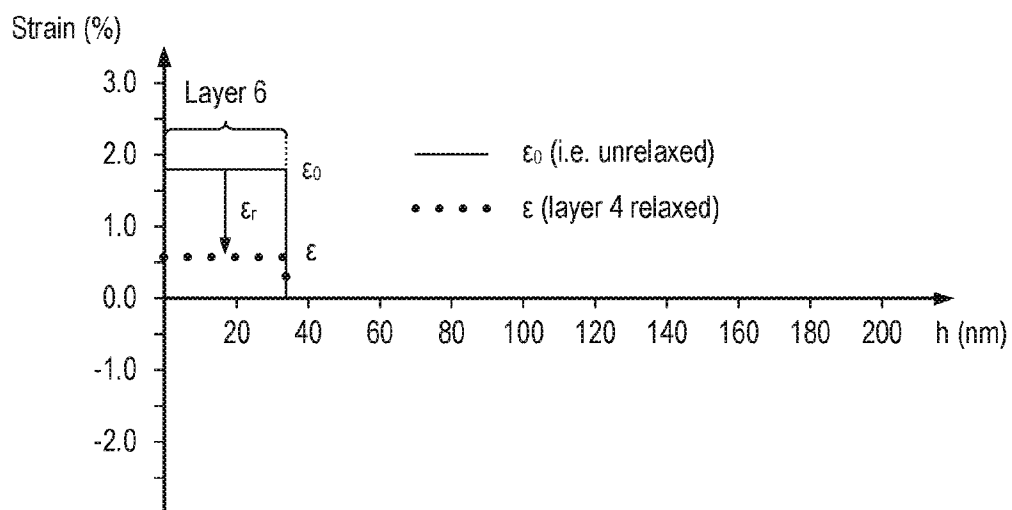


Fig. 2

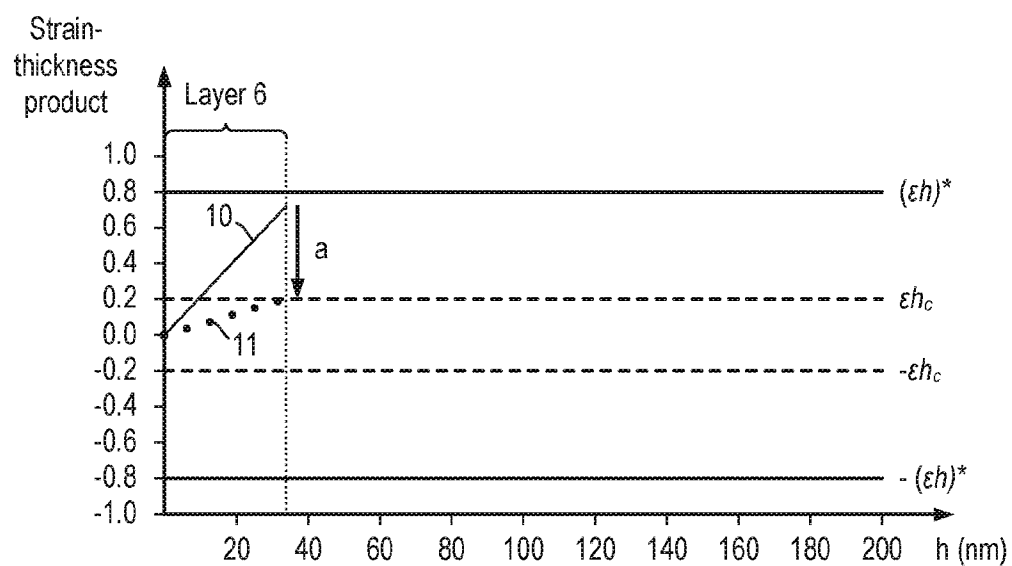


Fig. 3

2/13

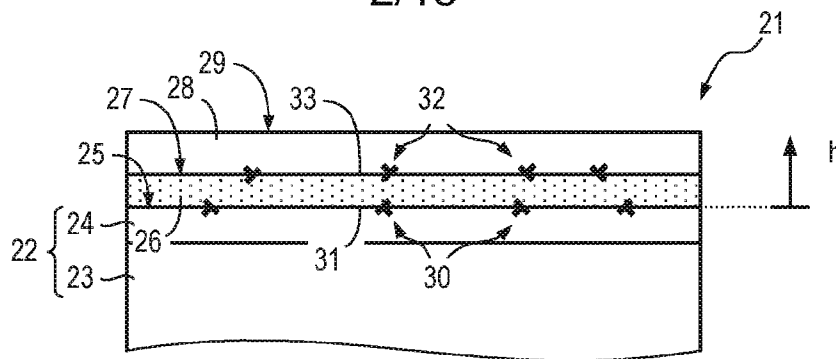


Fig. 4

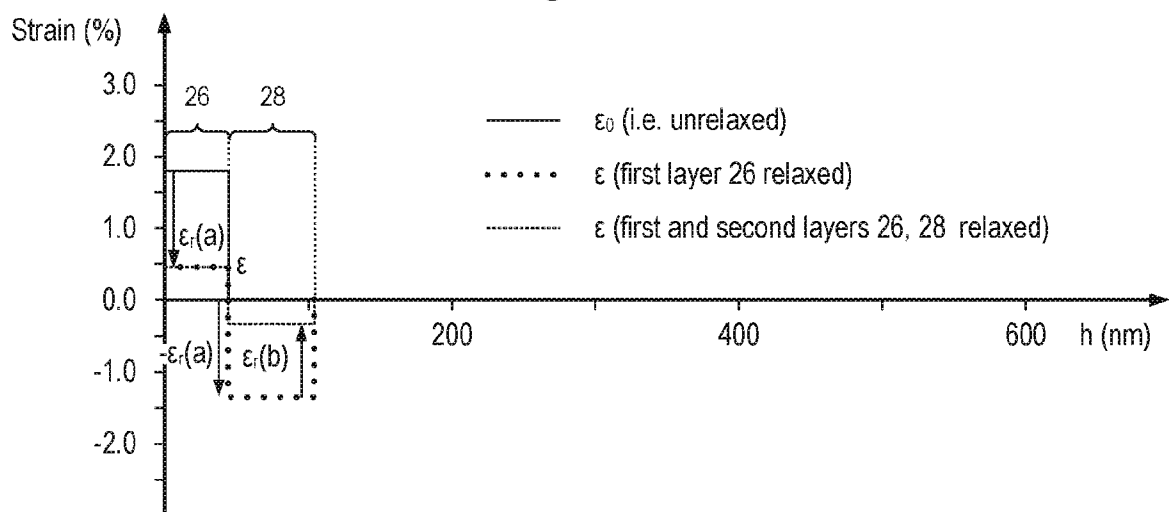


Fig. 5

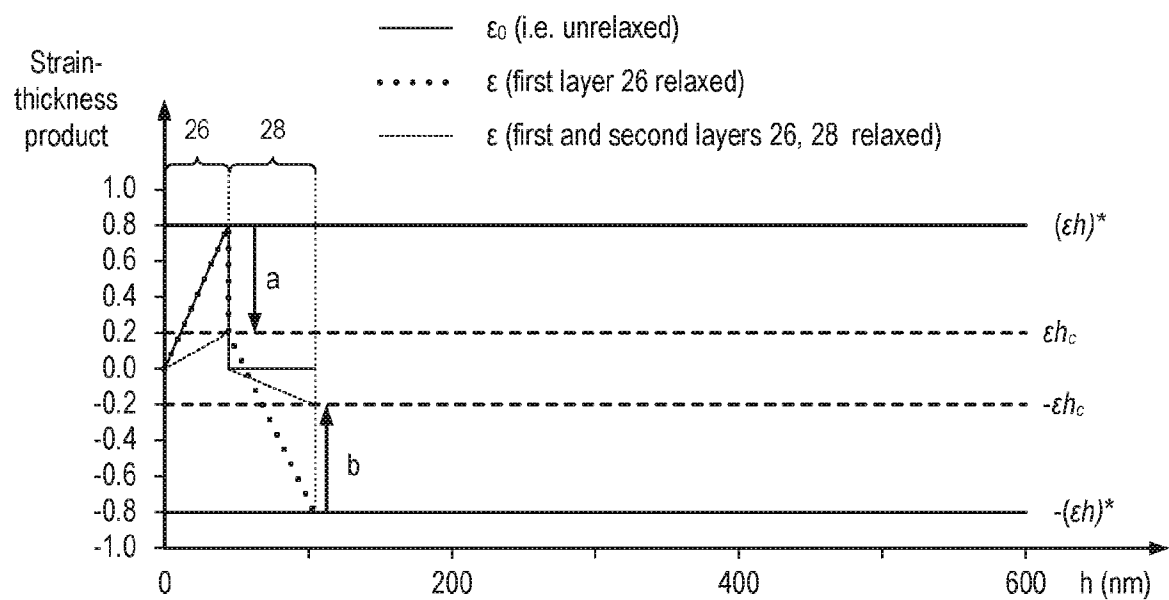


Fig. 6

3/13

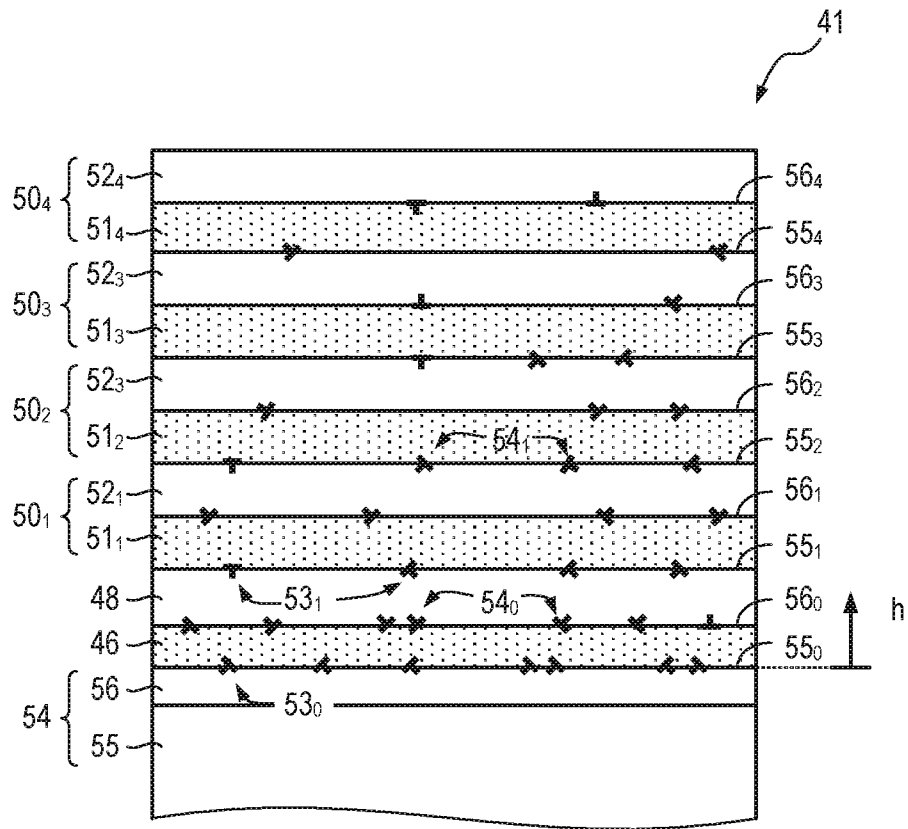


Fig. 7

4/13

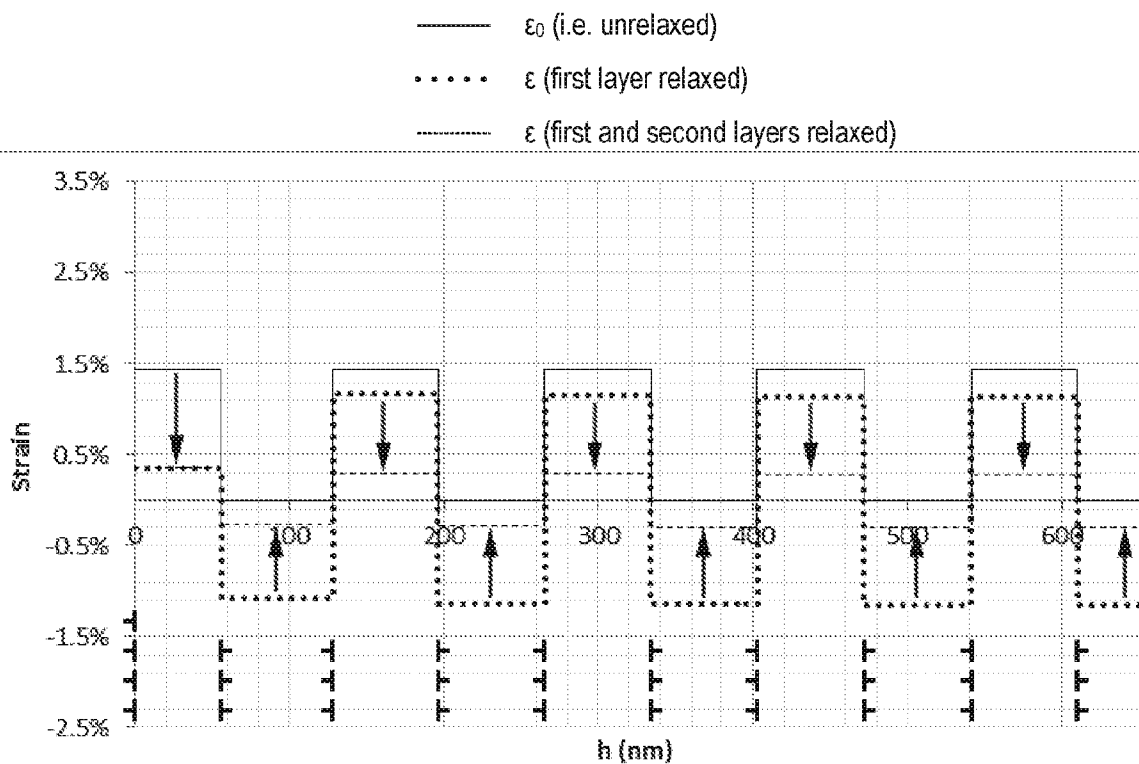


Fig. 8

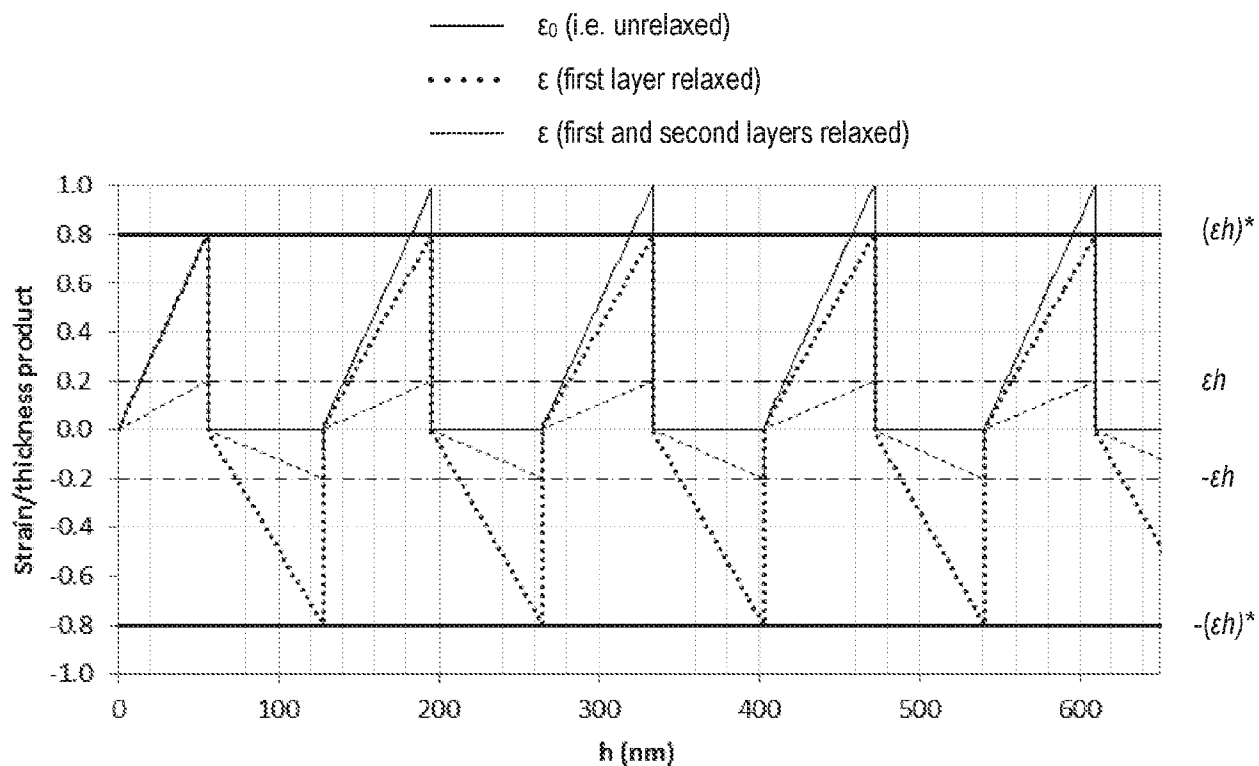


Fig. 9

5/13

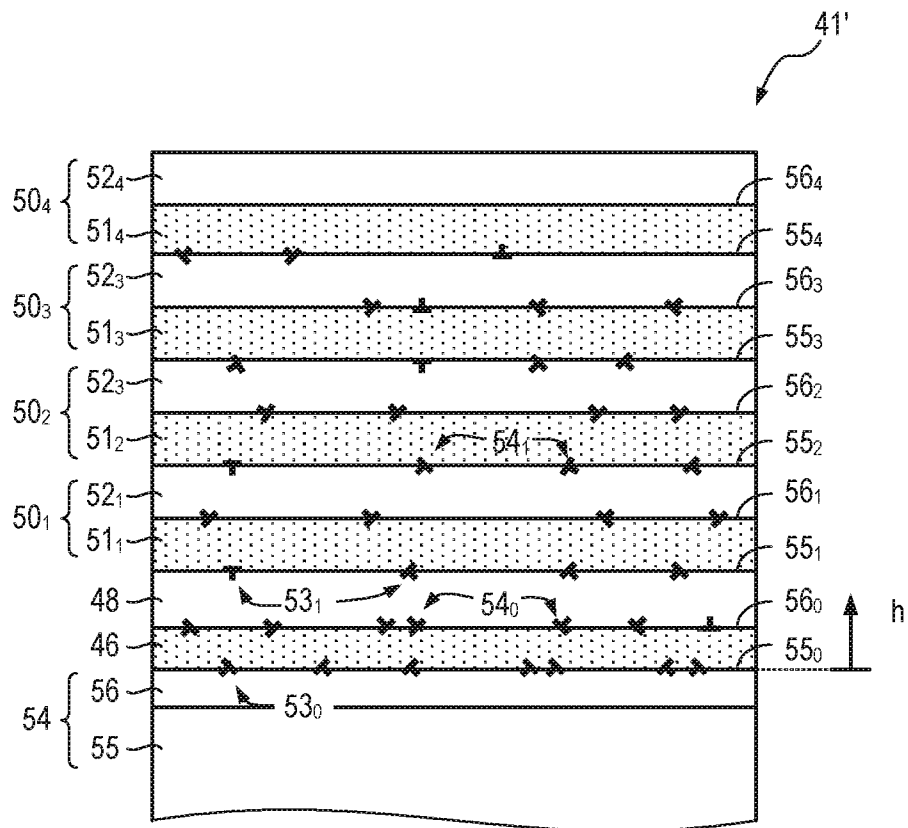


Fig. 10

6/13

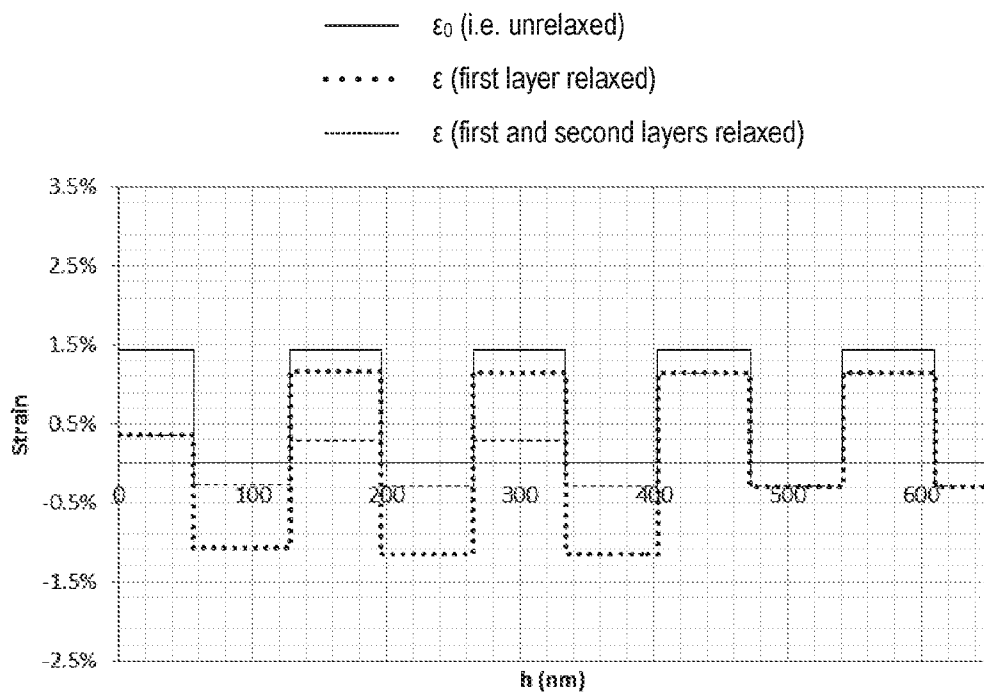


Fig. 11

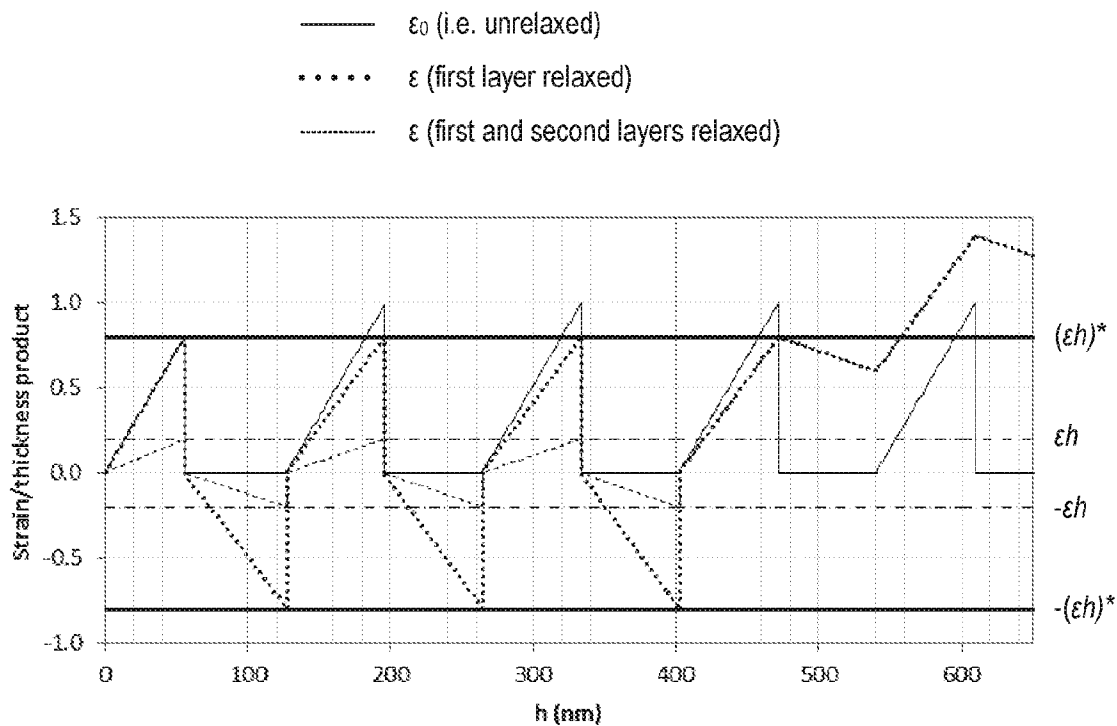


Fig. 12

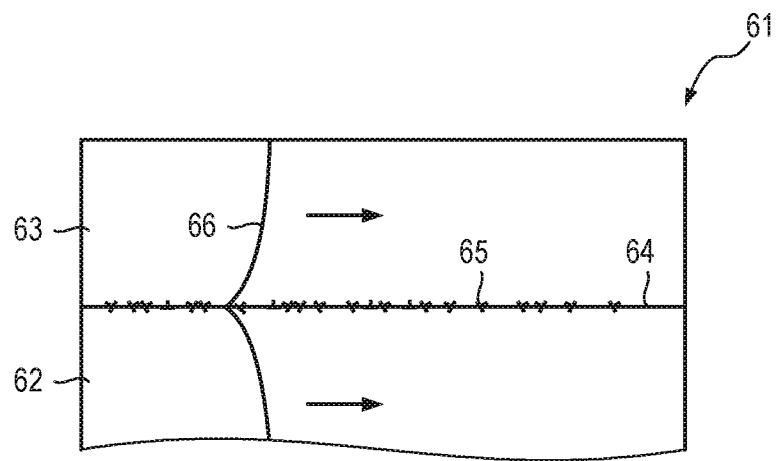


Fig. 13

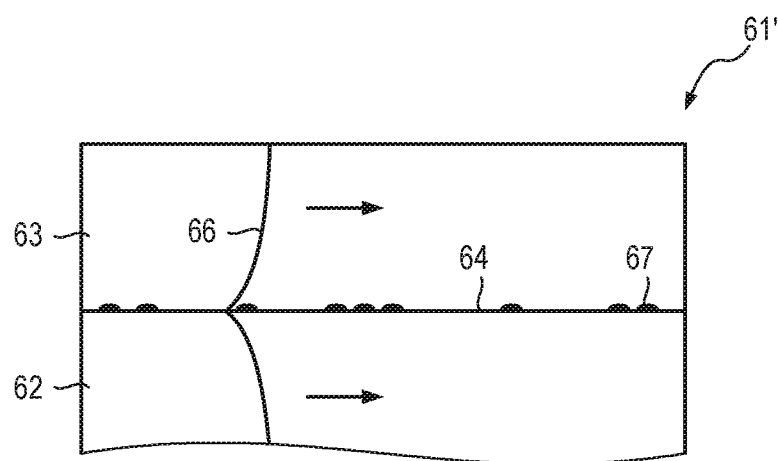


Fig. 14

8/13

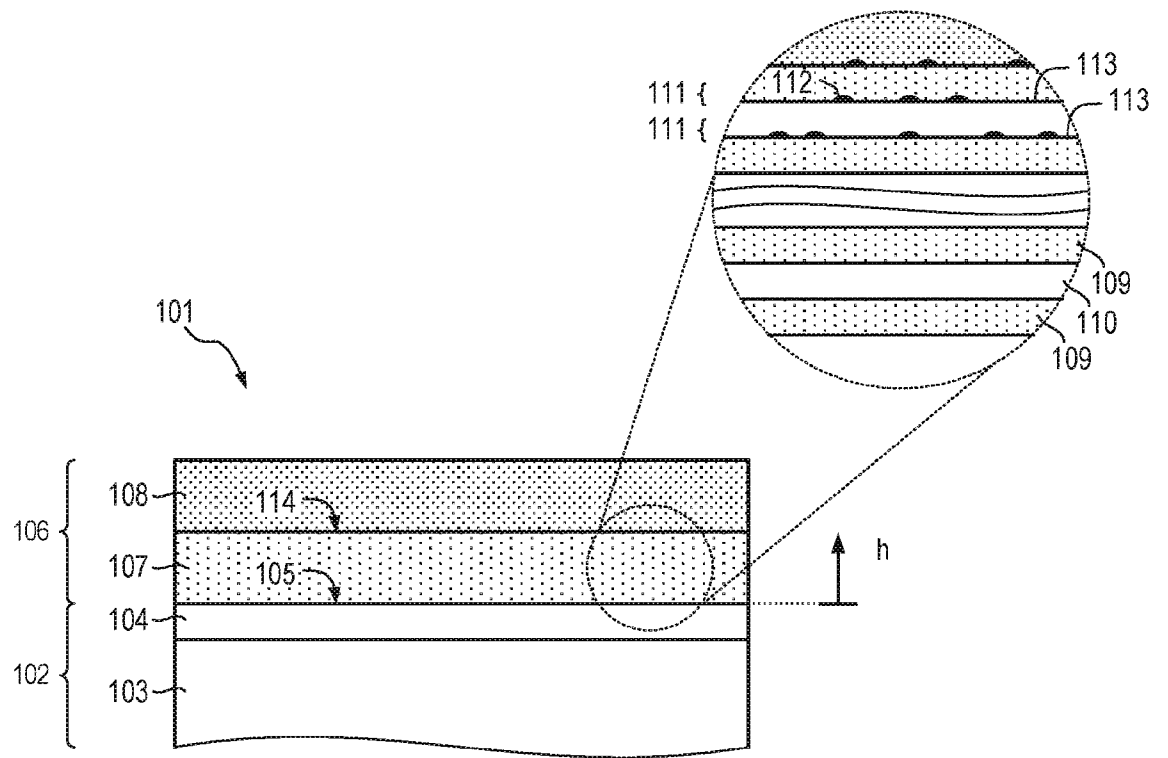


Fig. 15

9/13

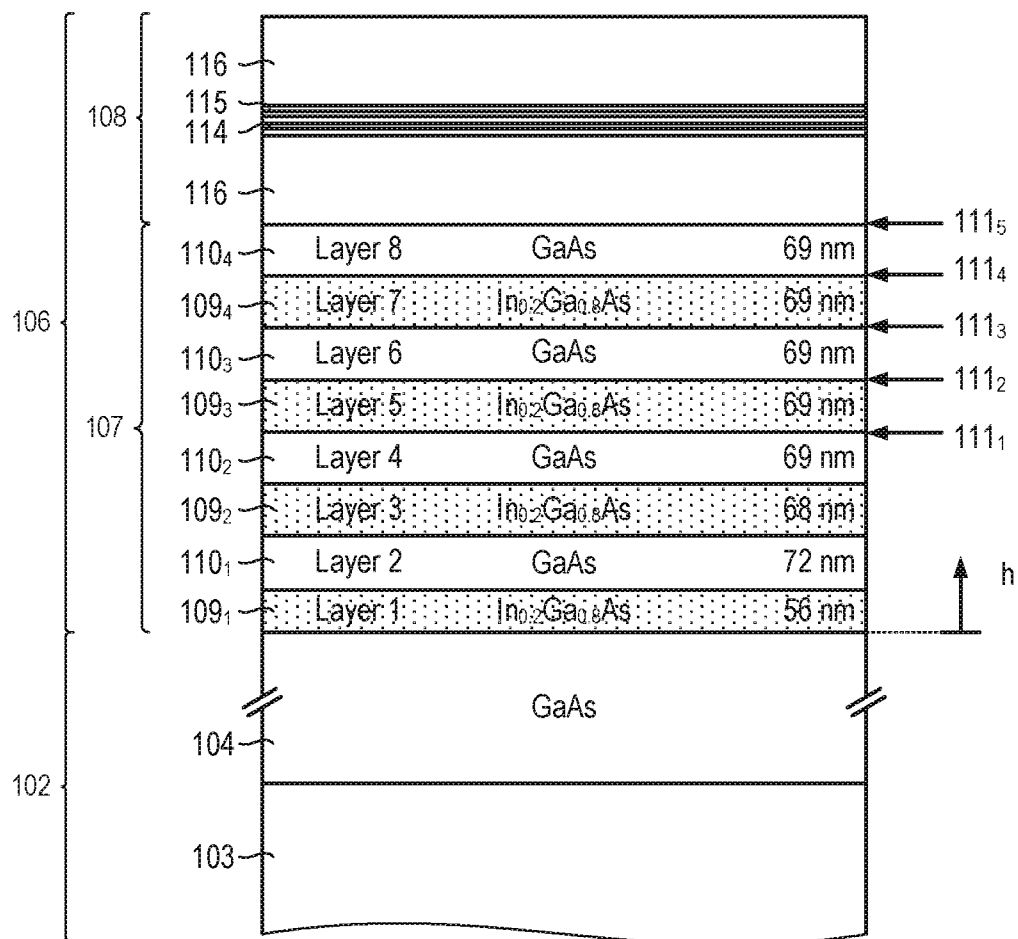


Fig. 16

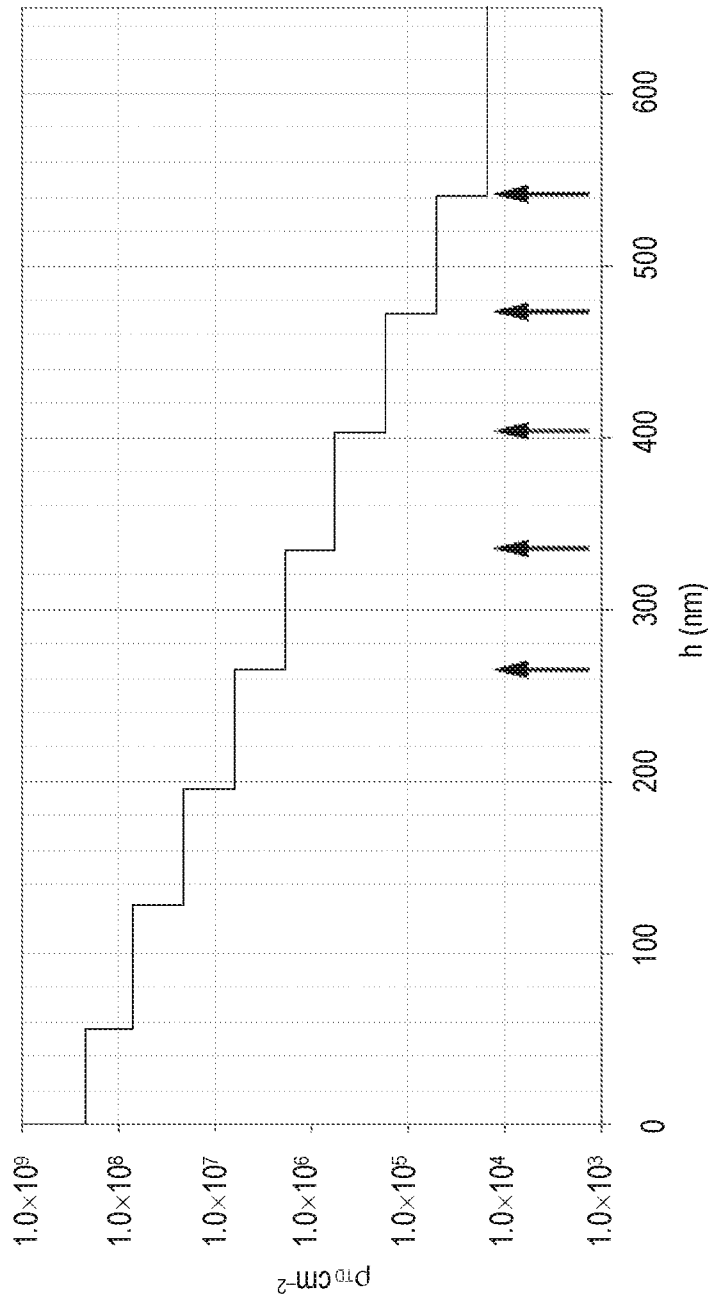


Fig. 17

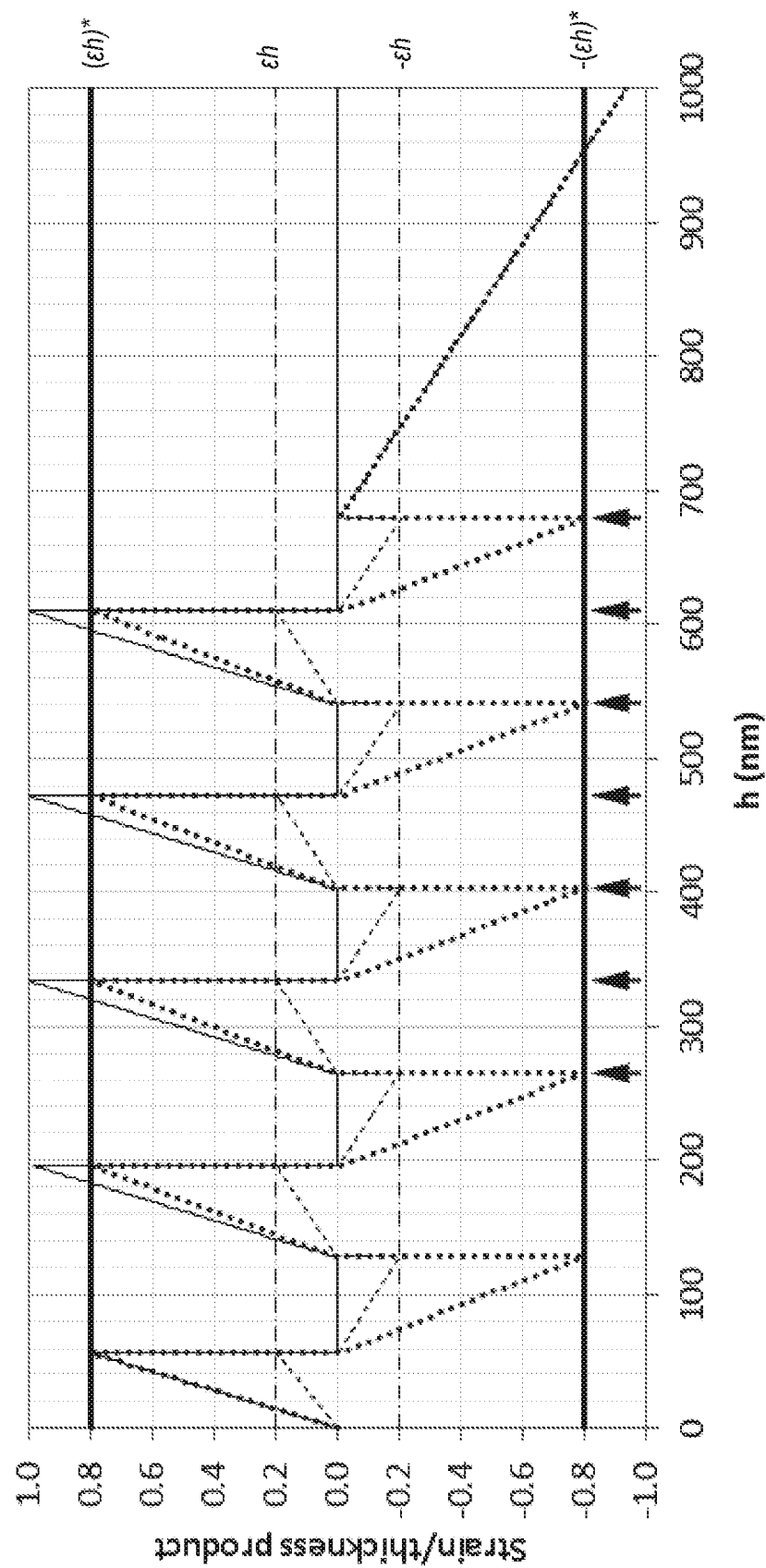


Fig. 18

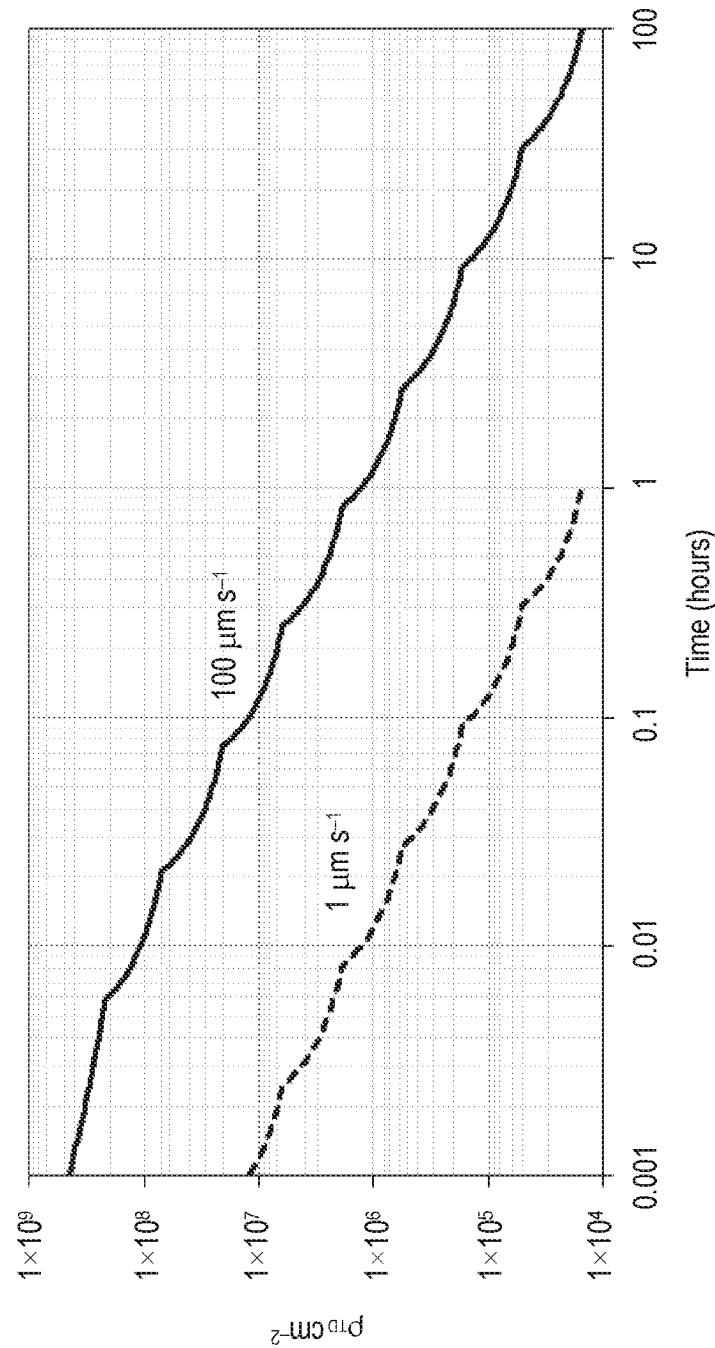


Fig. 19

13/13

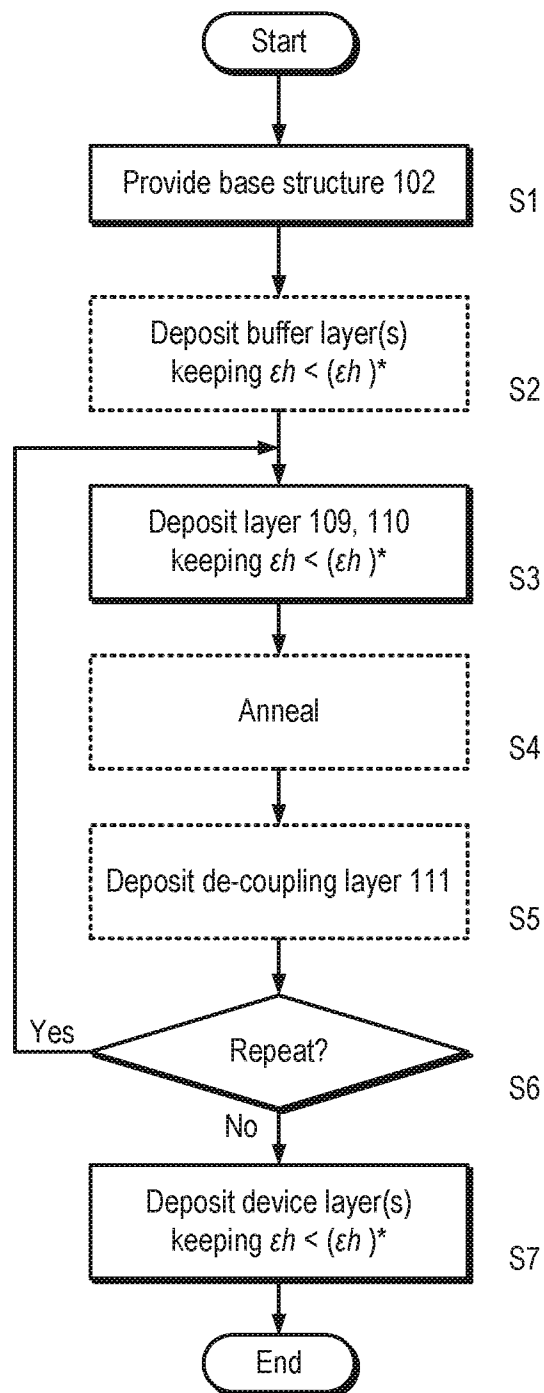


Fig. 20

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2017/050769

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/02
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 014 431 A2 (DAIMLER CHRYSLER AG [DE]) 28 June 2000 (2000-06-28)	1,3,5-8, 10-16, 19-21
A	paragraph [0009] - paragraph [0015] figure 4	2,4
X	----- EP 2 897 157 A1 (TOSHIBA KK [JP]) 22 July 2015 (2015-07-22)	1,3-8, 10,12, 13,15, 16,19-21
A	paragraph [0047] - paragraph [0060] paragraph [0135] - paragraph [0154] figures 7, 8 ----- -/-	2,11,14



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 May 2017

Date of mailing of the international search report

04/08/2017

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Bruckmayer, Manfred

INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2017/050769

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ZETIAN MI ET AL: "High-Performance Quantum Dot Lasers and Integrated Optoelectronics on Si", PROCEEDINGS OF THE IEEE, IEEE. NEW YORK, US, vol. 97, no. 7, July 2009 (2009-07), pages 1239-1249, XP011262464, ISSN: 0018-9219	1-7,9, 12,13, 15,16, 19-21
A	Chapter 'I. Introduction' Chapter 'II. Growth and characteristics of quantum dot lasers directly on Si substrates' figure 4(a)	8,14
A	----- WARD T ET AL: "Design rules for dislocation filters", JOURNAL OF APPLIED PHYSICS, AMERICAN INSTITUTE OF PHYSICS, US, vol. 116, no. 6, 14 August 2014 (2014-08-14), XP012188636, ISSN: 0021-8979, DOI: 10.1063/1.4892162 [retrieved on 1901-01-01] chapter 'I. Introduction' chapter 'IV. Measurement of interaction radius' chapter 'V. Discussion' -----	1-16, 19-21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2017/050769

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-16, 19-21

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-16, 19-21

A method / device comprising a layer for inhibiting movement of threading dislocations

2. claims: 17, 18

A device comprising a dislocation filter layer structure comprising a stack of at least two layers comprising first and second different materials respective

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2017/050769

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1014431	A2	28-06-2000	CA 2293060 A1 22-06-2000
			DE 19859429 A1 29-06-2000
			EP 1014431 A2 28-06-2000
			US 6313016 B1 06-11-2001

EP 2897157	A1	22-07-2015	CN 104779329 A 15-07-2015
			EP 2897157 A1 22-07-2015
			JP 2015133443 A 23-07-2015
			KR 20150085475 A 23-07-2015
			TW 201539739 A 16-10-2015
			US 2015200255 A1 16-07-2015
